

## **Power Supply Design Seminar**

# **Power Factor Correction Using the Buck Topology—Efficiency Benefits and Practical Design Considerations**

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# Power Factor Correction Using the Buck Topology—Efficiency Benefits and Practical Design Considerations

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## ABSTRACT

*Although active power factor correction (PFC) is typically accomplished with a boost power topology, this topic will show that a buck power stage offers significant efficiency advantages—particularly when universal line operation is required. Specific design and performance issues such as bus voltage choice, achievable total harmonic distortion (THD) and power factor (PF), control algorithms, and design practicalities will be discussed. Design choices are illustrated by a practical buck PFC design example based on a 90-W, high-density, slimline notebook adapter design (90WHD), demonstrating a >0.9 PF over a 20- to 90-W load range and over 100 to 230 VAC, and >96% full-load efficiency over 100 to 230 VAC.*

## I. INTRODUCTION

The benefits of improving the power factor (PF) of AC-to-DC power supplies have been well documented [1, 2]. The drive toward improving PF was initially mandated by European standard EN61000-3-2 [3] (and its forerunner IEC555) in an effort to reduce the harmonic content of the current flowing in the distribution network. Ironically, however, EN61000-3-2 (and its Japanese counterpart JIS C 61000-3-2) does not mandate PF limits directly, but rather the amount of harmonic current allowed at each individual harmonic of the fundamental-mains frequency up to the 39th. More recently, ENERGY STAR® [4] and European Commission [5] initiatives have started to add PF requirements alongside efficiency specifications. For example, ENERGY STAR EPS 2.0 for external AC power supplies (such as adapters) now requires a minimum PF of 0.9 at full load at 115 VAC for power supplies with input power in the range of 100 W to 250 W.

Improved PF by means of a PFC front-end must also be achieved with high efficiency of the PFC stage to maintain the same or better overall system efficiency [1]. For universal-mains-input power supplies, this high-efficiency performance must be maintained across the full AC line range to meet thermal constraints and avoid power derating at the AC line extremities. The industry has recognized that much electronic equipment

operates on average at only a small percentage of the full rated load for a large proportion of its operating life. Therefore, high-efficiency performance is being mandated across the full load range, down to 25% load, through the same ENERGY STAR and other initiatives. Many systems are also demanding better power-supply efficiencies in the 0 to 25% load range to meet stringent system-level power-consumption requirements in sleep/standby/idle modes. And of course, power supplies for computing and consumer applications have and always will be severely cost-challenged, requiring cost-effective solutions to deliver both improved PF and efficiency.

To summarize the design challenges facing power supply designers:

- **Power factor (PF)**—PFC is required for most designs with  $P_{\text{input}} > 75 \text{ W}$  to meet EN/JIS-61000-3-2 and  $P_{\text{input}} > 100 \text{ W}$  to meet ENERGY STAR.
- **Power density**—Higher power density to fit into smaller case sizes.
- **Universal input**—Ability to operate across universal AC-mains voltage range efficiently and cost-effectively, without power derating.
- **Light load**—High-efficiency operation at light loading, since this is the typical operating point for the majority of the product life.
- **Standby**—Very low standby or no-load power consumption, effectively heading toward zero power consumed at a zero load.

## II. THE NEED FOR PFC

Many techniques and topologies can and have been deployed for PFC. Numerous articles have been published that survey the options available for both passive and active PFC [6]. A detailed discussion of the full breadth of options, architecture and topologies would be beyond the scope of this topic, but some of the most commonly used approaches are briefly mentioned here.

To meet only the requirements of EN61000-3-2, as detailed in Appendix B, very low THD and unity PF are not required. Therefore, at low power levels (up to maybe 200 W), various passive PFC techniques have been employed to spread the conduction angle of the current waveform [7]. Although passive PFC can be low cost and easy to add to existing noncompliant designs (literally as a “bolt-on” fix) to meet EN61000-3-2, it does add considerable size and weight, degrades overall efficiency, and is limited in the extent of achievable PF improvement. A design that meets EN61000-3-2 with a 10% margin on all harmonics could have a PF as low as 0.76. Recent ENERGY STAR specs also now require a minimum PF of 0.9 at full load and 115 V/60 Hz. So a design that just about passes the requirements of EN61000-3-2 may not meet ENERGY STAR requirements. On the other hand, as cited in Reference [1], a PF of 0.9 could be achieved by drawing a square-input current waveform, but such a current waveform could not meet EN61000-3-2 because all harmonics above the 11th would exceed the limits.

There are many widely used active PFC circuits that can easily meet both EN61000-3-2 and ENERGY STAR 0.9 PF. Depending on the power level, input AC voltage range, required THD/PF performance, and cost constraints, many possible solutions may be adopted. Commonly used active PFC circuits include the flyback converter in discontinuous conduction mode (DCM), flyback in critical conduction mode

(CrCM), boost converter in continuous conduction mode (CCM), boost in DCM, and boost in CrCM. The boost converter is so widely deployed as a PFC front-end, that the term “PFC Front-end” has become almost synonymous with the term “boost PFC front-end” in industry. Although not widely used, the buck converter can and has been used as a PFC Front-end [8, 9, 10, 11].

## III. BUCK PFC TOPOLOGY OVERVIEW AND OPERATION

The basic circuit of the buck PFC power stage is shown in Fig. 1. This is a conventional buck (step-down) converter connected to an AC source and bridge rectifier. The output bus voltage is set at a level less than the peak AC voltage at the lowest line voltage. When the instantaneous AC input voltage is greater than the output bus voltage, the PFC stage is forward biased and current can be drawn from the AC input. When the AC input voltage falls below the bus voltage level, the diode bridge rectifiers become reverse biased, and no power can be drawn from the AC line. There will be an inherent “cross-over” distortion in the AC line current when the buck PFC stage is reverse biased. But in many applications, this distortion can be made acceptable with adequate line-current THD and PF performance. Some putative AC line

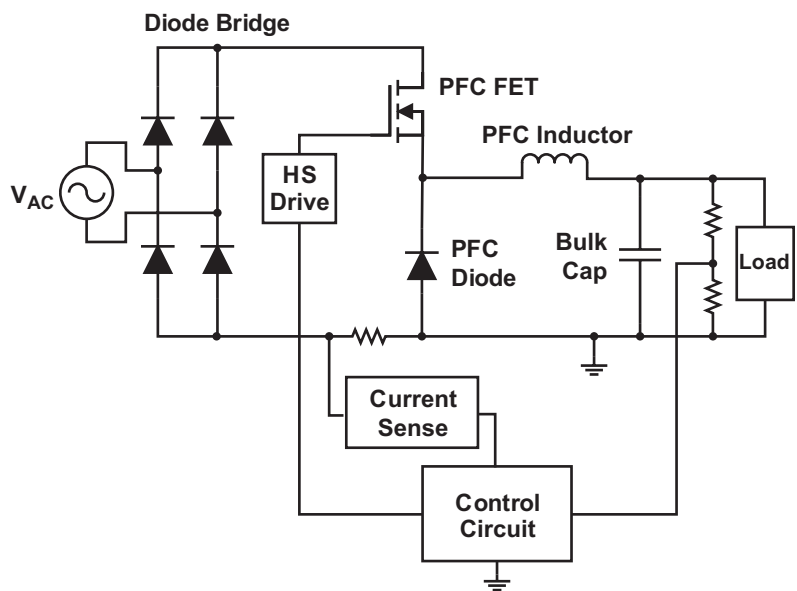


Fig. 1. Buck PFC basic power circuit.

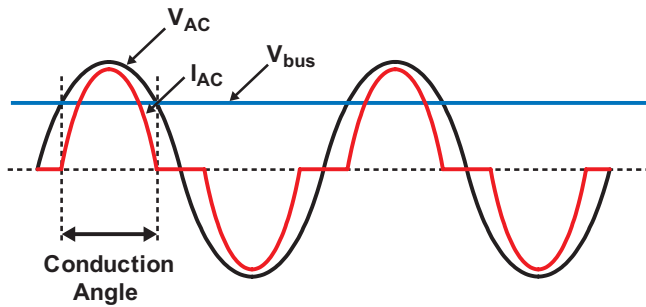


Fig. 2. Buck PFC line current and voltage at 100 VAC, with 80-VDC output, THD  $\approx$  44.3%, passing Japan JIS C 61000-3-2, potential PF  $\approx$  0.914.

voltage and current waveforms are shown in Fig. 2 at 90 VAC and in Fig. 3 at 230 VAC for a typical bus voltage level of 80 VDC. At a higher input voltage, the cross-over distortion becomes much less significant, with correspondingly lower THD and higher PF, as one would expect.

In a similar fashion to more conventional boost PFC stages, the buck PFC is typically controlled using an outer voltage-control loop to regulate the bus voltage, with an inner current-control loop to control the average current shape. The outer loop adjusts the demand applied to the inner loop to maintain the regulated average bus voltage in response to line and load changes. This loop is typically designed for slow response and low bandwidth so that it will not respond to output-voltage ripple, thus maintaining good PF of the input current. The inner current loop controls the PWM duty cycle of the PFC MOSFET over the AC half-cycle in response to the demand from the voltage loop. This controls the average AC line current to follow a pseudo-sinusoidal shape and essentially widening the conduction angle to deliver the required PF performance. These control loops are explained in more detail later.

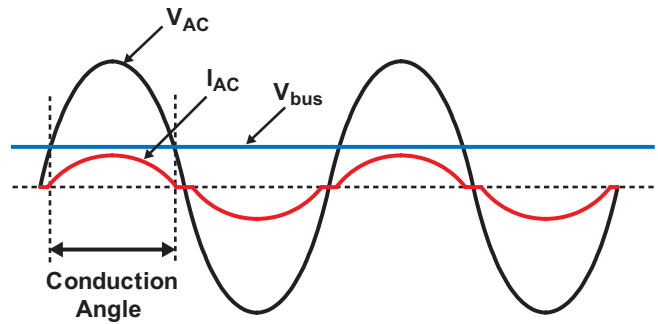


Fig. 3. Buck PFC line current and voltage at 230 VAC, with 80-VDC output, THD  $\approx$  16.7%, passing EN61000-3-2, potential PF  $\approx$  0.986.

## IV. BUCK VERSUS BOOST PFC COMPARISON

### A. Boost PFC Performance Advantages and Challenges

There are many reasons why the boost converter has become the topology of choice for a PFC front-end in many applications. Its many advantages include the following:

- Achieves very low THD, offering probably the best possible PF.
- High output voltage—volumetrically-efficient energy-storage capacitors, good hold-up.
- Low-side boost switch allows easy gate drive and switch current sense.
- Direct forward path from AC input to bulk storage capacitor eases lightning surge management.
- Wealth of available control ICs and design/analysis literature to aid designers.

The boost converter also has some limitations and drawbacks, some of which are simply the corollary of its advantages:

- Output voltage must always be higher than the instantaneous AC input voltage—for universal or high-line AC input (up to 264 VAC), bus voltage must be set at about 400 VDC.
- Requires a subsequent high-voltage primary regulation/isolation stage to step down to practical voltage levels required by most electronic loads.
- High bus voltage causes higher level of common-mode (CM) EMC noise.

- No inrush limitation at start-up (this is the flip-side of the surge advantage listed earlier), so a potentially dissipative or costly inrush limiting mechanism is required.
- Considerable drop in efficiency at low line because of the high voltage differential between the AC input voltage and the bus voltage and the consequent effect on PFC choke design.

## B. Buck PFC Performance Advantages and Challenges

Detailed operation of the buck PFC is outlined in the next section, but the advantages and disadvantages of the buck PFC are listed in order to compare with those of the boost PFC. Advantages include:

- The high-voltage AC input is immediately bucked to a lower voltage level by the PFC front-end which results in:
  - Easier functional safety spacing in the subsequent regulation/isolation stage.
  - Lower downstream voltages, improving robustness and reliability.
  - Low bus voltage results in lower CM noise.
  - Lower bus voltage for downstream stage, allowing more efficient designs, using lower-voltage MOSFETs with better figures of merit.
- Lower input-to-output voltage differential across PFC choke benefits include:
  - The ability to use a lower inductance value when compared to a boost PFC.
  - Input-output differential voltage across the choke varies in the opposite direction compared to a boost—thus a lower voltage differential at low line where efficiency is most challenged.
  - The buck has to work hardest at high line voltages where currents are much lower, whereas the boost works hardest at low line voltages when it boosts the most and currents are simultaneously the highest.
- Easy to control. Control flexibility helps achieve good THD and PF without the need for an AC line-sense reference and multiplier.
- Inherent “free” inrush limitation at start-up; no dedicated inrush limiting mechanism is required.

- Low output bus voltage allows downstream stage to make use of low-cost, low-voltage switches compared to conventional boost PFC bus voltages of ~400 V.

Of course, as with every circuit topology, the buck PFC has downsides and limitations—it’s not an appropriate solution for all applications. However, in many cases, the limitations can be overcome or sufficiently managed to offer a solution with distinct performance advantages over the boost PFC.

Disadvantages include:

- Inherent AC line current “cross-over” distortion limits achievable THD and PF performance.
- Requires use of either a high-side drive for the buck PFC switch or a high-side bus-voltage sense, depending on configuration used.
- No direct path from AC input to bulk-storage capacitor, complicating surge management.
- Lower output voltage results in less efficient bulk-capacitor energy storage, so bulk capacitors need to be larger and/or hold-up time is lower.
- A higher percentage bus-voltage ripple compared to boost PFCs requires voltage loops with lower bandwidths and a slower transient response.
- Limitation of available control IC, expertise and design/analysis literature to aid designers.

## V. BUCK PFC DESIGN APPROACH

### A. PFC Switching Frequency Selection

As with any AC/DC converter, switching frequency selection is a tricky compromise between efficiency, size, power density, EMC constraints, etc. There are always trade-offs between these conflicting constraints, and the selection of switching frequency depends on the priority of these constraints.

Where possible, the lowest practical switching frequency should be used for best efficiency and lowest losses. A lower switching frequency will lead to lower power-device switching loss, core loss, drive loss, and other AC losses. However, this goal is often in conflict with power-supply size and power-density requirements. A lower switching frequency will also result in much larger



magnetic components to handle the longer switching periods and maintain the same levels of peak and AC flux in the core. Typically, the maximum size of the power supply is constrained such that a practical minimum switching frequency is dictated.

The maximum allowed switching frequency is typically limited by EMC requirements. Because conducted emissions standard EN55022 and similar standards apply from 150 kHz upwards, the switching frequency is typically limited to perhaps 135 kHz maximum. This ensures that the second harmonic of the switching frequency is the first one of interest for conducted emissions. In some designs, if the switching frequency is kept below approximately 70 kHz, both the fundamental and second harmonic will be below the 150-kHz band, so that the third harmonic of switching frequency becomes the first one of interest for conducted emissions.

In practice, typically employed switching frequencies would be near 65 kHz for designs where highest power density is not required and 100 to 130 kHz for designs requiring higher power density, at the expense of possibly more EMC filtering.

In this topic, a nominal switching frequency of 100 kHz is assumed, unless otherwise stated. This frequency offers good performance in practical designs over the range of 50 to 400 W and is a reasonable compromise between efficiency, power density, and EMC constraints.

## B. Buck PFC Bus-Voltage Selection

The output bus voltage is probably the most important design parameter of the buck PFC, and is the starting point for a design. Fundamentally, the bus-voltage level must be lower than the minimum rated AC-line peak voltage, similar to the requirement that boost bus voltage must be

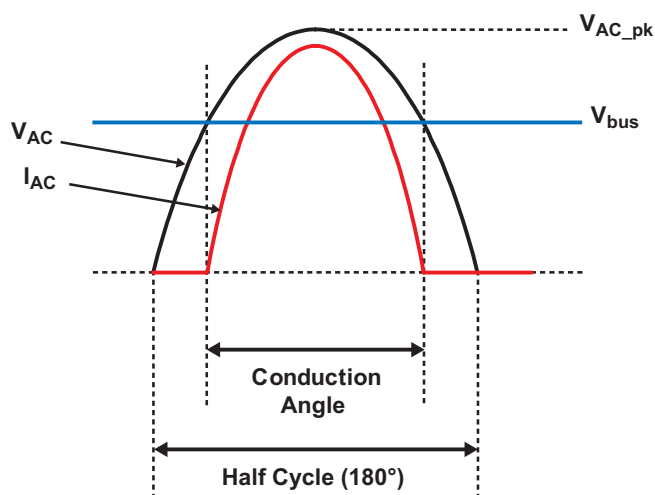


Fig. 4. Buck PFC line-current conduction angle.

greater than the maximum rated AC-line peak voltage. However, the bus voltage must be sufficiently lower than the minimum AC-line peak to allow a reasonable conduction angle.

Fig. 4 clearly illustrates the trade-off between the level of the bus voltage and the conduction angle. Setting the bus voltage level too high will result in a much shorter conduction angle, and lower bus voltage gives a wider conduction angle. Conduction angle can be calculated as the number of degrees out of each 180° half cycle that the buck PFC is forward biased, during which line current can be drawn:

$$\theta_{\text{cond\_deg}} = 2 \times \cos^{-1} \left( \frac{V_{\text{bus}}}{\sqrt{2} \times V_{\text{rms}}} \right) \times \frac{180^\circ}{\pi}. \quad (1)$$

The conduction angle may also be more conveniently expressed as a percentage of the AC line half-cycle (or indeed full-cycle) as:

$$\theta_{\text{cond}(\%)} = 2 \times \cos^{-1} \left( \frac{V_{\text{bus}}}{\sqrt{2} \times V_{\text{rms}}} \right) \times \frac{1}{\pi}. \quad (2)$$

### Minimum Conduction-Angle Constraint at Low Line Voltages

As can be seen in Fig. 5, conduction approaches the full 180° cycle as  $V_{bus}$  is reduced toward zero, but above 100 VDC, the conduction angle would drop unacceptably low for low line voltages of 90 to 120 VAC. To remain practical, the bus voltage should be set low enough to ensure at least a 50% conduction angle at the lowest line voltage. A conduction angle of less than 50% will result in very poor PF and very high peak currents, and will degrade efficiency at lowest line. For a typical minimum-rated line voltage of 90 VAC, the upper limit on bus voltage would be 90 VDC to ensure at least a 50% conduction angle. In practice, it is desirable to maintain a conduction angle reasonably greater than 50%, so that good PF can be maintained. However, bus voltage selection is more typically constrained by the availability of bus capacitor ratings and by downstream-stage bus voltage requirements.

### Available Capacitor Ratings

The choice of bus-voltage level will be strongly influenced by the choice and availability of suitable voltage ratings for bus capacitors. This is really the bottom-line constraint. Standard capacitor

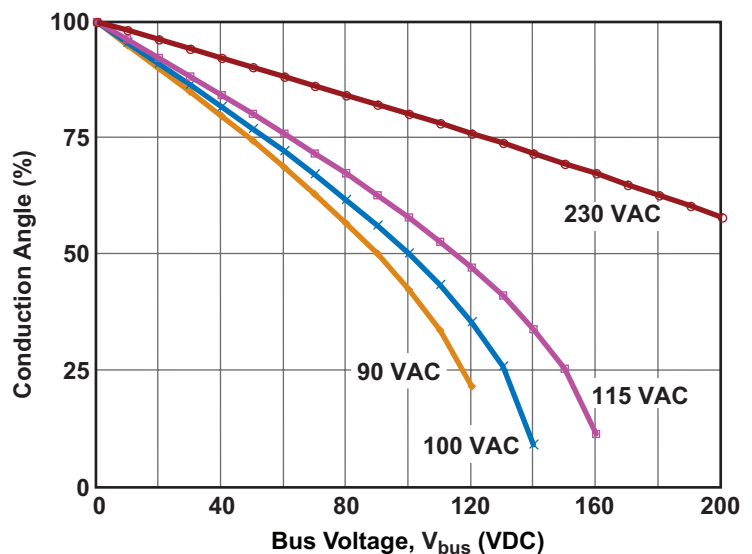


Fig. 5 Buck PFC conduction angle (in degrees) versus  $V_{bus}$  and AC line.

voltage availabilities are summarized in Table 1, together with suggested bus voltage settings based on appropriate derating.

### Recommended Bus Voltage Range

For universal input AC mains range from 90 to 264 VAC, the bus voltage should be chosen to allow a minimum 50% conduction angle at 90 VAC; this limits the maximum recommended bus

TABLE 1. SUMMARY OF STANDARD CAPACITOR VOLTAGE RATINGS AND POSSIBLE BUCK PFC BUS VOLTAGE LEVELS

Capacitor Rating	Maximum $V_{bus}$ (with 20% Derating)	Advantages	Disadvantages
50 V	40 VDC	Wide conduction angle, ~80% at 90 VAC, very good PF	Low efficiency, very high downstream currents, very poor energy storage/holdup
63 V	50 VDC	Wide conduction angle, ~74% at 90 VAC, very good PF	Low efficiency, high downstream currents, poor storage/holdup
100 V	80 VDC	Good conduction angle, ~57% at 90 VAC, good PF, good efficiency, moderate downstream currents, reasonable energy storage/holdup	Somewhat limited PF, < 100 VAC
160 V	120 VDC	Good efficiency, low downstream currents	Very poor conduction angle, ~22% at 90 VAC, very poor PF, not suitable for operation below 120 VAC
200 V	160 VDC		Not suitable for operation at low line voltages, only high line voltages of 180 to 264 VAC

voltage to 90 VDC. From Table 1, using bus capacitors rated at 100-V is a good compromise, so for a 20% typical derating, a bus voltage of approximately 80 VDC would be appropriate. This also gives good utilization of component ratings, particularly 100-V rated power MOSFETs for the downstream stage.

In practice, the actual bus voltage level may be varied somewhat to suit the specifics of the downstream isolation/regulation stage and the most suitable transformer turns ratio. Bus voltages in the range of 75 to 85 VDC have been used to good effect in a variety of designs.

### C. Buck-PFC Bulk Capacitor

Depending on the application, the bulk capacitance value required could be dictated by voltage-ripple requirements, required ripple-current rating of the bulk capacitors, or hold-up requirements. For notebook adapter and similar applications where a battery is present in the system, then hold-up is typically not a major concern. In this case, the bulk capacitor choice will be dictated by either the allowed peak-to-peak bus ripple voltage or by the required bulk capacitor ripple-current rating.

Unlike the boost PFC, the bus ripple voltage of the buck PFC will vary with line voltage, and moreover will typically be a much higher percentage of the DC regulated value. This is because the power transfer from the AC line only occurs during the conduction angle, when the instantaneous AC line voltage is greater than the bus voltage. When the buck PFC stage is reverse biased during the AC line cross-over, the bulk capacitor must supply all of the load current until the AC line voltage increases above the bus voltage level again. Since the dead-time interval will be longer at a lower line voltage, then the bus ripple voltage will be higher at a lower line voltage. For this reason, the 100-/120-Hz ripple-current rating required for the buck PFC bulk capacitor could be substantial, and could be the limiting factor in the choice of bus capacitance. In addition, the bus capacitors will need to carry the high-frequency ripple current from the PFC choke, as well as some additional ripple current drawn by the second isolation/regulation stage.

Compared to a boost PFC, the buck PFC will always offer less bulk-energy storage since the bus voltage is much lower. Thus, the buck PFC will always offer less hold-up, or require larger bulk capacitors, or suffer a greater percentage bus ripple, or all three. Clearly, for a similar hold-up requirement, the buck PFC will require more capacitance than the boost PFC, and the size of the buck PFC capacitance will be greater, taking up more space inside the power supply. This trade-off is difficult to quantify because of variations in capabilities and design rules of different capacitor manufacturers. The energy storage difference due to the voltage range of 100 V versus 400 V is straightforward to calculate—the higher voltage capacitors can store 16 times more energy for the same capacitance value. But from reviewing various capacitors in various can sizes for a few manufacturers, it seems that for a given can size, the 400-V capacitor will have maybe 8 to 10 times less capacitance than the 100-V type. So the net effect on energy storage capability is that the 400-V capacitors can likely store 50 to 100% more energy in the same physical can size. Or that the buck PFC bus capacitors would require 50 to 100% more physical volume for the same energy storage.

### Hold-Up Requirements

If hold-up is the limiting design constraint, then the amount of bulk capacitance required depends on the hold-up time needed, AC line voltage, power level, and the amount of bus voltage “headroom” provided in the design. The headroom is the margin allowed between the nominal bus voltage level and the minimum input voltage rating of the second stage.

The worst case hold-up of the buck PFC occurs when the AC line voltage is removed at the trough of the bus ripple, i.e., at a phase of the AC cycle where the buck PFC has just become forward-biased and can start to draw current from the AC line again. What is interesting is that if the bus capacitor is increased in order to increase the energy storage and provide more hold-up, the peak-to-peak ripple voltage will also decrease. Thus, the trough of the bus ripple will increase, further improving the resultant hold-up performance.



However, one of the main efficiency impacts of designing for large hold-up is the impact on the second isolation/regulation stage. For greater hold-up, this stage must be designed to operate over a wider input voltage range, with a consequent impact on efficiency of that stage.

The bus ripple at any operating point can be estimated as follows:

$$\Delta V_{\text{bus(p-p)}} = \frac{P_{\text{load}}}{C_{\text{bus}} \times V_{\text{bus}}} \times \frac{(1 - \theta_{\text{cond}(\%)})}{2 \times f_{\text{AC}}}, \quad (3)$$

where  $P_{\text{load}}$  is the load power drawn (usually by the second regulation/isolation stage),  $C_{\text{bus}}$  is the bus capacitance,  $\theta_{\text{cond}(\%)}$  is the conduction angle at the AC line of interest (as a decimal percentage of total cycle—e.g., a 50% conduction angle expressed as 0.5), and  $f_{\text{AC}}$  is the AC line frequency.

The maximum bus ripple can be estimated from Equation 3 at a maximum load, minimum AC line voltage/frequency, and minimum bus capacitance value. Knowing the bus ripple, the minimum bus level at the trough of the ripple can be expressed as:

$$V_{\text{bus\_min}} = V_{\text{bus\_nom}} - \frac{\Delta V_{\text{bus(p-p)}}}{2}, \quad (4)$$

where  $V_{\text{bus\_nom}}$  is the nominal PFC bus voltage.

Knowing the minimum allowable bus voltage at which the regulation stage can keep the output voltage in regulation ( $V_{\text{bus\_min\_reg}}$ ), the hold-up capability can be estimated as:

$$t_{\text{holdup}} = (V_{\text{bus\_min}}^2 - V_{\text{bus\_min\_reg}}^2) \times \frac{C_{\text{bus}}}{2 \times P_{\text{load}}}, \quad (5)$$

where  $P_{\text{load}}$  is the maximum load power drawn from the bus (accounting for efficiency of the second regulation/isolation stage). Thus, in order to achieve a required hold-up time, the required bus capacitance may be calculated as:

$$C_{\text{bus}} = \frac{t_{\text{holdup}} \times 2 \times P_{\text{load}}}{V_{\text{bus\_min}}^2 - V_{\text{bus\_min\_reg}}^2}. \quad (6)$$

For example, in order to achieve a 3-ms holdup with a nominal bus voltage of 80 VDC,  $\pm 5\%$  maximum bus ripple, and 70-VDC minimum bus-regulation level for the second stage, required bus capacitance would be calculated as follows

for a 90-W load, assuming 96.5% second stage efficiency:

$$C_{\text{bus}} = \frac{0.003 \times 2 \times \frac{90}{0.965}}{(80 \times 0.95)^2 - 70^2} = 639 \mu\text{F}. \quad (7)$$

### Bus Ripple Percentage

The allowed peak-to-peak ripple on the buck PFC bus voltage is usually the most restrictive constraint that dictates the required bus capacitance size. The bus ripple influences performance in several ways:

- Introduces small line-current phase shift and degrades PF.
- High ripple forces the second isolation/regulation stage to operate over a wider range, degrading efficiency performance of the second stage.
- Ripple peak voltage must be limited to the required component stress-derating levels.
- The ripple-voltage minimum limits the amount of bus voltage headroom to the second stage.
- The bus ripple is predominantly at twice the AC line frequency (100/120 Hz), so high ripple will affect the voltage loop design and degrade either PF or transient response.

The peak-to-peak bus ripple is estimated by Eq. 5-3, so the percentage bus ripple can be expressed as:

$$\Delta V_{\text{bus}(\%)} = \frac{P_{\text{load}} \times (1 - \theta_{\text{cond}(\%)})}{C_{\text{bus}} \times V_{\text{bus}}^2 \times 2 \times f_{\text{AC}}}. \quad (8)$$

For designs where holdup is not the design constraint, the bus capacitance required to achieve a desired percentage bus ripple can be expressed as:

$$C_{\text{bus}} = \frac{P_{\text{load}} \times (1 - \theta_{\text{cond}(\%)})}{V_{\text{bus}}^2 \times \Delta V_{\text{bus}(\%)} \times 2 \times f_{\text{AC}}}. \quad (9)$$

For a typical 90-W adapter using a buck PFC, the required bus capacitance for a  $\pm 6\%$  maximum ripple at 90 VAC/50 Hz (12% total ripple) and 80-VDC bus, assuming 96.5% efficiency of the second stage, would be:

$$C_{\text{bus}} = \frac{\frac{90}{0.965} \times 0.57}{80^2 \times 0.12 \times 2 \times 50} = 690 \mu\text{F}. \quad (10)$$

### Bus Ripple Impact on PF

Typically, the percentage bus ripple of the boost PFC is very low—less than  $\pm 1\%$  to  $\pm 2\%$  peak-to-peak. This allows simplification of the analysis and design equations for the boost PFC stage. By contrast, the buck PFC percentage ripple is often much more significant, typically  $\pm 5\%$ . So this amount of bus ripple can have a significant effect on performance.

As can be seen in Fig. 6, one noticeable effect of the bus ripple voltage is that the point in the AC line half-cycle at which the buck PFC becomes forward biased occurs earlier in time, as ripple increases. Similarly, the point at the end of the half-cycle at which the buck PFC becomes reverse biased also occurs earlier in time. The net effect is that the AC line current is slightly phase advanced with respect to the AC line voltage. This phase shift causes a reduction in displacement factor from unity, and as a result a reduction in PF.

### Transient Response

As discussed previously in section 2, because of the higher percentage bus ripple of the buck PFC, the voltage control loop must be designed for lower bandwidth, which will impact the speed of response to load transients. However, the buck-PFC dead time near the AC line cross-over has a more profound impact on transient response. Consider the condition where a load transient occurs during the dead-time interval—especially at lower line voltages where the dead-time is longer. In this case, regardless of the voltage control bandwidth, the bus-voltage transient drop will essentially be a function of the bulk capacitance. For this reason, the worst-case transient response can not be improved by employing many control-loop-based transient improvement techniques [12, 13].

In some cases, boost PFC transient response has been improved by the use of line-synchronized sample and hold, or notch filters tuned to 100 Hz or 120 Hz, or a parallel high-bandwidth voltage control loop that acts during transient events to drive the bus voltage outside a defined regulation window. However, none of these techniques can resolve the issue of buck PFC load transients that can occur during the AC cycle dead time. For the buck PFC, the easiest solution is to increase the amount and size of the bulk capacitance. This has the added benefit that the increased bulk capacitor will reduce bus voltage ripple, increase hold-up time, and improve PF. However, increased bulk capacitance does add cost, size, and weight to the power supply.

### D. Buck PFC Choke Design Considerations

As has been shown in previous publications [14], if the buck PFC stage is operated in discontinuous conduction mode (DCM) (i.e., the inductor current is allowed to go discontinuous in every switching cycle), then the control of the PFC stage is very straightforward. Operation with a fixed duty cycle over the AC line half-cycle can readily achieve good PF performance, with a very simple controller. Operation in DCM at all conditions means that reverse-recovery switching loss is not a big issue; thus, the more expensive high-voltage Schottky type diodes (e.g., SiC devices) can be avoided in favor of low-cost, ultrafast PFC diodes.

However, if the PFC choke were designed to maintain DCM operation over the full load and universal AC-line range, then the peak-to-peak currents at full load could become excessive, especially at high line voltages. At higher power levels in particular, very high peak currents could flow in the choke, requiring quite a large size

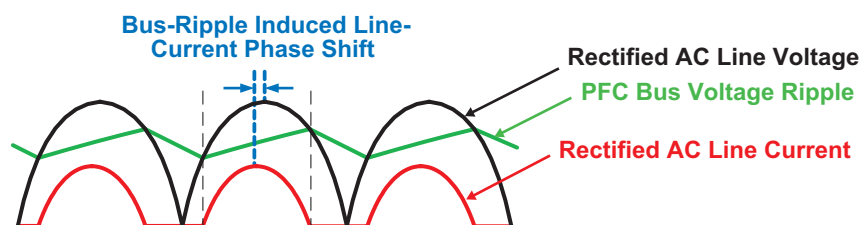


Fig. 6. Phase shift of line current due to the effect of bus ripple voltage.

choke to handle these peak currents and maintain reasonable flux levels.

For moderate power levels (up to 150 to 200 W), the PFC choke can be designed to operate in DCM at high line voltages over the full load range, and in CCM at low line voltages, heavy load conditions. This allows a more compact PFC choke design. Operating in CCM only at low line voltages can be seen as a reasonable compromise. At high line voltages, DCM operation avoids PFC-diode reverse-recovery issues, still allowing usage of a low-cost ultrafast rectifier. At low line voltages, reverse-recovery losses in CCM are more contained at the lower voltage levels and are more easily managed. This approach has been found to offer good performance for power levels from 50 to 150 W.

For higher-power designs (>200 W), this approach becomes more difficult. Designing the PFC choke to ensure DCM at high line becomes more challenging. The peak currents become very large. The required core air gap can become very significant to support the higher peak current. Turns count then has to increase and the physical core size has to get much larger. For >200-W designs, the choke and overall performance could be made more efficient by designing the PFC choke for CCM operation even at high line voltages, when load current increases beyond 60% of the full-load rating. In this case, the increased switching losses due to reverse recovery are more than compensated for by reduced choke air-gap fringing effects, reduced peak, and rms choke currents.

### PFC Choke Inductance Value

For modest power levels up to approximately 150 W, the PFC choke is typically designed for an inductance value that ensures DCM operation at high line (at all line voltages >160 VAC), right up to full peak load. With an appropriate value of inductance to ensure DCM at full load at the high end of the line-voltage range, operation at low line should then result in CCM operation over most of the conduction angle at full load. At least some CCM operation should occur at low line voltages for loads greater than approximately half the full-load rating.

The buck PFC has previously been analyzed to establish the limit or boundary of the choke inductance value to ensure CCM operation at low line voltages (see Reference [9] for full details). In a similar fashion, the following analysis determines the value of inductance required to set the boundary of CCM/DCM at a desired line voltage level for a given power level.

As shown in Fig. 7, if the AC line current is initially assumed to be proportional to the AC line minus the bulk voltage differential, then the peak AC line current can be estimated. In Fig. 7, input current follows a sinusoid of amplitude  $I_M$ , but with an offset during the conduction angle, and is zero outside the conduction angle. The angle at which conduction starts in the AC cycle is indicated as  $\theta_{start}$ , and the waveform is assumed to be symmetrical within the AC half cycle—i.e., it is assumed that  $\theta_{start} = \theta_{stop}$ . The current can be expressed for two conditions:

1. When  $\theta_{start} < \theta < (\pi - \theta_{start})$ , then  

$$i_{in}(\theta) = I_M \times (\sin\theta - \sin\theta_{start}) = I_{inpk} \times \sin\theta, \quad (11a)$$
where  $I_{inpk} = I_M \times (1 - \sin\theta_{start})$  and  

$$\theta_{start} = \sin^{-1}\left(\frac{V_{bus}}{\sqrt{2} \times V_{rms}}\right) = \sin^{-1}\left(\frac{V_{bus}}{V_{inpk}}\right).$$
2. When  $\theta < \theta_{start}$  or  $\theta > (\pi - \theta_{start})$ , then  

$$i_{in}(\theta) = 0. \quad (11b)$$

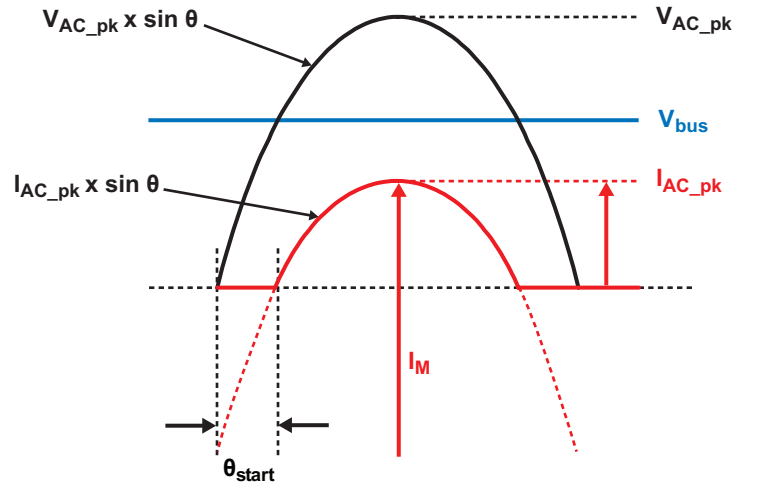


Fig. 7. Idealized input current and voltage waveforms of a buck PFC.

By integrating the product of voltage and current, the average input power may be expressed as:

$$P_{\text{inavg}} = \frac{1}{\pi/2} \times \int_0^{\pi/2} [v_{\text{in}}(\theta) \times i_{\text{in}}(\theta)] d\theta. \quad (12)$$

Substituting the expressions for current and voltage and recognizing that there is zero current outside the conduction angle, this can be written as:

$$P_{\text{inavg}} = \frac{2}{\pi} \times \int_{\theta_{\text{start}}}^{\pi/2} [V_{\text{inpk}} \times \sin\theta \times I_M \times (\sin\theta - \sin\theta_{\text{start}})] d\theta$$

and simplified to

$$P_{\text{inavg}} = \frac{2 \times V_{\text{inpk}} \times I_M}{\pi} \times \int_{\theta_{\text{start}}}^{\pi/2} [\sin^2\theta - \sin\theta \times \sin\theta_{\text{start}}] d\theta. \quad (14)$$

Rearranging for  $I_M$  and substituting into the equation for  $I_{\text{inpk}}$  gives:

$$I_{\text{inpk}} = \frac{P_{\text{inavg}} \times \pi}{2 \times V_{\text{inpk}}} \times \frac{(1 - \sin\theta_{\text{start}})}{\int_{\theta_{\text{start}}}^{\pi/2} [\sin^2\theta - \sin\theta \times \sin\theta_{\text{start}}] d\theta}. \quad (15)$$

Equation (15) can be evaluated more easily by solving the integral and rewriting the equation as:

$$I_{\text{inpk}} = \frac{P_{\text{inavg}} \times \pi}{2 \times V_{\text{inpk}}} \times \frac{(1 - \sin\theta_{\text{start}})}{\frac{\pi}{4} - \frac{\theta_{\text{start}}}{2} - \frac{\cos(\theta_{\text{start}}) \times \sin(\theta_{\text{start}})}{2}}. \quad (15a)$$

Assuming that the PFC choke is chosen so that operation is in CCM at peak of nominal low line (115 VAC) and in DCM at peak of nominal high line (230 VAC), then at a particular intermediate voltage, operation will be at the boundary of

CCM/DCM. Knowing  $I_{\text{inpk}}$ , the required PFC choke inductance can be calculated to set this CCM/DCM boundary operating point at any desired line peak voltage. If the line peak voltage at this boundary point is designated  $V_{\text{inpk\_BP}}$ , then the switch duty cycle at this point (designated  $D_{\text{BP}}$ ) will be the ratio of  $V_{\text{bus}}$  to  $V_{\text{inpk\_BP}}$ , or:

$$D_{\text{BP}} = \frac{V_{\text{bus}}}{V_{\text{inpk\_BP}}}. \quad (16)$$

Also at this operating point, the average and peak-to-peak inductor-ripple currents will be:

$$I_{L\_avg} = \frac{I_{\text{inpk}}}{D_{\text{BP}}} \quad (17)$$

$$I_{L\_pp} = \frac{V_{\text{bus}}}{L_{\text{pfc}} \times f_{\text{SW}}} \times (1 - D_{\text{BP}}). \quad (18)$$

Recognizing that at this boundary operating point, the average current will be exactly twice the peak-to-peak current, then the maximum allowed  $L_{\text{pfc}}$  can be calculated to ensure DCM at peak line voltages above any desired  $V_{\text{inpk\_BP}}$ :

$$L_{\text{pfc}} = \frac{1}{2 \times f_{\text{SW}} \times I_{\text{inpk}}} \times (V_{\text{inpk\_BP}} - V_{\text{bus}}) \left( \frac{V_{\text{bus}}}{V_{\text{inpk\_BP}}} \right)^2. \quad (19)$$

For example, to ensure DCM operation at >160 VAC for a 100-W buck PFC with an 80-VDC bus, the maximum allowed choke inductance could be calculated as follows. Initially, the peak AC line current can be estimated from Equation (15), (knowing from Equation (11) that  $\theta_{\text{start}}$  at 160 VAC will be 20.7° for a  $V_{\text{bus}}$  of 80 V):

$$I_{\text{inpk}} = \frac{90}{2 \times \sqrt{2} \times 160} \times \pi \times \frac{1}{\int_{\theta_{\text{start}}}^{\pi/2} [\sin^2\theta - \sin\theta \times 0.354] d\theta} \times (1 - 0.354) = 0.953 \text{ A (peak)}. \quad (20)$$



Knowing  $I_{\text{inpk}}$ , the critical value of  $L_{\text{pfc}}$  to ensure that the boundary operating point is at 160 VAC can be found (assuming a nominal switching frequency of 100 kHz):

$$L_{\text{pfc}} = \frac{1}{2 \times 100000 \times 0.953} \times (\sqrt{2} \times 160 - 80) \left( \frac{80}{\sqrt{2} \times 160} \right)^2 = 95.9 \mu\text{H}. \quad (21)$$

This is the maximum value of inductance that will ensure that the boundary of operation from CCM to DCM at line peaks occurs at 160 VAC. In practice, the actual inductance value used can be varied to suit the actual design, but the previous analysis shows that  $L_{\text{pfc}}$  values larger than those predicted here will result in CCM operation at higher line voltages, while smaller  $L_{\text{pfc}}$  values will result in DCM operation down to lower line voltages.

Compared to the boost PFC, much smaller values of PFC inductance can typically be used in the buck, because the voltage differential that needs to be supported across the choke is lower. Practical inductance values that have been used in various designs have ranged from about 150  $\mu\text{H}$  for a 50-W circuit, 80 to 100  $\mu\text{H}$  for a 90- to 150-W circuit, and down to 50 to 60  $\mu\text{H}$  for a 300- to 400-W circuit.

### **PFC Choke Losses**

At low line voltages, choke losses are dominated by rms currents and conduction losses, assuming deep CCM. It is important to choose a core set that is suitably large, with a sufficiently high core cross-section or effective area,  $A_e$ , to keep turns count low. A lower turns count results in lower DC resistance (DCR), less layers in the winding construction, and less associated proximity-effect AC resistance (ACR).

At high line voltages, assuming DCM, both core and copper losses are important. With DCM operation, peak-to-peak current will be high—twice the peak of AC line current at the CCM/DCM boundary operating point, and even greater as the operation becomes more discontinuous. The choke should be designed so that it can sustain the highest peak current at the highest line voltage and highest peak load, and with a good saturation margin where possible. Besides the extra safety

margin and reliability that will be achieved, this will reduce the peak-to-peak flux swing at high line 230 VAC and full load. This reduces the nominal flux swing and can greatly reduce core loss and improve efficiency performance further. The downside is that this extra saturation margin will translate to a slightly physically larger core and choke size, but it is a very useful way to get even better buck PFC efficiency where available space allows for a slightly larger choke.

At high line voltages, conduction losses are also very critical. Although average currents are lower at high line voltages, since operation can be very heavily into DCM, the rms current in the choke can be as significant as at low line. Moreover, the current at high line voltages will have a much more significant switching-frequency harmonic content, even for the same total rms current. So a winding design with a low AC-resistance (ACR) factor is also very important. For this reason, the choke should be designed to use stranded-wire bundles rather than single-strand solid-core wire. Ideally, the wire diameter chosen for the stranded wire should be no greater than the skin depth for the chosen switching frequency, especially since the discontinuous current waveform at high line voltages will contain significant harmonic components up to many multiples of the fundamental switching frequency. The stranded-wire bundle should then have a sufficient number of these strands to handle the required rms current.

This is a rule of thumb that has been found useful—at one skin depth, current density will have dropped to 63% of the value on the surface, so a wire thickness that is twice the skin depth can be used to ensure a current density of >63% everywhere. But for the higher-order switching harmonics, skin depth will decrease with the square root of frequency, so by limiting wire diameter to one skin depth, a >63% current density is ensured for harmonics up to four times the fundamental switching frequency. This is beneficial at high line voltages, where the DCM triangular current waveforms exhibit high peaks at maybe only 20% duty cycle.

True “Litz”-wound construction is overly complex and costly. Simple stranded wire or bundles of stranded wire are sufficient for most applications. However, it is vitally important that



the stranded wire is tightly twisted. This is to ensure that all strands spend an equal and uniform amount of time throughout the cross-section of the bundle; otherwise, some strands in the bundle may be forced to conduct more current than others, which can dramatically increase ACR.

The final constraint to be aware of is the effect of air-gap fringing flux, which can induce very high losses in the copper adjacent to the air gap. This effect can be very severe if the air gap is large, as is sometimes necessary to increase the saturation capability of the inductor. Again, it may prove beneficial to consider a slightly larger core  $A_e$  with a slightly smaller air gap.

In some designs, it can help to construct the choke with a deliberately fattened bobbin-wall thickness around the limb with the air gap (normally the center leg of an E-core construction). This increase in bobbin-wall thickness serves to physically remove the copper winding from the fringing flux field of the air gap, reducing induced eddy currents in the windings and improving choke efficiency.

Topic 5 in this seminar series covers all of these areas in greater detail.

## E. PFC MOSFET and Diode Choice

Compared to the boost PFC, the MOSFET rms current in the buck PFC is higher; thus the buck PFC will benefit from the use of a slightly lower  $r_{ds(on)}$  MOSFET. This can also benefit the size and thermal performance in the final design. For example, in an open-frame design with airflow, the efficiency drop between 115 and 90 VAC may not be so significant. By comparison, for an enclosed design such as a notebook adapter, 90 VAC is typically the most thermally challenged operating point. At this operating point, the PFC power stage would benefit from the use of a slightly better PFC MOSFET, allowing for a smaller and slimmer final design.

For the PFC diode, use of a conventional ultrafast or hyper-fast type is adequate; at low line voltages, the reverse-recovery losses associated with CCM operation are manageable at the lower voltages. At high line voltages, the average MOSFET duty cycle will be quite low—perhaps 15 to 25% at full

load—so the diode duty cycle will be very significant. Thus, it is important to minimize diode  $V_f$  to control diode losses at high line voltages. Use of very fast rectifiers, in particular SiC devices, usually comes at the expense of very high  $V_f$ , between 2 to 4 V. In the 80% diode duty-cycle range, this level of  $V_f$  can lead to significant extra loss. The fast recovery benefit is only beneficial if the design is operated heavily in CCM across the full line range—even then, the  $V_f$  versus reverse-recovery loss trade-off is difficult to call. Factoring in the high cost of SiC diodes, the design for DCM at high line with an ultrafast rectifier becomes attractive on cost grounds.

## F. Voltage-Control Loop Design

The bus voltage-control loop for the buck PFC is very similar to that of the boost PFC (or any PFC voltage-control loop). The purpose of the loop is to sense the bus voltage, compare to a reference, and create a demand signal for the inner current-control loop such that the bus voltage is regulated as AC line voltage and load current vary. The voltage loop is shown in Fig. 8. Note that the buck power stage is inverted compared to the power stage shown in Fig. 1.

This voltage-control loop operates (and is designed) in exactly the same way as a boost PFC loop [2]. The voltage error-amplifier feedback components are chosen to achieve low bandwidth in the error amplifier; in other words, attenuate the

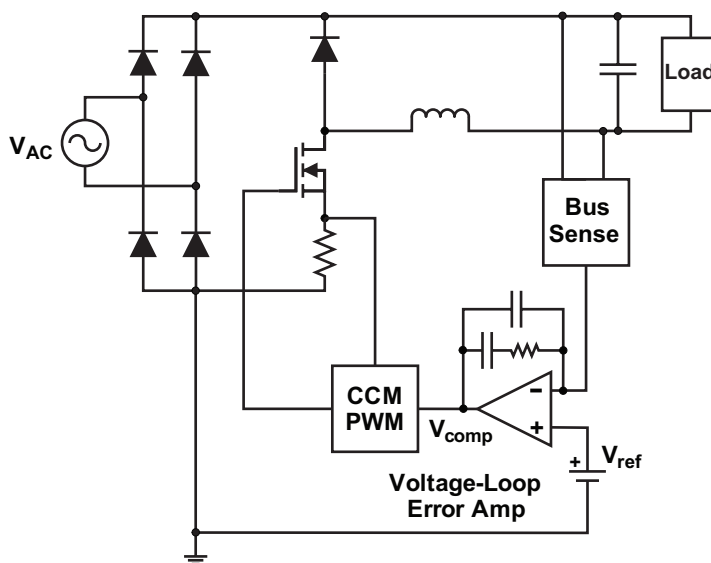


Fig. 8. Buck PFC voltage-control loop.

100-/120-Hz bus ripple at the voltage sense input so that the  $V_{\text{comp}}$  signal fed to the inner-current loop is as close to DC as possible. As already outlined in the “Bus Ripple Percentage” section, the gain of the error amplifier for the buck PFC must be made considerably lower than the equivalent boost circuit, given the higher percentage bus ripple present.

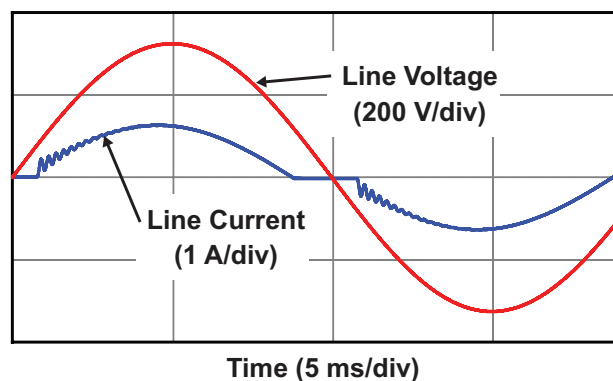
### G. Buck PFC Current-Control Schemes

As outlined in more detail in Appendix B, given the inherent dead time of the buck PFC and the resulting crossover distortion of the AC line current drawn, there is an upper limit on the achievable PF. Further degradation of PF will occur because of circuit practicalities such as bus-capacitor ripple, EMC film-capacitor current, etc. But how should the buck PFC power stage be controlled to achieve the PFC goal?

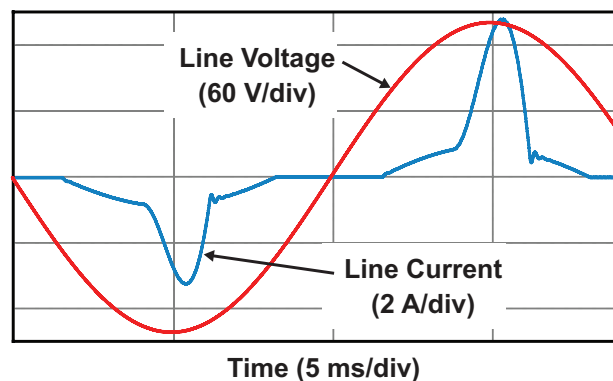
As previously analyzed [14], when operated in DCM, the buck PFC can be relatively easily controlled to give good PF. For example, a fixed duty cycle may be employed over the entire AC cycle, giving reasonable PF performance. Clearly, a control circuit will be required to adjust this fixed duty cycle in response to load demand to keep the output voltage in regulation. In its simplest form, this could be a basic voltage-mode controller that generates a DC error signal that is compared to a sawtooth ramp to produce the required duty cycle for the buck PFC MOSFET. This approach was simulated, with the resulting waveforms shown in Fig. 9. At high line, where operation is always in DCM, the current is well controlled and pseudo-sinusoidal in shape, with a good PF of  $>0.95$ . However, at low line, operation transitions from DCM to CCM for a portion of the AC cycle around the voltage peaks, depending on load level. Under these conditions, the current can easily “run away” because of the much higher loop gain in CCM; i.e., a small change in duty cycle can produce a large change in inductor current. This

peaking of the current greatly degrades the PF, and in extreme cases can cause the buck PFC stage to behave virtually like a diode rectifier with a capacitive filter. In applications with a narrow input range and suitable protection mechanisms against CCM operation and current runaway, the control approach may be suitable.

Because of the wide operating range required for universal range of AC mains, it is difficult to design the buck PFC to always operate in DCM and maintain good efficiency with a compact magnetic size. Moreover, if employing only voltage-mode



a. Operation is always in DCM at high-line voltages (230 VAC).



b. Operation changes to CCM during current peaks at low-line voltages (100 VAC).

Fig. 9. Simulated waveforms for buck PFC operated with only voltage-mode control at constant duty cycle.

control, then with transient conditions such as reduced AC input voltage (e.g., brownout) or output overload, operation may transition into CCM.

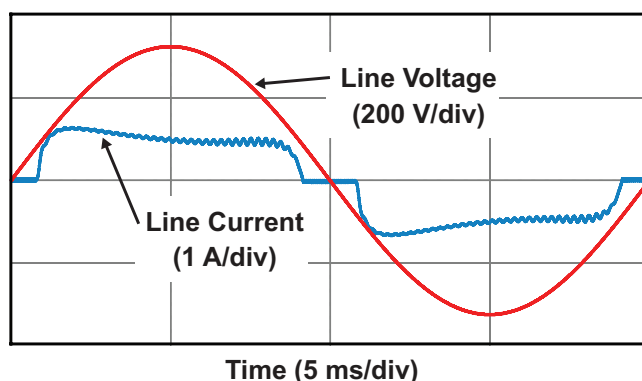
The buck PFC has also been analyzed in detail in CCM [9, 14]. Current-mode control limits the current in CCM and prevents the runaway issues cited earlier. Using current-mode control can also allow the use of clamped-current techniques, especially at low line voltages where currents increase [8, 10]. Clamped-current waveforms are deliberately non-sinusoidal, approaching a trapezoidal shape, to limit the peak current at the peak of the AC line voltage. Using clamped-current approaches can be advantageous in reducing the peak AC line current that is drawn at lower line voltages and higher power. This is particularly so at minimum line voltages, where the normally high peak currents of a sinusoidal or pseudo-sinusoidal waveform lead to much higher peak and rms currents in the PFC MOSFET and choke. The clamped-current buck PFC can still achieve good PF, while also reducing losses and improving efficiency performance at low line voltages.

Fig. 10 illustrates simulated waveforms at both high and low line when the buck PFC is operated with only current-mode control. It can be seen that the current peaking effects at low line during CCM are eliminated, and the current waveform becomes more trapezoidal in shape.

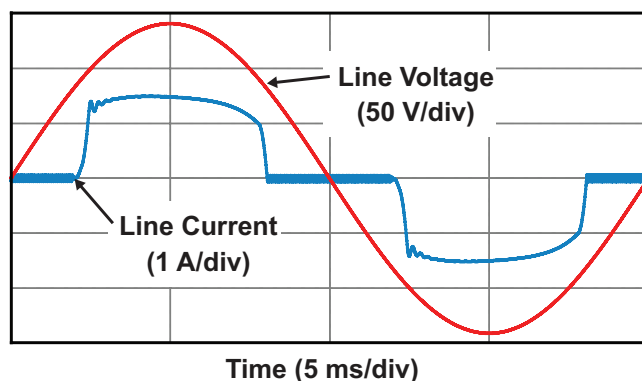
If the CCM buck PFC is operated heavily in current-mode control (with little or no added slope compensation ramp), then it is possible to practically achieve a line current shape that is very close to the theoretical “clamped-current trapezoid” [8]. However, very high current-loop gain can lead to instabilities and oscillations in the line-current waveform. Additionally, the harmonic content of the severely clamped-current waveform with a

sharp rise/fall of the current trapezoid can be problematic in meeting EN61000-3-2.

One good control approach is a mix of peak current-mode and voltage-mode control. Current-mode control is required to avoid the current runaway at the peak of AC line when in CCM. A voltage-mode slope-compensation ramp can be very usefully added to the current-sense signal to



*a. Operation is always in DCM at high-line voltages (230 VAC).*



*b. Operation is in CCM at low-line voltages (100 VAC) during peaks.*

*Fig. 10. Simulated waveforms for buck PFC operated with only current-mode control.*

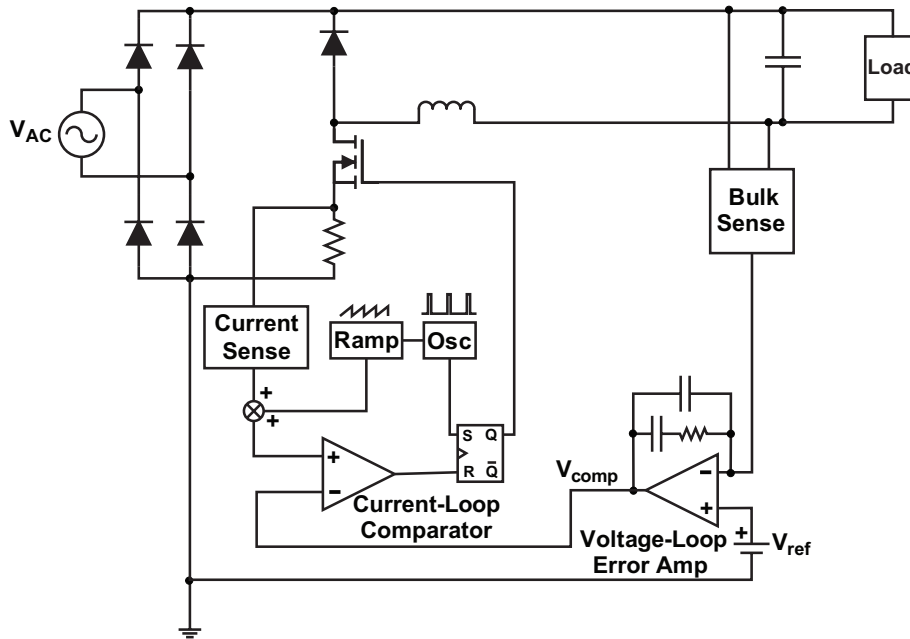


Fig. 11. Buck PFC current-control loop.

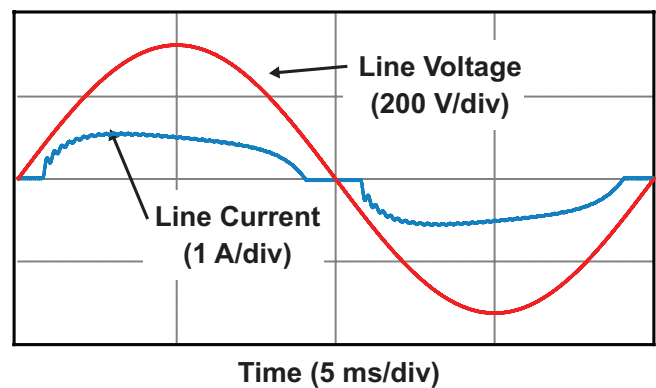
optimize this mix of voltage- and current-mode control. The added slope-compensation ramp can be used to adjust the shape of the AC line current to trade off PF performance against the harmonics limit of EN/JIS-61000-3-2. This control approach is illustrated in Fig. 11. Simulated waveforms achieved with this approach are shown in Fig. 12.

Fig. 13 illustrates actual practical circuit waveforms that were observed when only current-mode control (Fig. 13a) and then only voltage-mode control (Fig. 13b) were used. The current peaking effects are very pronounced in Fig. 13b.

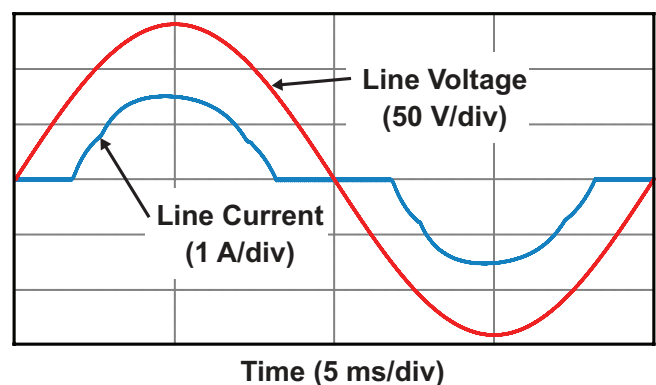
The current loop of the buck PFC has been successfully implemented with a variety of peak current-mode PWM controllers, including the industry-standard “3843,” and more recently using a dedicated buck PFC controller UCC29910 that greatly simplifies the control-loop design [15].

## H. EMC Considerations

Because a buck converter places the active control switch in the input path, with the inductor in series with the output, it is commonly assumed that the pulsating input current will be problematic from an EMC perspective. In practice, however, the pulsating input current is no worse than it would be for a similar power level with other topologies, such as DCM or transition-mode



a. Mixed current- and voltage-control modes at high-line voltages (230 VAC).

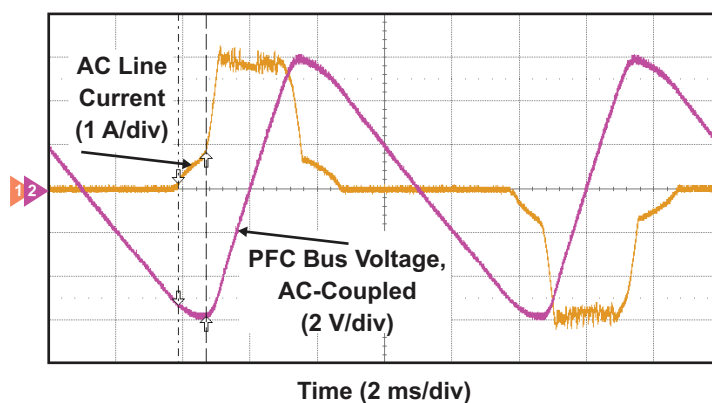


b. Mixed current- and voltage-control modes at low-line voltages (100 VAC).

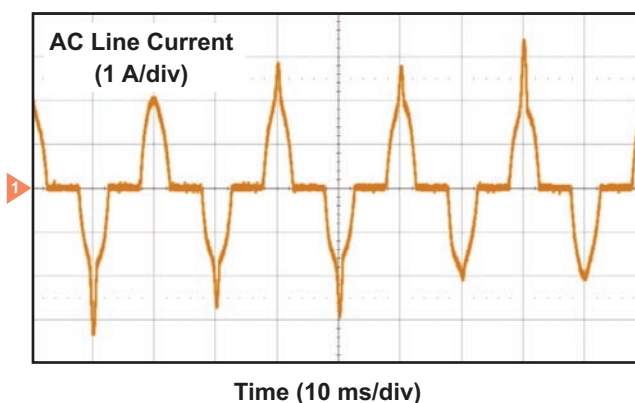
Fig. 12. Simulated waveforms for buck PFC operated in mixed control modes.

flyback, or boost. In those cases, the inductor current is allowed to go fully discontinuous, so there is also a high pulsating current in the input path. This pulsating current is typically filtered by a low-cost film capacitor as part of the EMC filter. So for the

buck PFC, the pulsating input current and filtering requirements are no worse than the transition-mode boost. Fig. 14 shows the schematic of the required EMC filter for a 100-W, buck-PFC front-end to meet EN55022 Class B with an 8-dB pass margin.



a. 90-VAC, full-load, clamped-current type waveform—high current-sense signal, low slope compensation.



b. 90-VAC, half-load, peaky-current waveform—low current-sense signal, high slope compensation.

Fig. 13. Line-current peaking and runaway effect when a buck PFC is operated in CCM with only voltage-mode control or with very low current-loop gain.

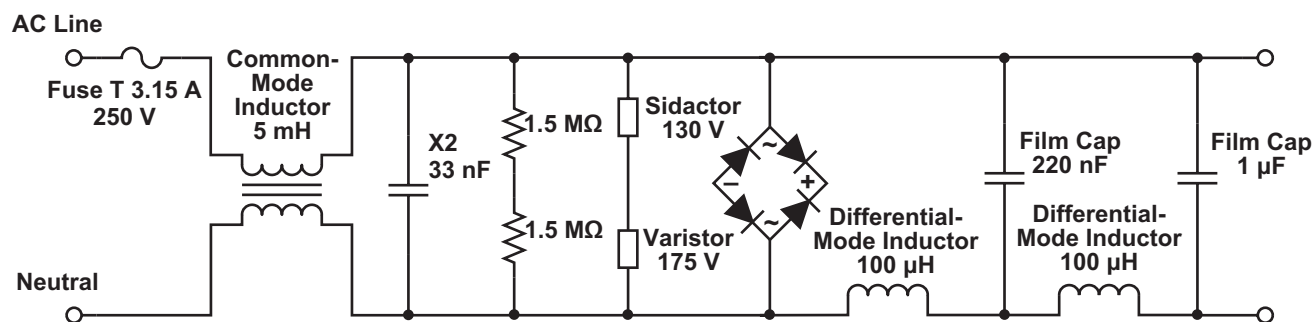


Fig. 14. Buck PFC 100-W-rated EMC filter.



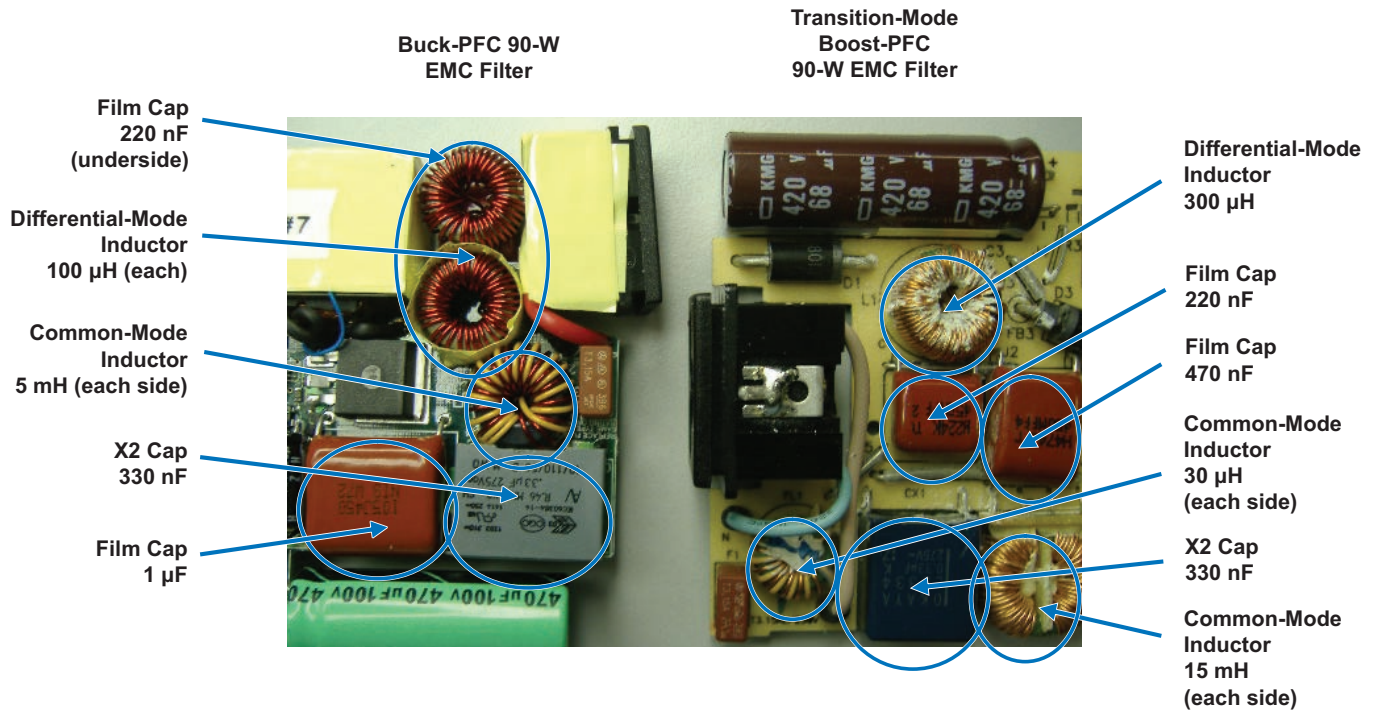


Fig. 15. Comparison of EMC filters for buck versus transition-mode boost.

Fig. 15 illustrates the size of this filter as implemented on a low-profile (16-mm total height), 90-W notebook adapter. For comparison, the required filter for a 90-W transition-mode boost circuit in similar profile is shown alongside. Note that the EMC filters are of similar size and complexity. The filter size for the buck PFC is approximately  $15 \text{ cm}^2$  ( $2.33 \text{ in}^2$ ), compared to  $17 \text{ cm}^2$  ( $2.64 \text{ in}^2$ ) for the boost circuit (adjusting for the looser packing density of the boost filter to give a fairer comparison).

The conducted EMC performance of this 90-W buck PFC stage is demonstrated in section VII. This design passes both quasi-peak (QP) and average (AV) limits of EN55022 Class-B with good margin in the worst-case configuration with an earthed load.

## VI. BUCK PFC DESIGN PRACTICALITIES AND CHALLENGES

### A. Buck PFC Power Stage Configuration

As shown in Fig. 16, the conventional buck power stage places the power switch in the high side, as is common in DC/DC converters. This necessitates the use of a high-side drive circuit to

drive the power-MOSFET gate. Alternatively, the power circuit could be inverted, as in Fig. 17, so that the power MOSFET is on the low side and thus easier to drive. This then references the output voltage to the positive rail of the input voltage, so that the output voltage is effectively floating. In this case a high-side, level-shifting voltage-sense circuit is required to generate a ground-referenced sense signal for the control circuit. With either power-stage configuration, a high-side element will always be required. Depending on the application specifics, one or the other configuration will often be preferable. In practice, the choice of power-stage polarity will depend on required cost, performance, and the nature of the downstream stage deployed.

### B. Conventional Buck Configuration

The conventional buck configuration with high-side MOSFET has advantages because the output bus voltage is referenced to the same ground as the control circuit. This allows for straightforward output-voltage sensing for control, using a simple resistor-divider network. A common ground can also be maintained between the PFC stage and

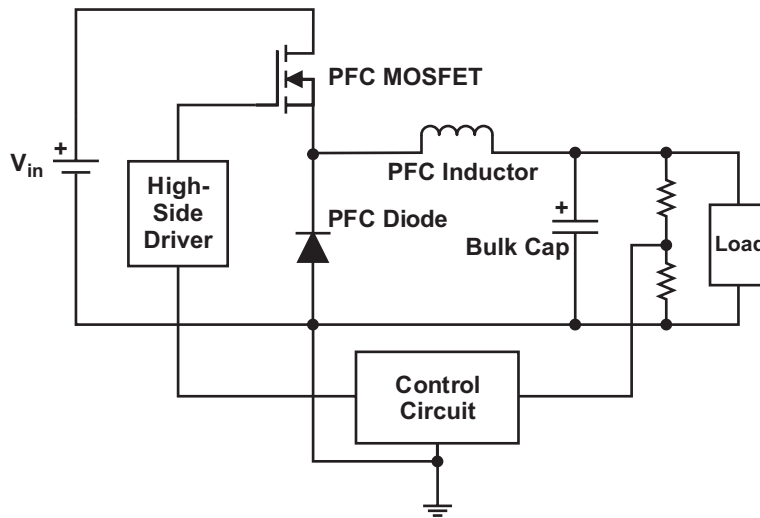


Fig. 16. Conventional buck power stage—high-side MOSFET.

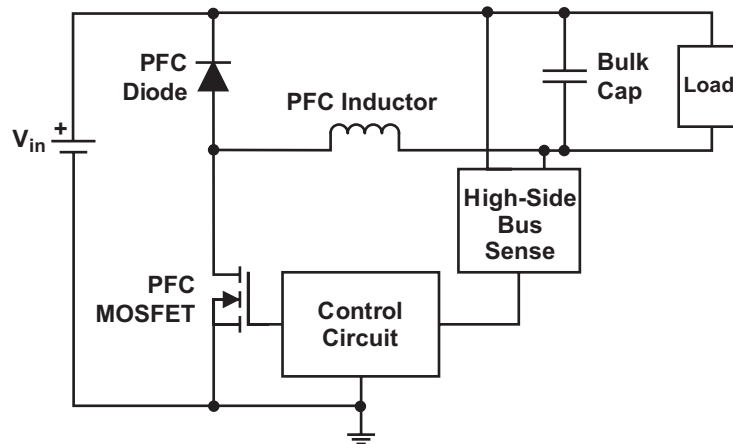


Fig. 17. Inverted buck power stage—low-side MOSFET.

downstream isolation/regulation stage, allowing a common control circuit to be deployed for both stages. This common ground also greatly simplifies voltage and current sensing of both stages by a shared “combo” control circuit. It simplifies handshaking and communications between PFC stage and isolation/regulation stage controllers, if using separate control circuits for each stage.

However, this power circuit configuration requires a floating high-side driver for the PFC MOSFET. This is a significant point—it requires the use of either a gate-drive transformer or high-side bootstrapped driver integrated circuit (IC). In either case, the design challenges are not trivial. A high-side gate-drive transformer may initially

seem attractive. However, the practical design constraints can be challenging:

- Functional isolation is required to withstand up to 400-V isolation at high line voltages.
- Transformer parasitics (especially capacitance) can cause common-mode difficulties with the drive signal.
- There is a trade-off between transformer size/cost versus performance.
- The maximum drive duty cycle will need to be limited (to maybe 80% or less) to allow the transformer to reset during the off time. This limits the buck PFC PF performance at the lowest AC line voltage.

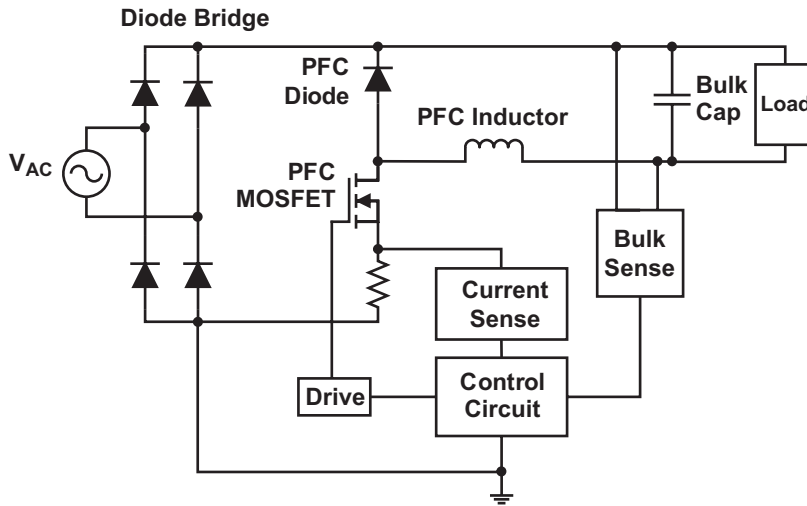


Fig. 18. Buck PFC inverted configuration with low-side PFC MOSFET.

A high-side boot-strapped driver IC is another possible solution to implement a high-side gate drive. This solution overcomes many of the drive transformer limitations, but also comes with another design challenge. Because this is a single-ended drive, there is a challenge in establishing the high-side drive rail during startup and in maintaining the rail during extended periods with no switching, such as heavy load-dump transients or light-load burst-mode operation.

### C. Inverted Buck Configuration

The buck PFC power stage may be “inverted,” and configured in an upside-down fashion as shown in Fig. 18, with the PFC MOSFET on the low side. In this case, the PFC MOSFET is referenced to the same ground as the control circuit, so the MOSFET is simply driven directly from the controller. Current sense for the low-side switch is also available very easily, without complications of negative polarity and the need for pull-up. Because of these advantages, this power-circuit configuration is deployed more often than the conventional one with a high-side MOSFET.

The main drawback of the inverted buck is that the output bus voltage is floating. The difficulty with this configuration is that the high-side referenced bus voltage must be sensed and level-shifted to the ground-referenced control circuit. There are several ways to implement this function,

as detailed below, with varying levels of performance and cost.

The second drawback with this configuration is that the buck PFC stage control will not share the same ground as the downstream isolation/regulation stage control. So common-ground “combo” controllers could not be used, and any signaling (such as fault communications) between the two stages will also need to be level shifted in a similar manner.

#### Level-Shifting V-to-I Converter

The high-side bus voltage of the inverted buck PFC may be sensed in many ways. As there is no requirement for safety isolation, just functional isolation, the task is more straightforward than sensing across an isolation barrier. Three possible schemes are briefly outlined here, but other approaches are possible.

A high-voltage PNP transistor may be connected across the high-side bus voltage as in Fig. 19 to provide a collector current that varies in proportion to the bus voltage. This current can be converted to a sense voltage by feeding into a ground-referenced resistor—with this connection, the voltage sense is also referenced to ground. This circuit is low cost, with only a few components more than a typical resistor divider. The PNP transistor needs to be rated for at least 500 V for high line-voltage operation, but these are available in suitable small surface-mount and leaded packages.

The sense voltage across  $R_{sense}$  will be related to the bus voltage as in Equation 22 below, assuming the bus voltage is sufficient to forward bias Q9.

### Differential Amplifier

A differential amplifier may also be used to sense the high-side bus voltage, as shown in Fig. 20. The circuit uses two resistor chains connected to either end of the bulk capacitor ( $C_{bus}$ ) to sense and scale the voltage difference across the bulk capacitor. The op-amp output can be readily referenced to ground by a suitable connection of R3 as shown, giving the required low-side voltage-sense signal,  $V_{sense}$ . However, a large number of resistors are required. Since two resistor chains are connected to high-voltage points, larger sized 1206 or 0805 resistors are required for voltage rating. The circuit requires a reasonably good op amp with rail-to-rail input (RRI) capability. Given the high common-mode signal content, good resistor matching is essential. Resistors with a tight tolerance of 0.1% or better and a low temperature coefficient are required.

This circuit is more expensive than the previous given the constraints on the op amp and resistors. The power dissipation of the two resistor chains will also likely be higher than the previous circuit. However, the performance of the circuit will be superior, yielding better accuracy, repeatability, linearity, and temperature stability.

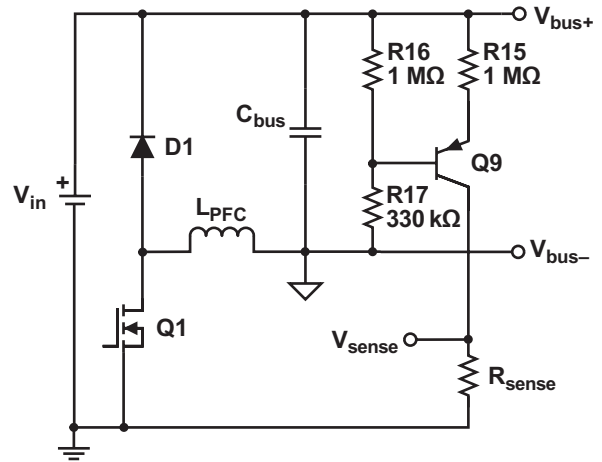


Fig. 19. High-side bus voltage-sense circuit using high-voltage PNP V-to-I converter.

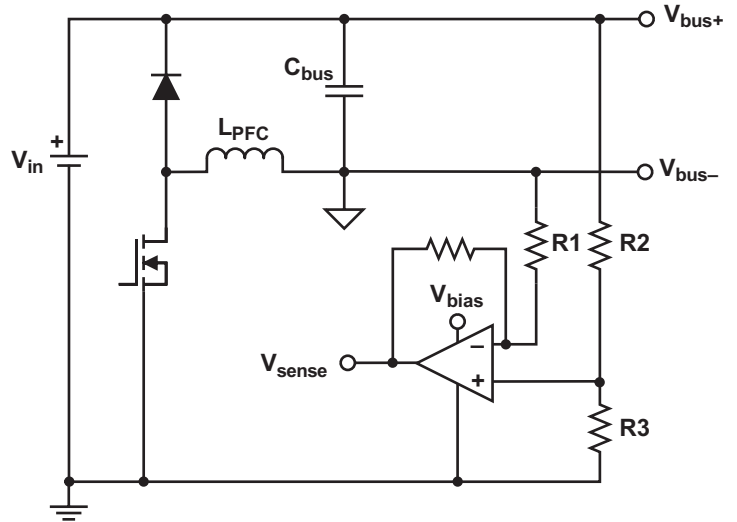


Fig. 20. Differential amplifier for high-side bus voltage sense and level shift.

$$V_{sense} = \frac{V_{bus} - V_{eb} \times \left(1 + \frac{R17}{R16}\right)}{\left[\frac{R15}{R_{sense}} \times \left(1 + \frac{1}{h_{FE}}\right)\right] \times \left(1 + \frac{R17}{R16}\right) + \left(\frac{R17}{R_{sense} \times h_{FE}}\right)}, \quad (22)$$

where  $V_{eb}$  is the PNP emitter-base forward voltage and  $h_{FE}$  is the DC current gain of Q9. This equation can also be rearranged as follows to calculate the regulated bus voltage as a function of error-amplifier reference ( $V_{ref}$ ) and chosen resistor values:

$$V_{bus} = \left[ R15 \times \frac{V_{ref}}{R_{sense}} \times \left(1 + \frac{1}{h_{FE}}\right) + V_{eb} \right] \times \left(1 + \frac{R17}{R16}\right) + \left(\frac{V_{ref} \times R17}{R_{sense} \times h_{FE}}\right). \quad (23)$$

### High-Side Error Amp Plus Optocoupler

In all applications, the scaled bus-voltage sense signal is used for the voltage regulation loop—the signal is compared to a reference by an error amplifier to generate an error signal. Fig. 21 illustrates the option of placing the voltage reference and error amplifier directly across the floating high-side bulk capacitor. The output of the error amplifier is level-shifted to the ground-referenced controller by a low-cost optocoupler. Since the optocoupler is only used to bridge high-side to low-side functional isolation rather than primary-to-secondary galvanic isolation, a low-cost device can be used.

The circuit does not suffer the accuracy or component-tolerance constraints of the previous level-shifting schemes because the actual bus voltage is not level-shifted, just the error signal. However, the bias rail used to drive the feedback optocoupler must be a regulated DC rail—any 100-/120-Hz ripple component on this rail will introduce a 100-/120-Hz ripple into the inner current loop that will reduce the PF.

### Summary of Power-Stage Configuration

Table 2 compares the advantages and disadvantages of the conventional and inverted buck power stage. Both configurations have distinct

advantages, but each one also has inherent drawbacks. Neither configuration is a clear winner over the other—the choice of configuration to use in a particular design depends on many system-level constraints and considerations.

### D. Inrush Versus Surge Immunity

Unlike the boost or flyback topology, there is no direct connection from the input to the output capacitor in a buck topology. For this very reason, the buck stage exhibits little or no inrush “sparking” at the initial application of AC power. The bulk capacitor can be very easily soft-started by appropriate drive control of the buck-PFC MOSFET. Inrush control is achieved for free, without the overhead and complications of a dedicated inrush limiter. And because there is a well-controlled inrush current, the current-sense resistor does not need a high  $I^2t$  rating, allowing the use of a small surface-mount thick-film part.

Yet, this inrush advantage is also a disadvantage when considering power line disturbances (e.g., lightning surges as defined by EN61000-4-5). The surge energy can only flow into the limited capacitance of the EMC filter. Consequently, the buck PFC requires dedicated surge-management components. The previous EMC filter circuit in Fig. 14 is an example of a proven

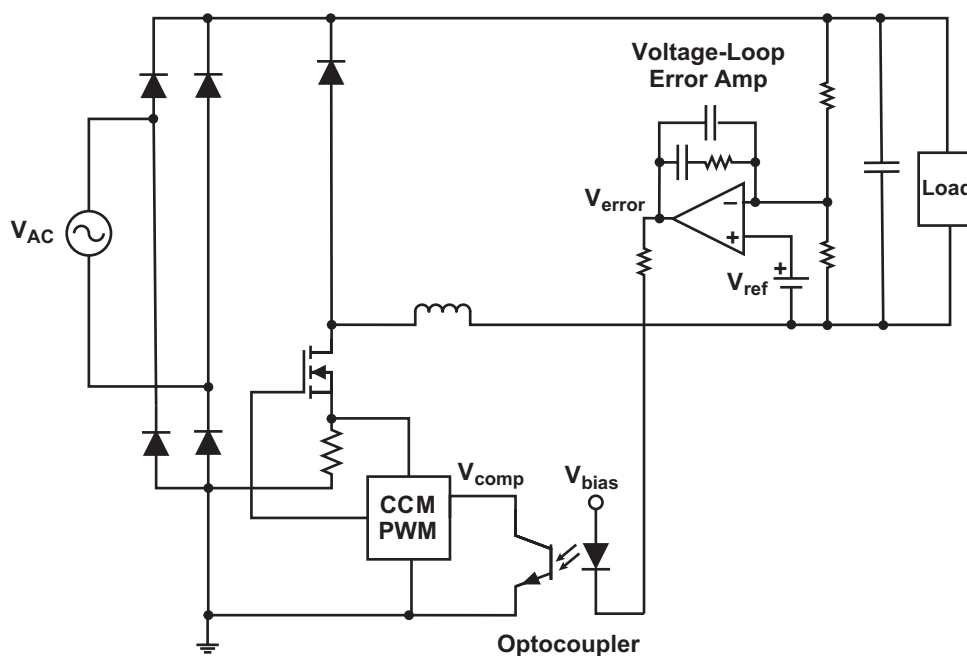


Fig. 21. High-side bus sense with error amp plus reference directly across the bus capacitor and an optocoupler for high- to low-side level shift.



**TABLE 2. COMPARISON OF POWER-STAGE CONFIGURATION ADVANTAGES AND DISADVANTAGES**

Power-Stage Configuration	Advantages	Disadvantages
<b>Conventional (High-side MOSFET)</b>	Allows use of common ground throughout system for PFC stage and regulation stage	Requires return-path current sense, inverted signal requiring pull-up offset or inversion
	Easy ground-referenced bus voltage sense	High-side driver adds cost/complexity
	Compatible with use of “combo” control IC for both stages	Transformer drive CM issues, $D_{max}$ limit for magnetic reset
	Choice of transformer or silicon driver for high-side MOSFET drive	IC drive issues with generation and maintenance of floating supply due to single-ended topology
<b>Inverted (Low-side MOSFET)</b>	Simple low-cost low-side MOSFET drive	Requires high- to low-side, level-shifting bus-voltage sense
	Ground-referenced low-side current sense	No common ground with PFC stage and downstream regulation stage
	High $D_{max}$ capability	Not compatible with “combo” controller, requires separate PFC and downstream control ICs

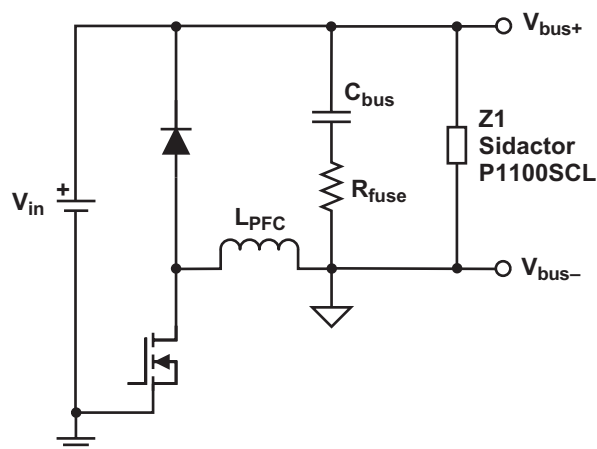
surge-management approach that allows the buck PFC to safely pass a 1-kV differential-mode surge per EN61000-4-5. This circuit uses low-voltage varistors in series with a sidactor switch—a diac-type device that is open until the voltage across it exceeds a break-over level, at which point it fires like a thyristor. Once the sidactor current exceeds a latching current level, it remains latched on until the current drops below a holding level, again just like a thyristor. The sidactor switch connects the varistors across the line whenever there is a sufficiently high surge voltage to exceed the sidactor break-over voltage, and keeps them switched out otherwise. The important criterion about varistor choice is that voltage clamping occurs below 600 V under surge conditions (to allow usage of standard 600-V rated MOSFETs and diodes) and to ensure that the varistors survive potential worst-case conduction for an AC half-cycle, assuming surge initiation at an AC zero-crossing.

### E. Bus Overvoltage Faults

For any PFC topology, in the event of an “open-feedback” situation, the control loop will advance the duty cycle toward the maximum value, potentially generating an overvoltage condition on the bus. Independent bus-overvoltage protection (OVP) is required to prevent catastrophic damage to bulk capacitors. In particular, the main PFC MOSFET is a potential issue for a buck

PFC. If the MOSFET failure is a short from drain-source, the bulk capacitor will be charged towards the peak of the AC line voltage. OVP control action that attempts to reduce duty cycle or inhibit switching will be ineffective in limiting or terminating the overvoltage event. Sustained overvoltage of the bulk capacitor can lead to venting of the capacitor and electrolyte leakage. This would be a safety agency concern, so steps must be taken to protect against such an event.

Many possible OVP schemes could be used. The challenge is to implement a circuit that is simple and low cost. The circuit shown in Fig. 22 is a very simple two-component solution. A small resistor fuse is placed in series with the bulk



*Fig. 22. Buck PFC bus overvoltage protection using “crowbar” device Z1.*

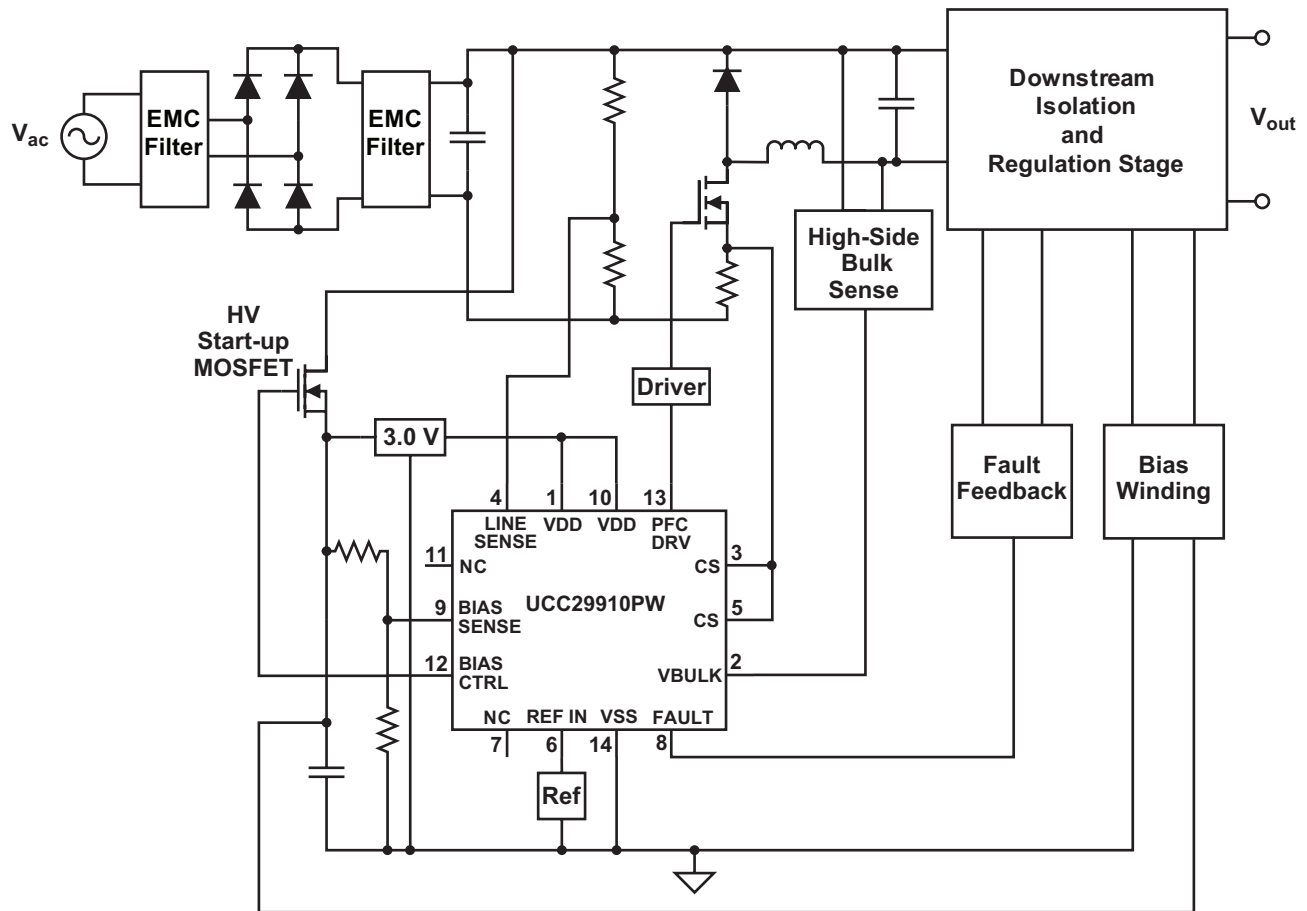


Fig. 23. Buck PFC front end as used in the 90WHD reference design to feed downstream isolation/regulation stage.

capacitors; this branch is shunted by a sidactor switch element. Under normal operation, the voltage on the bus will be below the break-over voltage of the sidactor, so it will be off. If the bus voltage increases above the break-over voltage, the sidactor will latch on, drawing a very large pulse of current from the bulk capacitance and causing the series resistor to fuse open, thereby disconnecting the electrolytic capacitors from the bus voltage to prevent venting.

## VII. BUCK PFC PERFORMANCE REVIEW: 90-W ADAPTER REFERENCE DESIGN

The buck PFC has been deployed as the PFC front-end in a 90-W, high-density, slimline notebook-adapter reference design (referred to as “90WHD”). This two-stage design uses a half-bridge isolation/regulation stage to down-convert the buck PFC bus voltage to an isolated and regulated 19.5-V output voltage [16]. Fig. 23 shows

a simplified block diagram of the buck PFC power-stage topology as deployed in this design based on a dedicated buck PFC controller, UCC29910. The 90WHD design specification is summarized in Table 3, with a photo of the final design shown in Fig. 24.



Fig. 24. 90WHD slimline, 90-W, buck-PFC adapter.

**TABLE 3. SUMMARY OF 90WHD SLIMLINE ADAPTER  
REFERENCE DESIGN SPECIFICATION**

Output power (continuous/peak)	90/110 W
Adapter dimensions (L x W x H)	90 x 67.5 x 16 mm (3.54 x 2.66 x 0.63 in)
EMI-conducted and radiated	EN55022 Class B
Output voltage, $V_o$	19.5 V $\pm$ 1 V
Output voltage total regulation	18.5 V to 20.5 V (At end of 6-ft cord, 16 AWG)
Output current	0 to 4.62 A (continuous)
Peak output current	5.62 A for 4 s (max)
$V_{in}$	90 to 264 VAC (47 to 63 Hz)
Efficiency (at 100% load, minimum line)	92.50% min (not including cable losses)
ENERGY STAR	Efficiency >89% average at 25%, 50%, 75% and 100% load; no-load power draw < 0.5 W; efficiency at 0.5-W load > 50%
PF at 115 VAC 60 Hz (90 W)	0.94 (typ)
PF at 230 VAC 50 Hz (90 W)	0.96 (typ)
Output ripple/noise	250 mV (typ), 400 mV (max)
Output transient load step	50% of rated load
Output transient voltage undershoot	1.5 V maximum
Overcurrent inception level	105% to 135% of peak load
Short-circuit protection	Unlimited, unconditional, latching. 10-ms activation delay
Overvoltage protection	26 V (max)
Turn on AC input to $V_o$	1 s (typ)
$V_o$ rise time	40 ms (typ) (10% to 90%)
$V_o$ fall time	100 ms (max)

### A. Buck PFC Front-End Performance

Figs. 25 and Fig. 26 demonstrate the efficiency performance of the buck PFC front-end stage as used on the 90WHD adapter design. These curves

show the efficiency of only the PFC stage, as both line voltage and load vary. Efficiency performance is pretty consistent over the full universal mains range and over the majority of the load range.

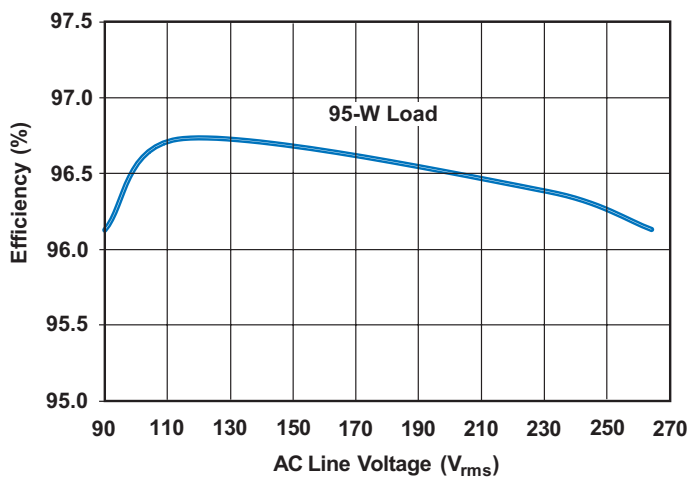


Fig. 25. Buck PFC front-end full-load efficiency versus AC line.

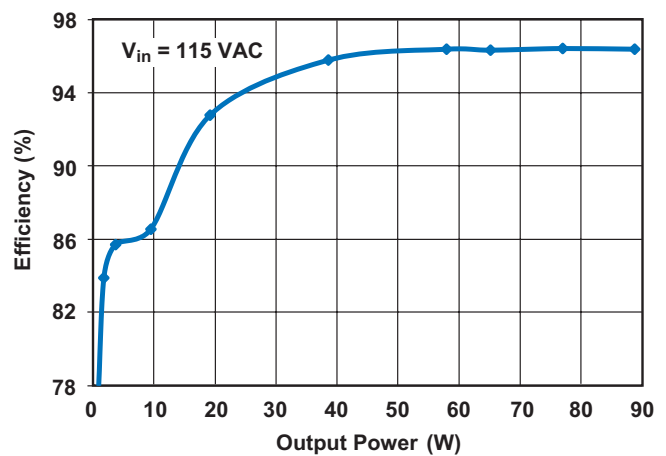
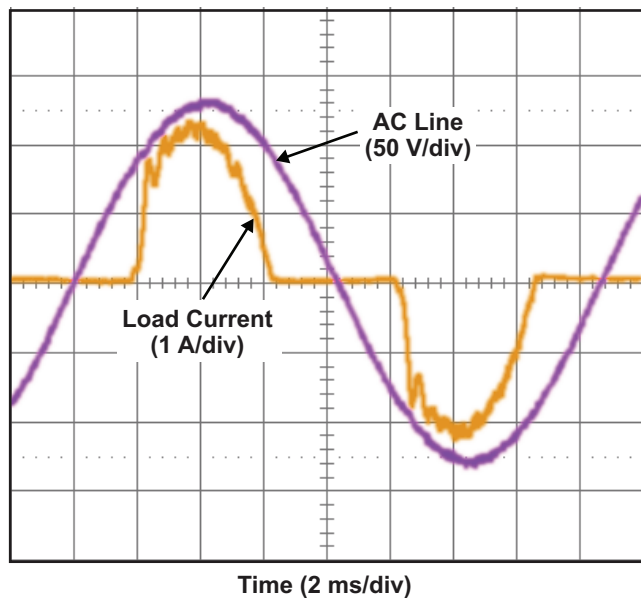


Fig. 26. Buck PFC front-end efficiency versus load at 115 VAC.

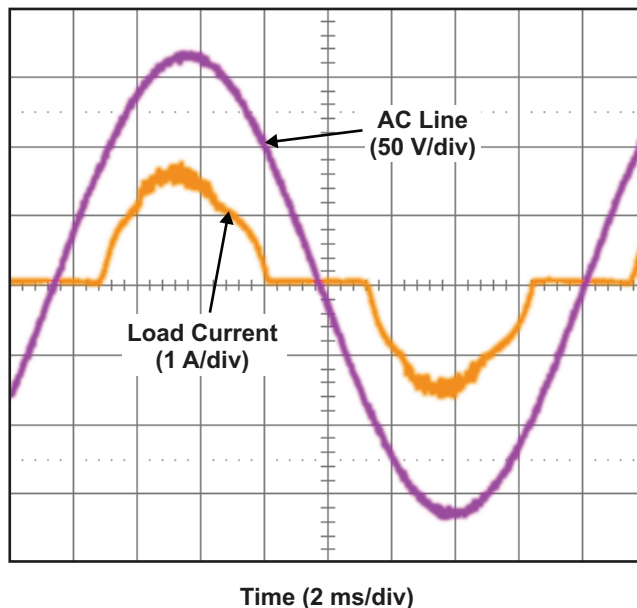
Fig. 27 demonstrates the line-current wave shape achieved at full load at various AC line settings, together with the actual THD and PF in each case. Fig. 28 summarizes the PF performance versus line and load.

## B. Overall Two-Stage Adapter Performance

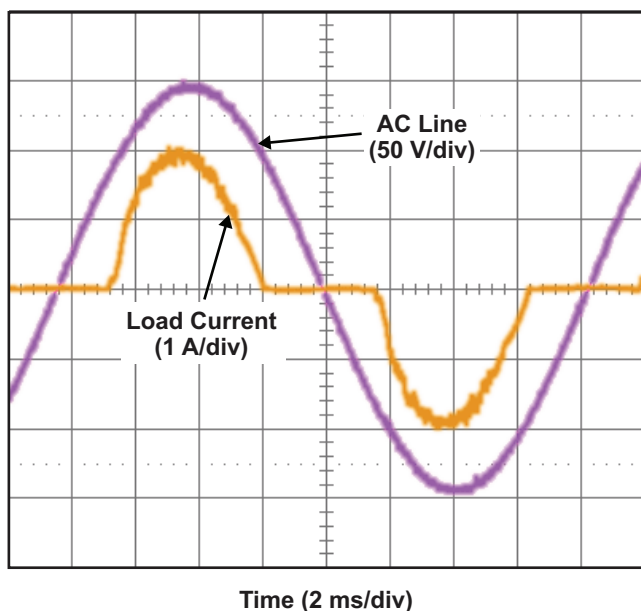
The following data illustrates the overall two-stage 90WHD adapter performance for the buck PFC front-end plus the downstream half-bridge



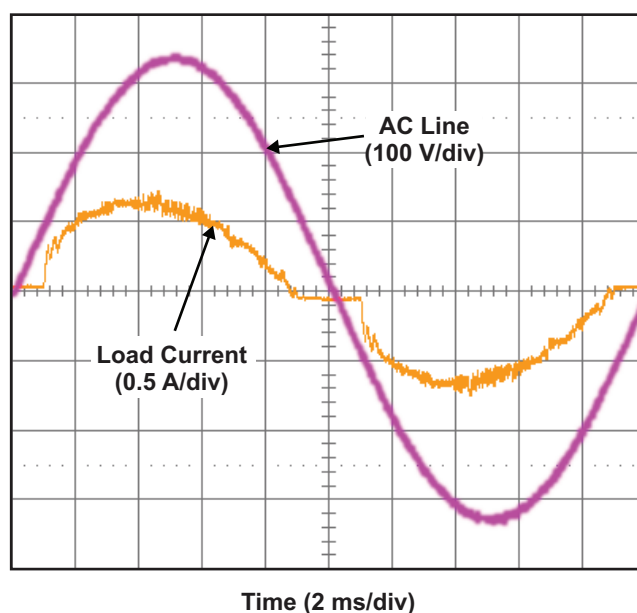
a. 90 VAC/60 Hz at full load with  
THD = 50.9% and PF = 0.889.



c. 115 VAC/60 Hz at full load with  
THD = 34.1% and PF = 0.944.



b. 100 VAC/60 Hz at full load with  
THD = 47.8% and PF = 0.902.



d. 230 VAC/50 Hz at full load with  
THD = 16.7% and PF = 0.966.

Fig. 27. AC line-current wave-shapes at full load for the 90WHD adapter.

isolation/regulation stage. Fig. 29 and Table 4 illustrate the efficiency performance up to full load, and Fig. 30 shows the efficiency over only the light load range (up to 10 W). Table 5 provides the no-load/standby power consumption of the adapter and it is well below the ENERGY STAR limit of 0.5 W. Fig. 31 illustrates typical conducted-EMC performance and shows a good pass margin against EN55022 level B.

**TABLE 4. SUMMARY OF 90WHD AVERAGE EFFICIENCY AT PCB LEVEL, NOT INCLUDING OUTPUT CABLE LOSS**

Input Voltage	Efficiency				
	25%	50%	75%	100%	Average
115 VAC	91.00%	93.00%	93.50%	93.10%	92.65%
230 VAC	88.55%	91.85%	92.65%	92.84%	91.47%

**TABLE 5. SUMMARY OF 90WHD NO-LOAD POWER CONSUMPTION**

Input Voltage	No-Load Input Power	Spec Limit
115 V	0.160 W	0.5 W
230 V	0.230 W	0.5 W

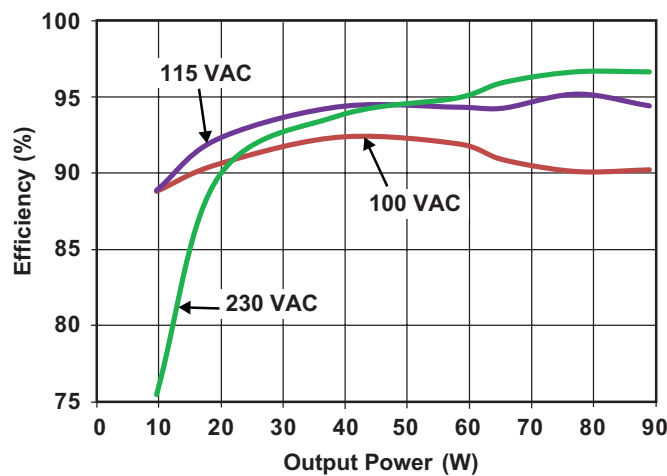


Fig. 28. Buck PFC PF versus line voltage and load for the 90WHD adapter.

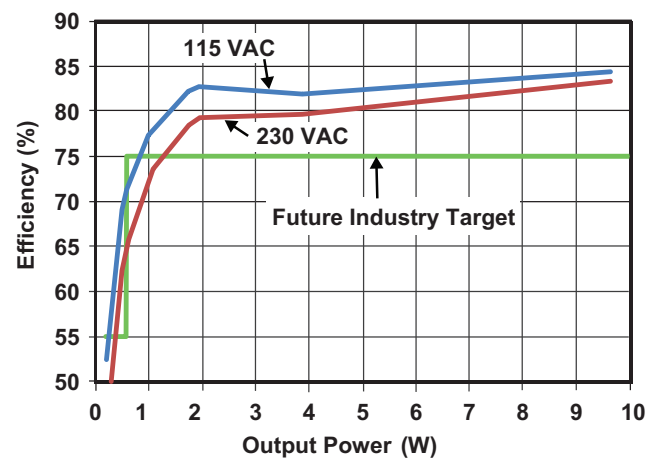


Fig. 30. Overall light-load (<10 W) efficiency performance.

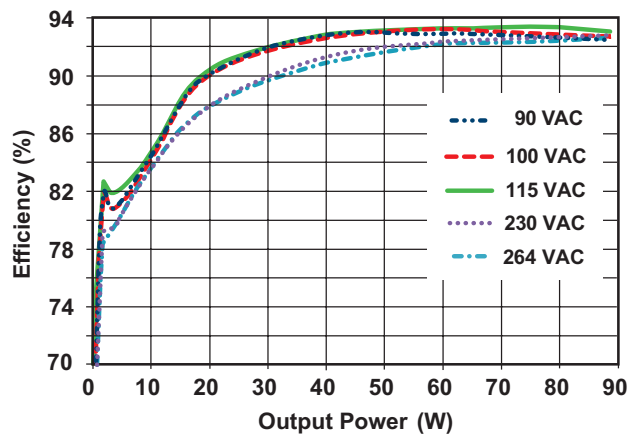


Fig. 29. Overall efficiency performance versus AC line and load.

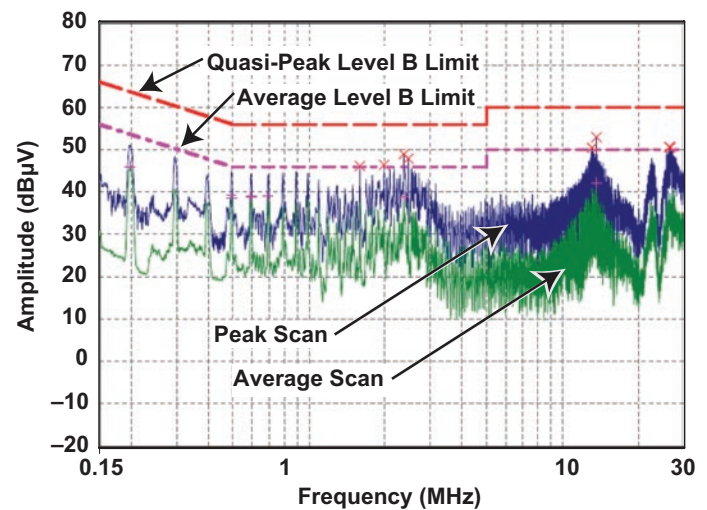


Fig. 31. 90WHD conducted EMC at 230 VAC with earthed load (worst-case operating point), showing minimum pass margin of 8 dB.



## VIII. CONCLUSION

The buck PFC topology can demonstrate excellent full-load efficiency of better than 96% at the lowest line voltage (90 VAC), typically the performance bottleneck operating point for boost PFC designs over the universal mains range. This level of high-efficiency performance is maintained over the full universal line-voltage range. This enables the design of very small format, low-profile AC/DC converters such as notebook adapters with power densities in excess of 16 W/in<sup>3</sup>.

Furthermore, the topology enables high efficiency over the full load range. Through use of the additional smart-burst mode controls provided by the UCC29910 buck PFC controller and UCC29900 ICC controller, overall two-stage efficiency performance can be further enhanced—achieving light-load efficiency of >80% at a mere 5% of full loading.

The inherent line-current cross-over distortion of the buck PFC topology does limit achievable PF—clearly it is not a suitable topology for all applications. For those applications that do not require very low THD performance, it offers a valuable solution to achieve good PF performance (>0.9 minimum, 0.95 at nominal line) while simultaneously delivering excellent efficiency.

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## APPENDIX A. POWER FACTOR, DISTORTION FACTOR, THD AND DISPLACEMENT FACTOR EXPLAINED

The terms “power factor,” “displacement factor,” “total harmonic distortion (THD),” and “distortion factor” and the relationship between them can be confusing. These terms are very thoroughly explained in Reference [17] and are summarized here.

Power factor (PF) is the ratio of real power (in watts) to apparent power (as a product of voltage and current, or VA):

$$PF = \frac{\text{Real Power (W)}}{\text{Apparent Power (VA)}}. \quad (\text{A-1})$$

Real power (also referred to as average power) is the average over a time interval T of the product of instantaneous voltage and current:

$$\text{Real Power (W)} = P_{\text{avg}} = \frac{1}{T} \int_0^T v(t) \times i(t) dt. \quad (\text{A-2})$$

Apparent power, S, sometimes referred to as complex power, can be shown to be the product of rms voltage and current, as in Equations A-3 and A-4:

$$S = \sqrt{\frac{1}{T} \int_0^T v^2(t) dt} \times \sqrt{\frac{1}{T} \int_0^T i^2(t) dt} \quad (\text{A-3})$$

$$\text{Apparent Power} = S = V_{\text{rms}} \times I_{\text{rms}} \quad (\text{A-4})$$

Because voltage, current and apparent power are all complex numbers (i.e., phasors or vectors with both an associated amplitude and phase), apparent power can be recognized as comprising real power (the real part of the complex number) and reactive power (the imaginary part of the complex number).

Periodic complex voltage and current waveforms may be represented by a sum of sinusoidal components at each and every multiple of the fundamental frequency of the waveform. Each individual sinusoidal component is referred to as a harmonic, and each harmonic will have an associated amplitude and phase.

The simplest example is that of a purely sinusoidal voltage source connected to a purely resistive load. In this case, both voltage and current

will be pure sinusoids, at the same frequency and in phase, so real power will equal the product of voltage and current. So in this case, PF will be unity. If the load is somewhat capacitive or inductive, however, then the current will still be sinusoidal at the same frequency as the voltage and there will be a phase angle  $\phi$  between the current and voltage. In this case the real power will be:

$$P_{\text{avg}} = V_{\text{rms}} \times I_{\text{rms}} \times \text{DispF}, \quad (\text{A-5})$$

where

$$\text{DispF} = \text{Displacement Factor} = \cos\phi; \quad (\text{A-6})$$

thus the PF will be

$$PF = \frac{P_{\text{avg}}}{S} = \frac{V_{\text{rms}} \times I_{\text{rms}} \times \text{DispF}}{V_{\text{rms}} \times I_{\text{rms}}} = \cos\phi. \quad (\text{A-7})$$

In this case, PF will be equal to the phase displacement factor. Where the current that flows is non-sinusoidal, Fourier analysis can determine the fundamental frequency component ( $I_1$ ). Real power is only transferred by the product of voltage and current components that are in phase and at the same frequency. Only similar frequency voltage and current harmonics can transfer power, and that transferred power is reduced as the phase angle between the voltage and current harmonic increases. The real power in this case will be:

$$P_{\text{avg}} = V_1 \times I_1 \times \cos\phi. \quad (\text{A-8})$$

Apparent power will be  $V_{\text{rms}} \times I_{\text{rms}}$ , as before. Thus in this case PF will be:

$$PF = \frac{V_1 \times I_1}{V_{\text{rms}} \times I_{\text{rms}}} \times \cos\phi. \quad (\text{A-9})$$

For AC power supplies, it can be assumed that the AC supply voltage is a perfect sinusoid with no distortion, such that  $V_{\text{rms}} \approx V_1$ . This simplifies the PF relationship to an analysis of the current waveform:

$$PF = \frac{I_1}{I_{\text{rms}}} \times \cos\phi. \quad (\text{A-10})$$

The distortion factor (DF) of the current waveform is the ratio of the fundamental frequency component to the total rms value:

$$DF = \frac{I_1}{I_{rms}}. \quad (A-11)$$

Fourier analysis can express the total rms current in terms of its individual harmonics:

$$I_{rms} = \sqrt{\frac{1}{T} \int_0^T i^2(t) \times dt} = \sqrt{\sum_{n=1}^{\infty} i_n^2}, \quad (A-12)$$

or

$$I_{rms} = \sqrt{I_1^2 + \sum_{n=2}^{\infty} i_n^2}. \quad (A-13)$$

The THD of the current waveform can be defined as:

$$THD = 100\% \times \frac{\sqrt{I_{rms}^2 - I_1^2}}{I_1}, \quad (A-14)$$

or alternatively:

$$THD = \frac{\sum_{n=2}^{\infty} i_n^2}{I_1}. \quad (A-15)$$

To summarize the most important relationships:

$$DF = \frac{1}{\sqrt{1 + THD^2}}, \quad (A-16)$$

$$THD = \sqrt{\frac{1}{DF^2} - 1}, \quad (A-17)$$

$$PF = DF \times \text{DispF}, \quad (A-18)$$

and

$$PF = \frac{1}{\sqrt{1 + THD^2}} \times \cos\phi. \quad (A-19)$$

## APPENDIX B. BUCK PFC POWER FACTOR LIMITATIONS

Extensive analysis of the buck PFC harmonics performance has been published, utilizing various methods of control and current wave shapes [8, 9, 10]. Many of these analyses have primarily explored the possible THD and line-current harmonics performance achievable and maximum power levels that can be delivered within the limits of EN61000-3-2. However, EN61000-3-2 does not impose any requirement for a minimum full-load PF. A current wave shape containing 90% of the maximum allowed harmonic current for each and every harmonic covered by the standard would have a THD of 85%, resulting in a PF as low as 0.76 (assuming displacement factor of unity). More recent initiatives such as ENERGY STAR EPS 2.0 have started mandating a minimum PF value of 0.9, which actually imposes much tougher requirements on THD. This puts a different perspective and constraint on buck PFC performance. Nonetheless, 0.9 PF is readily achievable with the buck PFC, even at low line voltages.

In the basic topology overview, some typical current waveforms were drawn. Three such waveforms have been simulated and analyzed for harmonic content, distortion factor and maximum possible power factor. The simulation assumed a nominal bus voltage of 80 VDC for the buck output with an assumed infinite buck-output capacitor (i.e. zero ripple on the buck output). Fig. B-1 illustrates the different waveforms, referred to as A (modified sine, where current is proportional to the input/output voltage differential during the conduction angle), B (truncated sine, where the

current is proportional to the input voltage during the conduction angle), and C (clamped-current “trapezoid,” where current is constant during the conduction angle). The resulting potential harmonic content and power factor (neglecting the effects of phase displacement) are summarized in Table B-1. The analysis was confined to low-line 100 VAC, since this is the operating point where PF is most challenged. At 230 VAC, cross-over distortion is much less and good PF is readily achieved.

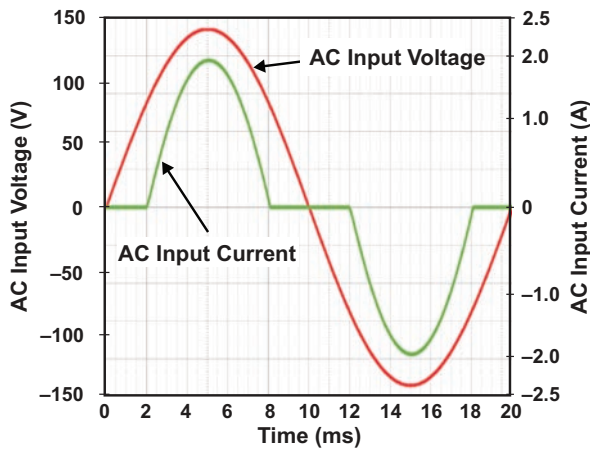
Analysis shows that there is a trade-off between the PF and individual harmonic content, depending on the current-control technique used and the shape of the AC line current. Waveform A (modified sine) has very low harmonic content at higher orders, but is dominated by a large third harmonic. This waveform passes the requirements of EN/JIS-61000-3-2 very easily, since those standards permit a high degree of third harmonic. However, the third harmonic results in a quite high THD of 44%, limiting potential performance at 100 VAC to 0.91 maximum PF (neglecting phase shift and other sources of distortion). In effect, the slow rate of current rise and fall within the conduction angle is good for limiting high-order harmonics, but results in poor utilization of the already limited conduction angle of the buck PFC, with limited PF.

Waveform B (truncated sine) has a faster rate of current rise and fall within the conduction angle and better use of the available window. Consequently, Waveform B has a much lower

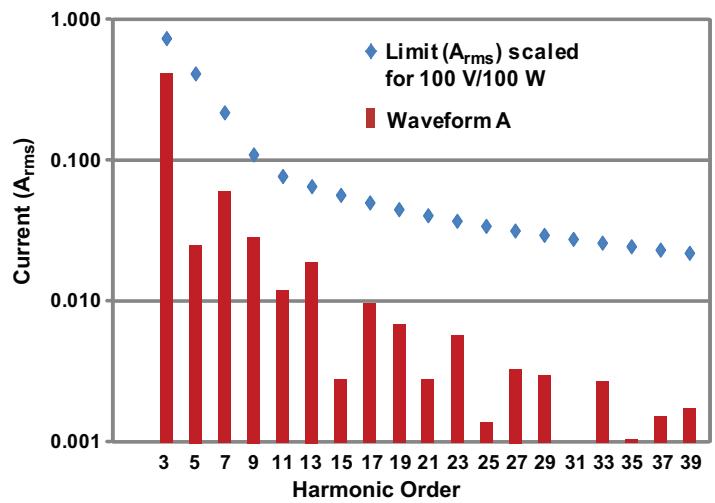
**TABLE B-1. SUMMARY OF SIMULATED WAVEFORM THD AND PF**

Parameter	Waveform A	Waveform B	Waveform C
$I_{rms}$ (total)	1.0886	1.0362	1.0527
$I_{1(rms)}$	0.9953	0.9866	1.0008
Real Power (W)	99.53	98.66	100.1
THD (%)	44.3	31.9	32.62
Distortion Factor	0.914	0.953	0.9507
Max Possible PF (no phase displacement)	0.914	0.953	0.9507

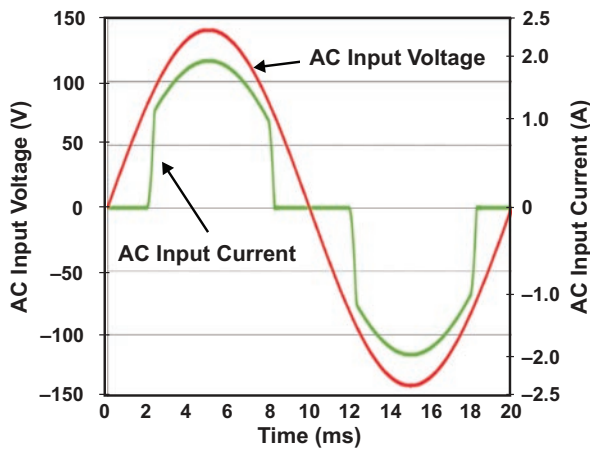




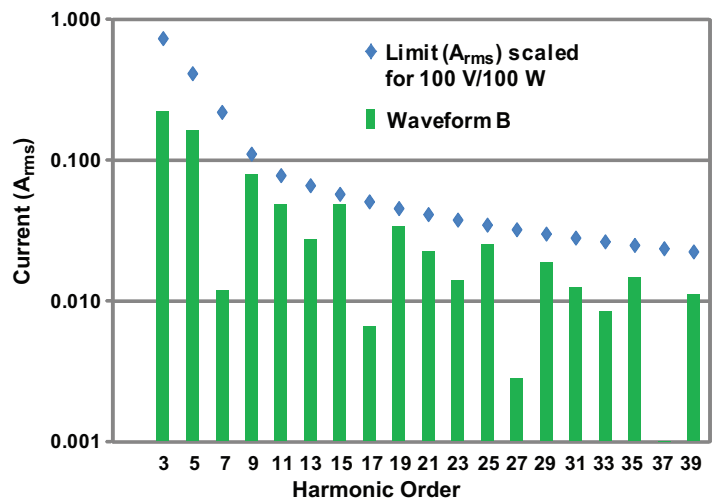
THD = 44.3% Maximum Possible PF = 0.914



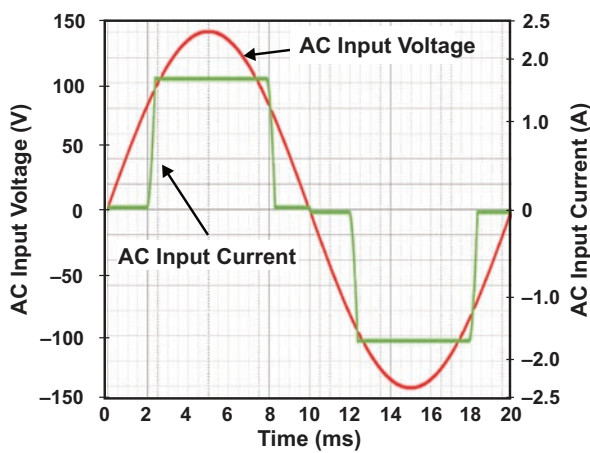
a. Waveform A. Modified sine and harmonic content.



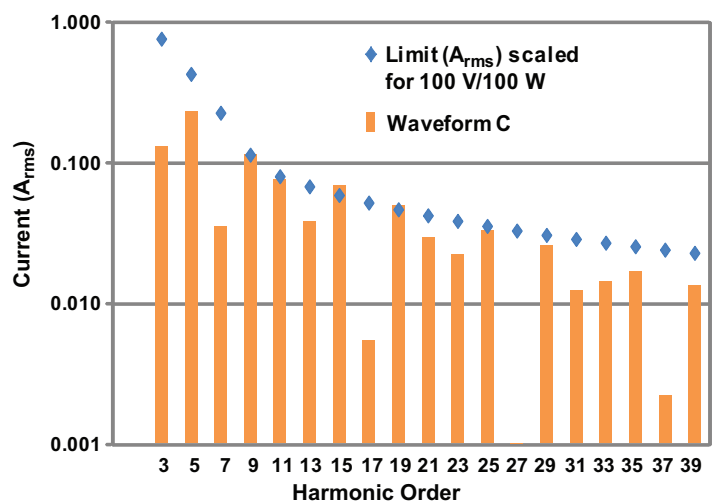
THD = 31.9% Maximum Possible PF = 0.953



b. Waveform B. Truncated sine and harmonic content.



THD = 32.62% Maximum Possible PF = 0.9507



c. Waveform C. Clamped-current trapezoid and harmonic content.

Fig. B-1. Buck PFC simulated current waveforms and their harmonic analyses.

third-harmonic content than waveform A. Within the conduction angle, the current shape is approximately sinusoidal, in proportion to instantaneous AC line voltage. This results in 32% THD, corresponding to a potential maximum PF performance of 0.952. Waveform B has a greater content of higher order harmonics due to the higher  $di/dt$  of the current at the “shoulders” of the waveform. This simulation assumed a  $di/dt$  of 4 A/ms, which is quite steep, and shows some harmonics that are close to the JIS61000-3-2 limits, particularly the 15th. Thus, careful design is required to ensure that all harmonics are kept within harmonic limits while still maximizing PF. In practice, besides the action of the current-control loop, the  $di/dt$  of the current is also limited by circuit practicalities such as filter impedance, PFC choke inductance, and control circuit  $D_{max}$ , so that slower  $di/dt$  values will usually occur.

Waveform C (clamped current trapezoid) is a variation of the truncated sine waveform B, where the sinusoidal variation is clamped, resulting in a flat-topped trapezoidal waveform. This type of waveform has been previously analyzed [10]. This also has a fast but limited rate of current rise and fall within the conduction angle. Waveform C has a very similar 32% THD and 0.952 PF, but the clamped current nature can offer an efficiency advantage, since the average and rms current flowing in the bridge rectifiers, PFC MOSFET, and choke will be lower. However, while the THD and PF are similar to waveform B, the harmonic distribution is different—in this case there is a greater higher-frequency content, while the EN/JIS61000-3-2 limits are much lower. This waveform actually fails harmonic limits at some frequencies (9th, 15th, and 19th), and comes very close at several others (11th, 25th, and 29th).

Some interesting conclusions can be drawn from these results. THD and PF are heavily influenced by the third harmonic, as evidenced by waveform A analysis. Waveforms with a low third harmonic but quite high levels of higher order harmonics can result in better PF performance, as evidenced by waveform B. Somewhat similar waveforms, with similar THD and PF, can result in quite different harmonic content—waveform B passes EN61000-3-2 while waveform C fails; yet both have almost identical PF.

### ***Practical Issues that Degrade Buck PFC PF***

Besides the current wave shape, many other practical factors affect PF. These can cause either current phase displacement of the fundamental component or increase current distortion and harmonic content. Many of these factors are problematic for all PFC topologies. Where noted, some are specific to the buck PFC.

- EMC-filter film-capacitor displacement current is problematic for all topologies.
- Voltage-loop bandwidth and resultant control-signal ripple at 100/120 Hz are more of a problem for the buck PFC due to a higher bus-ripple percentage.
- Bulk-capacitor ripple phase-shift effect is particular to the buck, where the bus ripple causes the conduction to be phase shifted, adding to filter-capacitor displacement effects.
- Circuit practicalities that limit current  $di/dt$  at the start/end of the conduction angle:
  - Source impedance.
  - PFC-choke inductance value.
  - Control-circuit maximum duty-cycle limit.

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