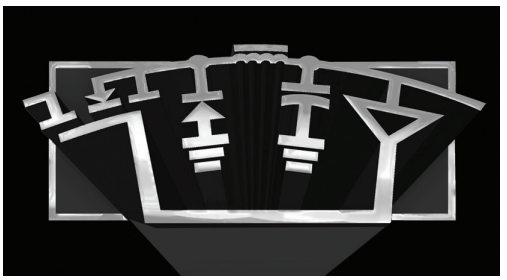

Power Supply Design Seminar

Exposing the Inner Behavior of a Quasi-Resonant Flyback Converter

Reproduced from
2012 Texas Instruments Power Supply Design Seminar
SEM2000, Topic 3
TI Literature Number: SLUP302

Power Seminar topics and online power-training modules are available at:
ti.com/psds

Texas Instruments

Exposing the Inner Behavior of a Quasi-Resonant Flyback Converter

Lisa Dinwoodie

ABSTRACT

Deciding that a flyback converter is the best choice for a given application is just the beginning of a long list of decisions you need to make when designing a power converter to meet specific requirements. Each choice in the design process will affect the performance and overall efficiency of the final product. But as each specified requirement rises to the top of your must-have list, the inevitable compromises will impact other requirements. In this paper, I'll present a simple and practical discussion about the decisions you must make during the design flow, and how to live with your choices.

I. INTRODUCTION

The overwhelming majority of isolated power supplies less than 50 Watts (W) are flybacks. Flyback converters are ideal for set-top boxes (typically 10 W to 35 W), chargers and auxiliary bias supplies (3 W to 5 W). They're also common in notebook computers, which can require as much as 120 W of power.

Flyback converters offer many advantages over other topologies that compete for this low- to mid-power range. The single magnetic component used in a flyback converter – although commonly referred to as a transformer – behaves as a coupled inductor, combining the functions of energy storage, energy transfer and isolation. Eliminating the need for a separate LC filter on each output greatly reduces the overall cost of multiple output designs.

Cost alone makes flyback converters a preferred topology in today's mass-market production world. But its advantages don't stop with the bill of materials. This superhero of converter topologies can accommodate a wide-input voltage range and have outputs higher or lower than the input voltage; the number of outputs is limited only by the number of available pins on the transformer bobbin.

Discontinuous current-mode (DCM) flybacks offer better line and load transient response when compared to continuous current-mode (CCM) flybacks, primarily because the inductance required for discontinuous current is smaller than that required for continuous current. DCM flybacks are also easier to compensate because their right half-plane zero is beyond the half-switching frequency of the converter – something that can't be said for CCM flybacks.

Lest you get the impression that flybacks are perfect and should be used everywhere, you will have to make compromises if you choose this topology. That single magnetic that heretofore has been so good at providing multiple outputs, ensuring isolation and reducing overall parts count? It is actually poorly utilized and fairly bulky when compared to other converters at the same power level because it provides energy storage as well as energy transfer. Cross-regulation of the outputs is dependent upon the coupled inductance and output load. Lightly loaded slave windings will tend to have higher output voltages when the main output is heavily loaded. Because of this, a post-regulator is often used when tight voltage regulation is required on each output.

DCM flybacks, although easy to compensate, have very high peak currents and sharp switching edges that require large input filters in order to meet electromagnetic interference (EMI) standards. These high peak currents also reduce the practical power limitation of flybacks. A 500-W flyback may be theoretically possible, but problems will arise when trying to find space for

that bank of output capacitors that you will need to meet the resultant huge output current ripple. Applicable power is also limited because the primary inductance value is inversely proportional to the required power. High power will require a relatively tiny inductance, but it is just not sensible to use an inductance so small that the circuit parasitics will completely dominate. That would lead to an unreliable design that would never be robust enough to be practical in a mass-market production lot.

Even when considering the drawbacks, power supplies that are within the appropriate power range, are cost-conscious, have a nominal number of outputs and require isolation are ideal candidates for flybacks. But once you've selected the flyback, the decisions made while winding down the design path should exploit its advantages and mitigate its less-than-ideal aspects so that a reliable, cost-effective and efficient converter is the result.

A. Quasi-What?

There have been many papers already written about flybacks. For the 2010-2011 Power Supply Design Seminar, Jean Picard's "Under the Hood of Flyback SMPS Designs" detailed the influence of parasitics on flyback behavior; most switched-mode power supply design textbooks cover flyback converter basics extensively. (See the references section at the end of this paper.) But this particular discussion is about quasi-resonant (QR) flyback converters.

What exactly is a QR flyback? Start with the adjective quasi, which means "having some resemblance usually by possession of certain attributes" or "resembling in some degree." In "Resonant Mode Converter Topologies," from the 1988 Power Supply Design Seminar, Bob Mammano described a resonant converter as a power-conditioning system that uses a resonant LC circuit as part of the conversion process. A resonant converter is a converter whose switching occurs when the sinusoidal-shaped voltage and/or current goes through zero, resulting in an almost lossless transition. The power waveforms of resonant converters are sinusoidal. Figure 1 shows an example in the waveform shape of the drain current, I_D.

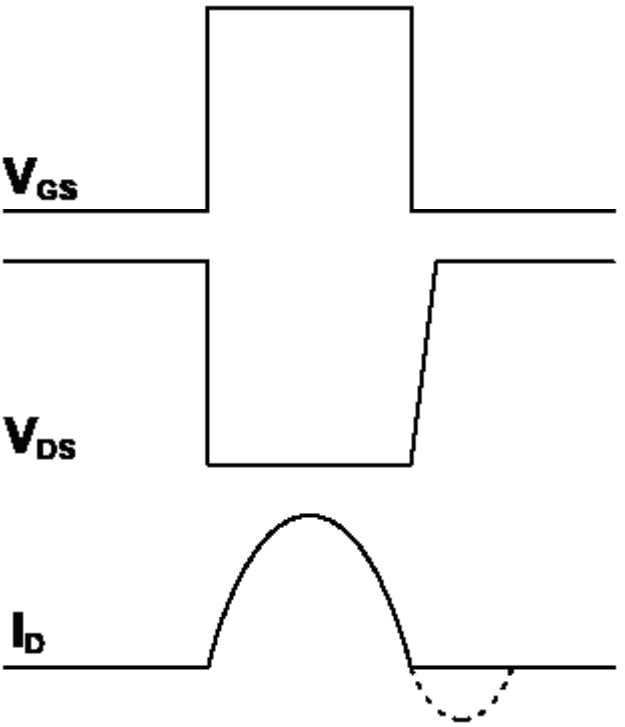

Figure 1 – Power waveforms of a typical resonant converter.

A quasi-resonant converter is sort of like a resonant converter, but not quite. The power waveforms in a quasi converter aren't sinusoidal like in a true resonant converter; a QR flyback still retains the distinct, familiar flyback waveform shapes. The difference between a QR flyback and a traditional flyback is simply that the irritating ringing caused by the circuit parasitics is put to actual use. The resonance referred to as "quasi" is not contained in the power portion of the switching cycle, but after the core has demagnetized, in the dead time; this resonant ringing is used as an indicator for the controller to initiate the next switching cycle.

Because there is no dead time in CCM flybacks, QR flybacks are forced to operate in DCM or on the edge of DCM/CCM operation, referred to as transition mode (TM) or critical conduction mode. Figure 2 shows the difference between the drain-to-source waveform of a DCM flyback that does not switch on the resonant valley and a TM flyback that does switch on the resonant valley.

Figure 2 – Comparison of drain-to-source voltage waveforms of DCM and TM flybacks.

B. The Quasi-Resonant Advantage

A quasi-resonant converter is actually a soft-switcher; utilizing an available resonant LC, the switching occurs at the valley of the resonant ring generated by the primary inductance and the parasitic capacitance of the circuit. Thus, its initial advantage could be its resourcefulness; there's no need to add Ls and Cs because this circuit uses what is already there. Quasi-resonant describes the soft switching action of the metal-oxide semiconductor field-effect transistor (MOSFET).

Soft switching has many advantages, most notably the reduction of switching losses. Turning on the MOSFET switch at the valley of the resonant ring – where the drain-to-source voltage is lowest – results in lower losses associated with the output capacitance of the MOSFET.

Another advantage to soft switching is that there will be less generated conducted and radiated EMI. Voltage ripple on the input capacitor results in slight variations in the switching frequency because the valley is a moving target. The dithering that results from hunting for and switching on an available valley spreads the radio frequency spectrum and reduces EMI. The required EMI filter may be a bit more challenging to design, however, because there isn't just one switching frequency to filter but a range of switching frequencies. Despite this challenge, the filter will still be smaller, saving on overall cost and size.

Table 1 summarizes the differences between a hard-switching traditional flyback and a soft-switching QR flyback.

Flyback Feature Comparison		
Operating	**Advantage**	**Disadvantages**
Quasi-Resonant	• Lower Switching Losses • Smaller EMI Filter • Low Parts Count = Low Cost • Isolated • Multiple Outputs • Operates Over a Wide Input Range • Better Transient Response (DCM) • Easier to Compensate (DCM)	• Poor Transformer Utilization • Poor Cross-Regulation • Limited to DCM or TM • Challenging EMI Filter Design • Limited to Low to Medium Power Levels
Traditional	• Low Parts Count = Low Cost • Isolated • Multiple Outputs • Operates Over a Wide Input Range • DCM, CCM or TM	• Poor Transformer Utilization • Poor Cross-Regulation • CCM Challenging to Compensate • Large EMI Filter • Limited to Low to Medium Power Levels

Table 1 – Comparison between traditional and QR flyback converter features.

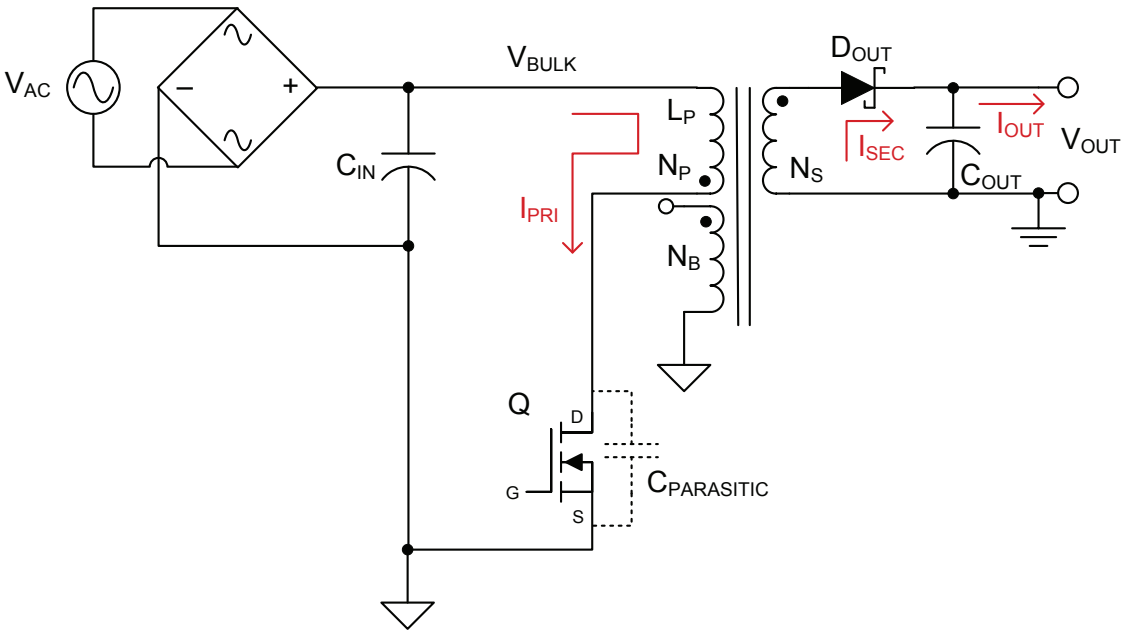

Figure 3 – QR flyback power stage.

II. The QR Flyback Power Stage

Figure 3 shows the power stage of a QR flyback. Looking closely, it doesn't seem any different from a traditional flyback; all of the basic building blocks are there, with no major circuit changes or additions. The power stage has an input capacitor, C_{IN}, that determines the minimum bulk voltage, $V_{BULK(min)}$, due to input voltage ripple. Equation 1 shows that V_{BULK} is equal to the rectified and filtered input AC voltage:

$$V_{BULK} = \sqrt{2} \times V_{AC} \quad (1)$$

The coupled inductor fulfills the energy-storage and energy-transfer functions and provides input-to-output isolation. The MOSFET switch, Q, allows the primary-side current, I_{PRI}, to flow. The turns ratio of the primary winding, N_P, to the secondary winding, N_S, sets the output voltage, V_{OUT}. The rectifying diode, D_{OUT}, feeds the secondary side current, I_{SEC}, to the output capacitor, C_{OUT}, and to the load.

The turns ratio of the secondary winding, N_S, to the bias winding, N_B, sets the voltage that will provide bias to the primary-side controller. This bias winding also gives an accurate, scaled-down, offset view of the primary-side switching waveform.

QR flybacks must operate in DCM or TM, but the only way to do this is to have some way of detecting when the flyback coupled inductor, or transformer, has completely reset. The bias winding creates an ideal signal to indicate when the core has completely demagnetized. A specialized controller that senses this transformer reset status is required in order to take advantage of this information. Texas Instruments' UCC28600, UCC28610, TPS92070, TPS92210 and TPS92010 controllers are all designed to detect the end of the demagnetization time of the flyback power stage.

The parasitic capacitance depicted in Figure 3 represents the sum of the output capacitance, C_{OSS}, of Q, the reflected junction capacitance of D_{OUT}, the winding capacitance of the flyback inductor, the capacitance of Q's package, and the capacitance of the heatsink that Q may be mounted to:

$$C_{PARASITIC} = C_{OSS} + C_{DIODEreflected} + C_{WINDING} + C_{Qpackage} + C_{HEATSINK} \quad (2)$$

Note that most of the components of $C_{PARASITIC}$ in Equation 2 are unknown and difficult to characterize. This parasitic capacitance, along with the primary inductance, L_P, is the cause of the resonant ring that is represented on the bias winding and used by the controller to mark the point at which the core is demagnetized. As I will show in the example, an initial assumption for the period of this resonance is required at the onset of the design process.

A. Flyback Fundamentals

The following brief discussion provides a basic description of a typical switching cycle of a peak-current-mode-controlled DCM flyback converter. Starting the cycle when the switch, Q, is turned on, the current on the primary side ramps up at a slope that is a function of the input bulk voltage and the primary inductance according to Equation 3.

$$\frac{dI_{PRIramp}}{dt} = \frac{V_{BULK}}{L_p} \quad (3)$$

As noted earlier, the transformer behaves like a coupled inductor; current does not flow through the primary and any of the secondary windings at the same time. During the on-time of Q, current is flowing in the primary winding but not the secondary windings. As a result, energy will be stored in the inductance of the primary (more specifically, in the gap) because it can't go anywhere else. Referring to Figure 4, the dot ends of the transformer are more negative than the undotted ends. The output diode, D_{OUT}, is reverse-biased and in blocking mode.

Because no current is actually flowing through the secondary windings, all of the output load current must be supplied by the output capacitor.

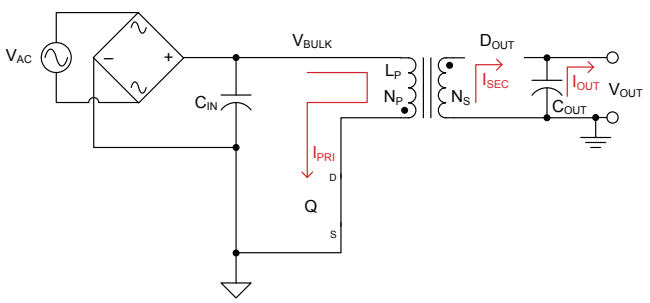

Figure 4 – The switch, Q, is on. The bias winding is not shown.

The on-time is complete when the primary current has ramped up to its designed peak threshold. Figure 5 highlights the significant current and voltage waveforms during the on-time of Q.

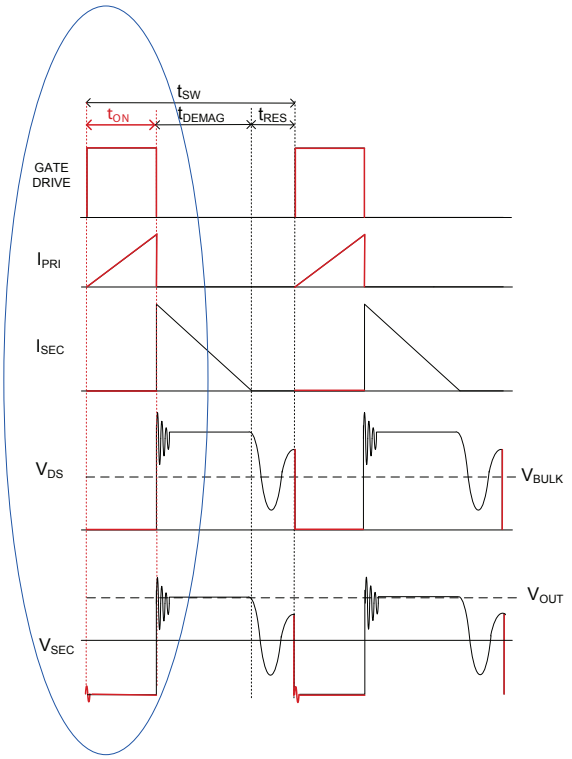

Figure 5 – Current and voltage waveforms highlighting the on-time of Q.

Once the primary current has ramped up to its peak value, the switch, Q, is turned off. A representation of the converter with Q off is shown in Figure 6. Figure 7 highlights the current and voltage waveforms during the demagnetizing portion of the switching cycle.

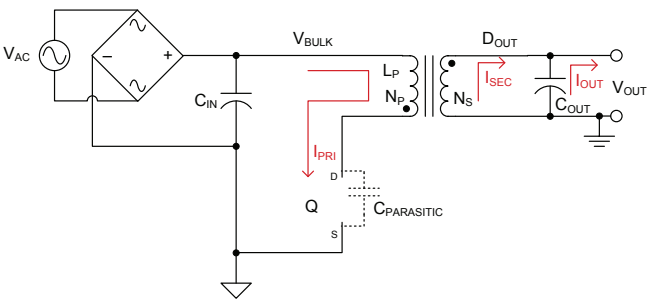

Figure 6 – The switch, Q, is off. The bias winding is not shown.

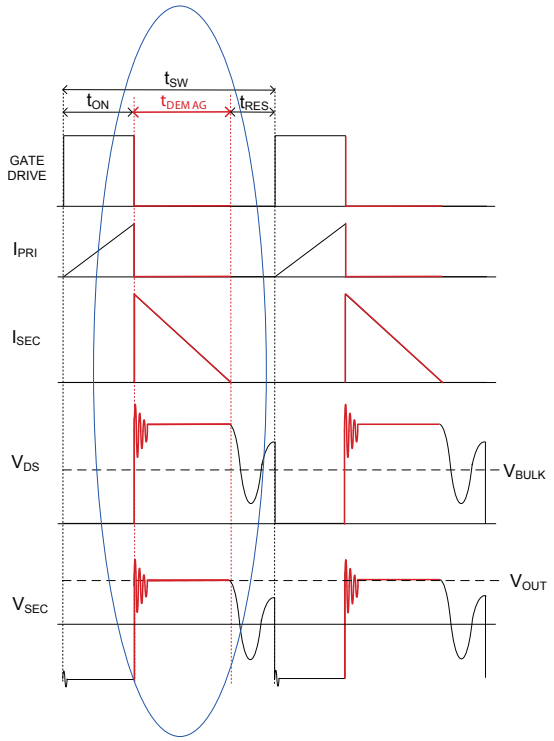

Figure 7 – Current and voltage waveforms, highlighting the demagnetizing time when Q is off.

With Q off, no current can flow in the primary. The drain voltage, V_{DS}, rises to a value equal to the bulk input plus the reflected output voltage, referred to as the flyback voltage, in addition to the voltage spike from the transformer's leakage inductance (see Equation 4).

$$V_{DS} = V_{BULK} + V_{FLYBACK} + V_{LEAKAGE} \quad (4)$$

The high-frequency ringing on the drain is a result of the resonance between the leakage inductance and the parasitic capacitance. The voltage across the secondary windings rises above ground; now the dot ends of the transformer windings are more positive than the undotted ends. The output diode, D_{OUT}, is forward-biased and begins to conduct, allowing the transformer to demagnetize. The secondary current, I_{SEC}, supplies the load and recharges the output capacitor during this demagnetizing time. The current on the secondary ramps downward, decreasing as a function the primary-to-secondary turns ratio, the output voltage and the primary inductance (Equation 5).

$$\frac{dI_{SECramp}}{dt} = -(N_{PS})^2 \times \frac{V_{OUT}}{L_P} \quad (5)$$

$$N_{PS} = \frac{N_P}{N_S}$$

Demagnetization is complete when the secondary current has ramped all the way down to zero. When the core has completely demagnetized, the energy stored in the parasitic capacitance will form a resonant tank with the primary inductance. The resonant frequency is equal to Equation 6.

$$f_{RES} = \frac{1}{2 \times \pi \times \sqrt{L_P \times C_{PARASITIC}}} \quad (6)$$

B. The Difference

The turn-off event does not change, regardless of whether the converter is a traditional peak-current-mode-controlled DCM flyback or a peak-current-mode-controlled QR flyback. Both versions will turn Q off when the primary current ramps up to a designed peak value. Both versions are operating in DCM, so the turn on will be after all of the energy has been transferred.

The difference is soft switching verses hard switching. In a traditional flyback, the fixed-frequency oscillator initiates the next switching cycle. Because this turn on is completely dependent upon the oscillator, turn on could be at any point during the resonant ringing of the primary inductance and parasitic capacitance. There's a 50 percent chance that turn on will occur when the drain voltage, V_{DS}, is higher than the input bulk voltage, and it may be after many resonant ringing cycles depending upon the operating conditions.

The QR flyback initiates the next turn-on cycle only after a resonant valley is detected. The switching frequency is modulated. Theoretically, a quasi-resonant controller does not need an oscillator; it just needs to detect a valley. The deepest valley occurs at the first resonant ring where the drain voltage, V_{DS}, could potentially swing down to a level as low as the bulk input voltage minus the flyback voltage.

Designing the power stage to operate at critical conduction mode at full load to take advantage of this low valley voltage will result in the lowest capacitive switching losses because these losses are calculated in Equation 7.

$$P_{CAPACTIVE\_SWITCHING\_LOSSES} = \frac{1}{2} \times C_{PARASITIC} \times V_{DS}^2 \times f_{SW} \quad (7)$$

At this operating point, the switching frequency will consist of the on-time, the demagnetizing time, and one half of the resonant period. Compare Figure 9, showing the QR switching waveforms, with the previous figures showing the traditional flyback switching waveforms (Figures 6 and 8) and notice where the switch is turned on (and what the voltage of V_{DS} is) to appreciate the considerable impact on overall efficiency switching at a valley will have, especially considering this voltage is squared.

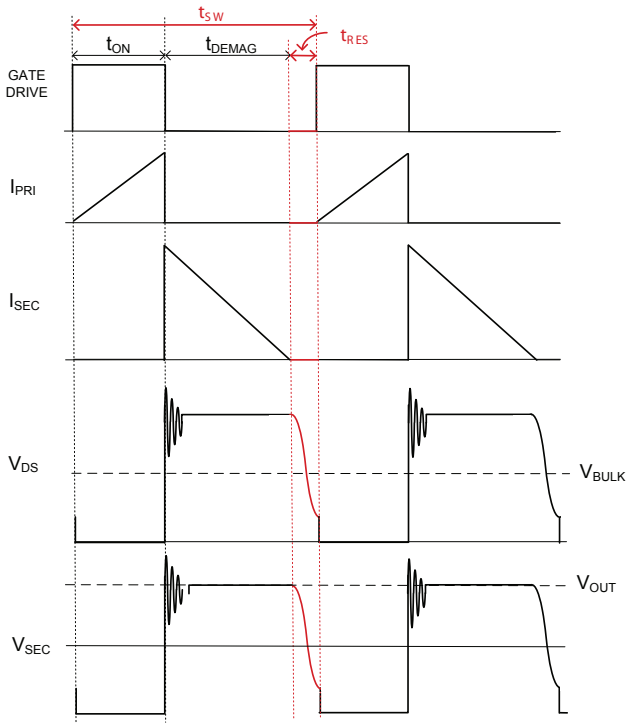

Figure 8 – Current and voltage waveforms of a QR flyback at critical conduction.

The on-time and demagnetizing time did not change when compared to Figures 5 or 7, but the resonant time and (as a result) switching period changed. At lighter loads, switching may wait for several resonant cycles because the switching frequency is ultimately a function of the required energy transfer. But even if the first resonant valley is missed, the QR converter will switch at the next available valley. As a result, switching will never occur when the drain voltage, V_{DS}, is greater than the input voltage.

III. Choosing the Controller

Different quasi-resonant controllers use different modulation methods to achieve regulation. It is important to understand the basic premise under which any particular controller operates. The controller will determine the operating mode based upon input voltage and load current. All of the controllers rely on the switching waveform for valley detection, either by detecting a change in slope or a zero-crossing threshold; as a result, all of the controllers force DCM.

Some controllers, such as the UCC28600 and TPS92070, will modulate both the switching frequency and the peak primary current over most of the operating range. Other controllers, such as the UCC28610 and TPS92210, will modulate the switching frequency but maintain constant peak primary current over much of the operating range. There are subtle differences to the design approach based upon the specific controller's modulation method.

A. Frequency and Peak Current Modulated

Some QR flyback controllers will modulate both the switching frequency and the peak primary current for a given input voltage and load range. When operating in TM, the switching frequency will increase as the load decreases. Also, for the same load, the switching frequency will be higher for higher-input voltages. The peak primary current is also modulated while operating in TM. As the output load decreases, the peak current decreases. This makes it very difficult to calculate the switching frequency and peak current at any specific operating point.

As Michael Madigan explained in his 2006 Power Supply Design Seminar paper, "Green-Mode Power by the Milli-Watt," solving a cubic

equation is necessary to determine the peak primary current; the peak primary current is then used to calculate the switching frequency for this type of controller. Because the peak current varies with input voltage, the power limit will be unavoidably input-voltage dependent.

Figure 9 shows the relationship of the switching frequency and peak primary current as a function of the input bulk voltage and output load for a converter that modulates both frequency and current in order to establish regulation.

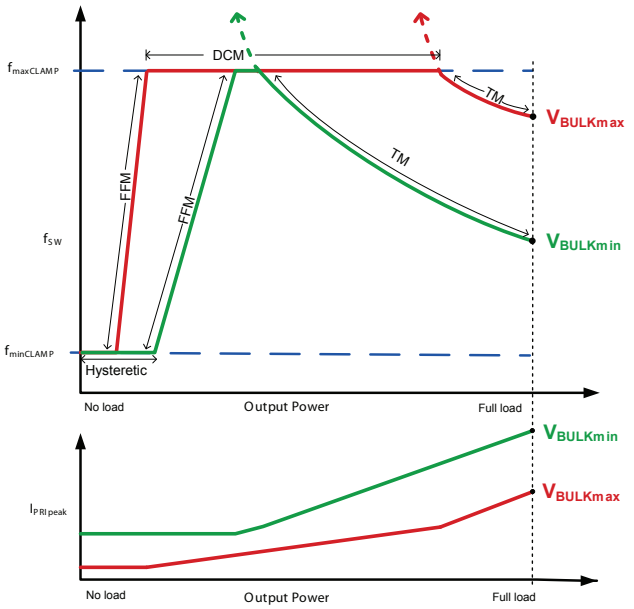

Figure 9 – Switching frequency and peak primary current of a frequency- and current-modulated QR converter. The Texas Instruments UCC28600 is an example of this type of controller.

As the load decreases from its maximum full-load design point, the switching frequency increases. Why would the frequency be lower if the output power is higher? Higher power means that a longer on-time is required to store the higher energy, and thus a longer demagnetizing time to transfer the higher energy. A longer on-time and longer demagnetizing time will result in a longer switching period and reduced switching frequency. At a higher input voltage, the same amount of energy can be stored and transferred in a shorter amount of time, so the switching frequency for the same load will be greater.

The importance of a maximum frequency clamp is subtly implied in Figure 9. Note that without this $f_{maxCLAMP}$, the switching frequency would increase at a rapid rate as the output load decreased. The unlimited increase in the switching frequency would be, to put it plainly, very bad. Power losses at light loads would be disproportionately high despite the modulated peak current, thanks to the switching losses in the MOSFET and the output diode, along with the higher core losses (all functions of switching frequency).

The size of the input EMI filter would have to be much larger for increased switching frequencies. Because of this, the chosen controller will clamp the maximum switching frequency and prevent the unlimited rise in frequency as the load decreases. The upper limit of this clamp should be less than 150 kHz so that the input filter can be relatively small but still meet EMI limits. The converter will operate in DCM while switching at the clamp level; the frequency will be relatively constant while the peak current is modulated. The current is "relatively constant" specifically because the controller will still be hunting for the resonant valley in order to switch. The actual switching frequency from one cycle to the next may dither within the range of one-half of the resonant period of the $L_PC_{PARASITIC}$ ringing.

To further maintain efficiency, as the load is decreased, the controller will transition into frequency foldback mode (FFM) when the load and input voltage demand a lower switching frequency than the clamped DCM level, although switching will still occur at the resonant valley. In FFM, the switching frequency is modulated but the peak current is held constant. This mode of operation may pose a problem for the regulation of multiple outputs, as the switching period is increasing with a constant on-time and ensuing constant demagnetizing time. The drop in overall percentage of demagnetizing time with respect to the switching period will result in lower voltages of the bias winding and other slaves during light load conditions when compared to full load. With a further reduction in load, the controller will operate down to its lower frequency clamp, $f_{minCLAMP}$, in hysteretic mode in order to minimize

the light load and no-load power consumption that is so important to meet green initiatives.

When designing with QR flyback controllers that modulate both the switching frequency and the peak current as a function of line and load conditions, it is best to size the transformer at the minimum input voltage and maximum output power operating point. When calculating the optimum inductor value, assign the switching frequency to be between the minimum and maximum frequency clamps as a starting point for the power-stage design. Experience shows that setting the frequency too close to the minimum frequency clamp at maximum load and minimum input will result in relatively high peak currents. Also consider that you do not want transient conditions, temperature or device tolerances to force the controller to try to operate at less than its $f_{minCLAMP}$; skipped pulses and unstable conditions may result.

Assigning too high of a switching frequency at maximum load, minimum line will result in transitioning out of TM and into DCM over most of the input voltage range and maximum load. Although still reaping the benefits of resonant valley switching, the transformer will not be as well-utilized as it would be if the design started with an assigned switching frequency at minimum line, maximum load that was at a more optimum point: mid-level between the maximum and minimum clamps.

B. Frequency Modulated, Constant Current

In contrast, there are QR flyback controllers that only modulate the switching frequency while keeping the peak current constant over most of the operating range. As shown in Figure 10, these controllers essentially force FFM mode and then, as the output load decreases, transition into DCM, where the switching frequency is constant and the amplitude of the peak current is modulated.

Throughout FFM and DCM, the controller will switch at an available resonant valley. Because the peak current is fixed over the majority of the line and load range, calculating the switching frequency at any given operating point becomes much easier. With decreasing load, the switching frequency will decrease, which will result in decreased switching losses. Another advantage is that power limit is no longer line-dependent, as the full load switching frequency and peak current do not vary with input voltage but only with output load.

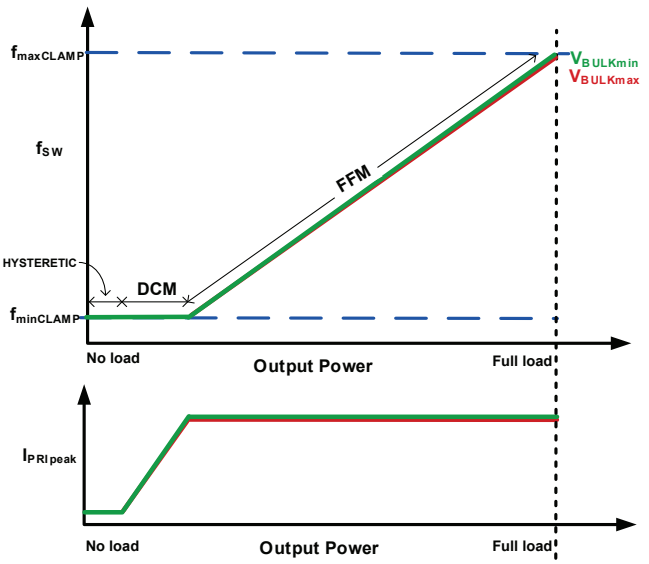

Figure 10 – Switching frequency and peak primary current of a frequency-modulated, constant-current QR converter. The UCC28610 is an example of this type of controller.

Frequency-modulated, constant-current QR controllers still require maximum and minimum frequency clamps. The maximum frequency clamp provided by the controller will be less than 150 kHz for the same EMI benefits stated earlier. The switching frequency will be limited to the minimum clamp level when the load dictates transitioning into DCM, peak current amplitude modulation, and then to hysteretic light load and no-load operation.

When designing with QR flyback controllers that modulate the switching frequency but maintain constant peak current as a function of load conditions, it is best to size the transformer at the minimum input voltage, maximum output power, maximum frequency clamp operating point.

C. The Effect on EMI

Flybacks are noisy. They are isolated supplies and will generate common- and differential-mode noise. Traditional hard-switching flybacks have fast rising and falling edges. Increasing the switching speed has been known to help improve efficiency but creates a major source of noise. The high current and voltage through the transformer will generate strong EMI fields that will require extensive filtering.

In the October 2007 edition of Electronics Components World, L. Haachitaba Mweene pointed out in his article, "Spread Spectrum Switching Improves EMI Compliance in Switching Power Converters," that although the design of an EMI filter for a fixed-frequency converter is relatively easy thanks to the well-defined frequencies under all operating conditions, passing EMI is difficult because the excess energy is concentrated at narrow frequency bands.

QR converters help mitigate conducted and radiated noise by switching at the resonant valley, which softens the switching action due to the lower voltage switching. Hunting for the valley results in cycle-to-cycle dithering, which spreads out the frequency spectrum. Instead of concentrating the excess energy at a narrow frequency, this same amount of energy is distributed over a wider range. The resultant peaks are lower, as shown in Figure 11.

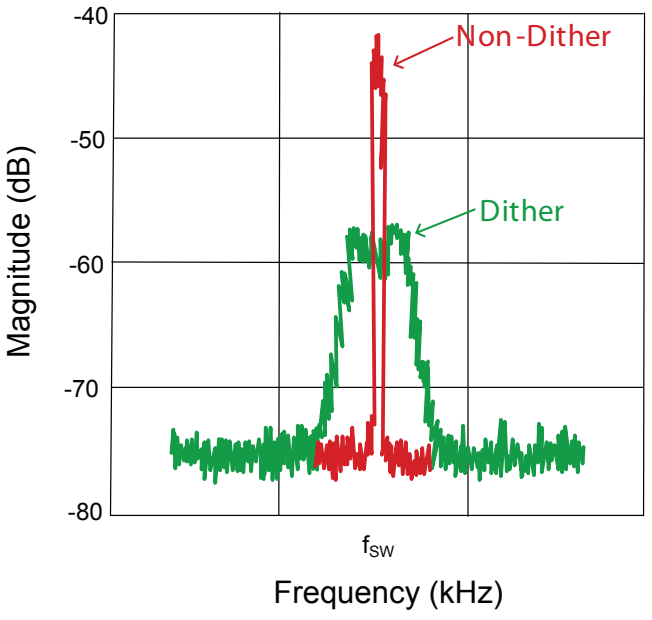

Figure 11 – Comparison of the noise spectrum of a fixed-frequency non-dithering converter with a QR converter that searches for a valley in order to switch, resulting in dithering.

IV. The Design Requirements

Assuming that the design is suitable for a quasi-resonant flyback, being aware of all of the requirements of the end product is very important. Simply knowing the basics (such as input voltage, line frequency, output voltage and output current) will get you started, but you may not end up with an appropriate design that meets all of the specifications. Are there cost constraints? Efficiency, size and ambient temperature will impact your component choices. EMI compatibility, safety and isolation requirements will have an impact on layout and should be accommodated at the onset of the design process. Hold-up requirements and whether or not power factor correction is needed will dictate input capacitor selection. Output ripple requirements, overvoltage protection, short-circuit protection, load transients and regulation may require additional circuitry. The more information you have at the beginning of the design, the better your choices will be as the design progresses.

A. The Design Strategy

Figure 12 shows the design process as a series of decisions, and the results of the calculations based upon those decisions. The design example in this paper will follow the path shown in Figure 12.

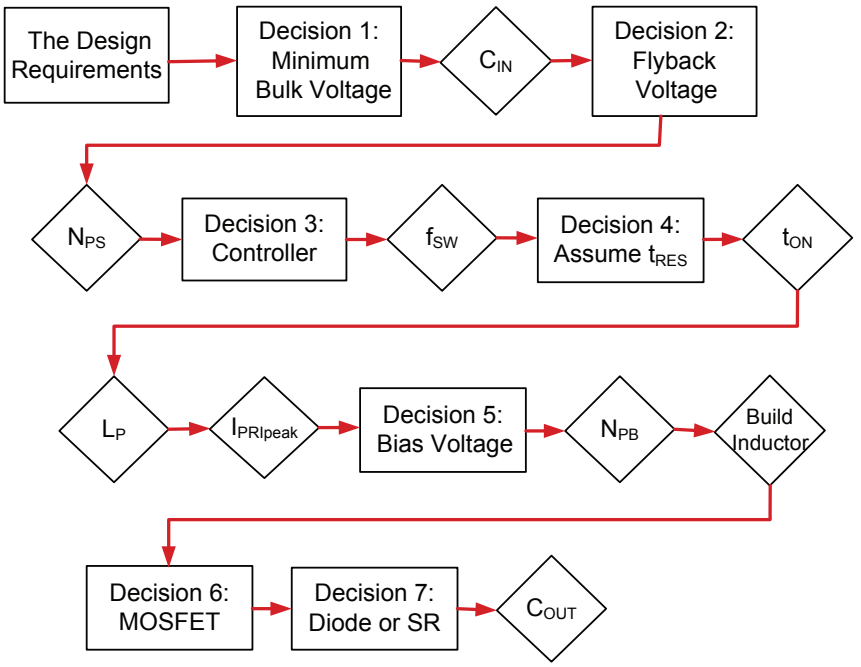

Figure 12 – The design path used in the example.

PARAMETER	REQUIREMENT
Input Voltage	$V_{ACmin} = 85\ V_{RMS}$
	$V_{ACmax} = 265\ V_{RMS}$
Line Frequency	$f_{LINEmin} = 47$ Hz
	$f_{LINEmax} = 63$ Hz
Output Voltage	$V_{OUT} = 5$ V
Output Current	$I_{OUT} = 2$ A
Output Peak Power	$P_{OUTpeak} = P_{OUTmax} = 10$ W
Cost	Low
Efficiency	h > 0.8
Size	Small
EMI Compatibility	n/a
Safety Requirements	n/a
Temperature	Ambient, No Air Flow
Hold Up	No
Output Ripple	$V_{OUTripple} = 0.15\ V_{PP}$
Overvoltage Threshold	$V_{OVP} = 6$ V
PFC	n/a
Reliability	Of Course
Load Transient	Full Range
Regulation	± 10%
Brown Out	$V_{BROWNOUT} = 80\ V_{RMS}$

Table 2 – The specifications for the design example, similar to the requirements for a typical tablet charger (see Appendix A). The term n/a means "not addressed."

V. The Design Example

The remainder of this paper will be devoted to a step-by-step procedure for designing a quasi-resonant flyback converter. The specific requirements listed in Table 2 will be used for this design example and shown with the design calculations. All of the equations used in this procedure can be directly applied to similar designs by modifying the values shown. The parameters that are outside of the scope of this topic, such as EMI filter design, will not be addressed.

A. Decision 1: $V_{BULKmin}$

The rectified AC input voltage is filtered by the input capacitor, C_{IN}, to establish the bulk voltage, V_{BULK}, which will be the input to the power stage of the converter. The power stage for a reliable and robust design should be based upon the minimum bulk voltage $V_{BULKmin}$, which is at the valley of the V_{BULK} ripple at the lowest AC input, V_{ACmin}. Because the power stage is so dependent upon this minimum voltage operating point, and the input capacitor for an offline supply takes up a considerable amount of real estate on the printed circuit board due to its voltage rating, it is wise to choose this component first.

There are trade-offs to consider for this first component. Using the smallest and cheapest input capacitor will result in a lower bulk voltage and higher peak currents. There will be more stress on the MOSFET, the transformer and the output capacitor thanks to these higher currents. Using a larger input capacitor isn't an ideal solution either, as the peak current drawn from the mains will be higher due to the reduced charge time. The input capacitor itself will need to be rated for this ripple current and will be physically larger. An acceptable compromise is to use an input capacitor that will limit the input voltage ripple to 20 to 30 percent. For this design example, specified in Table 2, the minimum bulk voltage calculation is:

$$V_{BULK\,min} = 0.7 \times \sqrt{2} \times V_{AC\,min}$$
$$V_{BULK\,min} = 84\ V$$

To achieve this voltage, the input capacitor is calculated using the energy balance equation, considering that the energy gained during the capacitor charge time will be delivered to the power stage during the capacitor discharge time:

$$\frac{1}{2} \times C_{IN} \times \left[\left(\sqrt{2} \times V_{AC\,min} \right)^2 - V_{BULK\,min}^2 \right] = P_{IN} \times t_{DISCHARGE}$$

To calculate $t_{DISCHARGE}$, refer to Figure 13, where you can see that the capacitor discharge time is equal to the time it takes for the capacitor voltage to drop from its peak value to the desired minimum bulk voltage.

The discharge time is calculated with Equation 8 using the minimum line frequency and timing factors depicted in Figure 13:

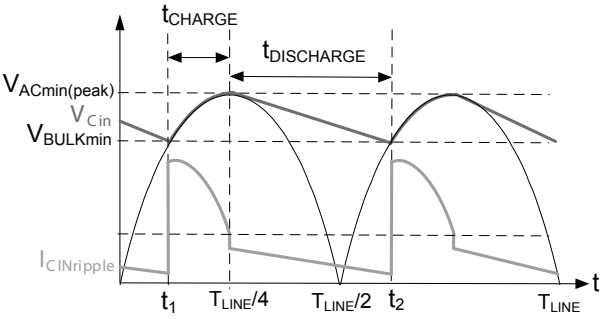

Figure 13 – Input capacitor voltage and current waveforms.

$$t_1 = \frac{T_{LINE}}{2\pi} \times \sin^{-1}\left(\frac{V_{BULK\,min}}{\sqrt{2} \times V_{AC\,min}} \right) \tag{8}$$
$$= \frac{T_{LINE}}{2} + t_1$$
$$t_{DISCHARGE} = t_2 - \frac{T_{LINE}}{4}$$
$$f_{LINE} = 47\ Hz$$
$$T_{LINE} = 21\ ms$$
$$t_{DISCHARGE} = 7.95\ ms$$

Rearranging the energy balance equation allows the ideal C_{IN} value to be calculated per Equation 9:

$$C_{IN} = \frac{2 \times P_{IN} \times t_{DISCHARGE}}{\left(\sqrt{2} \times V_{AC\,min} \right)^2 - V_{BULK\,min}^2} \tag{9}$$
$$P_{IN} = \frac{P_{OUT}}{\eta}$$
$$C_{IN} = 27\ \mu F$$

Of course, the design specification shown in Table 2 requires a low-cost small converter as the final result. Because of this – and because 27 µF is not a standard value – you would expect that the actual capacitor used in the design would be the next lower standard value available. This would be equal to 22 µF. But because a lower-than-calculated input capacitor is selected, it is wise to determine the actual minimum bulk voltage and iterate the calculations starting at the t_1 equation.

After a few iterations, the calculated C_{IN} value converges with the actual C_{IN} used and that determines the actual minimum bulk voltage. The iteration begins (and will ultimately end) by determining $V_{BULKmin}$ in Equation 10, assuming the same $t_{DISCHARGE}$ as calculated in the previous step:

$$V_{BULK\,min} = \frac{\sqrt{2 \times C_{IN} \times (C_{IN} \times V_{AC\,min}^2 - P_{IN} \times t_{DISCHARGE})}}{C_{IN}} \quad (10)$$

After three iterations, using a 22-µF capacitor yields a $V_{BULKmin}$ of 76 V. Because heating caused by ripple current is the leading cause of failure in capacitors, it is necessary to calculate the peak current ripple and estimate the rms ripple current for which the input capacitor must be rated. Looking at the current waveform shown in Figure 13, a conservative approximation for the ripple current is calculated with Equation 11 as:

$$C_{IN} = \frac{Q}{\Delta V} = \frac{t_{CHARGE} \times I_{CINpeak}}{\sqrt{2} \times V_{AC\,min} - V_{BULK\,min}} \quad (11)$$

$$t_{CHARGE} = \frac{T_{LINE}}{4} - t_1$$

$$I_{CINpeak} = \frac{C_{IN} \times \left(\sqrt{2} \times V_{AC\,min} - V_{BULK\,min}\right)}{t_{CHARGE}}$$

$$I_{CINrms} = \frac{I_{CINpeak}}{\sqrt{3}}$$

For this design example, the peak input current, $I_{CINpeak}$, is equal to 0.323 A, with a corresponding rms ripple current of 0.187 A.

B. Decision 2: $V_{FLYBACK}$

Most flyback converter designs select $V_{FLYBACK}$ based upon the voltage stress on the MOSFET drain, V_{DS}, which has already been defined in Equation 4 as:

$$V_{DS} = V_{BULK} + V_{FLYBACK} + V_{LEAKAGE}$$

There are merits to this approach, as choosing $V_{FLYBACK}$ to be as high as the maximum bulk input voltage will result in zero voltage switching (ZVS) over the entire operating range, which will minimize switching losses. However, this will impose a huge voltage stress on the MOSFET and it will have to be rated for more than twice the maximum bulk voltage plus the leakage inductance spike; higher-voltage-rated devices tend to cost more than lower-voltage devices. A high-voltage MOSFET will have a higher on-resistance, R_{DSon}, and higher gate capacitance when compared to a MOSFET rated for a lower voltage. As a result, choosing a higher $V_{FLYBACK}$ will gain you lower switching losses but higher conduction losses and higher component cost.

Choosing $V_{FLYBACK}$ to be lower than the input bulk voltage allows you to use a lower-voltage-rated MOSFET, with lower R_{DSon}, lower gate capacitance and lower component cost. Because this is a QR flyback, choosing a lower $V_{FLYBACK}$ will eliminate ZVS switching, but the sacrifice will be minimized, thanks to valley switching.

For a more practical approach, consider that the flyback voltage, $V_{FLYBACK}$, will impact not only the MOSFET rating but also the blocking stress on the output diode and whether a synchronous rectifier (SR) can be used on the output. As the flyback voltage decreases, the blocking voltage stress on the output diode increases. The flyback voltage is directly proportional to the primary-to-secondary turns ratio, N_{PS}, whereas the output rectifier's blocking voltage is inversely proportional to the same turns ratio.

The desire for high efficiency requires a little foresight to the secondary-side design. The output diode, D_{OUT}, is a major contributor to poor efficiency. The design example will use secondary-side rectification for improved efficiency and a controller will be used to drive the synchronous rectifier. The blocking voltage is limited to the absolute maximum rating of the drain of the secondary-side rectifier, $V_{Drating}$, which is equal to 50 V (see the data sheet "UCC24610 Green Rectifier Controller Device," TI literature No. SLUSA87). By limiting the blocking voltage to 70 percent of the absolute maximum value allowed by the secondary-side controller to accommodate

the voltage spike due to leakage inductance, N_{PS} is set and $V_{FLYBACK}$ is established as shown in Equations 12-14, assuming that V_F is equal to the forward voltage drop of D_{OUT} or the forward drop of the SR body diode:

$$V_{Dblocking\_max} = 0.7 \times V_{ABSMAX} \quad (12)$$
$$V_{ABSMAX} = 50\ V$$
$$V_{Dblocking\_max} = 35\ V$$

$$N_{PS} = \frac{V_{BULK\,max}}{V_{Dblocking\_max} - V_{OUT}} \quad (13)$$
$$V_{BULK\,max} = \sqrt{2} \times V_{AC\,max}$$
$$N_{PS} = 12.492$$

$$V_{FLYBACK} = N_{PS} \times \left(V_{OUT} + V_F\right) \quad (14)$$
$$V_F = 0.6\ V$$
$$V_{FLYBACK} = 70\ V$$

The actual turns ratio used in the design example was equal to 12, resulting in a $V_{FLYBACK}$ of 67.2 V and a blocking voltage of 36.2 V.

C. Decision 3: Chose the Controller

Controller choice defines the switching frequency for the power-stage calculations. QR controllers that modulate the switching frequency and set the peak primary current to a fixed value involve less complex calculations and are well-suited for low-power designs. Because the UCC28610 (TI data sheet literature No. SLUS888) uses this control method, I selected it as the controller for this design. The calculations for the power stage will be based upon setting the switching frequency at minimum input voltage, maximum load, at the minimum $f_{maxCLAMP}$ value for the UCC28610 to ensure a reliable design.

$$f_{SW} = f_{max\,CLAMP} = \frac{1}{7.875\ \mu s} = 127\ kHz$$

D. Decision 4: t_{RES}

The resonance created by the primary inductance and parasitic capacitance must last for a long-enough time so that the waveform can ring down to a level that the controller can interpret as indication that another switching cycle can begin. This time, t_{RES}, is equal to at least one-half of the resonant period – which is the time to transition from peak to valley. The switching period is equal to the inverse of f_{SW} and (at its minimum, such as during TM) must consist of the on-time, t_{ON}, the demagnetizing time, t_{DEMAG}, and t_{RES} (Equation 15):

$$T_{SW} = t_{ON} + t_{DEMAG} + t_{RES} \quad (15)$$

Unfortunately, as mentioned earlier, the parasitics that make up the capacitance causing this resonance are essentially unknown, so t_{RES} is assumed with an initial value. Luckily, by designing for mass market and using worst-case values as opposed to typical values, this guess for t_{RES} will be close enough with minimal design impact and can be measured and verified once the converter is built. Assume that f_{RES} will be less than 1 MHz, so an initial assumption of t_{RES}=500 ns is a valid starting point.

I. Calculate t_{ON}, L_P, $I_{PRIpeak}$

Figure 14 represents the volt second product during the on-time and the volt second product during the demagnetizing time. During every switching cycle, the flyback transformer maintains energy balance. Equating the on-time energy with the demagnetizing energy (with respect to the primary side) and then substituting for t_{DEMAG} allows the calculation of t_{ON}. Equations 16-18 calculate the on-time for the specific design example:

$$V_{BULK\,min} \times t_{ON} = N_{PS} \times \left(V_{OUT} + V_F\right) \times t_{DEMAG} \quad (16)$$
$$t_{DEMAG} = T_{SW} - t_{ON} - t_{RES} \quad (17)$$
$$t_{ON} = \frac{N_{PS} \times \left(V_{OUT} + V_F\right) \times \left(T_{SW} - t_{RES}\right)}{V_{BULK\,min} + N_{PS} \times \left(V_{OUT} + V_F\right)} \quad (18)$$
$$t_{RES} = 500\ ns$$
$$T_{SW} = \frac{1}{f_{SW}} = 7.875\ \mu s$$
$$t_{ON} = 3.46\ \mu s$$

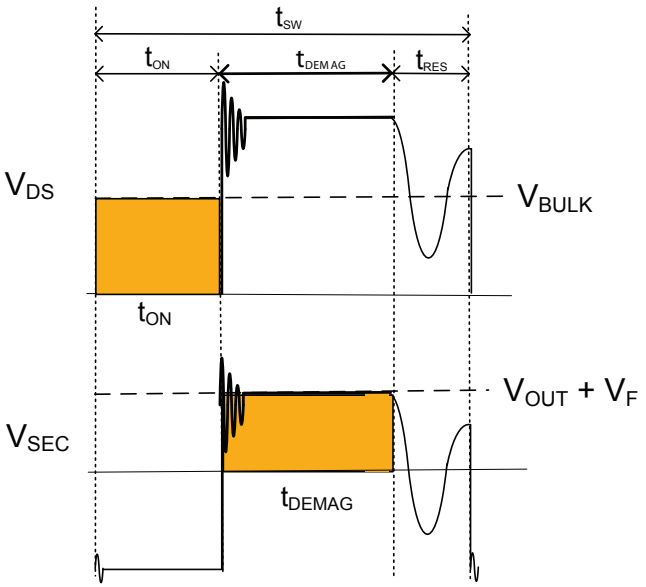

Figure 14 – Volt seconds during the on-time must equal the volt seconds during the demagnetizing time for energy balance.

After calculating the initial on-time, it is necessary to calculate the primary inductance, L_P, which will satisfy the energy requirement of the load at the switching frequency set for the minimum input voltage. Calculating the primary inductance using Equations 19 and 20 is closely followed by the calculation of the resulting peak primary current, $I_{PRIpeak}$:

$$L_P = \frac{\eta \times \left(V_{BULK\,min} \times t_{ON}\right)^2 \times f_{SW}}{2 \times P_{OUT}} \quad (19)$$

$$I_{PRIpeak} = \sqrt{\frac{2 \times P_{OUT}}{\eta \times L_P \times f_{SW}}} \quad (20)$$

Initial calculations result in a primary inductance, L_P, of 369 µH and a peak primary current, $I_{PRIpeak}$, of 0.713 A. Note that the frequency-modulated, constant-peak-current controller's internal logic requires a 1-A minimum and 4-A maximum programmed set value for the $I_{PRIpeak}$ current. This unmodulated peak current is attained at each cycle during FFM operation, whether the output load demands 25 percent or 100 percent of its rated value (as shown in Figure 9). The controller will modulate how often, but not the level.

Control also requires limitations of the maximum on-time. If initial calculations for t_{ON} and $I_{PRIpeak}$ fall outside the dynamic modulation range of the controller, the value for L_P must be iterated so that regulation is achieved over the frequency range enveloped by the minimum and maximum frequency clamps – all while satisfying the maximum on-time, $I_{PRIpeak}$, and power limit for the specified input voltage range and output power. The UCC28610 design calculator tool (UCC28610DESIGN-CALC) facilitates the iterative calculations. After iterating to meet the controller's requirements, the final results for L_P, $I_{PRIpeak}$, t_{ON} and f_{SWmax} calculated to be 191 µH, 1.16 A, 2.9 µs and 98 kHz, respectively.

E. Decision 5: V_{BIAS}

As previously stated, the QR controller allows the switching cycle to begin only after demagnetization has been detected. The bias winding plays a very important role in most QR flyback converters. Not only must the bias be designed to supply the operating current to the controller, but it is also used to indicate when the core has demagnetized and to detect an output-overvoltage. The winding is scaled down by the primary to bias turns ratio, N_{PB}, so that the controller can directly monitor the switching event, showing a high to low transition when demagnetization is finished and the resonant ring has begun. Note that any filtering on this signal will delay detection, so proper layout is always better than external filtering. Excessive ringing from the leakage inductance when the switch turns off must also be avoided. If this leakage inductance ringing is severe enough, it may cause the on-time to be stunted. Low leakage inductance and good layout are always in order, but some snubbing may still be required.

During the off-time of the primary side, the bias winding will have a voltage on it that is proportional to the reflected output voltage and is used for output overvoltage protection. Good coupling to the secondary winding is required for an accurate signal. A series resistor will prevent peak charging of the energy storage capacitor on the bias pin of the controller; otherwise the voltage level could rise and overvoltage the controller at turn on, especially at high line voltages. Always

use an external zener clamp on VDD, even if the controller indicates that one is present internally; why dissipate more heat inside the control center than necessary?

Note that when the load is light on the secondary output but still within FFM, the bias winding will sag. This is because the controller will be modulating the switching frequency to decrease as the load decreases, but the peak current and on-time are held constant. This leads to a proportionally shorter demagnetizing time and less energy transferred to the bias winding. Setting the bias winding to 16 V is recommended in the data sheet for the UCC28610 green-mode flyback controller (TI literature No. SLUS888) for the most efficient operation and will give enough headroom to avoid hitting the absolute maximum rating during turn on and transitions. This setting will also minimize the size of the capacitor needed to hold up the voltage on the bias pin, VDD, during the light-load hysteretic mode of operation.

The following calculations determine the primary to bias turns ratio, N_{PB}, to set the bias voltage. Admittedly, the bias voltage is directly related to the number of turns on the secondary, N_S, but most magnetic manufacturers do not disclose the actual specific number of turns (such as N_P, N_S, N_B) used in the manufacture of their magnetics. They specify only the turns ratios with respect to the primary. In Equation 21, V_F refers to the output diode's forward voltage drop; V_{Fbias} refers to the forward voltage drop across the diode used on the bias winding, assumed to be 0.7 V:

$$N_{PB} = \frac{\left(V_{OUT} + V_F\right) \times N_{PS}}{V_{BIAS} + V_{Fbias}} \quad (21)$$

$$N_{PB} = \frac{N_P}{N_B}$$

$$V_{BIAS} = 16 \text{ V}$$

$$N_{PB} = 4$$

i. More about the Magnetic

The design of a flyback inductor is covered in Lou Diana's "Practical Magnetic Design Inductors and Coupled Inductors" from the 2012 Power Supply Design Seminar, and will not be repeated here. But some guidelines are necessary to ensure a successful design. It is crucial that the bias winding is well-coupled to both the secondary and primary windings, as it plays such an important role in determining the QR switching status and is used for accurate fault detection. You should interleave the bias and secondary windings between the primary, as shown in Figure 15 – or better still, use a bifilar winding technique as opposed to leaving the bias for the outermost layer. Using bundled stranded wire so that the winding layers are distributed across the entire width of the bobbin is also recommended.

Excessive ringing due to leakage inductance must be avoided. To minimize the leakage inductance, use triple-insulated wire to satisfy the isolation requirements instead of layers of tape barrier between the windings. Using a core with a round center post so that the wires lay well will reduce leakage.

The transformer is a major contributor to EMI. Placing the end of the primary winding that is connected to the MOSFET drain in the innermost layer, closest to the core, will help shield the dV/dt noise. Likewise, wind the secondary so that if multiple layers are required, the outer layer is not the switch node. Winding in this way may help avoid the need for a copper radiation shield, or "belly band," around the entire assembly. Adding a small capacitor (less than 100 pF) to primary ground from the diode end of the bias winding will help divert noise out of the transformer. Gapping only the center leg will reduce the radiated EMI from fringing that would be present if the gap was distributed across all of the outer legs.

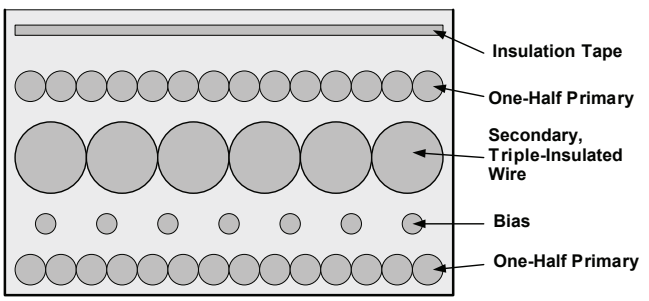

Figure 15 – Recommended winding configuration for a QR flyback transformer, also known as a flyback coupled inductor.

A feature of this modulation method is that the switching frequency at any appreciable load is beyond the audible range. During very light load operation, when the converter is in hysteretic mode, the packets of burst pulses may be within the audible range but at such a low power level that it should not be a problem. Any minor audible noise can be eliminated by filling the center gap with flexible epoxy and varnishing the entire magnetic assembly to reduce any mechanical chatter between the core, coil and bobbin.

The magnetic specification for this specific flyback inductor, with manufacturing guidelines, is shown in Appendix A.

F. Decision 6: MOSFET

The primary switch is selected to meet the drain to source, V_{DS}, requirement; the peak primary and rms currents; and the allocated size constraints, with enough derating for a robust design. Conduction losses in the MOSFET will be higher at the minimum bulk voltage because I_{PRIrms} will increase with decreasing input while the on-resistance, R_{DSon}, increases with temperature. Be sure to use the on-resistance specified for elevated temperature. Conduction loss estimates are calculated in Equation 22 as:

$$P_{FETconduction} = I_{PRIrms}^2 \times R_{DSon} \quad (22)$$

$$I_{PRIrms} = I_{PRIpeak} \times \sqrt{\frac{t_{ON}}{3 \times T_{SW}}}$$

$$I_{PRIrms} = 0.356 \text{ A}$$

$$R_{DSon} = 1.2\ \Omega$$

$$P_{FETconduction} = 0.152 \text{ W}$$

The real appeal of QR converters is revealed in the calculation of the MOSFET switching losses. These losses are estimated assuming first-order effects where the output capacitance of the MOSFET, C_{OSS}, is considered constant over all of the operating conditions. The fall time, t_f, of the signal is estimated using the value reported in the MOSFET data sheet, and the losses associated with the off-time due to the MOSFET's leakage current, along with the gate drive losses, are considered small and negligible for these calculations. Appreciation for the maximum frequency clamp becomes evident as the switching losses are directly proportional to the switching frequency (Equation 23).

$$P_{FETswitching} = f_{max} \times \left[\frac{C_{OSS} \times V_{DS}^2}{2} + \frac{(V_{BULK\,max} + V_{FLYBACK}) \times I_{PRIpeak} \times t_f}{2} \right]$$

$$V_{BULK\,max} = \sqrt{2} \times V_{AC\,max} \quad (23)$$

As Figure 16 shows, DCM switching can occur at any point on the resonant ring. The waveform shown as "a" represents a hard switcher whose turn on occurs at the peak of the first resonant cycle, which could be almost as high as the combined V_{BULK} voltage with $V_{FLYBACK}$. The waveform shown as "b" depicts an ideal valley switcher where the turn-on occurs at the first and deepest valley. The switching voltage at this point could be almost as low as V_{BULK} minus $V_{FLYBACK}$. Using a typical C_{OSS} of 143 pF and a t_f of 10 ns for both situations, the difference in the estimated switching losses is dramatic.

For the situation where the MOSFET is turned on at the peak of the first resonant cycle:

$$V_{DS} = V_{BULK} + V_{FLYBACK}$$

$$P_{FETswitching} = 1.6 \text{ W}$$

For the situation where the MOSFET is turned on at the valley of the first resonant cycle:

$$V_{DS} = V_{BULK} - V_{FLYBACK}$$

$$P_{FETswitching} = 1.0 \text{ W}$$

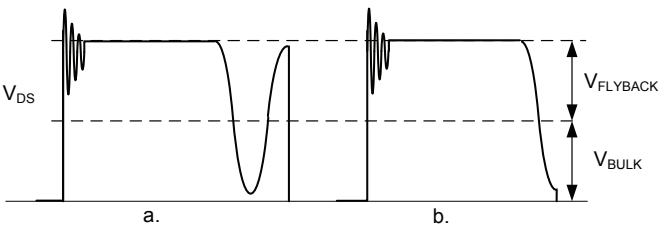

Figure 16 – Comparison of V_{DS} at turn-on for DCM (a) and QR valley switching (b).

G. Decision 7: D_{OUT}

By far, one of the lossiest components in an offline QR flyback converter will be the output diode because of the conduction losses from the high output current. Luckily, the output diode commutates off when the current reaches zero in DCM so it will not have reverse recovery losses.

There are two types of diodes that can be used for output rectification: ultra-fast or Schottky. Ultra-fast diodes are cheaper, but their forward voltage drop is higher than Schottky diodes. The resulting conduction losses will be higher and may require a large heat sink, creating a less-efficient, more-expensive and bulkier design. To make matters worse, the fast switching from these diodes creates radiated and conducted noise that will require filtering to meet EMI requirements. This less-expensive device may require extra costly components for adequate performance.

Because a Schottky diode's forward voltage drop is lower than typical p-n junction devices, it is the rectifier of choice for overall efficiency. Unfortunately, the blocking voltage rating of Schottky diodes doesn't have the same range as ultra-fast diodes. So if the turns ratio results in considerable blocking voltage, the option to use a Schottky may not be possible.

Another consideration is that Schottky diodes have a much higher junction capacitance that requires charging and discharging over every cycle. Potentially, this capacitance could cause ringing with any parasitic stray inductances present. Table 3 compares these two popular rectifiers. For most applications, if the blocking voltage allows, Schottky diodes are usually chosen. The improved efficiency and reduced heat dissipation are usually worth the added cost.

The selected Schottky diode must have sufficient margin for the previously calculated blocking voltage. The rated voltage should accommodate the reflected primary voltage summed with the output voltage, and include enough margin for the leakage inductance spike (Equation 24). If the device has a maximum-rated reverse voltage that is less than adequate, the reverse leakage current will be beyond specification, as Schottky diodes become very leaky at elevated temperatures.

Parameter	Ultra-fast	Schottky	Impact
V_F	Higher	Lower	Conduction Losses
dl/dt Transition	Faster	Slower	Switching Losses
			Noise
Cost	Lower	Higher	Cost
Blocking Voltage	Higher	Lower	Power Stage Design (N_{PS})
Heat Sink	Larger	Smaller	Cost
Capacitance	Lower	Higher	Potential to Resonate

Table 3 – Comparing rectifier options for D_{OUT} and the resulting design impact.

$$V_{BLOCKINGrated} = 1.3 \times \left(\frac{V_{BULK\,max}}{N_{PS}} + V_{OUT} \right) \quad (24)$$

The diode also must be able to handle the peak current and the average current on the secondary side. The junction temperature, T_J, will exceed its safe operating range if the load current rises beyond its maximum average forward current rating. The entire load current goes through the diode during each switching cycle. During conduction, the diode current not only supplies the load, but also re-charges the output capacitor with the current that the capacitor discharged while supplying the load during the time the diode was reverse-biased. The reflected peak primary current should never exceed the peak repetitive forward current limit of the device (Equation 25).

$$I_{SECpeak} = I_{PRIpeak} \times N_{PS} \quad (25)$$
$$I_{SECpeak} = 13.9\ A$$

Power loss in the Schottky diode consists of the summation of the conduction losses and the reverse leakage losses. Conduction-loss calculations are straightforward. Because all of the load and replenished output capacitor current must flow through the diode, the average forward current is equal to the steady-state load current. The reverse leakage losses result from the reverse leakage current and the blocking voltage during the primary switch on-time (Equations 26 and 27):

$$I_{SECavg} = I_{OUT} \quad (26)$$
$$I_{SECavg} = 2\ A$$
$$I_{Dleakage} = 2\ mA$$

$$P_{DIODE} = \left(V_F \times I_{SECavg}\right) + \left(I_{Dleakage} \times V_{BLOCKING} \times \frac{t_{ON}}{T_{SW}}\right)$$

$$P_{DIODE} = 1.23\ W \quad (27)$$

The output diode has a brutal impact on the efficiency of high-current converters. An output current of 10 A across a typical 0.5-V forward voltage drop produces a huge amount of losses. Obviously, there must be a better alternative than even a Schottky for high-current applications.

i. Decision 7: Or Synchronous Rectification?

A more efficient option for the output rectifier is to use synchronous rectification. SRs can only work with QR controllers if they can be forced to behave as a diode and allow discontinuous operation. A dedicated SR controller such as the UCC24610 (TI data sheet literature No. SLUSQA87) or a discrete drive circuit are required for proper function. The efficiency benefits of using synchronous rectification justify the added complexity and cost, especially for low-voltage, high-current applications. To reduce the need for a high-side driver – and still more complexity – placing the SR on the return leg of the secondary side, as shown in Figure 17, simplifies the design. It also eliminates the need for another winding on the transformer.

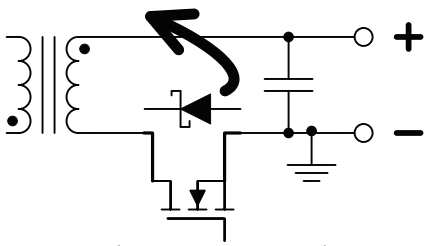

Figure 17 – Replacing D_{OUT} with an SR is greatly simplified when D_{OUT} is on the return leg of the secondary side.

Figure 18 compares the voltage drop across the SR, equal to the product of the R_{DSon} and the secondary-side current, with that of a Schottky diode. MOSFETs used for this function have an R_{DSon} of typically less than 8 mΩ. This results in much less of a forward voltage drop across it than what the Schottky it replaced would have had, which significantly reduces conduction losses. The reduced losses result in a converter of smaller size and weight, with less or even no heat sinking.

The efficiency improvements extend beyond the secondary side, as the currents across the transformer and through the primary side switch will be lower for the same energy transfer. Reliability is enhanced from the reduced component stresses. Figure 19 shows the difference in the measured power loss when a Schottky diode is replaced by an SR, driven by the UCC24610, on the circuit used for this design example. The improved efficiency with the SR was approximately 6 percent over the operating range of the converter when compared to the Schottky.

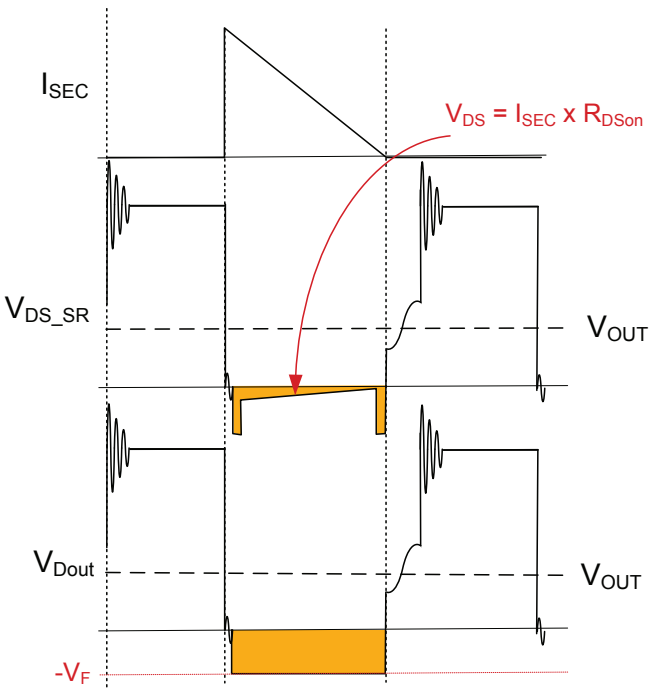

Figure 18 – The shaded regions compare the power dissipation of an SR with a Schottky.

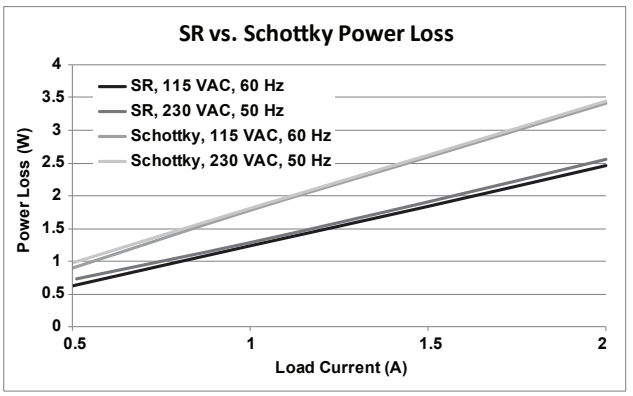

Figure 19 – Measured power loss, in the same converter, of an SR compared with a Schottky diode.

ii. C_{OUT}

Thanks to the high ripple currents in DCM and QR flyback converters, the output capacitor, C_{OUT}, experiences a relatively large amount of stress. The output capacitor should always be based upon its working voltage rating, ripple current rating and equivalent series resistance (ESR). The working voltage rating should be greater than the output overvoltage threshold, allowing margin for any overshoot during transients that may occur before the overvoltage protection, OVP, fault is acted upon. The ESR is dependent upon the capacitor's thermal rating and is a function of the capacitor's I^2R losses.

Aluminum electrolytic capacitors are the least expensive and offer a lot of capacitance, but also occupy a lot of space due to their large size. They tend to have a wide tolerance range and their capacitance decreases with temperature and age, although it is possible to double the specified lifetime of an aluminum electrolytic capacitor simply by reducing its temperature by 10°C. Tantalums are physically smaller than aluminums but only have moderate capacitance values. Multilayer ceramic capacitors have very low ESR, enabling them to handle a lot of ripple current. But they are only available in a few hundred microfarads or less and tend to be very costly. Organic polymer capacitors offer a good compromise, with stable ESR over temperature, but cost slightly more than aluminum electrolytic.

The current ripple that the output capacitor sees is an offset triangular-shaped waveform whose value is calculated with Equation 28.

When the output rectifier turns on, current will flow into the capacitor, replenishing its charge. When the output rectifier turns off, the capacitor supplies the load current to the output. C_{OUT} is selected to meet this ripple current requirement at the converter's switching frequency and operating temperature. Chances are good that a single capacitor will not be rated for the calculated current, and several will be used in parallel to form an output capacitor bank.

$$I_{Cout} = \sqrt{I_{OUT}^2 + \left[\frac{t_{DEMAG}}{T_{SW}} \times \left(\frac{I_{SECpeak}^2}{3} - I_{SECpeak} \times I_{OUT}\right)\right]}$$

$$I_{Cout} = 3.96 \text{ A} \tag{28}$$

The calculations for the output voltage ripple shown in Equation 29 originate from the combination of the capacitance ripple and the ESR ripple. The ripple caused by the ESR of the capacitor will account for the majority of the output ripple. The actual capacitance value of the output capacitor bank used to meet the ripple current requirement will be quite high, so it will contribute very little to the total output voltage ripple (Equation 29).

$$V_{OUTripple} = \sqrt{V_{rippleESR}^2 + V_{rippleCout}^2} \tag{29}$$

$$V_{rippleESR} = I_{SECpeak} \times ESR_{total}$$

$$V_{rippleCout} = \frac{I_{OUT} \times t_{ON}}{C_{OUTtotal}}$$

$$ESR_{total} = 9 \text{ m}\Omega$$

$$C_{OUTtotal} = 660 \text{ } \mu\text{F}$$

$$V_{OUTripple} = 125 \text{ mV}$$

If the resulting output ripple exceeds the desired specification, you can add an output LC filter. The two-stage design can have ceramic capacitors on the first stage to handle the high ripple currents and aluminum for the bulk storage required for transients.

H. The Design Example Schematic

The design example was built, tested and confirmed using the schematic shown in Figure 20.

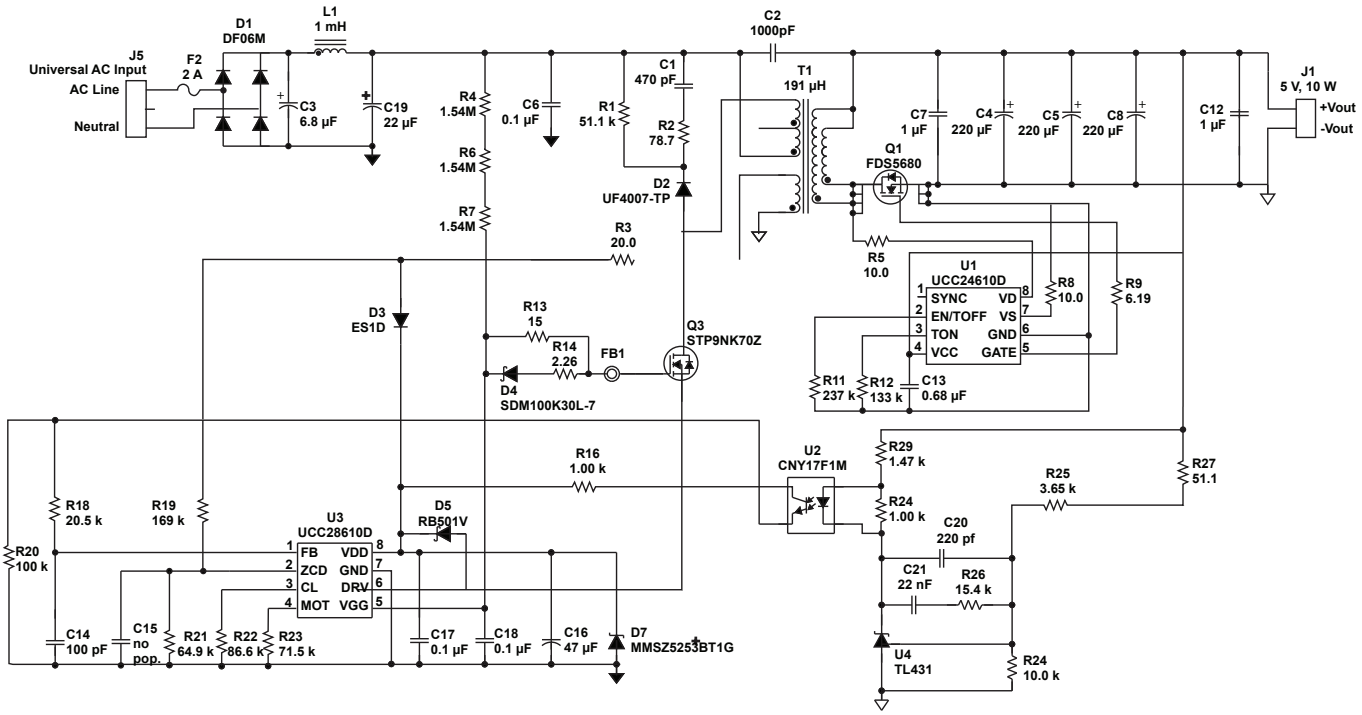

Figure 20 – QR flyback design example schematic.

VI. Conclusion

A quasi-resonant flyback converter is ideal for low- to mid-power offline isolated applications. Many decisions are necessary throughout the design process, and each decision has an impact on the overall performance of the final product. Being aware of the effect of each decision is important when weighing the trade-offs and compromises.

The quasi-resonant controller's modulation method for regulation sets a known operating point for the design process. Selection of the input capacitor will place restrictions on the primary inductance. Bias windings carry much more responsibility than typically expected, so careful consideration must be given to the coupling of all windings. The turns ratio will determine the viability of using a Schottky or a synchronous rectifier, and the end result will have a dramatic effect on the efficiency and reliability of the entire system. This practical step-by-step approach of the available options and actual results showed the benefits of each component selection and the efficiency improvements to be gained.

VII. References

[1] Billings, Keith. *Switchmode Power Supply Handbook*. New York: McGraw-Hill, Inc., 1989.

[2] Pressman, Abraham I. *Switching Power Supply Design*. New York: McGraw-Hill, Inc., 1991.

[3] Lenk, Ron. *Practical Design of Power Supplies*. Piscataway, New Jersey: McGraw-Hill, IEEE Press, 1998.

[4] Brown, Marty. *Power Supply Cookbook, Second Edition*. Woburn, Massachusetts: Newnes, 2001.

[5] Betten, John, and Brian King. "Boost Efficiency for Low-Cost Flyback Converters." April 2, 2008. http://www.edn.com/article/472292-Boost_efficiency_for_low_cost_flyback_converters.php.

[6] Basso, Christophe. "The Dark Side of Flyback Converters." APEC 2011. Accessed May 4, 2012. http://www.google.com/url?sa=t&rct=j&q=&esrc=s&source=web&cd=1&ved=0CHIQFjAA&url=http%3A%2F%2Fcbasso.pagesperso-orange.r%2FDownloads%2FPPTs%2FChris Basso APEC seminar 2011.pdf&ei=A0GkT6b9Eczeggf7mYmyAQ&usg=AFQjCNF-SWY-NpZK0VbFDUJnZsa5XgQ1.

[7] Zhang, Jacky, Jimmy Liu, and Bing Lu. "A High Efficiency Synchronous Rectifier Flyback for High Density AC/DC Adaptor. TI literature No. SLUA604.

APPENDIX A. 10-W QUASI-RESONANT CONVERTER FOR THE POWER SUPPLY DESIGN SEMINAR 2000 REFERENCE DESIGN EXAMPLE FEATURING THE UCC28610 AND UCC24610 CONTROLLERS.

The transformer used in a QR flyback converter is an essential component that requires careful and specific design. The following is an example of the specification that was submitted to the magnetic manufacturer, Wurth Midcom, which achieved a successful design on the first build.

GENERAL:	
Topology	Quasi-Resonant Flyback
Main Output Power	10 W
Maximum Switching Frequency at Full Load	100 kHz
Minimum Switching Frequency at Light Load	30 kHz
Operating Temperature	-40°C to 125°C including temp. rise
Bobbin	THT
Creepage and Clearance	8-mm over-surface/4-mm through-air spacings maintained between primary and each safety-isolated circuit

INPUT:	
Minimum Input Voltage	85 V_{AC}
Maximum Input Voltage	265 V_{AC}
Minimum Line Frequency	47 Hz
Minimum Rectified Bulk Input Voltage	76 V
Minimum Rectified Brown Out Voltage	67 V
Primary Side Peak Current	1.155 A
Primary Side RMS Current	0.356 A
Maximum On-Time at Minimum Input, Maximum Load	2.900 µs

OUTPUTS: One Secondary Winding, One Bias Winding	
Secondary Output Voltage	5 V
Secondary Side Peak Current	13.861 A
Secondary Side RMS Current	4.541 A
Demagnetizing Time	3.222 µs
Bias Voltage	16 V
Bias Current	50 mA

INDUCTANCE AND TURNS RATIOS:		
Primary Inductance	190.918 µH	< +/- 10%
Leakage Inductance	3.818 µH	max
Primary to Secondary Turns Ratio (NP:NS)	12.492	< +/- 10%
Primary to Bias Turns Ratio (NP:NB)	4.097	< +/- 10%
Hipot: Pri to Sec, 2 Seconds	3750 V_{AC}	
Reinforced Insulation		

Notes for Design:

- The bias windings must be well-coupled to the primary and secondary. Interleave the bias and secondary windings between the primary for good coupling.
- Place the undotted end of the primary winding as close to the core as possible to help shield dV/dt noise.
- Wind the secondary so that, if multiple layers, the undotted end is the outermost layer.
- Use triple-insulated wire on the secondary to meet isolation requirements while minimizing leakage inductance.
- Must be potted or heavily varnished to reduce audible noise. Also, fill the gap with flexible epoxy to reduce audible noise.
- Distribute bias windings over entire width of bobbin.
- Use bundled stranded wire to distribute across layer.
- Use round post core to reduce leakage inductance.
- Gap only the center leg.

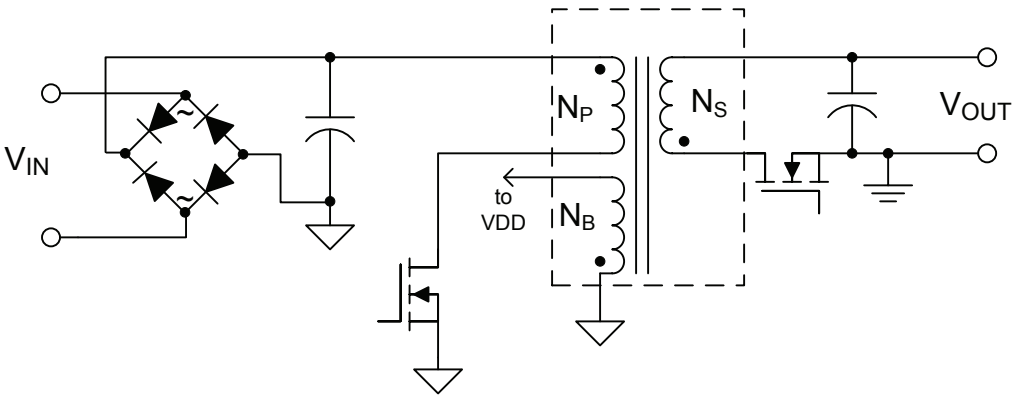

Figure A1 – Simplified schematic.

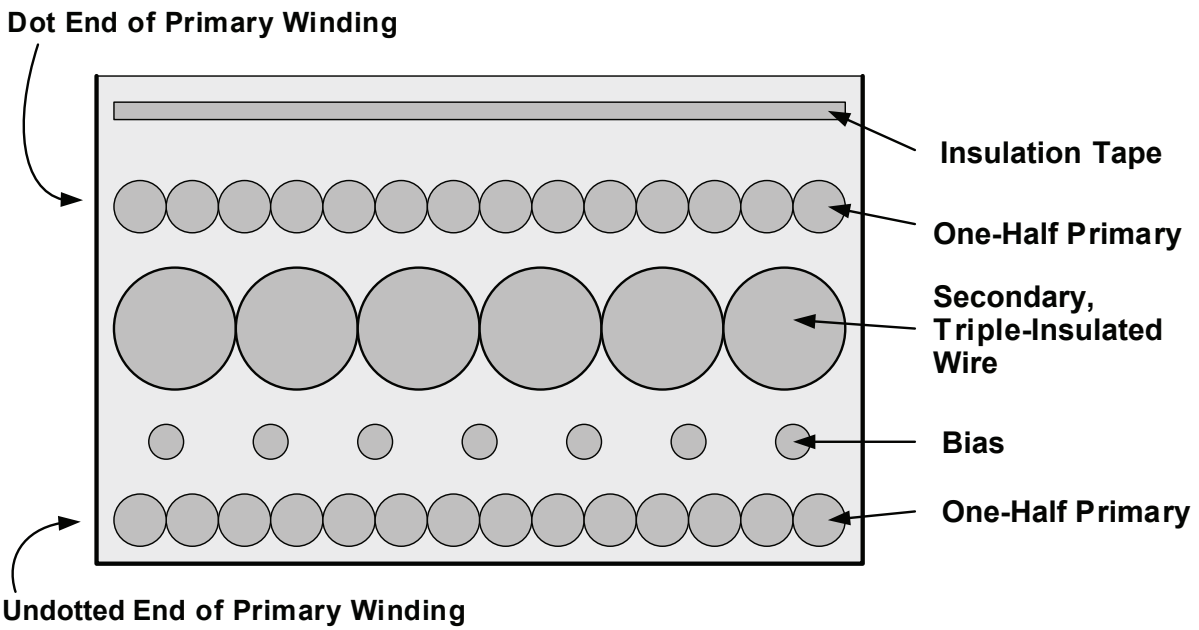

Figure A2 – Recommended winding configuration.

TI Worldwide Technical Support

Internet

TI Semiconductor Product Information Center Home Page
support.ti.com

TI E2E™ Community Home Page
e2e.ti.com

Product Information Centers

Americas	Phone	+1(512) 434-1560
Brazil	Phone	0800-891-2616
Mexico	Phone	0800-670-7544
	Fax	+1(972) 927-6377
	Internet/Email	support.ti.com/sc/pic/americas.htm

Europe, Middle East, and Africa

Phone

European Free Call	00800-ASK-TEXAS (00800 275 83927)
International	+49 (0) 8161 80 2121
Russian Support	+7 (4) 95 98 10 701

Note: The European Free Call (Toll Free) number is not active in all countries. If you have technical difficulty calling the free call number, please use the international number above.

Fax	+(49) (0) 8161 80 2045
Internet	www.ti.com/asktexas
Direct Email	asktexas@ti.com

Japan

Phone	Domestic	0120-92-3326
Fax	International	+81-3-3344-5317
	Domestic	0120-81-0036
Internet/Email	International	support.ti.com/sc/pic/japan.htm
	Domestic	www.tij.co.jp/pic

Asia

Phone

International	+91-80-41381665
Domestic	Toll-Free Number

Note: Toll-free numbers do not support mobile and IP phones.

Australia	1-800-999-084
China	800-820-8682
Hong Kong	800-96-5941
India	1-800-425-7888
Indonesia	001-803-8861-1006
Korea	080-551-2804
Malaysia	1-800-80-3973
New Zealand	0800-446-934
Philippines	1-800-765-7404
Singapore	800-886-1028
Taiwan	0800-006800
Thailand	001-800-886-0010

Fax	+8621-23073686
Email	tiasia@ti.com or ti-china@ti.com
Internet	support.ti.com/sc/pic/asia.htm

A090712

Printed in U.S.A. by (Printer, City, State)

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265