Design of a high-frequency series capacitor buck converter

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The series capacitor buck topology enables small, high-efficiency point-of-load voltage regulators operating in the megahertz range.

Power converters often take up considerable board space. The operation of converters in the megahertz range enables the use of smaller passive components (inductors and capacitors). However, switching losses are prohibitively large in conventional buck converters when attempting operation in high-frequency, high-current and high-voltage-conversion-ratio (for example, 10-to-1) applications.

The series capacitor buck converter topology can significantly reduce the size of point-of-load (POL) voltage regulators. This paper focuses on the limitations of conventional high-frequency buck converters and how the series capacitor buck converter overcomes these challenges, highlighting efficiency, switching loss, inductor current ripple, current sharing, transient response and total solution current density. The paper also includes design guidelines for selecting switching frequency, inductance, capacitance, current limit and soft-start time in a 12-V input, 10-A output application, along with layout recommendations and sample experimental results.

Introduction

The power-delivery system used in many applications today follows the intermediate bus architecture shown in **Figure 1**. A power supply or bus converter converts power from the alternating current (AC) mains or another power source to produce an intermediate bus voltage (12 V in this example). Several POL voltage regulators (usually step-down buck converters) take energy from the intermediate bus and supply various loads in the system. These typically low load voltages (less than 2 V) supply digital circuits such as processors, memory and logic arrays. Voltage regulators with high-voltage conversion ratios are common in these applications. The input voltage of the voltage regulator is often 10 times larger than the output voltage.

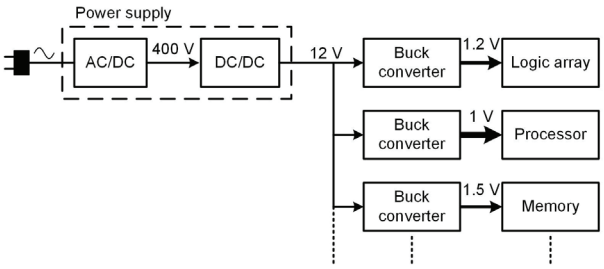


Figure 1. *Power-delivery system using the intermediate bus architecture with POL buck converters.*

Unlike digital circuits – which can shrink by scaling transistor dimensions – power electronics are only a little smaller than they were 10 or 20 years ago. Power converters often take up significant space. Passive components such as inductors and capacitors play a vital role in energy transfer and filtering. These are also the largest components in most converters.

Figure 2 shows a 12-V input, 10-A output buck regulator operating at 500 kHz, with the inductor and capacitors highlighted. The inductor volume is 232 mm^3 and the total converter volume is 1,270 mm^3. The height of the inductor, which is 4.8-mm tall and the largest component, significantly impacts converter volume.

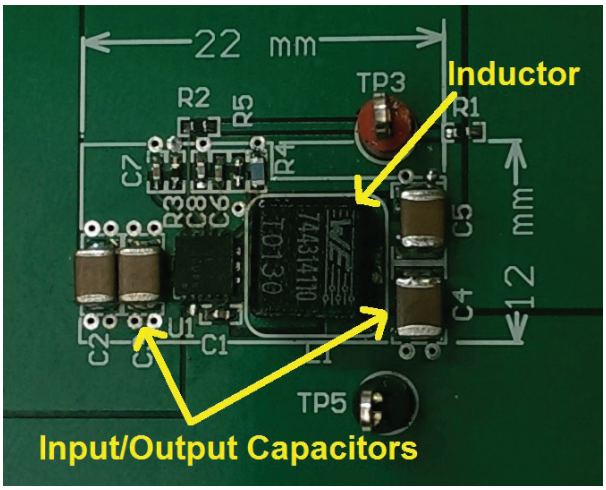


Figure 2. *A 12-V input, 10-A output buck converter operating at 500 kHz.*

The primary way to reduce the size of passive components is to increase the switching frequency. Increasing frequency reduces the required energy storage per switching cycle. This means that you need less inductance to achieve the same peak-to-peak current-ripple specification. Fewer turns of wire create lower inductance values. As a result, inductors with lower inductance tend to be physically smaller, assuming that other parameters like direct current resistance (DCR) are equal.

Input and output capacitance requirements also benefit from high switching frequency. Because the converter slew rates are higher, you can attain fast load-transient performance with less capacitance and only small deviations in output voltage.

Figure 3 shows an example of the size-reduction potential of a 12-V input, 10-A output series capacitor buck converter operating at 2 MHz. The inductor height is reduced to 1.2 mm in this case, and the resulting volume for the inductors is 19.2 mm^3. The overall converter volume is 157 mm^3. This converter is actually smaller than the inductor used in the buck converter shown in **Figure 2**.

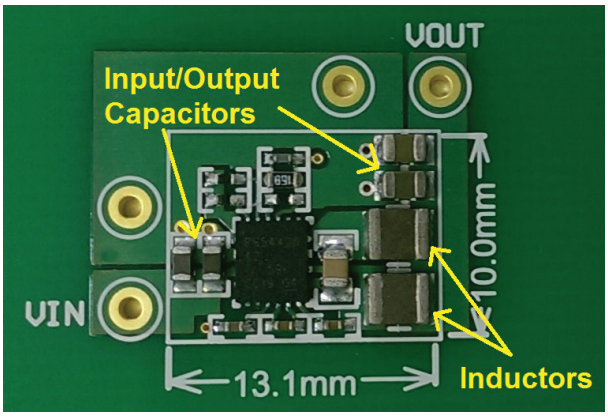


Figure 3. *A 12-V input, 10-A output series capacitor buck converter operating at 2 MHz.*

Another benefit of smaller power converters is lower bill-of-materials (BOM) costs. With fewer and/or smaller external components, material costs go down. Take the inductors shown in **Figure 4**, for example. Conventional buck converters today use the inductors on the left. The low-volume (1,000-unit) distributor pricing for these inductors is in the $2 to $3 range. On the other hand, the low-volume pricing for small inductors used in the new series capacitor buck converter (shown on the right) is in the $0.20-$0.30 range. The same general principle applies to capacitors; you can use fewer and smaller capacitors.

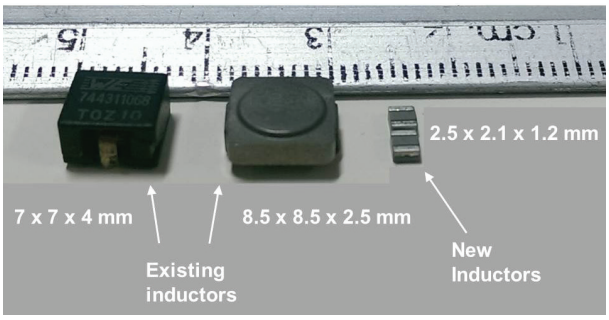


Figure 4. *Size comparison of two 500-kHz inductors and two 2-5 MHz inductors.*

The purpose of this paper is to enable the design of high-frequency series capacitor buck converters. The next section includes background information on buck-converter limitations at high frequency. After that we will introduce the series capacitor buck converter, then explain the design guidelines. Finally we will provide some example experimental results.

Buck-converter limitations

The buck converter has been the workhorse DC/DC converter topology for decades. It is simple, efficient and effective at voltage step-down conversion. Figure 5 is a diagram of a single-phase buck converter. There are two switches, an inductor and input/output capacitors. The switches are usually metal-oxide semiconductor field-effect transistors (MOSFETs) in low-voltage DC/DC converters. Basic buck-converter control is well known and not very complex. A drawback of the buck converter is that it reaches some fundamental limits when increasing switching frequency. The two major challenges for high-frequency, high-conversion-ratio applications are switching loss and minimum on-time.

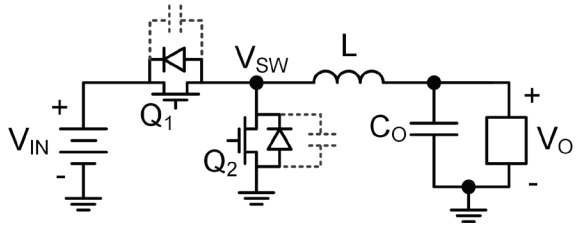


Figure 5. *Diagram of a single-phase buck converter.*

Switching loss

Every time the switches in a buck converter turn on or off, there is some energy loss. A variety of factors contribute to switching loss. The transition between the on and off state is not instantaneous. Some overlap usually exists between the voltage across and current through each switch, which creates loss. There is also parasitic capacitance charging and discharging each switching cycle, diode reverse-recovery loss, gate-drive loss and dead-time loss. Reference [1] explains these loss mechanisms further. The important point is that these loss terms scale proportionally with switching frequency, as shown in Equation 1:

$$P_{loss,sw} \propto f_{sw} \quad (1)$$

As switching frequency increases, power loss increases. Switching loss is relatively small at low frequencies but presents a practical frequency limit when attempting operation at high frequencies.

Minimum on-time

Another challenge for high-frequency buck converters is the high-side switch minimum on-time. The on-time in high-voltage-conversion-ratio applications often limits voltage regulators. It is difficult to generate a short on-time in a controllable manner. For example, consider a buck converter operating with a 10-to-1 voltage-conversion ratio at a 5-MHz switching frequency. Figure 6 shows the switch-timing diagram for this scenario. For these conditions, the switching period is 200 ns and the high-side switch (Q1) on-time is nominally 20 ns. It is difficult for a power MOSFET to turn on and off in this short time interval. Additionally, the blanking time required in most peak current-mode controllers is longer than 20 ns. As a result, most high-frequency converters available on the market today are limited to low-voltage conversion ratios (less than 5-to-1) and low current (1 A or less).

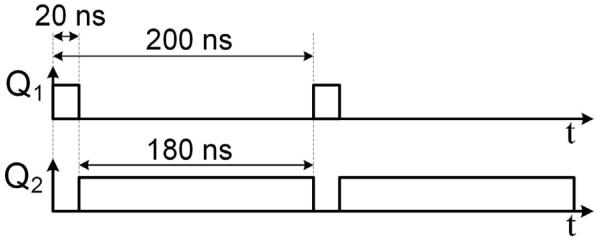


Figure 6. *Switch-timing diagram for a 5-MHz buck converter.*

Series capacitor buck converter

The series capacitor buck converter overcomes many of the challenges encountered by buck converters in high-frequency and high-conversion-ratio applications. **Figure 7** shows a two-phase series capacitor buck converter. It is quite similar to a two-phase buck converter except that it adds a series capacitor (Ct) and changes a few connection points.

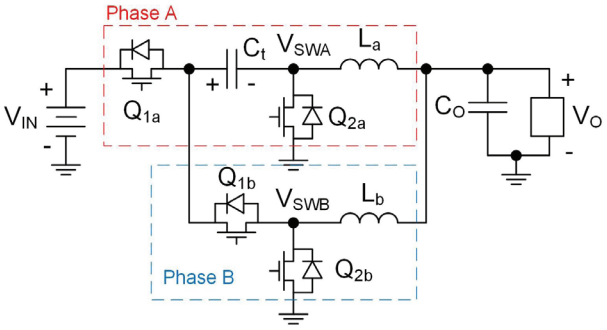


Figure 7. Two-phase series capacitor buck converter.

These minor adjustments provide several benefits. The converter topology essentially combines a switched-capacitor circuit and a two-phase buck converter into a single-stage converter. The series capacitor (whose voltage is half the input voltage nominally) provides a 2-to-1 voltage step-down. From the output-filter perspective (output inductors and capacitors), it looks like a buck converter with half the input voltage. The switch nodes (VSWA and VSWB) see only half the input voltage instead of the full-input voltage in a buck converter.

The effect is only half the input voltage across each switch during turn on and turn off, which reduces switching loss. The high-side switches' duty ratios also double. The inductors charge and discharge the series capacitor in a "soft" manner, unlike the "hard" charging of conventional switched-capacitor circuits. This topology automatically balances inductor currents without any current-sensing circuits or load-sharing control loops. All of these aspects are beneficial for high-frequency, high-voltage-conversion-ratio voltage regulators. References [2] and [3] describe these benefits in more detail.

The series capacitor buck converter has a couple of drawbacks; understanding its limitations is important for proper application and converter design. The primary constraint is the voltage-conversion ratio, because both high-side switches cannot turn on at the same time. In other words, the converter has a 50 percent duty-cycle limitation. Combining that 50 percent duty-cycle limitation with the inherent 2-to-1 voltage step-down created by the series capacitor limits the converter voltage-conversion ratio to 4-to-1 at minimum. The practical limit may be closer to 5-to-1 when accounting for parasitic elements, margins and delays.

In practice, this means that the minimum input voltage for the converter is five times larger than its output voltage (**Figure 8**). Alternatively, the maximum output voltage is one-fifth the input voltage (**Figure 9**). Although this constraint is not acceptable in some applications, many POL voltage regulators will have no problem with this. The input bus voltage is often high enough and well regulated.

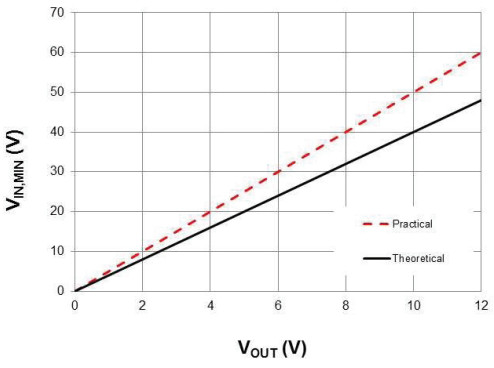


Figure 8. Minimum input voltage for a given output voltage.

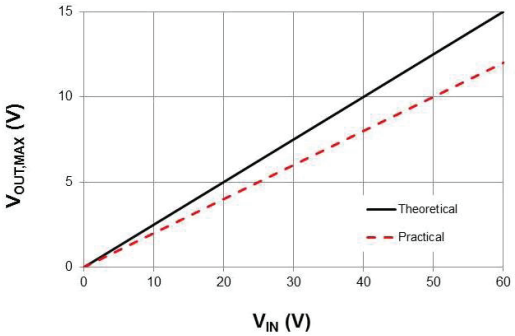


Figure 9. *Maximum output voltage for a given input voltage.*

Another potential downside of the series capacitor buck converter is that phase shedding and adding is not feasible. In multiphase buck converters, phase shedding and adding improve light-load efficiency. But because the phases of a series capacitor buck converter work together and interact during the conversion process, phases are not addable or removable. Other techniques exist to improve light-load efficiency [4].

Steady-state operation

Figures 10-15 show the periodic steady-state operation of the series capacitor buck converter. Figures 10-12 show the continuous conduction mode (CCM) converter configurations. The switching period splits into four repetitive time intervals (**Figures 13-15**). The waveforms in **Figures 13-15** represent converter behavior for a 12-V input POL voltage-regulator application. The average series capacitor voltage is approximately half the input voltage (such as 6 V).

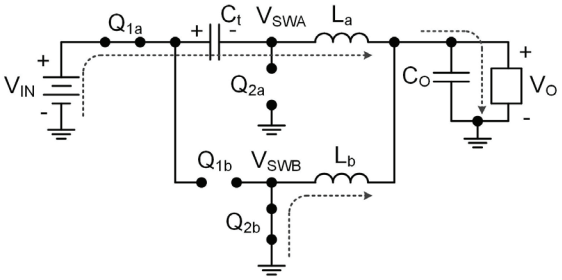


Figure 10. *Phase A high-side switch on (interval 1).*

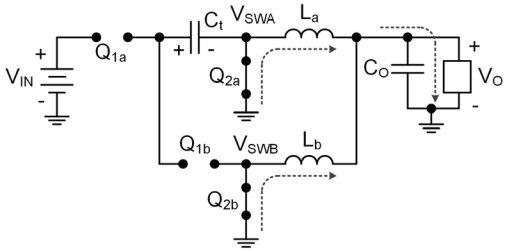


Figure 11. *Low-side switches on (intervals 2 and 4).*

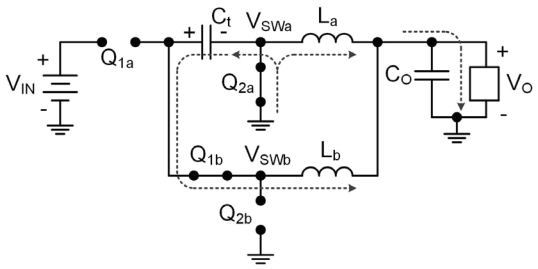


Figure 12. *Phase B high-side switch on (interval 3).*

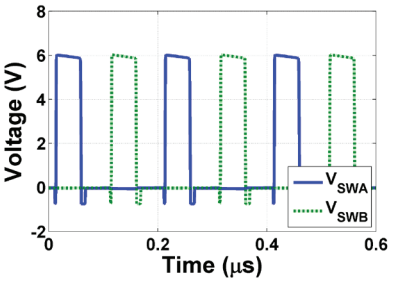


Figure 13. *Switch-node voltages.*

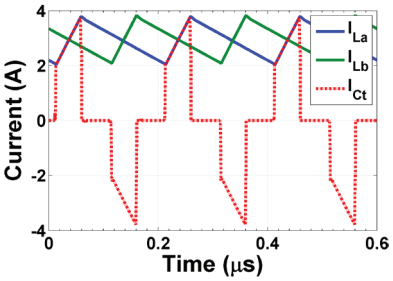


Figure 14. *Inductor and series capacitor currents.*

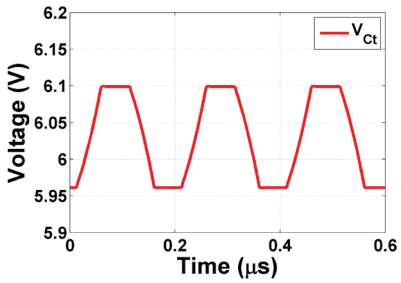


Figure 15. *Series capacitor voltage.*

The first time interval (t_1) occurs when the phase A high-side switch (Q_{1a}) is on and the phase B low-side switch (Q_{2b}) is on (**Figure 10**). The phase A switch node (V_{SWA}) pulls up to approximately half the input voltage (6 V in this case) (**Figure 13**). The series capacitor has half the input voltage across it. The phase B switch node (V_{SWB}) is connected to ground. The phase A inductor current (I_{La}) increases (**Figure 14**), and simultaneously charges the series capacitor, as indicated by the positive series capacitor current (I_{Ct}) in Figure 14. The series capacitor voltage (V_{Ct}) increases linearly with relatively small ripple (less than 150 mV in this case) (**Figure 15**). The phase B inductor current (I_{Lb}) ramps down since the voltage across it is negative.

The second time interval (t_2) occurs when both low-side switches (Q_{2a} and Q_{2b}) are on (**Figure 11).** Both switch nodes (V_{SWA} and V_{SWB}) are connected to ground (**Figure 13**). Both inductor currents (I_{La} and I_{Lb}) decrease and the series capacitor current (I_{Ct}) is zero (**Figure 14**). The series capacitor voltage (V_{Ct}) remains constant (**Figure 15**), because it is neither charging nor discharging. This time interval is similar to a conventional buck converter when the low-side switch is on.

The third time interval (t_3) occurs when the phase B high-side switch (Q_{1b}) is on and the phase A low-side switch (Q_{2a}) is on (**Figure 12**). The phase B switch node (V_{SWB}) pulls up to approximately half the input voltage (6 V in this case) (**Figure 13**). The phase A switch node (V_{SWA}) is connected to ground. The series capacitor acts as the input voltage source for phase B. The phase B inductor current (I_{Lb}) increases (**Figure 14**), and simultaneously discharges the series capacitor, as indicated by the negative series capacitor current (I_{Ct}) in **Figure 14**. The series capacitor voltage (V_{Ct}) decreases linearly with relatively small ripple (less than 150 mV in this case) (**Figure 15**). The phase A inductor current (ILa) ramps down, since the voltage across it is negative.

The fourth time interval (t_4) is identical to the second time interval. It occurs when both low-side switches (Q_{2a} and Q_{2b}) are on (**Figure 11**). Both switch nodes (V_{SWA} and V_{SWB}) are connected to ground (**Figure 13**). Both inductor currents (I_{La} and I_{Lb}) decrease and the series capacitor current (I_{Ct}) is zero (**Figure 14**). The series capacitor voltage (V_{Ct}) remains constant because it is neither charging nor discharging (**Figure 15**). After this time interval, the cycle repeats itself.

Switching-loss reduction

One of the major benefits of the series capacitor buck converter is switching-loss reduction. There are several components of switching loss, noted in the introduction. The voltage and current overlap during switch commutation generates less loss because the voltage is lower. The energy loss in the parasitic switch capacitance is also lower. For example, consider the energy stored in MOSFET parasitic output capacitance (**Figure 16**). When commutating the example MOSFET at a 12-V drain-to-source, approximately 30 nJ of energy is lost. Reducing the commutation voltage to 6 V drain-to-source causes less than 10 nJ of lost energy. This represents a more than two-thirds reduction in switching loss due to parasitic capacitance. Reference [5] offers more details of this switching-loss reduction. These reductions enable you to push the switching frequency higher than was previously feasible.

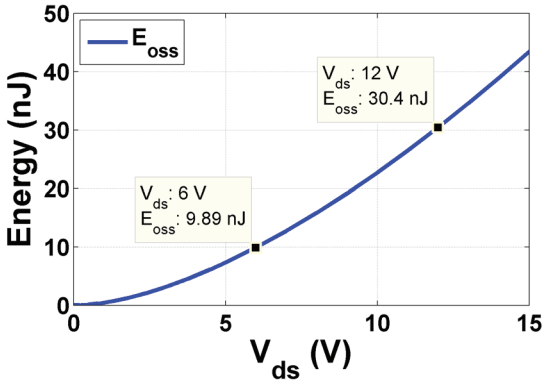


Figure 16. *Energy stored in an example MOSFET parasitic-output capacitance.*

Inductor current ripple reduction

Another benefit of the series capacitor buck converter is inductor current ripple reduction. This benefit is apparent when comparing to the current ripple of a buck converter. Equation 2 expresses the steady-state inductor current ripple in a buck converter as:

$$\Delta i_{L,buck} = \frac{V_O\left(1-\frac{V_O}{V_{IN}}\right)}{Lf_{SW}} \quad (2)$$

Equation 3 expresses the inductor current ripple in the series capacitor buck converter as:

$$\Delta i_{L,SCbuck} = \frac{V_O\left(1-2\frac{V_O}{V_{IN}}\right)}{Lf_{SW}} \quad (3)$$

Divide Equation 3 by Equation 2 to get the inductor current ripple ratio (Equation 4):

$$\frac{\Delta i_{L,SCbuck}}{\Delta i_{L,buck}} = \frac{(1-2\frac{V_O}{V_{IN}})}{(1-\frac{V_O}{V_{IN}})} \quad (4)$$

This ratio represents how much smaller the inductor current ripple is relative to the inductor current ripple in a buck converter for a given input-to-output voltage-conversion ratio (V_O/V_{IN}). This ratio assumes the same inductance and switching frequency.

Figure 17 shows the percentage ripple reduction. For a 10-to-1 voltage-conversion ratio, the inductor current ripple drops by about 11 percent. For lower conversion ratios, the inductor current ripple can drop as much as 33 percent.

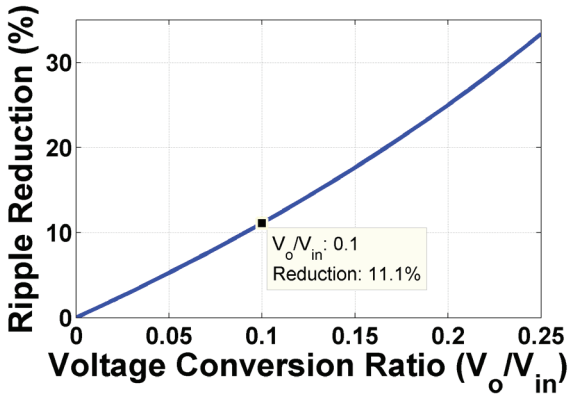


Figure 17. *Reduction in inductor current ripple.*

Inductor current ripple reduction leads to lower core loss. Equation 5 shows a general form of the Steinmetz equation commonly used to approximate core loss:

$$P_{core} = k_0 f_{sw}^{\alpha} B_{pk}^{\beta} \quad (5)$$

where k_0 is a loss constant, fSW is the switching frequency, α is a frequency-based constant slightly greater than 1, Bpk is the peak flux density and β is a flux-based constant slightly greater than 2.

The peak-to-peak flux density in the inductor is directly proportional to the inductor current ripple. As a result, reductions in inductor current ripple result in significant reductions in core loss. Equation 6 simplifies the approximate relationship of core loss as:

$$P_{core} \propto k_0 f_{SW} \Delta i_L^2 \quad (6)$$

Another approach could be to design the inductor for the same current ripple. In that case, the inductance required to attain the same ripple would drop.

Automatic current sharing

One of the most unique benefits of the series capacitor buck converter is automatic inductor current balancing. Unlike conventional multiphase buck converters, the series capacitor buck converter does not require any current-sensing circuits or control loops for load current sharing purposes. Current balancing is passive and automatic. The automatic current-sharing mechanism is robust and not negatively impacted by variations in resistance, inductance or capacitance. Unequal on-times can cause a DC shift in inductor currents. Reference [3] offers a thorough explanation of the current-sharing mechanism.

The series capacitor is a key component of automatic current sharing. Because the inductor currents repeatedly charge and discharge the series capacitor, the average inductor currents must be equal in steady state to maintain charge balance. If there is a disturbance or offset in current, the series capacitor forms an inherent feedback loop and adjusts the average switch-node voltages until the inductor currents match. The inductance values do not need to be equal since the charge is equal (assuming equal on-times) (**Figure 18**).

Figure 19 shows an example experimental result that demonstrates equal current sharing when using unmatched inductors. One inductor is approximately 100 nH and the other inductor is approximately 200 nH. **Figure 20** shows the "perfect" average current sharing over a 0- to 8-A load range. Both inductors provide the same current to the output.

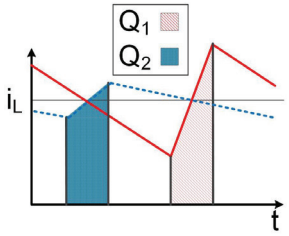


Figure 18. *Inductor currents with unequal inductance but equal charge.*

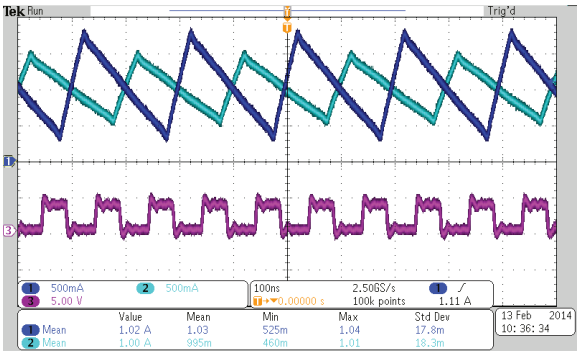


Figure 19. *Experimental result demonstrating equal average inductor currents with unequal inductance values.*

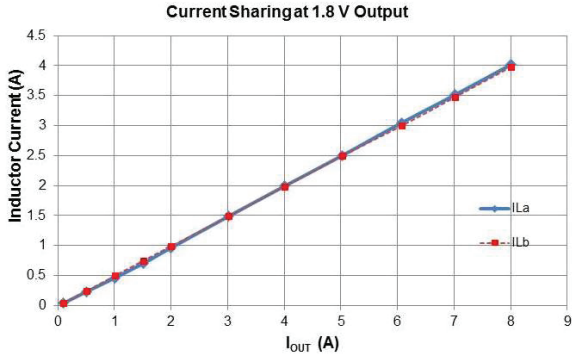


Figure 20. *Matched inductor currents with unequal inductance.*

Design guidelines

High-frequency series capacitor buck-converter designs follow the same basic procedure as the design of a regular buck converter. The first step is to define the converter's electrical specifications; these depend on the application requirements. **Table 1** gives some sample specifications that apply to this design example. You might find this design in a computer server or telecom equipment application.

Parameter		Conditions	Min	Typ	Max	Unit
VIN	Input voltage		10	12	14	V
VOUT	Output voltage			1.2		V
IOUT	Output current		0		10	A
ΔVOUT	Output ripple	5-A load step		24		mV

Table 1. *Example series capacitor buck-converter specifications.*

The first item to consider is if you can use the series capacitor buck converter topology in this application. This converter is only usable if the output voltage is at least four times lower than the minimum input voltage. In this example, the minimum input voltage is over eight times larger than the output voltage. This passes the conversion-ratio constraint shown in **Figures 8-9** with ample margins.

Selecting an integrated converter minimizes component count and size. An integrated converter includes the power MOSFETs, gate drivers, controller and other supporting circuitry. A discrete converter design would require a discrete switch selection, gate-driver design, including other aspects that are outside the scope of this paper. I used the TPS54A20 converter to implement this solution, so some design decisions are based on its properties [8].

Switching frequency

Converter switching frequency is an important design parameter. As with most design parameters there are trade-offs to consider. Converters with high switching frequencies tend to result in smaller solution size, fewer components, faster transient response and higher control bandwidth. Less inductance and fewer capacitors are required to meet the same converter specifications. The downside of high switching frequencies is that converter efficiency will typically be lower than converters designed with lower switching frequencies.

Consider the measured efficiency of 12-V input, 1.2-V output series capacitor buck converters operating at three different frequencies (**Figure 21**). The converter switching at 2 MHz per phase has higher efficiency than the converters switching at 3.5 MHz and 5 MHz per phase, respectively. For this design example, 2 MHz is the switching frequency. It is high enough to provide benefits in terms of small size and fast response, while at the same time maintaining fairly high efficiency and low power loss.

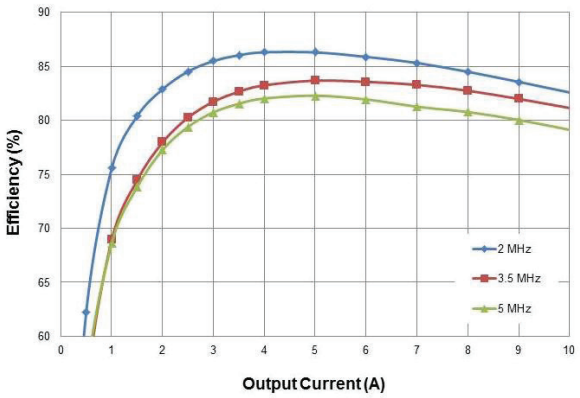


Figure 21. *Efficiency comparison of 12-V input, 1.2-V output series capacitor buck converters.*

Inductors

Inductor selection is a key step in converter design. The inductor dominates overall solution size in conventional buck converters. Inductors also impact efficiency, transient response and closed-loop bandwidth. The inductor design equation is a rearranged Equation 3, shown as Equation 7:

$$L = \frac{V_o \times (1 - D) \times T}{\Delta I_L} = \frac{2 \times V_o \times \left(V_{IN,max} - 2 \times V_o\right)}{k_L \times I_o \times V_{IN,max} \times f_{sw}} \quad (7)$$

where L is the inductance, $V_{IN,max}$ is the maximum input voltage, V_O is the output voltage, I_O is the full-load output current, f_{SW} is the per-phase switching frequency and k_L is the inductor current ripple ratio.

Note that the series capacitor buck converter duty ratio is double that of a buck converter. Equation 8 expresses the duty ratio as:

$$D = \frac{2 \times V_O}{V_{IN}} \quad 8)$$

Some small changes to the design equations used for normal buck converters will be necessary.

The next design decision is the selection of k_L, the inductor current ripple ratio. This coefficient is the ratio of the inductor peak-to-peak current ripple to the average full-load inductor current. The average inductor current is half the output current in a two-phase converter (that is $I_L = I_O/2$). Equation 9 expresses the current ripple ratio as:

$$k_L = \frac{\Delta I_L}{I_L} = \frac{2 \times \Delta I_L}{I_O} \quad (9)$$

Typical values for k_L are in the 0.1 to 0.4 range. A low k_L value will result in a higher inductance value and lower peak-to-peak current ripple; high k_L values result in lower inductance and higher current ripple. Assuming all other factors are the same, higher inductance tends to have these benefits:

- Lower core loss
- Lower root-mean-square (RMS) currents
- Less power loss in the MOSFETs
- Higher peak efficiency

Lower inductance has other benefits, including:

- Lower winding resistance (DCR)
- Faster transient response
- Higher closed-loop bandwidth
- Higher full-load efficiency

For this design example, start by choosing a k_L value of 0.4. Equation 10 calculates the resulting inductance as:

$$L = \frac{2 \times 1.2V \times (14V - 2 \times 1.2V)}{0.4 \times 10A \times 14V \times 2MHz} = 249\,nH \quad (10)$$

You could select the nearest standard inductance value of 220 nH for this design. This might result in slightly lower peak efficiency, but would likely provide fast converter response and reduce full-load power loss (assuming the same size inductor with lower DCR). Another nearby standard inductance value is 330 nH. If you select 330 nH, the effect would be a k_L value of around 0.3.

Figure 22 highlights the efficiency impact of inductance selection and shows the measured efficiency for a 12-V input, 1.2-V output and a 2-MHz per phase series capacitor buck converter with three different inductance values. For comparison, the size of all inductors is 3.2 mm by 2.5 mm by 1.2 mm. The lowest inductance value (250 nH) has the lowest peak efficiency but the highest full-load efficiency. Increasing the inductance increases the peak efficiency but decreases the full-load efficiency. The DCR of the 470-nH inductor is higher than the other inductors because you need more turns of wire to create this inductance value. The impact is more conduction loss and lower full-load efficiency. In this way, the selected inductance value shapes the efficiency curve. For more discussion and analysis of the trade-offs, see Reference [5].

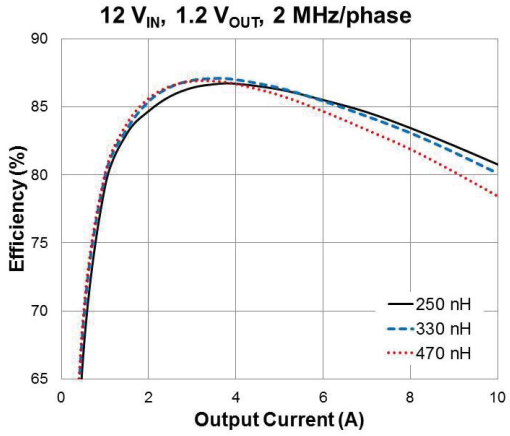


Figure 22. Efficiency comparison for different inductance values.

Inductor size also impacts converter performance. All else being equal, physically larger inductors generally result in higher efficiency. This is primarily due to the reduction in conduction loss. Thicker wire leads to lower DCR.

You can draw this conclusion from **Figure 23**, which shows the efficiency of a 12-V input, 1.2-V output, 2-MHz per phase series capacitor buck converter with different sizes of 330-nH inductors from the same vendor. You can see that as the inductor size gets smaller, the converter efficiency decreases over the entire load range.

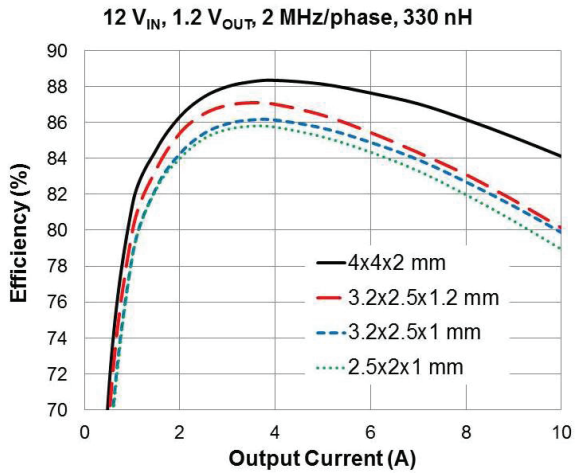


Figure 23. *Converter efficiency with different sizes of 330-nH inductors.*

It may be worthwhile to explore different inductor vendors. The core material, construction, testing, and so on, is different for each manufacturer. Figure 24 shows the impact of these differences on efficiency by graphing the measured efficiency of a 12-V input, 1.2-V output, and a 2-MHz per phase series capacitor buck converter using 330-nH inductors from four different vendors. All inductors are the same size (3.2 mm by 2.5 mm by 1.2 mm). Peak efficiency can differ by as much as 2 percentage points, while full-load efficiency can differ by as much as 3 percentage points depending on the inductor vendor.

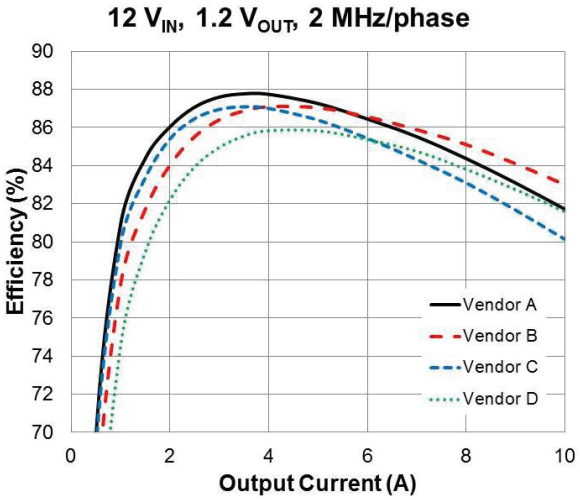


Figure 24. *Converter efficiency with different vendors of 330-nH inductors.*

Keep in mind that inductance values have appreciable variation in practice. The manufacturing tolerance of most inductors is around ±20 to ±30 percent. As an inductor's average current (DC bias) increases, the inductance will decrease. The inductor saturation current rating is typically based on the current level, which causes a 30 percent decrease in inductance from the zero DC bias inductance. Other factors like temperature, humidity and mechanical stress can shift inductance as well.

Experimentally testing a few potential inductors is one of the best ways to reach a decision. Most converters and controllers have evaluation modules (EVMs) that you can test with different inductors. Most inductor suppliers will provide free inductor samples. Although building loss models and transient simulations can be helpful for refining the design, the fidelity of accurate experimental data is hard to beat.

Input capacitors

Input bypass capacitors act as a voltage-source input to the converter. Their primary role is to provide decoupling; they also act as an energy buffer during load transients. For the purposes of

this discussion, assume that the bus capacitance is sufficient to maintain the input voltage within the desired voltage range during transients. You can then design the input-decoupling capacitors around steady-state ripple requirements.

Figure 25 shows the model of the bus converter (power supply) and its output-filter components as a current source during steady state. The input-capacitor current is the difference between the power-supply current and the current pulses drawn by the POL converter. The rate at which the pulses are drawn is equal to the switching frequency.

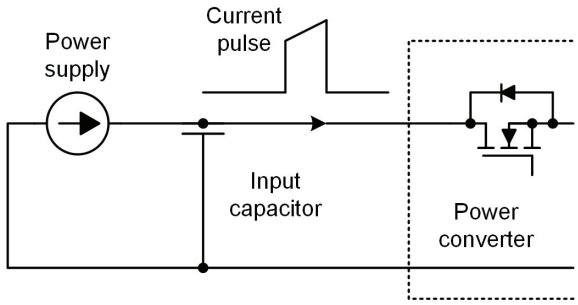


Figure 25. *Converter current pulses impact input capacitor RMS current.*

Equation 11 estimates the input-capacitor voltage ripple as:

$$\Delta V_{IN} = \frac{I_{IN} \times (1 - D)}{C_{IN} \times f_{SW}} = \frac{I_O \times V_O \times (V_{IN} - 2 \times V_O)}{C_{IN} \times V_{IN}^2 \times f_{SW}} \quad (11)$$

Keep in mind that even though the series capacitor buck converter has multiple output inductors, only one of them is drawing current from the input during a switching period. This means that there is no input voltage ripple reduction due to interleaving, unlike what is common in multiphase buck converters.

You can select the input capacitance based on the desired input voltage ripple. The largest input ripple will occur at the full load current, lowest frequency and lowest input voltage (highest duty ratio). Rearranging Equation 11 results in Equation 12, the design equation for estimating the input capacitance:

$$C_{IN} \geq \frac{I_O \times V_O \times (V_{IN,min} - 2 \times V_O)}{\Delta V_{IN} \times V_{IN,min}^2 \times f_{SW}} \quad (12)$$

For this design example, choosing 25 mV of input voltage ripple in steady state, Equation 13 expresses the minimum input capacitance as:

$$C_{IN} \geq \frac{10A \times 1.2V \times (10V - 2 \times 1.2V)}{25mV \times (10V)^2 \times 2MHz} = 18.2\ \mu F \quad (13)$$

This calculated value is a good starting point, although you'll need to consider several other aspects to complete the design. Ceramic capacitors commonly used for decoupling can exhibit a large decrease in capacitance upon the application of a DC bias voltage. The decrease in capacitance can be as much as 60 to 80 percent of the nominal value with the DC voltage bias applied.

Check the capacitor data sheet to find its effective capacitance when applying the full input voltage and adjust the required nominal capacitance accordingly. Capacitance also varies with temperature, so take that in to account as well. I recommended X5R or X7R ceramic capacitors because they have a high capacitance-to-volume ratio and are fairly stable over temperature.

Select the input capacitor so that the RMS capacitor current does not cause an excessive capacitor temperature. The temperature rise in a capacitor is mainly due to self-heating from capacitor current. The RMS current is largest at the full load current, minimum input voltage (highest duty ratio) and highest ambient temperature. Equation 14 estimates RMS current in the input capacitor as:

$$I_{CIN,RMS} = \frac{I_O}{2} \sqrt{\frac{2 \times V_O}{V_{IN,min}} \times \left(1 - \frac{2 \times V_O}{V_{IN,min}}\right)} \quad (14)$$

For this design example, Equation 15 expresses the input-capacitor RMS current as:

$$I_{CIN,RMS} = \frac{10A}{2}\sqrt{\frac{2\times1.2V}{10V}\times\left(1-\frac{2\times1.2V}{10V}\right)} = 2.14\ A \quad (15)$$

Placing multiple capacitors in parallel helps meet the RMS current rating and provides sufficient capacitance when accounting for DC voltage bias.

Output capacitors

The output capacitor you select will have a considerable impact on the load voltage. For most applications, the primary consideration is how the regulator responds to a large change in load current. You may also select the output capacitance based on steady-state output-voltage ripple or closed-loop bandwidth design objectives.

Steady state

Equation 16 estimates the output capacitance required to maintain an output voltage ripple (ΔVO) during steady-state operation as:

$$C_O \geq \frac{\Delta I_L}{16\times\Delta V_O\times f_{SW}} \quad (16)$$

Given a 10-mV steady-state output voltage ripple and a kL value of 0.4, Equation 17 calculates the output capacitance as:

$$C_O \geq \frac{0.4\times5A}{16\times10mV\times2MHz} = 6.25\ \mu F \quad (17)$$

Load transient response

The more stringent requirement is generally the capacitance needed to keep the output voltage within bounds during a large change in load current. The output capacitor supplies the difference between the load current and the inductor currents during load steps. When there is a large, fast change in the load current, such as a load step-up or step-down, the output-capacitor voltage dips or overshoots. The output capacitor must be the right size to supply the extra current to the load until the converter responds to the load change.

Load increase

Consider the load-step increase shown in Figure 26 to estimate the required output capacitance. This figure also shows the phase A inductor current and half the load current for simplicity and clarity. Because phase A provides half the load current, it only needs to respond to half the load-current change (for example, ΔIO/2). The area Q_{CO} represents the charge supplied by the output capacitor, while the phase A inductor current is rising to the new steady-state current level. The converter response in Figure 26 assumes the use of a hysteretic, constant on-time-based controller. Phase A and B high side on-times occur sequentially, with no overlap or delay during the transient. This assumes an almost ideal response but makes analysis simpler. The dashed line represents the approximate slew rate for the phase A average inductor current. Equation 18 expresses the slope of the line as:

$$\frac{dI_L}{dt} = \frac{\left(\frac{V_{IN}-2\times V_O}{2\times L}\right)\times D\times T + \left(\frac{-V_O}{L}\right)\times D\times T}{2\times D\times T} = \frac{\left(\frac{V_{IN}}{4}\right)-V_O}{L} \quad (18)$$

Equation 19 estimates the charge Q_{CO} as:

$$Q_{CO} = \frac{1}{2}\times\left(\frac{\Delta I_O}{2}\right)\times\Delta T = \frac{L\times(\Delta I_O)^2}{2\times(V_{IN}-4\times V_O)} \quad (19)$$

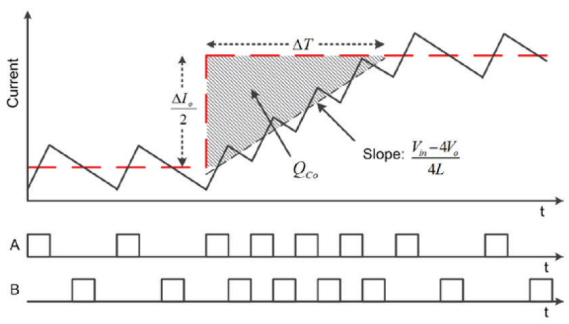


Figure 26. *Load-step increase transient response with phase A inductor current and switching signals.*

Assume that the phase B inductor current slews in the same manner and the charge supplied by the output capacitor is identical. You can then estimate the output capacitance with Equation 20:

$$C_O \geq \frac{2\times Q_{CO}}{\Delta V_O} = \frac{L\times(\Delta I_O)^2}{(V_{IN} - 4\times V_O)\times \Delta V_O} \quad (20)$$

Here, ΔVo is the allowed change in the output voltage. Equation 20 is very optimistic and does not account for delays, minimum off-times, variations in capacitance or a number of other nonideal aspects. A more accurate, conservative approach would be to use Equation 21:

$$C_O = \frac{2\times L\times(\Delta I_O)^2}{(V_{IN,min} - 4\times V_O)\times \Delta V_O} \quad (21)$$

For this design example, you could estimate the following output capacitance for a ΔVO of 24 mV (2 percent dip) and a 5-A load step assuming 330-nH inductors at the minimum input voltage (Equation 22):

$$C_o = \frac{2\times 330nH\times(5A)^2}{(10V - 4\times 1.2V)\times 24mV} = 132\ \mu F \quad (22)$$

The preceding approach assumes an infinitely fast load slew rate, an assumption that can result in a more conservative design. If you know the maximum load slew rate, you can refine the equations. Consider the load slew rate shown in **Figure 27**. Assuming the same average inductor current slew rate, you can refine the charge Q_{CO} estimate with Equation 23:

$$Q_{CO} = \frac{1}{2}\times\left(\frac{\Delta I_O}{2}\right)\times(\Delta T - \Delta T_S) = \frac{L\times(\Delta I_O)^2}{2\times(V_{IN} - 4\times V_O)} - \frac{(\Delta I_O)^2}{8\times S} \quad (23)$$

where S is the load current slew rate. Its units are amperes per second (A/s).

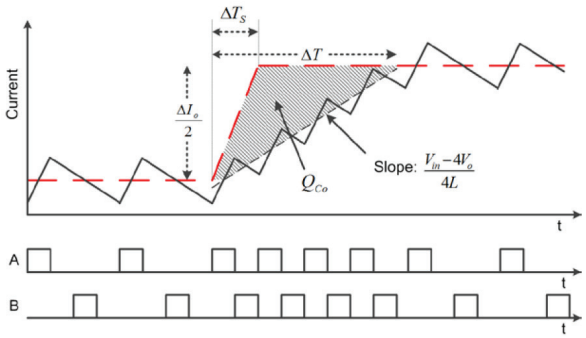


Figure 27. *Load-slew increase transient response with phase A inductor current and switching signals.*

Estimate the output capacitance with Equation 24:

$$C_o \geq \frac{2\times Q_{CO}}{\Delta V_O} = \frac{(\Delta I_O)^2}{\Delta V_O}\times\left[\frac{L}{(V_{IN} - 4\times V_O)} - \frac{1}{4\times S}\right] \quad (24)$$

As before, this estimate is optimistic and does not account for numerous delays nor other aspects. Equation 25 may be a more practical estimate:

$$C_o = \frac{2\times(\Delta I_O)^2}{\Delta V_O}\times\left[\frac{L}{(V_{IN,min} - 4\times V_O)} - \frac{1}{4\times S}\right] \quad (25)$$

Load decrease

The inductor slew rate in low-voltage applications is sometimes slower during a load-step decrease than during a load-step increase. You can take a similar approach to what I described above to estimate the output capacitance necessary to keep the output voltage within bounds during load step-down.

Consider the load step-down shown in **Figure 28**. This figure shows the phase A inductor current and the switching signals for each phase during the transient. The inductor current decreases by turning on the low-side switch and leaving it on. No high-side switch on-times trigger during the transition. This behavior is characteristic of hysteretic controllers (for example, constant on-time). Equation 26 expresses the inductor current slope during the interval as:

$$\frac{dI_L}{dt} = \frac{-V_O}{L} \quad (26)$$

The area QCo represents the excess charge that the output capacitor receives from the inductor during the transient. This excess charge causes the output voltage to overshoot. Equation 27 estimates the charge QCo as:

$$Q_{Co} = \frac{1}{2} \times \left(\frac{\Delta I_O}{2}\right) \times \Delta T = \frac{L \times (\Delta I_O)^2}{8 \times V_O} \quad (27)$$

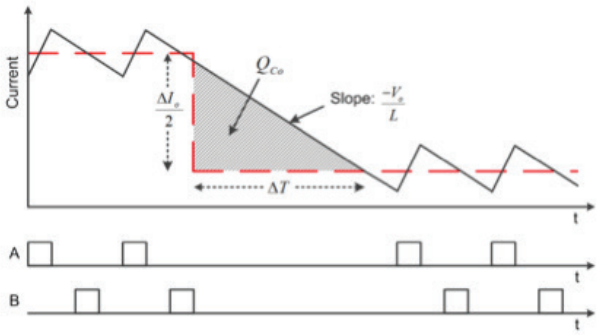


Figure 28. *Load-step decrease transient response with phase A inductor current and switching signals*

You can estimate the output capacitance assuming a symmetric response by the phase B inductor and the same amount of excess charge supplied to the output capacitor. Equation 28 shows the result:

$$C_O \geq \frac{2 \times Q_{CO}}{\Delta V_O} = \frac{L \times (\Delta I_O)^2}{4 \times V_O \times \Delta V_O} \quad (28)$$

This equation is fairly close to the actual converter response. While you should also account for sensing delays, component variation and other aspects, Equation 28 is a good starting point. For the design example, Equation 29 expresses the calculated output capacitance to meet the load step-down requirement:

$$C_O = \frac{330nH \times (5A)^2}{4 \times 1.2V \times 24mV} = 71.6\ \mu F \quad (29)$$

If you know the maximum load slew rate, you can adjust the equations so they are more accurate. Consider the load slew down shown in **Figure 29**.

Equation 30 refines the charge QCo estimate to:

(30)

where S represents the absolute value of the load-current slew rate (a positive number).

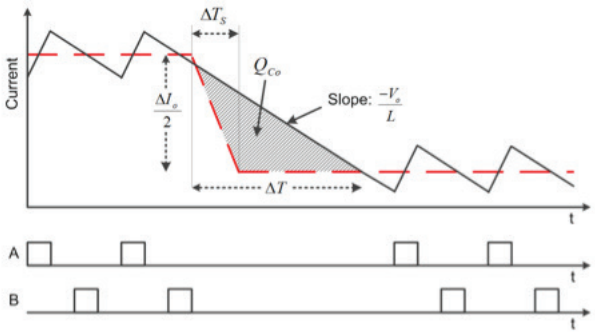


Figure 29. *Load-slew decrease transient response with phase A inductor current and switching signals.*

Equation 31 estimates the output capacitance:

$$C_O \geq \frac{2 \times Q_{CO}}{\Delta V_O} = \frac{(\Delta I_O)^2}{8 \times \Delta V_O} \times \left[\frac{L}{V_O} - \frac{1}{S}\right] \quad (31)$$

For the example converter design, the load step-up transient was the worst-case scenario. You should select the output capacitance based on that condition. Keep in mind, though, that the calculated values do not account for equivalent series resistance (ESR), DC voltage bias derating, temperature variation or other aspects. For ceramic capacitors, the ESR is usually small enough to ignore. Factor in additional capacitance deratings for aging, temperature and DC bias, which also increases the selected value.

You should also consider feedback-resistor tolerance and reference-voltage accuracy during design. If your overall design objective is to keep the output voltage within ±4 percent, you might need to size the output capacitance for ±2 percent variation if the feedback-resistor tolerance is ±1 percent and

the reference-voltage accuracy is ±1 percent. Using resistors with lower variation can help alleviate this requirement.

Closed-loop bandwidth

The output capacitance also impacts the converter's closed-loop bandwidth. A larger output capacitance tends to result in a lower crossover frequency. This is primarily due to the lower frequency of the inductor-capacitor (LC) double pole. For example, consider the Bode plots in Figure 30, which plots measurements taken on a 12-V input, 1.2-V output, 2-MHz per-phase prototype with two different values of nominal output capacitance. The converter with 91 µF of output capacitance has a crossover frequency of 319 kHz; with 138 µF of output capacitance, the crossover frequency drops to 219 kHz. The phase margin for both scenarios is adequate at over 50°.

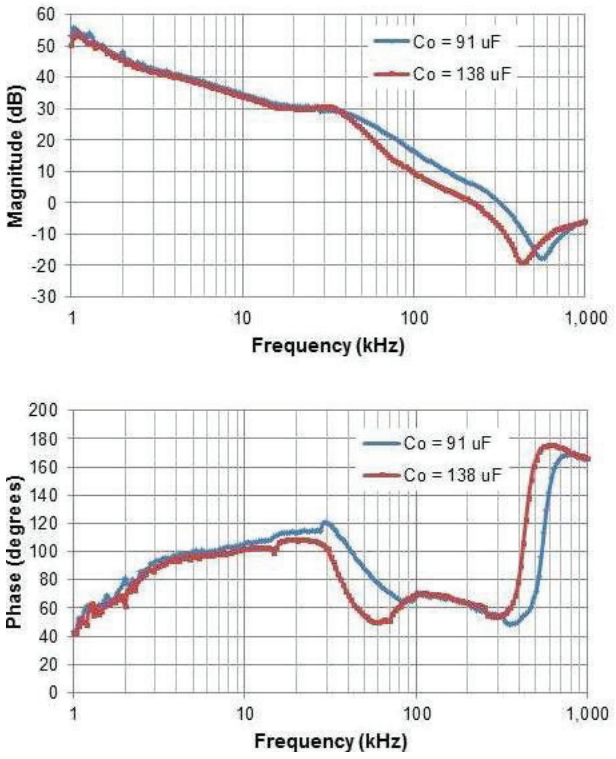


Figure 30. *Bode plot measurements for two different output-capacitance values.*

Series capacitor

The series capacitor is a somewhat unique addition. Unlike input and output capacitors, a series capacitor's primary role is not decoupling but energy transfer. As a result, the RMS currents in a series capacitor are generally larger than input and output capacitors. Other converter topologies like single-ended primary-inductor converters (SEPICs) and boost-buck (Ćuk) converters also use capacitors for energy transfer. The design methodology for the series capacitor follows a similar approach.

In the series capacitor buck converter, the series capacitor acts as a DC voltage source. It is not designed for resonant operation with a large voltage ripple like an inductor-inductor-capacitor (LLC) converter. Instead, the voltage ripple is designed to be limited to about 5 to 10 percent of the nominal DC voltage of $V_{IN}/2$. During operation, the phase A inductor charges the capacitor, increasing its voltage; the voltage decreases as the phase B inductor discharges it. A larger capacitance value will result in less peak-to-peak ripple than a lower capacitance value (**Figure 31**).

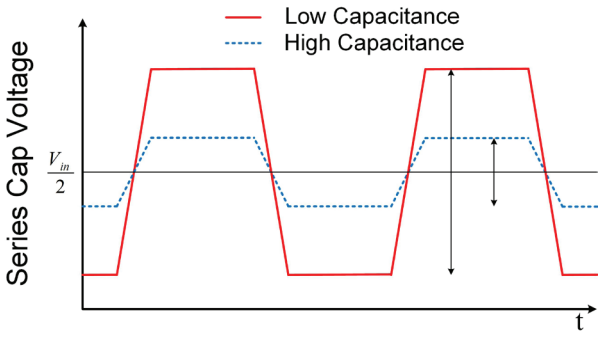


Figure 31. *Series capacitor ripple with low and high capacitance values.*

Equation 32 describes the voltage ripple in the series capacitor:

$$\Delta V_{Ct} = \frac{D \times T \times I_{Ct}}{C_t} = \frac{\left(\frac{2 \times V_O}{V_{IN}}\right) \times \left(\frac{I_O}{2}\right)}{C_t \times f_{SW}} \quad (32)$$

Rearranging Equation 32, you get the series capacitor design equation (Equation 33):

$$C_t \geq \frac{2 \times V_O \times I_O}{k_{Ct} \times V_{IN,min}^2 \times f_{sw}} \quad (33)$$

Here, ΔV_{Ct} is replaced with $k_{Ct} \times V_{IN}$,min/2. The coefficient k_{Ct} represents the percentage voltage ripple and is selectable in the 0.05 to 0.1 range. The operating conditions that will result in the largest voltage ripple are the lowest input voltage (highest duty ratio) and highest load current. For this design example, the value for k_{Ct} is 0.08.

Equation 34 then expresses the calculated series capacitance as:

$$C_t = \frac{2 \times 1.2V \times 10A}{0.08 \times (10V)^2 \times 2MHz} = 1.5\ \mu F \quad (34)$$

This calculated value assumes an ideal capacitor. As I mentioned previously, ceramic capacitors suffer from reduced capacitance as a DC voltage is applied. The nominal DC voltage for the series capacitor is V_{IN}/2, or 5 V to 7 V for this design example. Check the capacitor data sheet for the capacitance derating at the operating voltage and increase the nominal capacitance accordingly. You may calculate 1.5 µF and ultimately select a 2.2-µF capacitor.

You must also consider the series capacitor's RMS current. The capacitor current will cause self-heating, and it is important not to exceed the capacitor's operating temperature rating. For most applications, I recommend X7R capacitors with a temperature rating up to 125°C. If the RMS current is too high for a single capacitor, you can place multiple capacitors in parallel.

The series capacitor current waveform illustrated in **Figure 14** is similar to the high-side MOSFET current waveform. Equation 35 expresses the RMS current squared as:

$$I_{Ct,RMS}^2 = 2 \times D \times I_{L,RMS}^2 \quad (35)$$

Equation 36 expresses the RMS current of the capacitor as:

$$I_{Ct,RMS} = \sqrt{\left(\frac{4 \times V_O}{V_{IN}}\right) \times \left[\left(\frac{I_O}{2}\right)^2 + \left(\frac{\Delta I_L}{12}\right)^2\right]} \quad (36)$$

The largest RMS current occurs at the highest load current and lowest input voltage (highest duty ratio). Equation 37 calculates the series capacitor RMS current for the design example as:

$$I_{Ct,RMS} = \sqrt{\left(\frac{4 \times 1.2V}{10V}\right) \times \left[\left(\frac{10A}{2}\right)^2 + \left(\frac{0.4 \times 5A}{12}\right)^2\right]} = 3.49\ A \quad (37)$$

There is a trade-off in series capacitor selection. A larger series capacitance will reduce voltage ripple, but it will also delay startup. Using the TPS54A20 as an example, the series capacitor is pre-charged to half the input voltage before switching begins. This enables a predictable, smooth startup. **Figure 32** shows an example startup sequence.

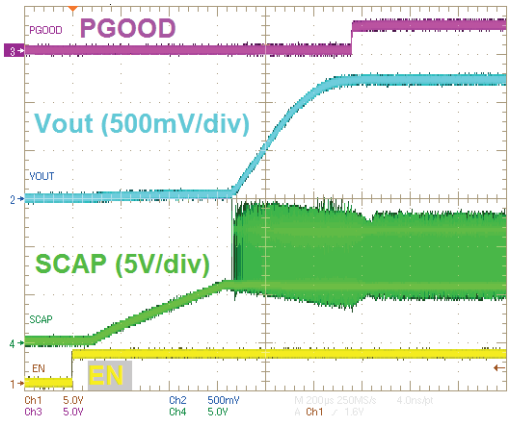


Figure 32. *Converter startup with series capacitor pre-charge delay.*

The converter uses a constant current source to pre-charge the series capacitor. Equation 38 estimates the delay due to pre-charging as:

$$t_{PC} = \frac{C_t \times \left(\frac{V_{IN}}{2}\right)}{I_{PC}} \quad (38)$$

where I_{PC} is the pre-charge current and t_{PC} is the pre-charge delay time. In **Figure 32**, with 1-µF series capacitance and a 10-mA pre-charge current, the pre-charge delay is approximately:

$$t_{PC} = \frac{1\mu F \times 12V}{2 \times 10mA} = 600\ \mu s \quad (39)$$

Feedback network

You have several options to consider when designing the feedback network. **Figure 33a** shows a basic feedback network consisting of two feedback resistors connected to form a voltage divider from the output voltage to the controller's feedback pin. You might select 10 kΩ for the lower resistor (R_2) as a starting point. Equation 40 calculates the value of R_1 as:

$$R_1 = \frac{R_2 \times (V_{OUT} - V_{FB})}{V_{FB}} \quad (40)$$

where VFB is the reference voltage.

In **Figure 33b**, a capacitor (C_1) is added to the feedback path in parallel with R_1. The feedback network in **Figure 33c** adds C_1 and resistor R_3. In both configurations, C_1 helps improve the closed-loop response of the converter. Both the transient-response characteristics and the phase margin will improve if designed correctly. References [6] and [7] offer more details, analysis and experimental results describing these feedback networks.

The network shown in **Figure 33d** adds resistor R_4. In combination with the parasitic capacitance on the FB pin, R_4 forms a low-pass filter with a high cutoff frequency. It primarily helps filter out unwanted noise from impacting the converter behavior. This can be beneficial if the converter is operating at a high switching frequency.

As usual, there are design trade-offs. The feedback network in **Figure 33a** is the simplest, but does not provide any phase boost. The network in **Figure 33b** provides phase boost, but the network in **Figure 33c** has more flexibility and lower high-frequency gain. The last network shown in **Figure 33d** has a lot of flexibility and robustness, but comes at the cost of more components.

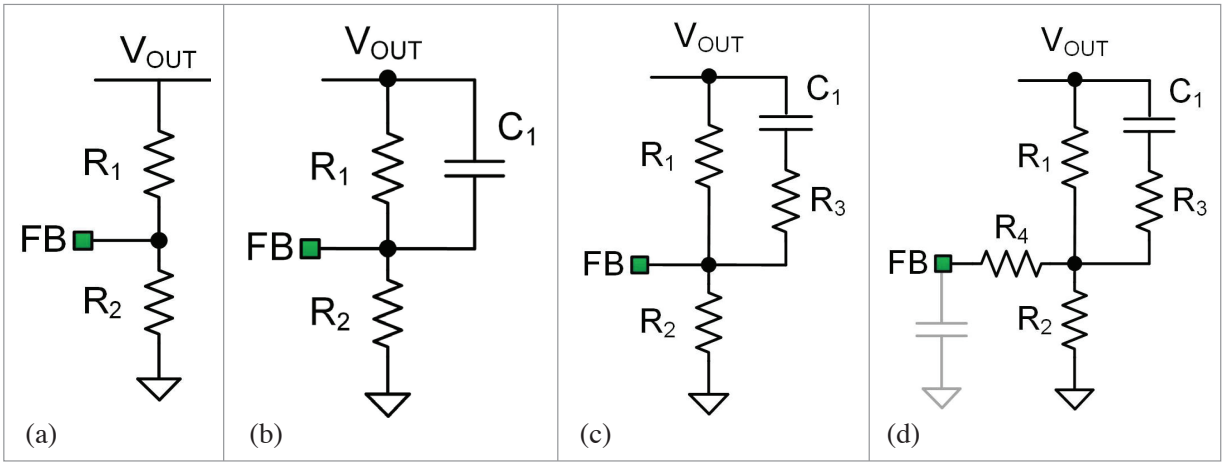


Figure 33. *Four different options of output voltage feedback network configurations.*

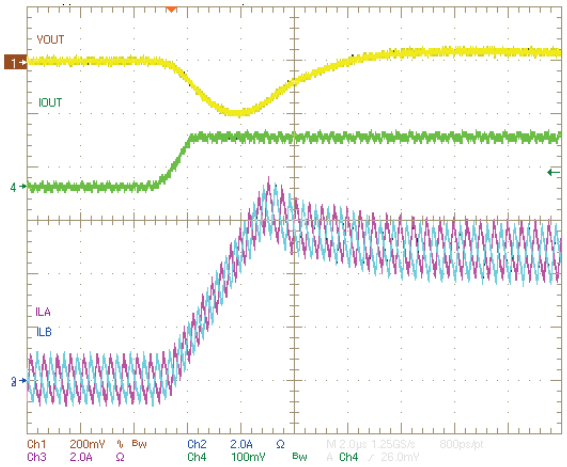
Table 2 compares the first two feedback network designs, measuring the results from a prototype converter with 12-V input, 1.2-V output, 250-nH inductors, 191-µF output capacitance, 2-MHz per phase frequency and a 4.8-A load. As the results indicate, the crossover frequency and phase margin improve just by adding C_1. For this reason, I recommend including C_1 in most designs. Even though it is an additional component, the increased bandwidth and phase margin can help reduce the output capacitance required to meet load-transient specifications.

Configuration	Crossover frequency	Phase margin
(a)	188 kHz	36.9°
(b)	196 kHz	48.8°

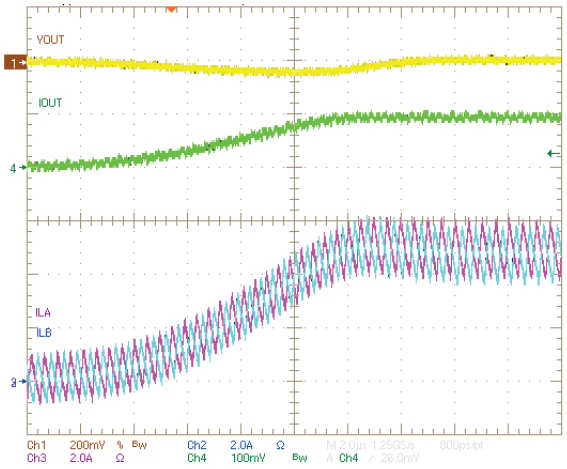
Table 2. *Crossover-frequency and phase-margin comparison.*

Current limit

Overcurrent protection is a common feature in power converters. In the event of an overload condition or a short circuit on the output, the converter turns off when the output current exceeds the overcurrent level. To detect the output current, you typically measure the inductor current. There are some cases (like during large, fast load transients) where the inductor current will exceed the output current level, as shown in **Figure 34a**. This could cause a false overcurrent trip if you set the current limit too low. To avoid this scenario, set the current-limit level to approximately 1.5 times the full-load current level. If the maximum load current slew rate is relatively slow, as shown in **Figure 34b**, you may be able to be more aggressive with the current-limit level.



(a)



(b)

Figure 34. *Inductor currents and output-voltage response to a fast transient (a) and a slow transient (b).*

Soft-start time

Most converters have a selectable soft-start time. This feature limits inrush current by slowly increasing the output voltage during startup. One important objective is to avoid tripping the overcurrent protection of the bus converter or POL converter. Select the soft-start time for a given output capacitance and output voltage based on your

desired output-current limit. Assuming a constant output-voltage rise rate during soft start, Equation 41 estimates the soft-start time as:

$$t_{ss} = \frac{C_o \times V_o}{I_o} \quad (41)$$

where Io represents the combined output current from the inductors used to charge the output capacitance (C_O) to the voltage level (V_O). It does not assume a load applied to the output of the converter.

Alternatively, if you select the soft-start time from a few pre-programmed values, you can estimate the average output current during startup as:

$$I_o = \frac{C_o \times V_o}{t_{ss}} \quad (42)$$

HotRod™ package

The TPS54A20 benefits from the HotRod packaging used to enclose the integrated circuit (IC). This packaging technology is a flip-chip form of quad flat no-lead (QFN) packaging. It removes bond wires and their associated parasitic resistance and inductance.

Figure 35 is a photograph of the bottom side of the TPS54A20, while **Figure 36** shows the pin assignments from a top-down view (through the IC). The pinout design enables a simple, single-sided layout of the converter. The IC is 3.5 mm by 4 mm.

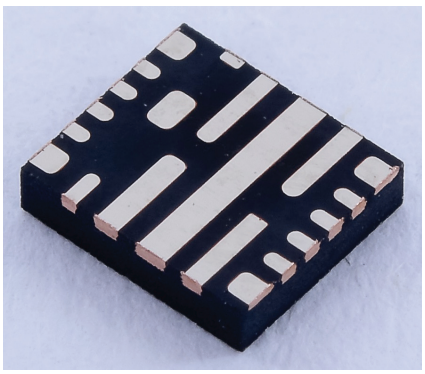


Figure 35. *Photograph of the TPS54A20 showing the flip-chip HotRod packaging.*

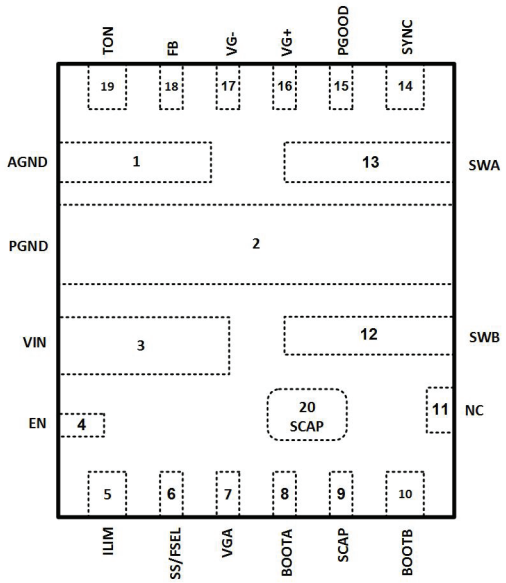


Figure 36. *Pinout of the TPS54A20 with a top-down view.*

Converter layout

Physical layout is critical for design success. A general principle is to keep power-converter layouts as compact as possible. This helps reduce conduction loss, switching loss and EMI. The most important placement is the input capacitors and series capacitor. You must place these components as close as possible to the IC that contains the power MOSFETs. Placing these capacitors close to the IC keeps high-frequency switching-loop inductance low and reduces switching loss and voltage stress on the MOSFETs. For the same general reason, you should also place the bootstrap capacitors and gate-drive capacitors close to the IC. See **Figures 37-38** for example layouts.

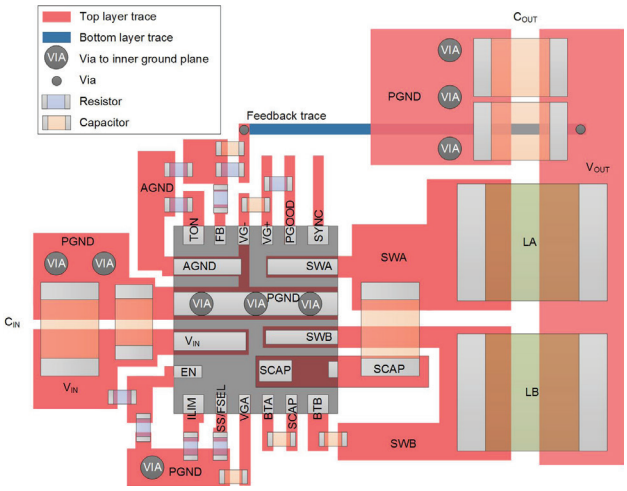


Figure 37. Example layout diagram for the TPS54A20.

Proper ground-return paths are also important. Internal ground planes not only provide a low-impedance current return path but also act as a heat sink for the converter. Insert vias on the power ground (PGND) pins that connect with the internal ground planes.

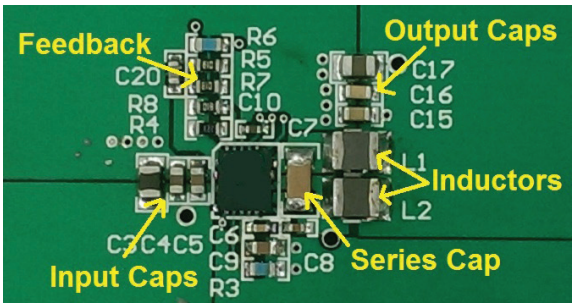


Figure 38. Example printed circuit board (PCB) layout for the TPS54A20.

Also, I recommend keeping sensitive signal lines away from switching nodes. For example, route the feedback trace coming from the output voltage away from the switching nodes and place the feedback network close to the IC. **Figure 37** shows the blue feedback trace routed on the bottom layer, away from the switching nodes (for example, SWA, SWB, SCAP). Treat other sensitive analog traces similarly. For more detailed layout recommendations, see Reference [8].

Experimental results

Following are a few experimental results to highlight the capabilities of the series capacitor buck converter. The target application is 12-V input, 1.2-V output with 10-A current-output capability. I used the TPS54A20 integrated converter in this example [8].

Figure 39 shows a simplified schematic of the converter.

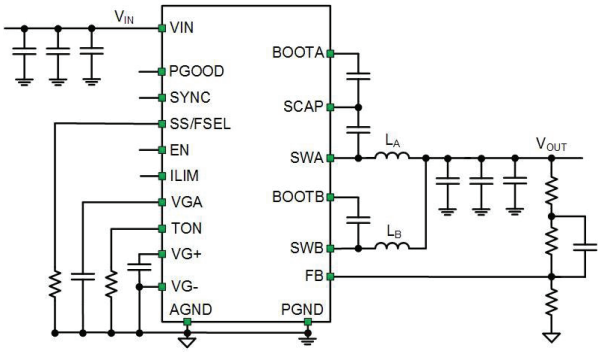


Figure 39. Simplified schematic of the experimental prototype using the TPS54A20.

High-frequency controller

The TPS54A20 contains a high-frequency controller; **Figure 40** shows its block diagram. The heart of the controller is an adaptive constant on-time control scheme. This scheme provides very fast transient response and is internally compensated. The error amplifier monitors the feedback pin voltage and triggers a high-side switch on-time when the output is lower than the trigger value. An input voltage feed-forward block sets the nominal on-time for the converter and corrects for changes in the input voltage.

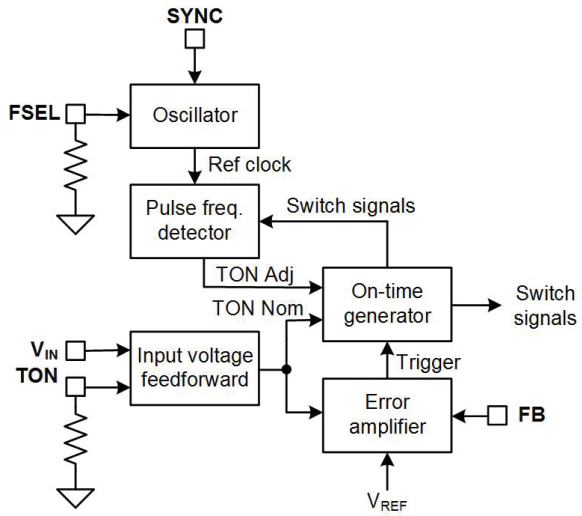


Figure 40. High-frequency controller block diagram.

A unique feature of this controller is that a phase-locked loop (PLL) adjusts the on-time. This adaptation works to lock the frequency and phase of on-time pulses to a reference clock. The reference clock can be an internal clock or an externally supplied synchronization clock. The PLL keeps the converter operating at a fixed frequency in steady state despite changes in input voltage, temperature, load current and other variables.

Efficiency comparison

Figure 41 compares series capacitor buck-converter efficiency to a standard 10-A buck converter. Both converters are designed to operate from a 12-V input and provide 10 A under full load conditions at a 1.2-V output. The conventional buck converter uses the TPS54020 and is switching at 530 kHz. The series capacitor buck converter uses the TPS54A20 and is switching at 2 MHz per phase. The inductors of both converters were sized for roughly the same DCR. I took efficiency measurements at room temperature with no airflow.

As **Figure 41** indicates, the series capacitor buck converter has higher efficiency even though it is operating at an almost four-times-higher switching frequency. Peak efficiency is 2 percentage points better.

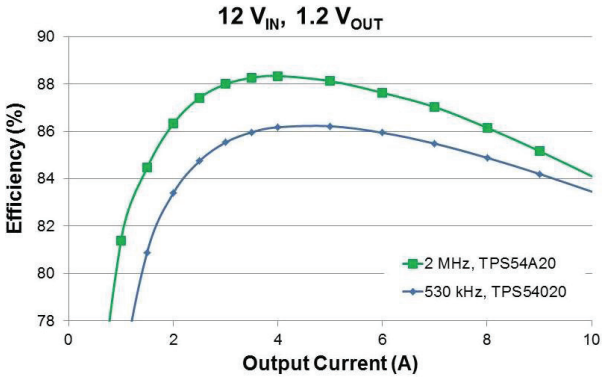
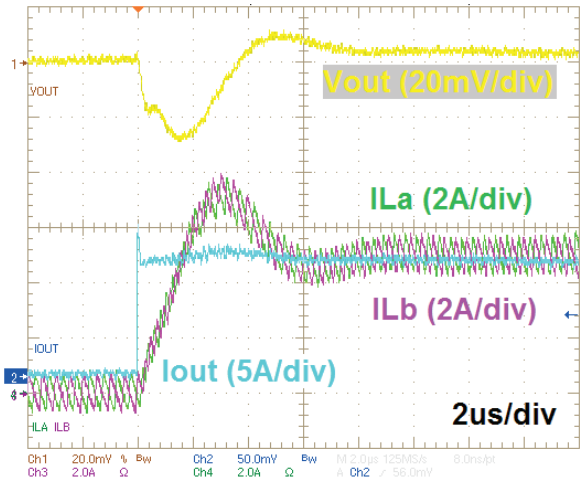


Figure 41. Measured efficiency comparison of a buck converter (blue) and a series capacitor buck converter (green).

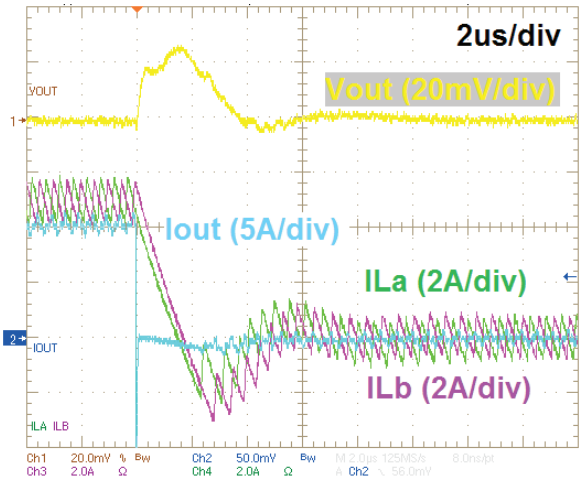
Transient response

Figure 42 shows the series capacitor buck converter's response to a large, fast load transient, displaying the output voltage, inductor currents and load current. The load transient is a full-load (10 A) step-up and step-down at a slew rate of approximately 500 A/µs. The converter is operating at 12 V_{IN}, 1 V_{OUT} and 2 MHz per phase with about 390 µF of output capacitance. The output-voltage deviation is less than 25 mV and the recovery time is less than 4 µs.

During load step-up, the controller triggers on-time pulses in rapid succession in order to increase the inductor currents. During load step-down, the controller does not trigger any on-time pulses but allows the low-side switches to remain on and the inductor currents to decrease. The frequency is not fixed during the transient but is fixed during steady state.



(a)



(b)

Figure 42. *Transient response to a 10-A load step-up (a) and step-down (b).*

Note that the inductor current sharing is excellent during the transients. During load increase, the average inductor currents are well matched. At the end of load decrease, there is a slight mismatch in the inductor currents due to the timing of the controller response. However, the inductor currents naturally return to even current sharing within a few switching cycles.

Thermal

Thermal dissipation is often a concern for converter designers. Heat can affect other devices in the system and make converters less efficient. The series capacitor buck converter reduces overall size without creating a thermal issue. **Figure 43** shows an example thermal image of the converter shown in **Figure 38**. The operating conditions are 12 V_{IN}, 1.2 V_{OUT}, 2 MHz per phase, 10-A load current, room temperature and no forced airflow.

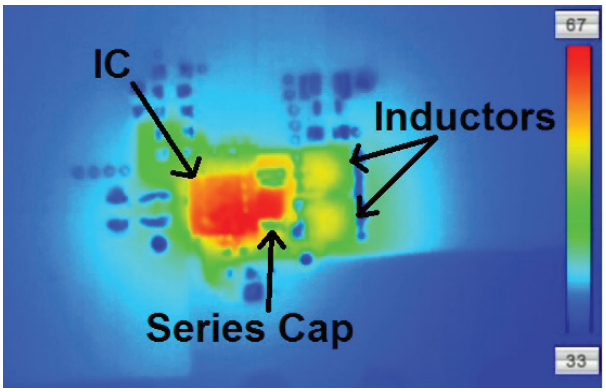


Figure 43. *Thermal image taken at a 10-A load, room temperature, no airflow.*

Most of the power loss is in the IC, and it shows up as one of the hottest components. The power loss and physical size of the IC are roughly the same as other 10-A buck converters. You should still follow appropriate layout guidelines to provide ample thermal-dissipation paths.

The inductors are much smaller in a series capacitor buck converter. Nonetheless, the reduction in inductor size does not create a thermal bottleneck. As shown in **Figure 43**, the temperature rise in the inductors is moderate, and does not create a hot spot.

Solution-size comparison

Figure 44 compares the total solution size of the series capacitor buck converter to other converters with similar ratings. The current density of POL converters on the market today is less than 20 A/cm3. Some research converters using compound semiconductors or special magnetics exceed 30 A/cm3 [9], [10]. The series capacitor buck converter (TPS54A20) enables converters with over 60 A/cm3. This represents a three- to seven-times improvement compared to state-of-the-art buck converters.

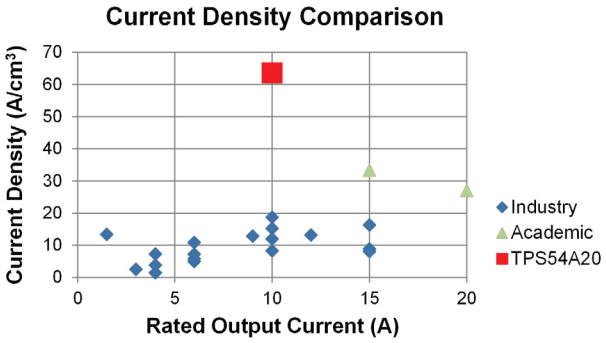
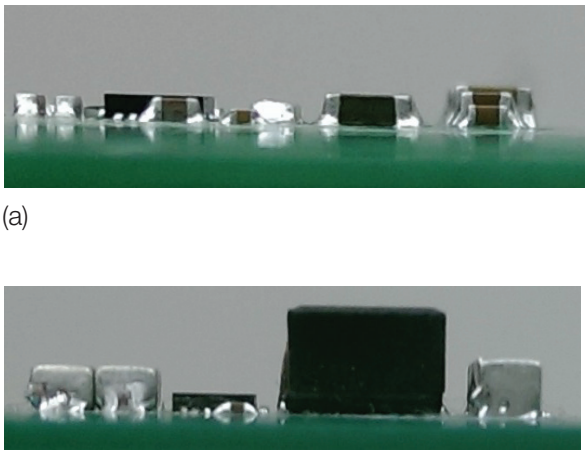


Figure 44. *Current density comparison of voltage regulators designed for a 12-V input.*

One of the key benefits is height reduction; you can place low-profile series capacitor buck converters on the back side of circuit boards. **Figure 45** is a height comparison. The series capacitor buck solution is 1.2-mm tall, as shown in **Figure 45a**. Conventional buck converters used in the same application are typically 4- to 5-mm tall, as shown in **Figure 44b**.



(a)

(b)

Figure 45. *Height comparison between series capacitor buck solution (a) and conventional buck converters (b).*

Figure 46 highlights the groundbreaking nature of this converter topology. The figure shows a 10-A series capacitor buck converter power-module prototype next to an inductor used on a 10-A buck converter evaluation module. The module prototype is 16 mm by 10 mm by 1.85 mm, including printed circuit board (PCB) thickness, which results in a total volume of 296 mm3. The buck converter inductor is 10.2 mm by 10.2 mm by 4.7 mm, resulting in a volume of 489 mm3. The volume of the entire series capacitor buck converter, including PCB thickness, is 40 percent smaller than just the buck inductor.

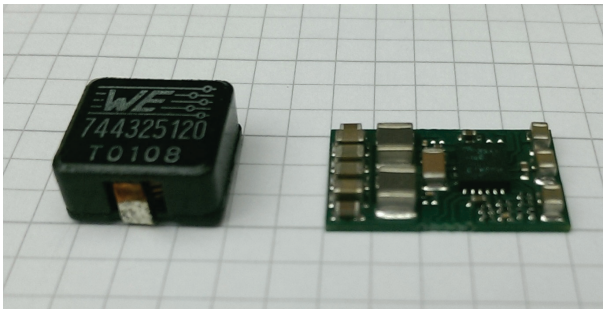


Figure 46. *Size comparison of a 10-A buck inductor and a 10-A series capacitor buck converter.*

Summary

Point-of-load buck converters commonly regulate the supply voltage of processors, memory, application-specific integrated circuits (ASICs) and field-programmable gate arrays (FPGAs). Power converters take up a large amount of board space in most applications. Increasing switching frequency reduces converter size and also leads to improved transient response and lower BOM costs. But buck converters have fundamental limitations that prevent designers from pushing switching frequencies higher. Their primary limitations are switching loss and narrow on-time pulse widths.

The series capacitor buck converter overcomes many of the challenges of attempting high-frequency operation – reducing switching loss, doubling on-times, automating inductor current balancing, and decreasing inductor current ripple. Compared to state-of-the-art buck converters, the series capacitor buck converter enables three- to seven-times smaller size, higher efficiency and fast transient response.

This paper included design guidelines for the series capacitor buck converter, with a discussion of switching-frequency and inductor-selection trade-offs, and a focus on efficiency impact. I provided input- and output-capacitor estimation equations; covered the affect on transient performance and closed-loop response; reviewed series capacitor selection and ratings, feedback-network designs, current-limit selection, and soft-start time; and included some sample efficiency, load transient and thermal profile results. Layout guidelines centered on compact component placement to reduce parasitic elements.

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