**Power Supply Design Seminar**

# Flyback transformer design considerations for efficiency and EMI

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TEXAS INSTRUMENTS

# Flyback transformer design considerations for efficiency and EMI

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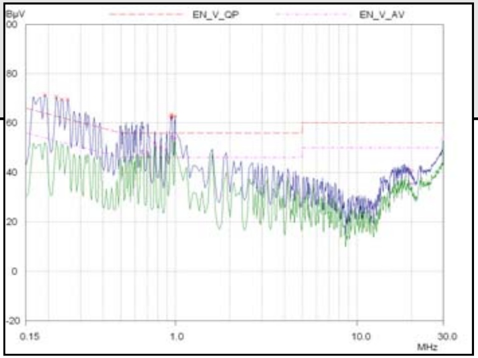
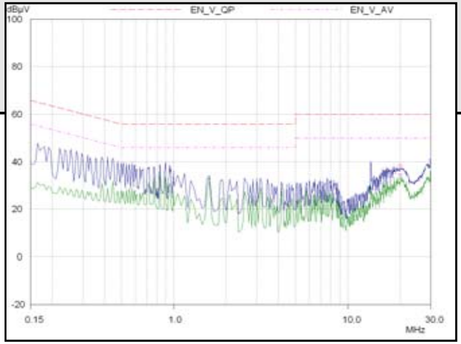
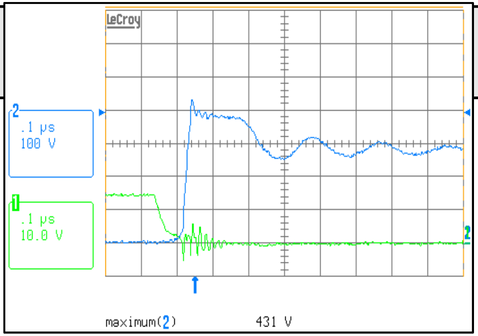
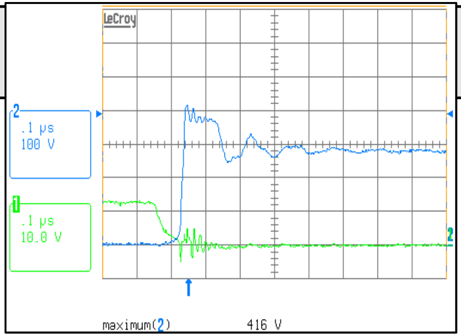
# Agenda

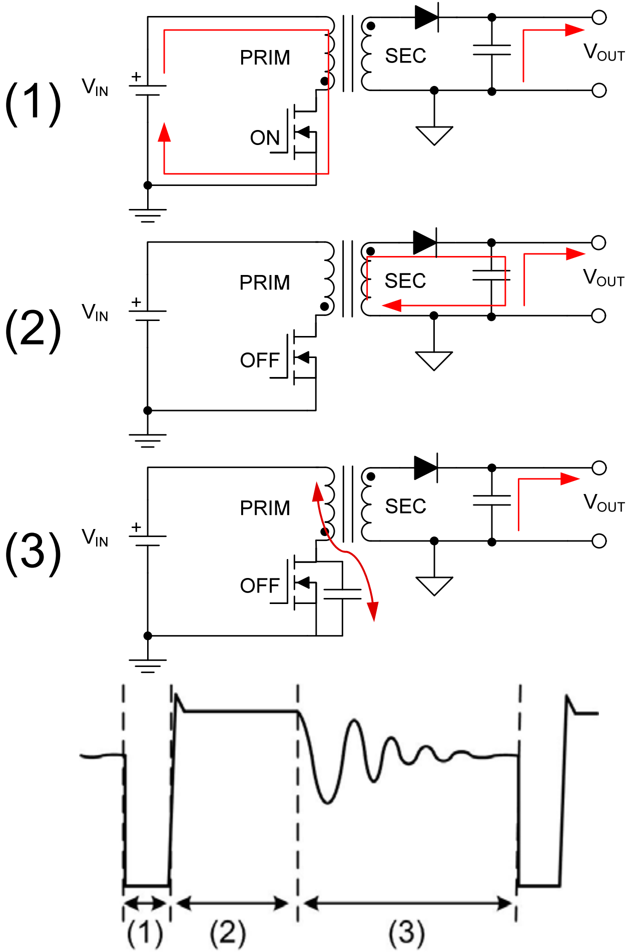
- Flyback transformer basics
- Review of Flyback transformer losses:
  - Core loss – dependence on DC bias, duty cycle, wave-shape
  - Causes of AC copper loss
  - Proximity effects explained
  - Leakage inductance & how to estimate it
  - Effect of snubber clamp voltage on leakage losses
  - Design optimisation example
    - Choice of wire size, strands, layer stack-up to reduce leakage inductance and proximity effects
- EMI
  - CM cancellation & balancing techniques
  - Design example

# Transformer is critical!

Change only the transformer – can simultaneously improve efficiency and EMI

| Parameter | TR #5A (poorest implementation tested) | TR #2 (best implementation tested) |
|---|---|---|
| Efficiency<br>(115 V ac, 65 W) | 86.3% | 88.9% |
| EMI – Quasi-peak & average emissions vs. limit | +8 dB over<br><br> | <br> <br>-16 dB under |
| Leakage inductance | 6.8 uH | 3.2 uH |
| Leakage Spike | 431 Vpk,<br>~200 ns<br><br> | <br> <br>416 Vpk,<br>~100 ns |

# Flyback transformers



- Conventional transformer stores minimal energy
- Flyback “transformer” – really coupled-inductor
  - FET ON ⟶ only primary current flows
    - Stores energy in air-gap
    - Load current from output capacitor only
  - FET OFF ⟶ only secondary current flows
    - Air-gap energy transferred to load
  - FET OFF, diode OFF ⟶
    - DCM circulating current
    - Load current from output capacitor only
- DCM ⇒ all stored energy delivered to load
- CCM ⇒ not all stored energy delivered to load, primary current starts when secondary still non-zero

# Flyback transformer losses

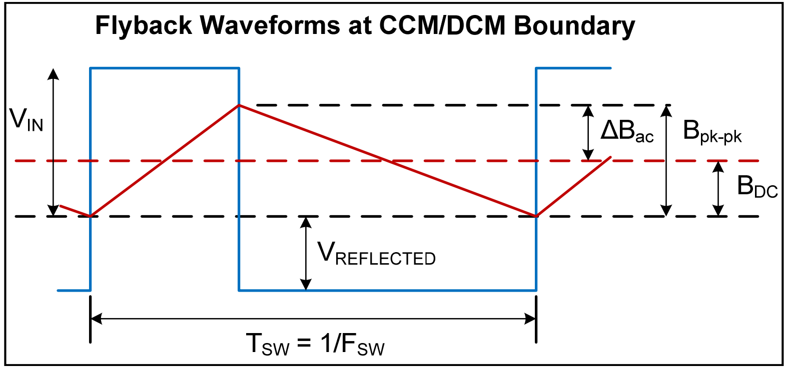
- Core loss
  - Depends on core material characteristics, $B_{DC}$, $B_{ac}$, $F_{SW}$, dB/dt – wave-shape & duty-cycle
- Copper loss
  - DCR – depends on the wire cross-section and length (N, MLT)
  - ACR – depends on choice of wire diameter versus $F_{SW}$ and construction (layer stackup, proximity effects)
- External loss:
  - Leakage inductance energy

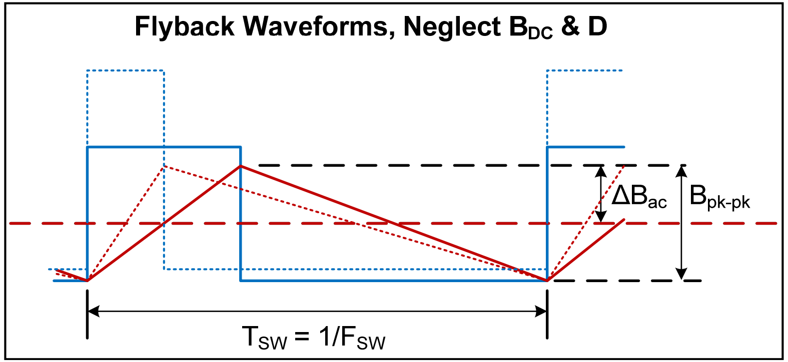
$$P = \frac{1}{2} \cdot L_{leak} \cdot I_{pk}^2 \cdot f_{sw}$$

    - Large percentage of this power dissipated in external snubber, clamp circuit
    - Magnetising energy also dissipated, depends on clamp level and leakage inductance

# Core loss – effect of waveform and DC flux bias [1, 2]

- Traditional assumptions:
  - DC bias has no effect
  - Square-wave close to sine
- Traditional method:
  - Calculate $\Delta B_{ac}$ at $F_{SW}$, neglect $B_{DC}$
  - Core material manufacturer data sheet:
    - Read core loss at $\Delta B_{ac}$ and $F_{SW}$
    - Loss data provided for sine excitation
- The reality:
  - DC bias can have significant impact on core loss
  - Waveform and duty cycle can have significant impact
  - Several papers published on the subject. See references 1 and 2.





# Effect of waveform on core loss

- Proposed curve fit equation[1] for square-wave excitation, based on measured data:

$$\frac{P_{v\_rect}}{P_{v\_sine}} = F_{waveform} = \frac{8}{\pi^2\cdot[4D\cdot(1-D)]^{\gamma+1}}$$ *(Eq. 1)*

- $P_{V\_SINE}$ – conventionally-calculated core loss
  - For sinewave excitation of equal flux swing (available from the material data sheet)
- $D$ – duty cycle of square-wave
- $\gamma$ – correction factor
  - Depends on material, frequency and temperature
  - Could be measured and provided by the magnetic material manufacturers
  - Values for several ferrites at 25°C empirically determined by Mingkai Mu [1]

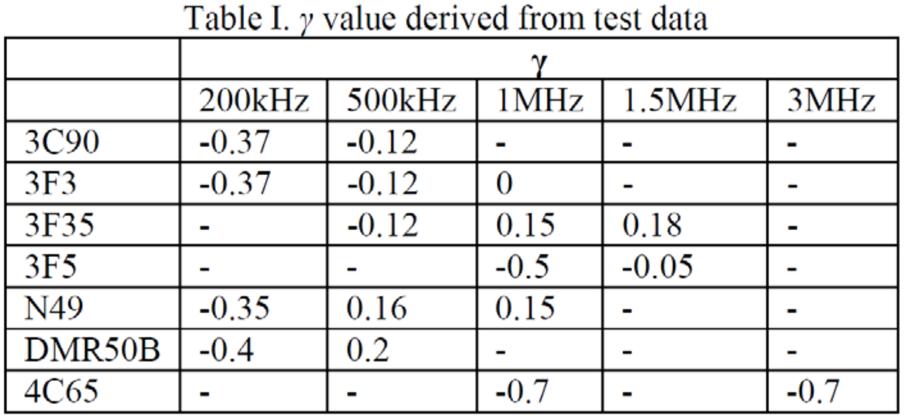


Table I. $\gamma$ value derived from test data

| | $\gamma$ | | | | |
|---|---|---|---|---|---|
| | 200kHz | 500kHz | 1MHz | 1.5MHz | 3MHz |
| 3C90 | -0.37 | -0.12 | - | - | - |
| 3F3 | -0.37 | -0.12 | 0 | - | - |
| 3F35 | - | -0.12 | 0.15 | 0.18 | - |
| 3F5 | - | - | -0.5 | -0.05 | - |
| N49 | -0.35 | 0.16 | 0.15 | - | - |
| DMR50B | -0.4 | 0.2 | - | - | - |
| 4C65 | - | - | -0.7 | - | -0.7 |

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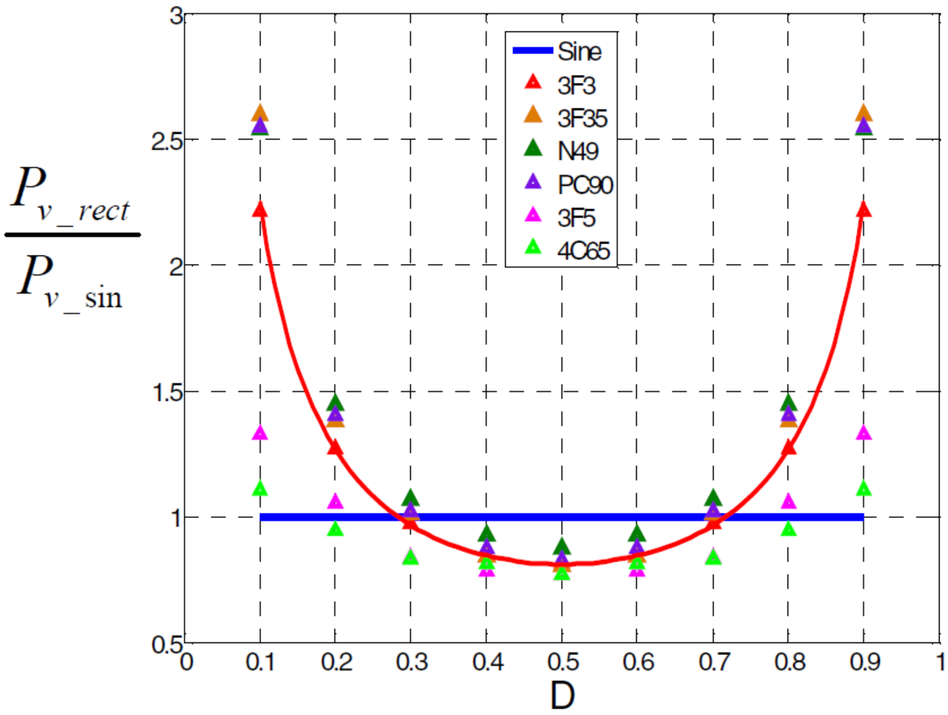
# $F_{WAVEFORM}$ for square-wave versus $D$ at $F_{SW}$ 1 MHz [1]

- 50% duty-cycle ⇒ lower loss versus sine
- Significant loss increase as D ⟶ 100% or D ⟶ 0%
- Why?
  - dB/dt induces $I_{EDDY}$ flow in core, eddy loss proportional to $I_{EDDY}^2$
- Some new HF materials better at duty cycle extremes, e.g. 3F5 & 4C65
- Recommend that you make your own measurements



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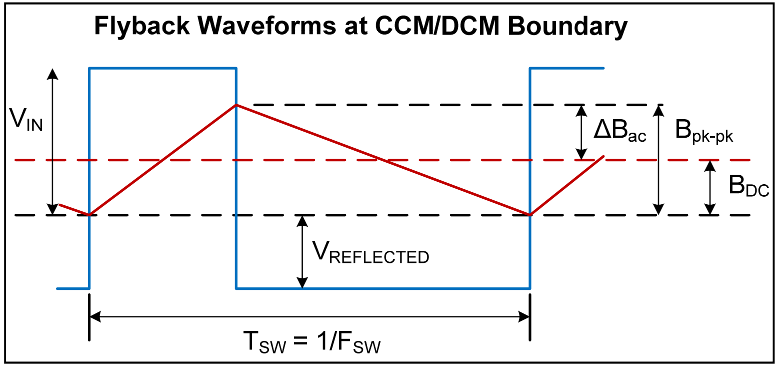
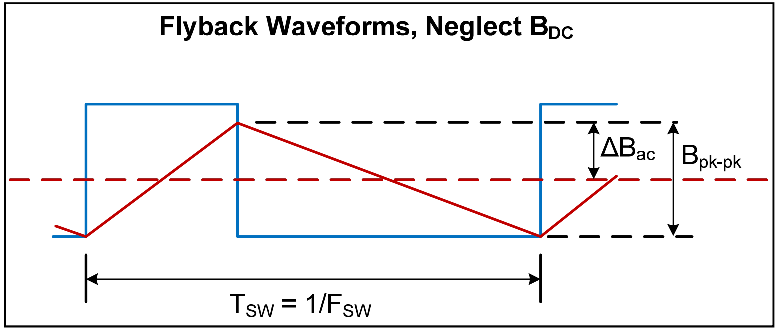
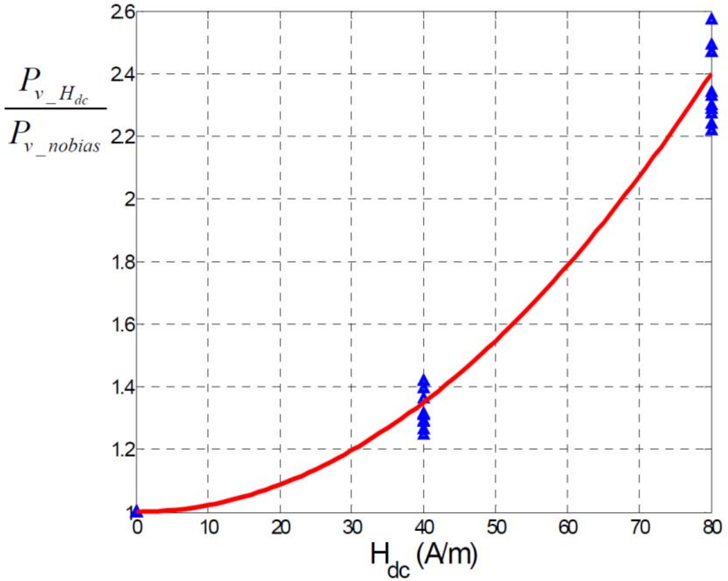
# Effect of DC bias

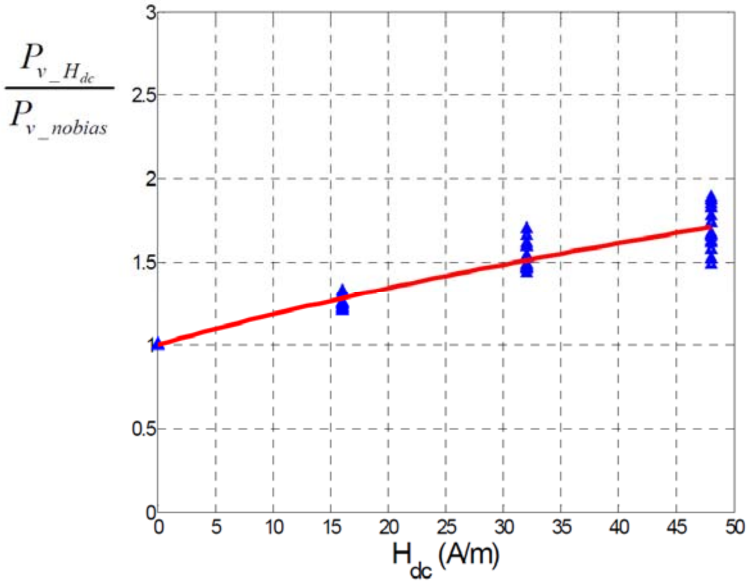
- DC bias shown to have significant impact
  - Many different papers published
  - None of the papers offers convincing explanation of the causes of this effect
- Ref [2] – The effect is measured and quantified for two ferrite core materials:
  - 3F35
  - PC90
- A function $F(H_{DC})$ is developed (by curve fit to measured data)
- Enables calculation of core loss under DC bias





# Loss versus DC bias normalized to zero DC bias





3F35 @ 500 kHz, vary $B_{PK}$, $D$

Curve fit: $F(H_{dc}) = 2.1875\times10^{-4} H_{dc}^{2} + 1$

PC90 @ 1 MHz, vary $B_{PK}$, $D$

Curve fit: $F(H_{dc}) = \sqrt{0.04\times H_{dc} + 1}$

*Reproduced from [2] with permission*

# Core loss discussion points

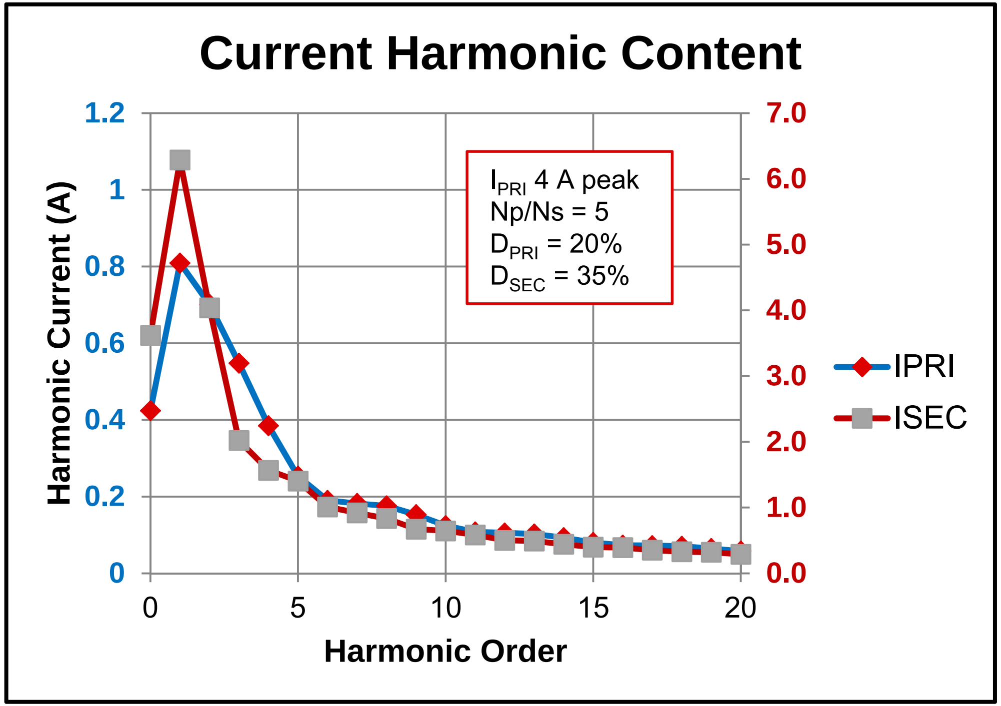
- DC bias, wave-shape and duty-cycle cannot be neglected!
  - *May explain excess core loss in some situations*
- Practical method to account for effects:

$$P_{v\_total} = P_{v\_sine} \cdot F_{waveform}(\gamma, D) \cdot F_{DC}(H_{DC}) \quad \textit{(Eq. 2)}$$

- Effect of wide duty cycle range:
  - Often-neglected penalty for wide input/output voltage range
  - ***Advantage of flyback over forward***
- Effect of DC bias:
  - May reduce benefit of deep CCM operation
  - Illustrates advantage of double-ended topologies over single-ended
- Need to insist that ferrite manufacturers provide more and better loss data:
  - *Loss versus DC-bias and D, provide $\gamma$ and $F_{DC}$ data*
- Recommend making your own in-circuit measurements

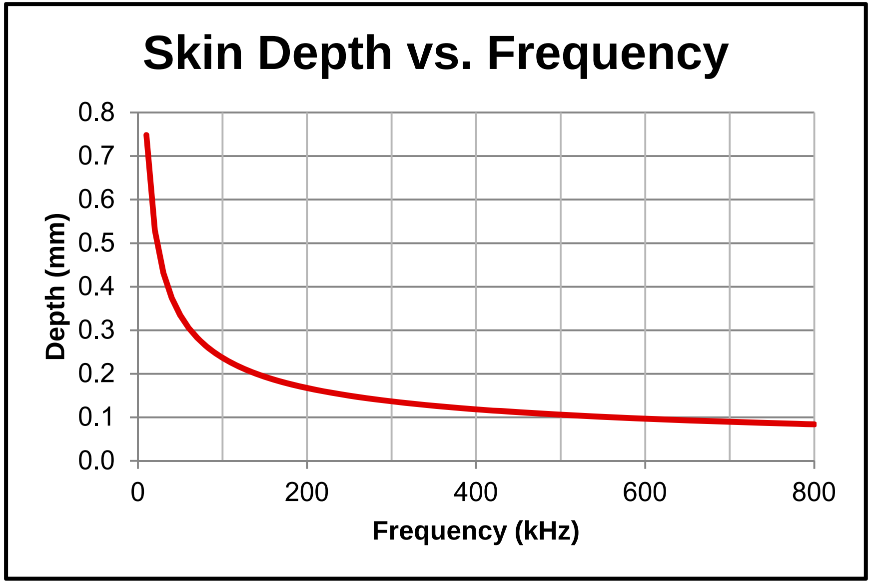
# Copper loss mechanisms

- Caused by winding resistance
- Flyback cares about DCR and ACR
  - ACR/DCR ratio
    - Can range from 1-2 to > 100!
  - ACR/DCR ratio depends on:
    - Frequency
    - Wire thickness
    - Layer construction
- AC Cu loss causes:
  - Eddy current effects
    - Skin depth effect
    - Proximity effect
    - Air-gap fringing effect



# Skin effect

- DC current ⇒ uniform current density over wire cross-section.
- High frequency AC current
  - o Eddy current effects
  - o Non-uniform current density
- Skin depth – also called penetration depth
  - o Depth from surface where current density drops by $^1/_e$, i.e. to ~37% of the surface value
  - o Also depth to which the field penetrates the wire
- Depends on:
  - o Wire conductivity $\rho$
  - o Permeability $\mu_0$ , $\mu_r$
  - o Frequency of interest $f$
- Normally designated $\delta$, $D_{PEN}$ or $D_{SKIN}$:



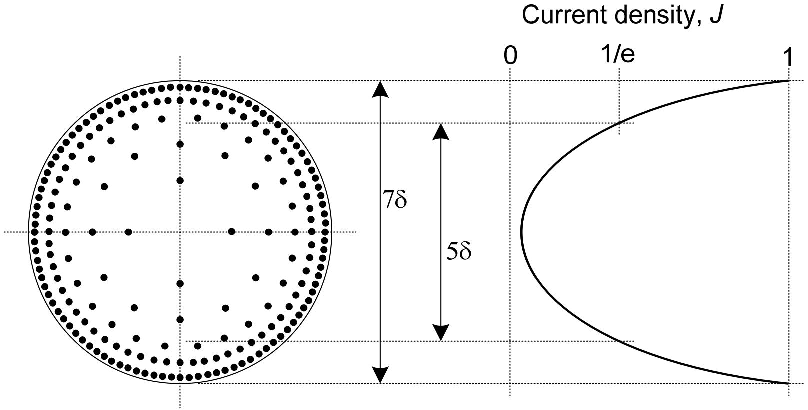
$$\delta = \sqrt{\frac{\rho}{(\pi \cdot \mu_0 \cdot \mu_r \cdot f)}}$$

# Skin depth example

- For copper at 100°C (f in kHz):

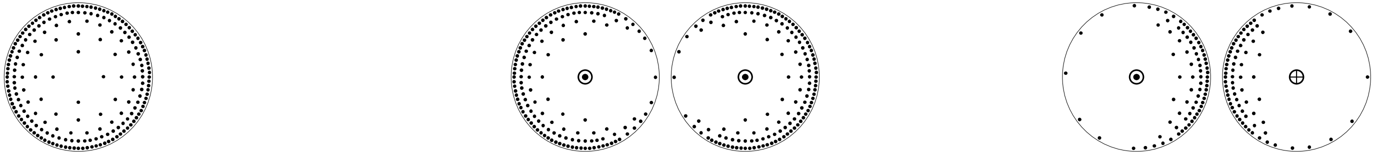
$$\delta = \sqrt{\frac{2.3 \cdot 10^{-8}}{(\pi \cdot 4\pi \cdot 10^{-7} \cdot 1 \cdot 1k)}} \cdot \frac{1}{\sqrt{f}} = \frac{2.4\ mm}{\sqrt{f}}$$

- For copper at 60 kHz: $\delta = \frac{2.4\ mm}{\sqrt{60}} = 0.31\ mm$
- Example, large wire diameter d >> δ
  - Assume d = 7δ
  - Most current flows in outer skin depth “annulus”
  - Rac/Rdc ~ 200% ($7^2$ / ($7^2$ – $5^2$))
  - If inner 5δ section is removed
    - Rac ~ same value, but Rdc increase ~2x
    - Rac/Rdc ⟶ ~1x

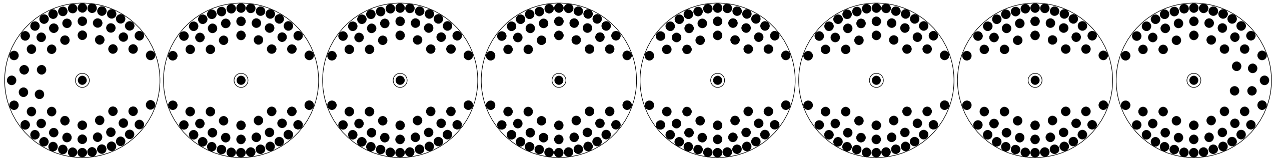


# Proximity effect in a single layer

- Proximity effect – eddy currents induced by adjacent wires. *Much worse than skin effect*
- *Example – assume wire diameter d >>* $\delta$ *(for ease of illustration)*
- Two wires placed beside each other (< 3-wire diameters apart)
  - Magnetic field between wires causes current to concentrate:
    - At *further* edges with current in the same direction
    - At *nearer* edges with current in opposite directions.

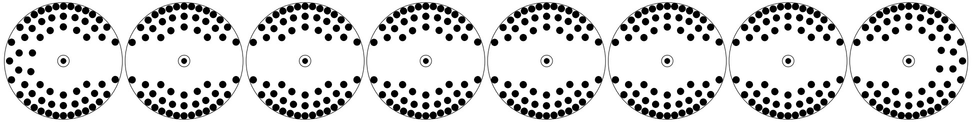


- *Even for single layer winding, proximity effect occurs*
- Increase in AC resistance more significant than skin effect alone

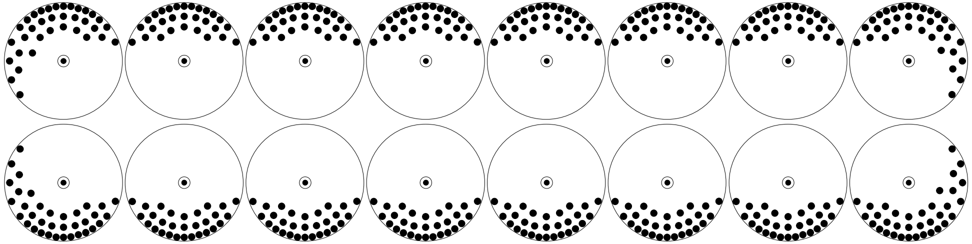


# Proximity effect in two layers of wires

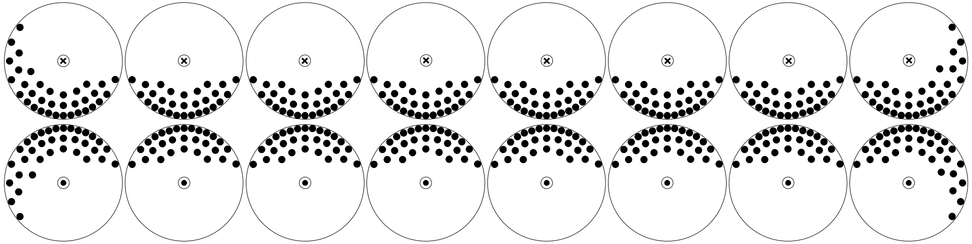
- Single-layer ⇒ current in the same direction



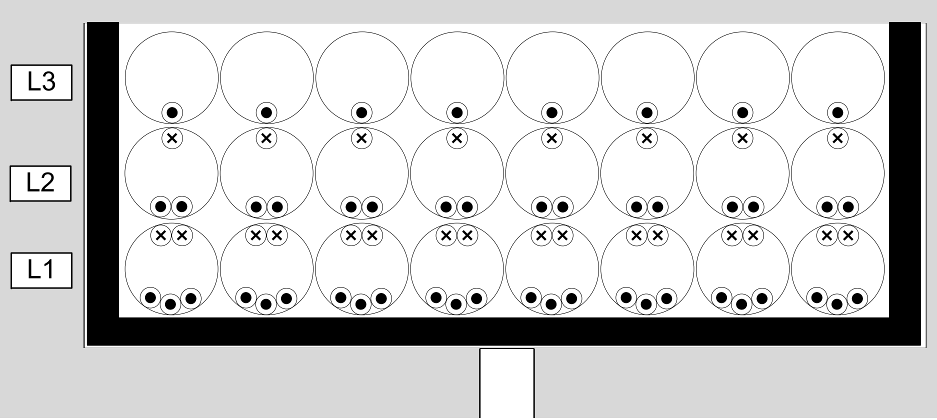
- Add second layer, current in same direction (conducting primary or secondary of flyback)



- Primary and secondary winding adjacent layers
  - Current in opposite directions (for forward-mode transformer, or during Flyback transition)



# Proximity effect with multiple layers



- Example: Flyback 3-layer primary, d >> δ
  - All layers turns = $N_P/3$
  - All layers in series, same net current $I$
  - Total MMF = $[3 * (N_P/3) * I] = N_P * I$
- Large d >> δ ⇒ field cannot penetrate wires
  - Layer 1: all current $3I$ along bottom face
  - Layer 1: cancelling current $2I$ along top face
  - Layer 2: $2I$ on bottom face, cancelling $I$ on top
  - Layer 3: only net current $I$ flows on bottom face
- *Negative cancelling/balancing current flows on opposite faces!*
- Expected loss ∝ $(3 * I^2)$, but actually ∝ $[I^2] + [I^2 + (2I)^2] + [(2I)^2 + (3I)^2] = 19 * I^2$
- Add further layers, losses increase exponentially!
  - 4 layers, total loss -> $(44 * I^2)$ vs $(4 * I^2)$
  - 5 layers, total loss -> $(85 * I^2)$ vs $(5 * I^2)$

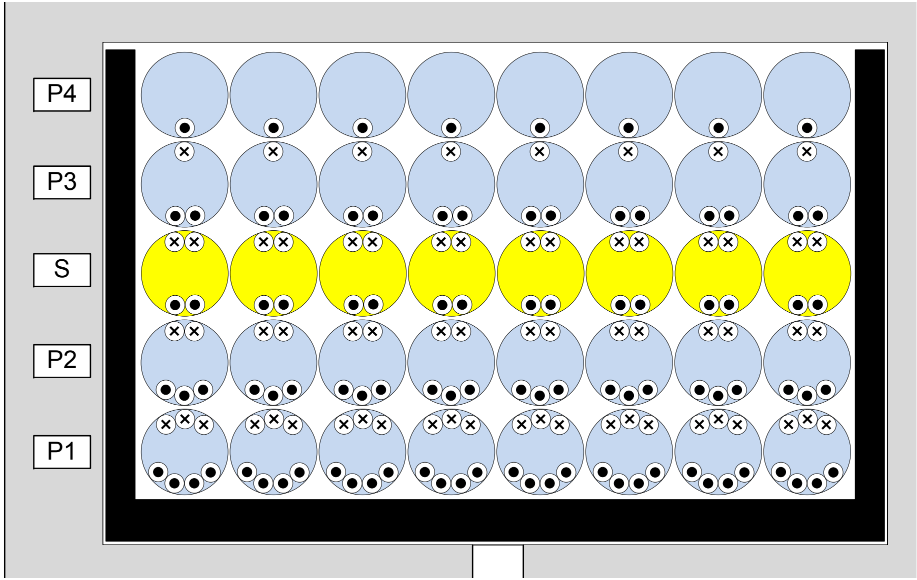
# Proximity effect on passive layers

- *Passive Layers* – conductors that carry no net useful current – either all of the time, or some of the time
- Examples:
  - Screening shields
  - Flyback non-conducting primary or secondary
  - Centre-tapped windings (push-pull or half-bridge)

o Passive layer between conducting active layers

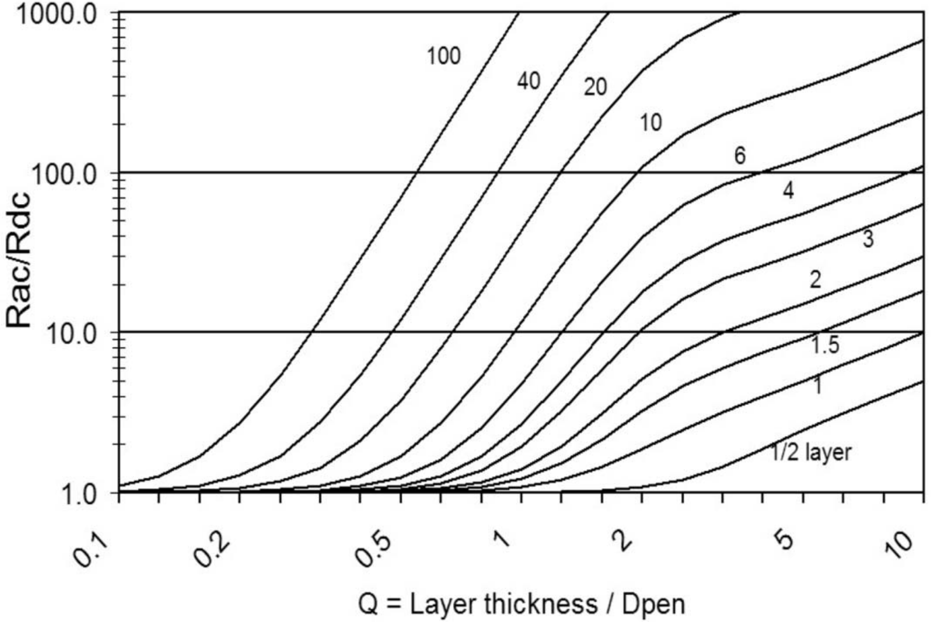
  - Proximity effect eddy current losses

- Example:
  - Interleaved Pri-Sec-Pri
- Illustration:
  - 2-layer primary, 1-layer secondary, 2-layer primary
  - Proximity-induced cancelling currents +2$I$ and -2$I$ on opposite sides of secondary
    - 8x loss in *"non-conducting"* secondary versus primary outer layer 4!



# Proximity effect factor $k_p$

- Dowell equations – proximity effect factor $k_p$
- $k_P = R_{AC}/R_{DC}$
- $Q = \frac{Layer\ thickness}{Penetration\ depth}$
- Layer thickness $h \neq$ wire diameter $d$
  - *Convert round wire to equivalent square cross-section*
    - $h^2 = \pi d^2/4$
  - *Round wire diameter*
    - $h = d \cdot \sqrt{\pi/4} \simeq d * 0.886$
- Large diameter
  - Significant $R_{AC}$ / $R_{DC}$
- Large layer count
  - Require diameter << $D_{PEN}$
- Non-sinusoidal waveforms
  - High frequency harmonics

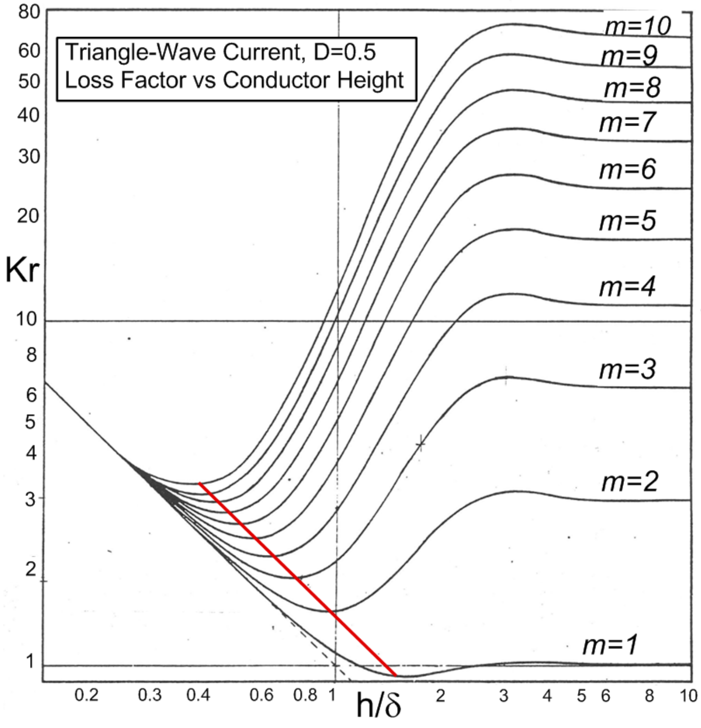


# Flyback – DCR vs ACR compromise

- Bruce Carsten used Dowell to generate $K_R$ resistance factor for triangular currents at 50% duty [3]
- $K_R$ is “normalized effective resistance factor”

  $$K_\mathrm{R} = \frac{R_\mathrm{WE}}{R_\mathrm{W0}}$$

  $R_{WE}$ = effective resistance
  $R_{W0}$ = DCR, with h/δ = 1 at fundamental frequency
- Plot $K_R$ vs. $h/\delta$ for various layer counts $m$
- Optimum $h$ depends on number of layers $m$
  - More layers ⇒ smaller *h*
  - 1-layer m =1 ⇒ h/δ ≅ 1.5 (⇒ d/δ ≅ 1.7)
  - 10-layer m =10 ⇒ h/δ ≅ 0.4 (⇒ d/δ ≅ 0.45)
  - Ideal diameter 45-170% of fundamental frequency δ
- Lower $K_R$ at lower layer count ⇒ avoid many layers
- Ger Hurley analysis [5] also very useful and applicable



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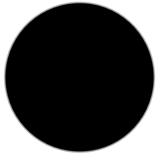
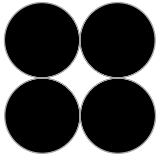
# DCR versus ACR – Litz and stranded wire

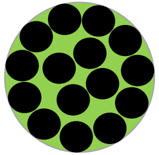
- Solid core wire – good DCR, bad ACR
  - Minimise AC loss ⇒ thin wire, optimum $h/\delta$
  - Minimise DC loss ⇒ max cross-section
- Multi-strands ⇒ reduce AC loss (thin wire) & maintain low DCR (multiple strands)
- No. strands > 4 in parallel ⇒ use twisted wire bundles
  - Beware twisted bundles can increase loss if not carefully manufactured
- True Litz is woven together – *all strands equally occupy all positions in the cross-section => equal current-share*
- Litz advantages
  - Very good at high frequency, if wire size/count properly chosen – N strands equiv. to $\sqrt{N}$ layers – need to choose optimum wire diameter
- Litz disadvantages
  - High cost
  - Difficult to handle, solder, strands can break
  - Poor window utilization – high % of insulation and spaces
  - Can make loss worse if not correctly chosen



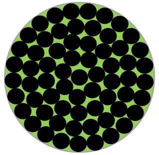
Single-strand diameter *d*



4-strand diameter *d/2*
Same DCR



15-strand bundle, diameter *d/5*
167% DCR



65-strand bundle, diameter *d/10*
154% DCR

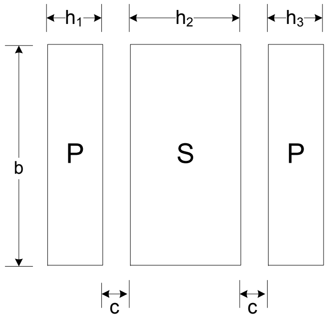
# Leakage inductance

- Caused by flux in spaces between windings
- Flux from one winding that does not couple to the other
- Results in energy storage in these air spaces that must be dissipated
- Empirical formula (ref Bruce Carsten [3])
  - o *Estimate leakage using physical geometry:*

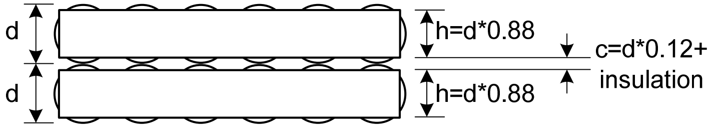
$$L_{leak} = \frac{\mu_0 \cdot N^2 \cdot MLT \cdot (\sum h + 3\sum c)}{3b} \cdot \frac{1}{m^2}$$

*m = number of winding "portions," i.e. amount of interleaving*

- Note wide bobbin width *b* => lower leakage
- Wider *b* facilitates smaller *Σh* & *Σc*



- *N = turns on winding to which leakage is referred*
- *MLT = mean length per turn*
- *b = winding "breadth" (or width)*
- *m = number of winding "portions" (degree of interleaving)*
- *Calculate h for every winding layer, and c between every layer*
- *h is effective rectangular layer thickness, h = round diam * 0.886*
- *c includes insulation (enamel, TEX), tape, shield layers, etc.*
  - – *c also includes the extra separation when round wires are converted to equivalent rectangular layers, i.e. c = diameter * 0.12*



# Interleaving to reduce leakage

- Interleaving – reduces field intensity H at pri-sec interface, in proportion to number of winding “portions,” *m*
- Energy storage in leakage proportional to $H^2$
  ⇒ each interleaving portion can reduce leakage energy
- Leakage drops in proportion to $H^2$, i.e., also $m^2$
  - 1 step of interleaving, m = 2
    - $L_{LEAK}/4$
  - 2 steps of interleaving, m = 3
    - $L_{LEAK}/9$
- However, extra gaps c between windings limit leakage reduction
  - In practice m=2 ⇒ ~$L_{LEAK}/2$
  - *Beware – increased inter-winding capacitance!*

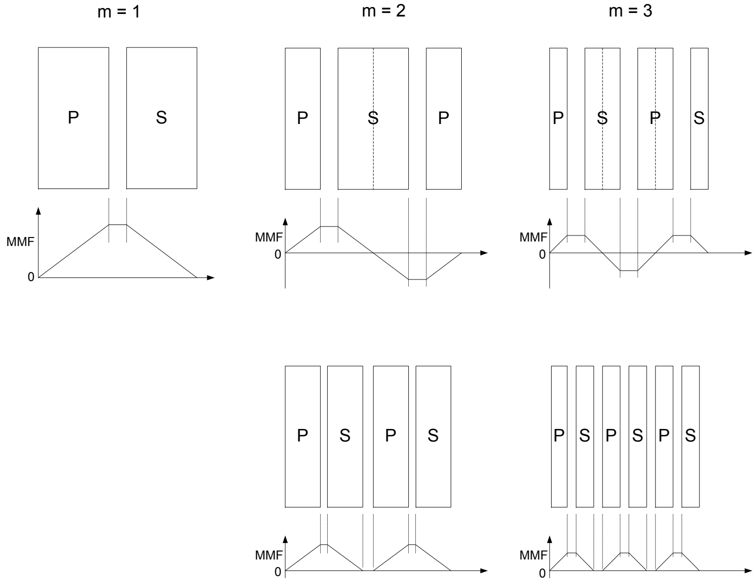
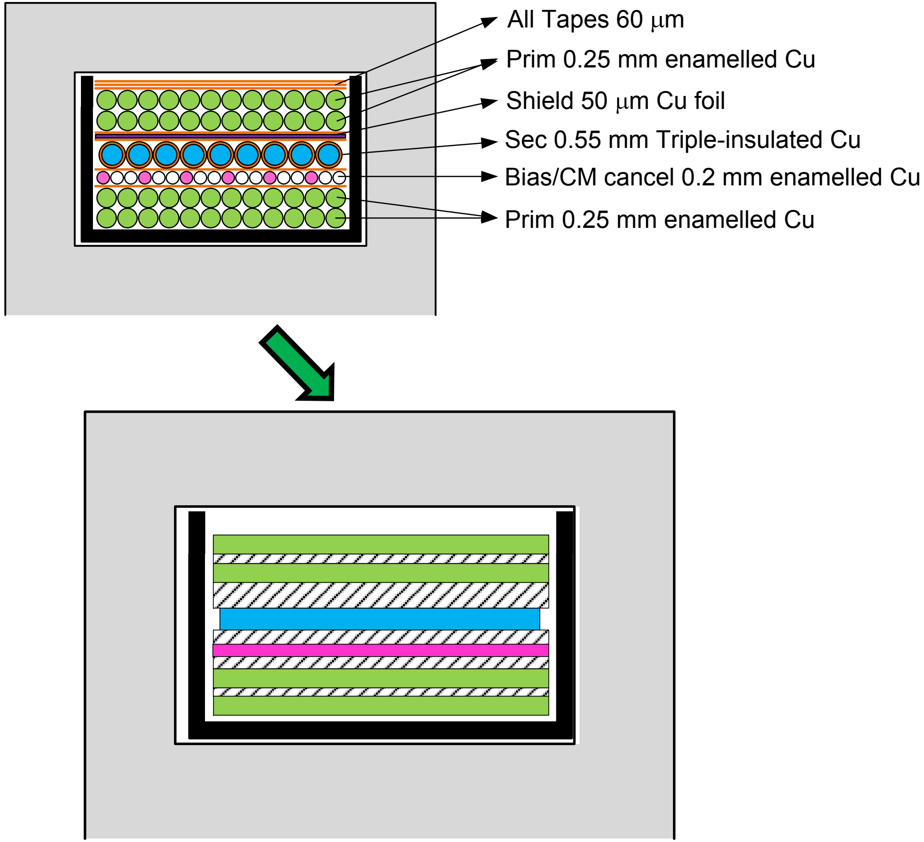


*Illustration of interleaving benefit in forward-mode transformer – similar benefit with Flyback*

# Leakage inductance calculation example



- Round wire ⟶ equivalent rectangular layer height $h_i$
- Spaces, gaps – $c_i$ include all wire enamel, insulation, tapes, shields, etc.
  - $\Sigma h = 1.54$ mm, $\Sigma c = 0.78$ mm
- RM10/I core:
  - MLT = 52 mm, Np = 34, b = 9 mm (assume 90% width utilization)

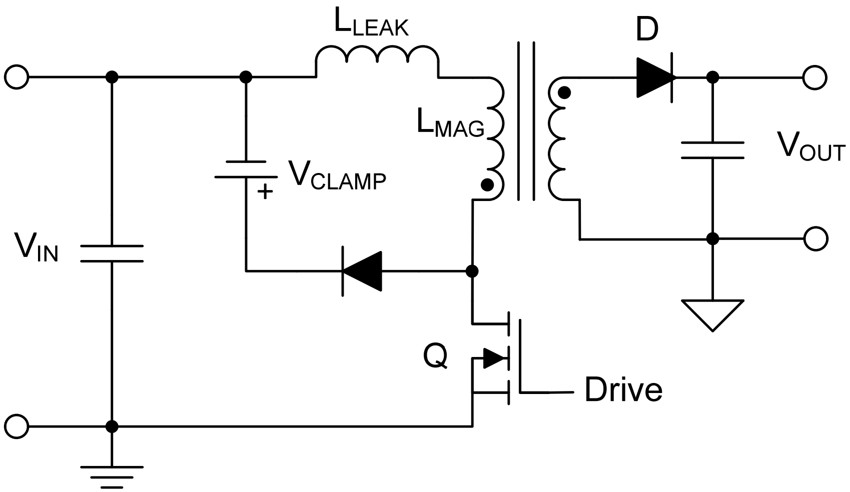
$$L_{leak} = \frac{\mu_0 \cdot N^2 \cdot MLT \cdot (\sum h + 3 \sum c)}{3b} \cdot \frac{1}{m^2}$$

$$= \frac{\mu_0 \cdot 34^2 \cdot 52 \cdot (1.54m + 3 \cdot 0.78m)}{3 \cdot 9} \cdot \frac{1}{2^2} = \mathbf{2.71 \mu H}$$

- Measured leakage inductance ***~3.2 µH***
  - Close to calculated value
  - Larger due to winding practicalities, extra thickness of “return” wires, tape creasing, etc.

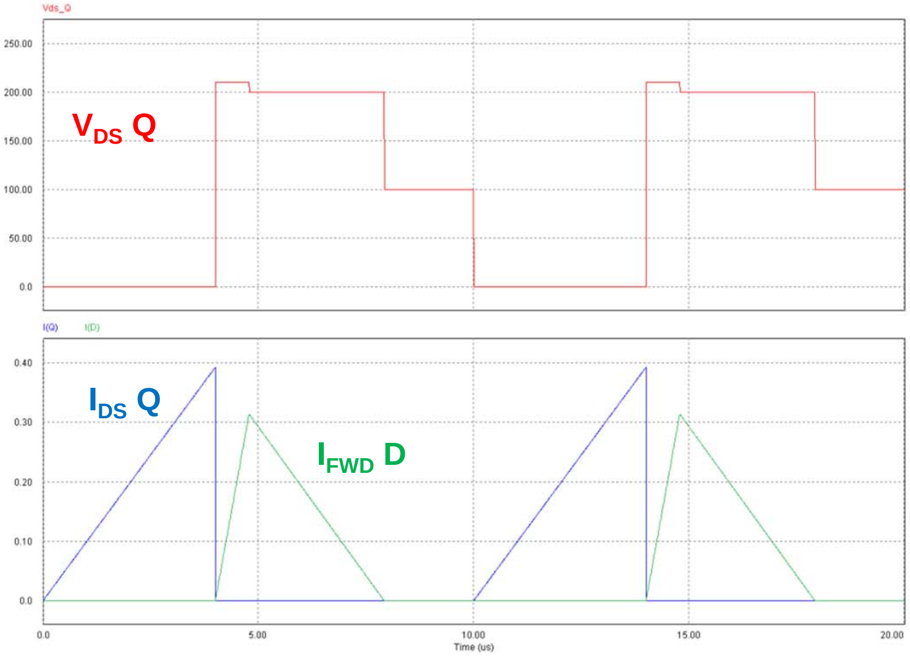
# Impact of snubber clamp level

- Switch Q turn-off
  - Energy ⟶ clamp until $L_{LEAK}$ current ⟶ zero
  - Time depends on ($V_{CLAMP}$ – $V_{REFLECTED}$) difference & $L_{LEAK}$ value
  - Some magnetising energy ⟶ clamp
  - Smaller difference ($V_{CLAMP}$ – $V_{REFLECTED}$)
    - More magnetising energy absorbed by clamp
- Lower clamp level
  - Lower voltage FET, lower $R_{DS(on)}$
  - But extra clamp loss
    - *Clamp loss can out-weigh FET loss saving*
- Higher clamp level
  - Higher voltage FET => worse $R_{DS(on)}$

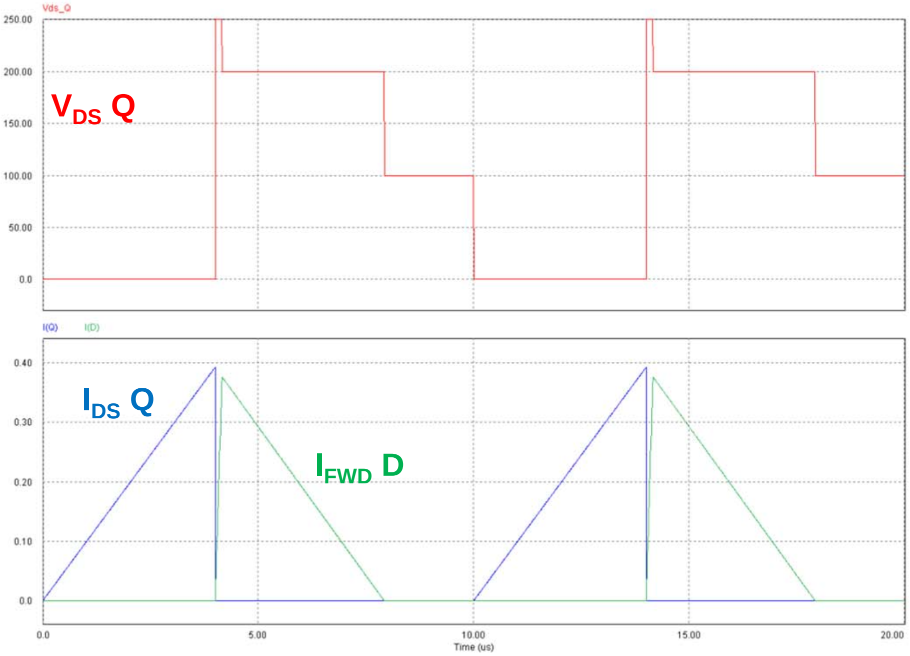


# Comparison of clamp level effect

$V_{CLAMP}/V_O*1.1\ (N_P/N_S=1)$



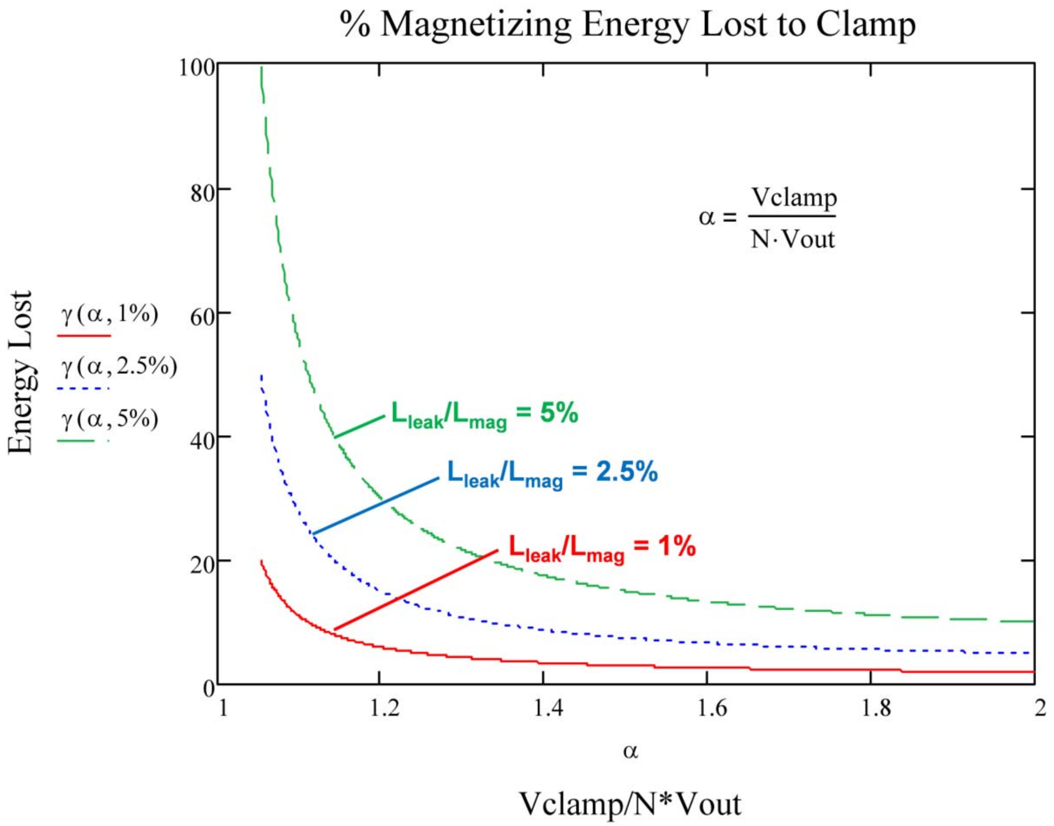
$V_{CLAMP}/V_O*1.5\ (N_P/N_S=1)$



# Effect of clamp voltage on energy loss

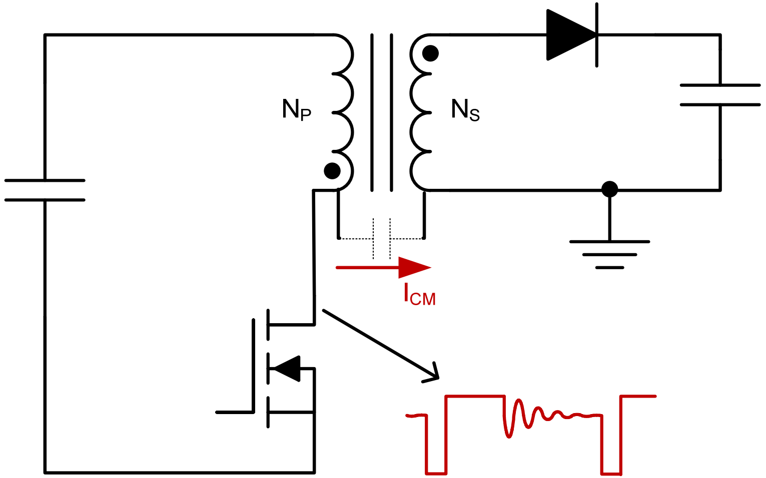
- Lower clamp voltage attracts more magnetizing energy to the clamp!

- Can defeat, or even out-weigh, benefit of lower $R_{DS(on)}$



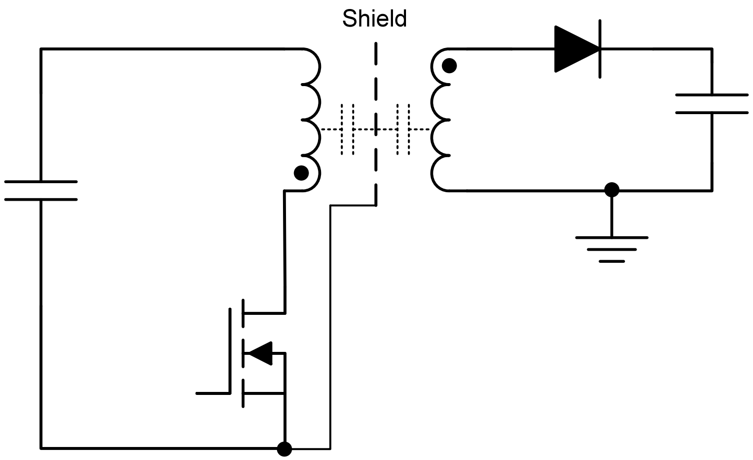
# EMI problems due to capacitance

- Switching waveform at primary switch node
- Couples common-mode current to secondary earth through inter-winding capacitance
- Generally, lower leakage construction ⇒ windings closer together ⇒ higher capacitance ⇒ worse EMI issues



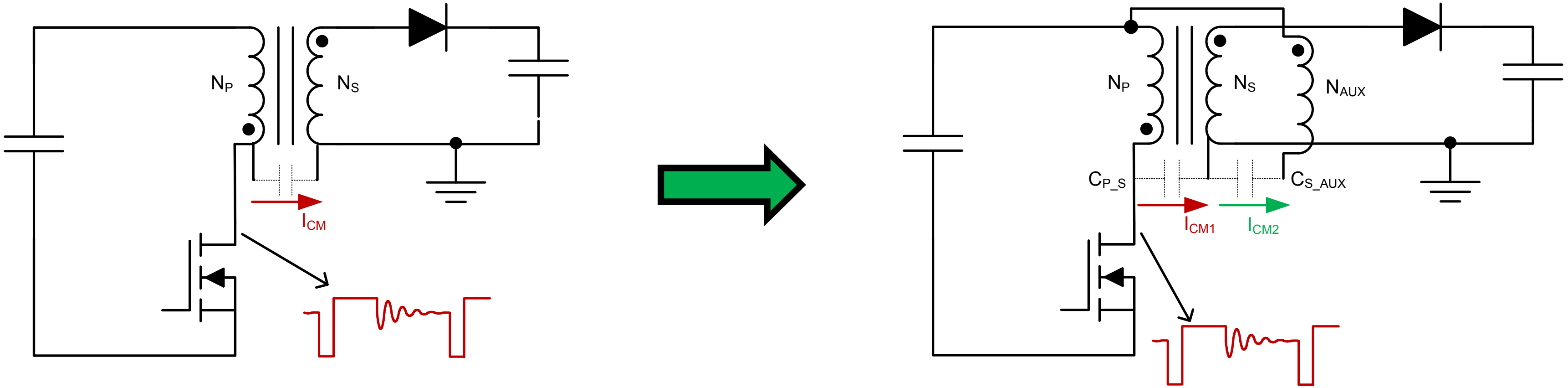
# Shield layers

- Keep CM currents local to primary
- Tied to primary return ⇒ reduced CM current flow from shield to secondary
- Can also be tied to DC side of primary winding (positive bulk cap terminal)
- Shield – as thin as possible, minimise induced eddy current loss (passive layer)
- Connection typically made at the centre of the shield
  - *Sometimes beneficial to connect to one end of the shield*



# CM cancellation windings

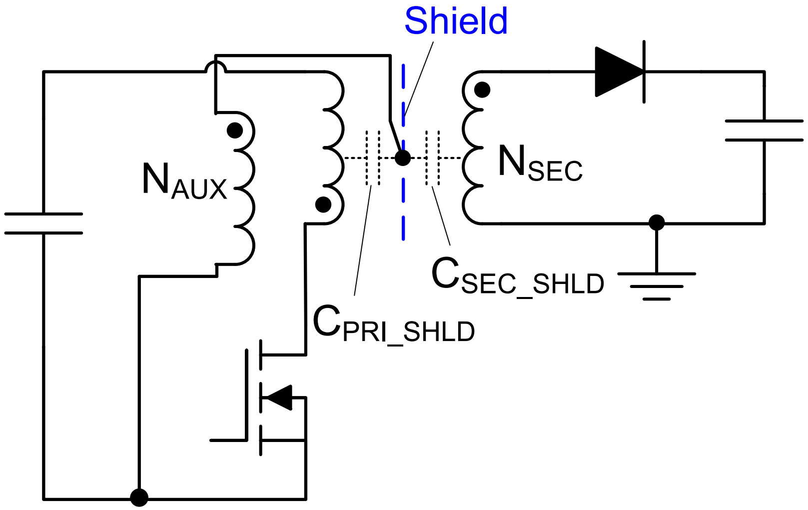
- Cancellation winding ($N_{AUX}$) can be added to null the CM current



- Adjust $C_{S\_AUX}$ and $N_{AUX}$ ⇒ current $I_{CM2}$ tuned to cancel $I_{CM1}$
- Practical challenges to control $C_{S\_AUX}$ to maintain CM nulling
- Depends on winding width, tape and winding layer thicknesses, etc.

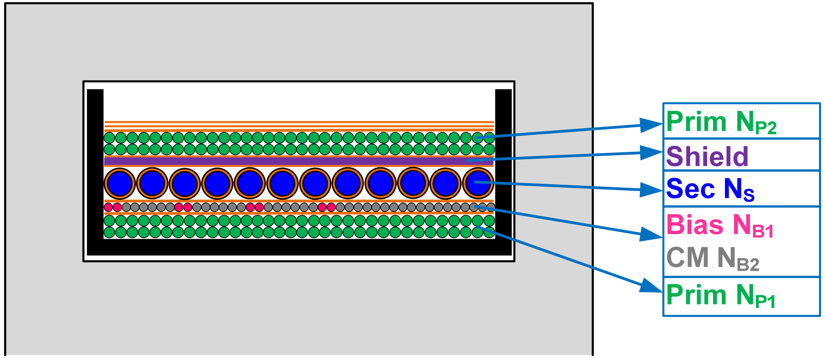
# CM balance

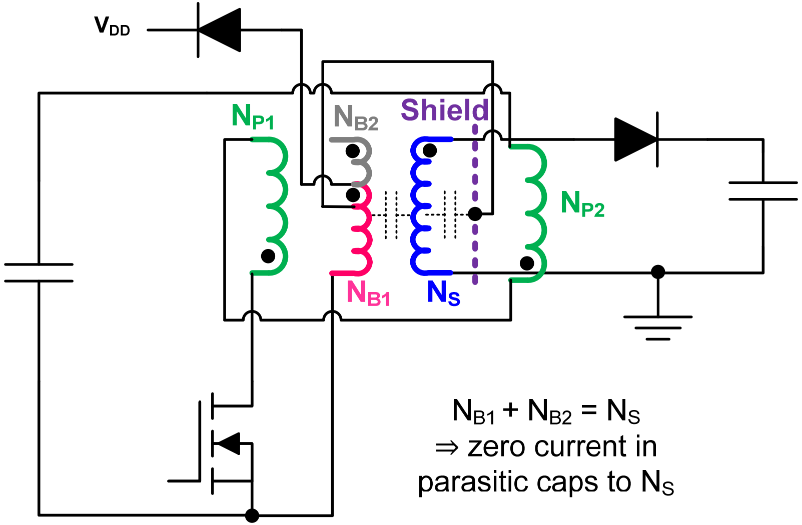
- Connect shield in series with $N_{AUX}$, elevate voltage level to cancel CM current
- Choose $N_{AUX}$ = ½ $N_{SEC}$ ⇒ balance voltage across parasitic cap $C_{SEC\_SHLD}$
  - Average voltage across shield ≅ average voltage across secondary
  - Same voltage at both sides of cap ⇒ zero CM current flow
- Better repeatability – applies same voltage both sides of parasitic cap $C_{SEC\_SHLD}$
- Does not depend on controlling value of parasitic capacitance $C_{SEC\_SHLD}$



# Balanced CM shielding

- Design example:
  - Vo = 20 V, $N_S$ = 6T
  - $N_{B1}$ = 4T ⇒ Vdd ~13 V
  - $N_{B2}$ = 2T
- Average voltage across $N_S$ ~10 V
- Average voltage across $N_{B1}$+$N_{B2}$ ~10 V
- $N_s$ & $N_{B1}$/$N_{B2}$ have same polarity
  - Zero CM current between bias and secondary winding
- $N_{b1}$ tap at 3T to connect to centre of shield
- Average voltage across shield ~10 V
  - Zero CM current between shield and secondary winding
- CM current into secondary winding ~0
- Caution – more capacitance from shields
  - Can increase switching loss, especially at higher frequencies

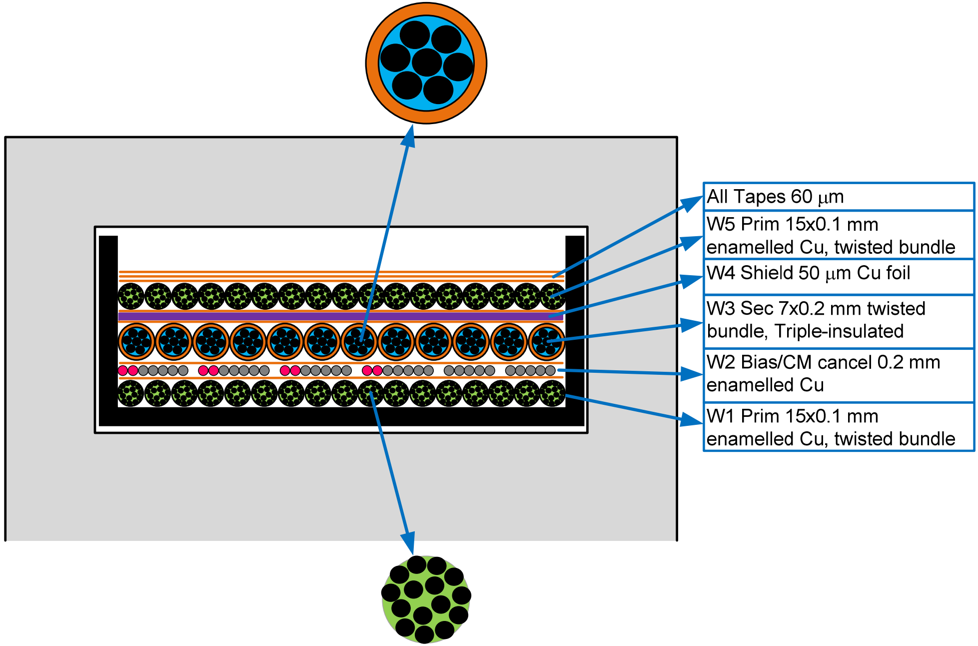




$N_{B1} + N_{B2} = N_S$
⇒ zero current in
parasitic caps to $N_S$

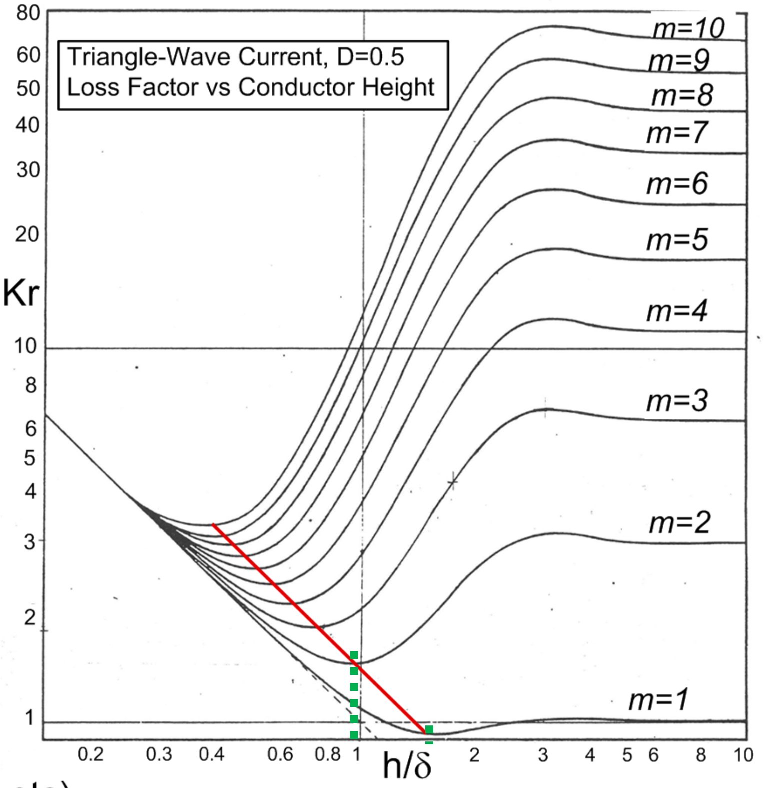
# Example transformer improvement

- Example: UCC28630-EVM572, 19.5 V @ 65 W, universal input AC mains [6]
- Version #1 standard EVM:
  - Pri1: 17T, twisted bundle, over 1L
  - Sec: 6T, triple-insulated (safety requirement), x 2 strands over 1L
  - Bias: 4T x 2 strands
    Cancellation: 6T x 5 strands
    Multi-filar over 1 L (full layer)
  - Pri2: 17T, twisted bundle, over 1L
- $L_{LEAK}$ ~4.5 uH (measured)
- Can this implementation be improved?
  - $h/\delta$ = 29% ⇒ very low
  - 15 x 0.1 mm ⇒ DCR quite high
  - 7 x 0.2 mm TEX ⇒ very tight fit in bobbin for 1 layer



# Apply Bruce Carsten ACR/DCR trade-off

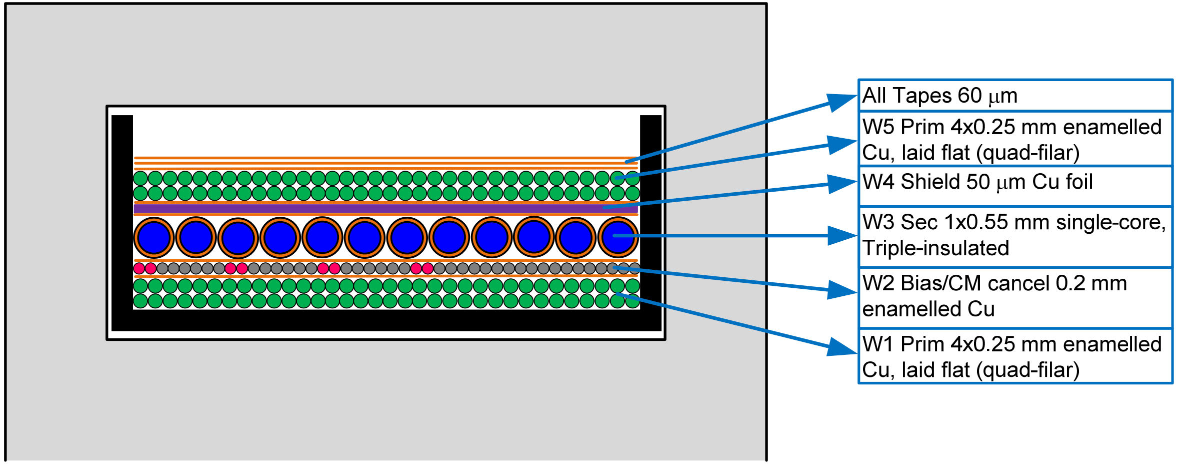
- Version #2 assumptions:
  - $N_P = 34$, $N_S = 6$, $N_B = 4$
  - Target primary over 2L each section
  - Target secondary over 1L
- At 60 kHz $\delta = 0.31$ mm
- Primary 2L ⇒ optimum $h/\delta = 0.9$
  - h = 0.28 mm ⇒ d = 0.32 mm
  - Too big to fit in 10 mm RM10 bobbin width
  - Actually used d = 0.25 mm x 4 strands – good fit
- Secondary 1L ⇒ optimum $h/\delta = 1.6$
  - h = 0.5 mm => d = 0.56 mm
  - To fit 10 mm bobbin width, use 0.55 mm TEX x 2 strands
  - Good fit outer diameter = 0.75 mm
  - (Need triple-insulated secondary for safety requirements)



*Reproduced from [3] with permission*

# Transformer 2 – interleaved, multi-strand

- Version #2 final implementation:
  - Optimized layer thickness
  - Primary 4 x 0.25 mm
  - Sec 2 x TEX 0.55 mm
  - Bias/cancellation 8 x 0.2 mm
- Cost difference?
  - Similar total cost to #1
  - Lower cost secondary
  - Slightly higher cost primary
- Performance difference?
  - $L_{LEAK}$ ~3.2 uH (measured) ~72% of version #1
  - Similar EMI (pass with good margin)
  - Efficiency ~ 1.3% better @ 65 W load (saved 1.1 W loss)



All Tapes 60 µm

W5 Prim 4x0.25 mm enamelled Cu, laid flat (quad-filar)

W4 Shield 50 µm Cu foil

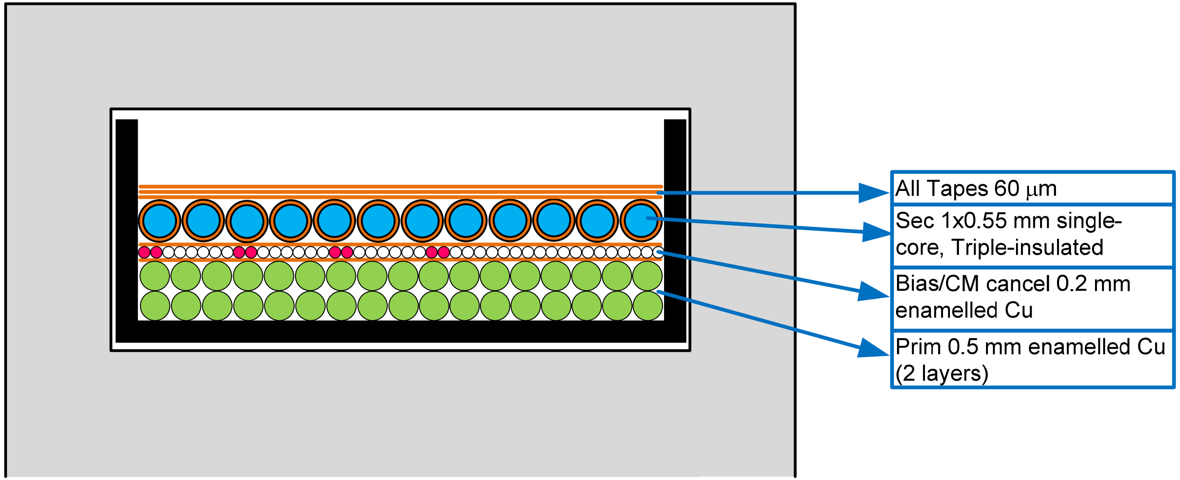
W3 Sec 1x0.55 mm single-core, Triple-insulated

W2 Bias/CM cancel 0.2 mm enamelled Cu

W1 Prim 4x0.25 mm enamelled Cu, laid flat (quad-filar)

# Transformer 5A – non-interleaved, single-strand

- Version 5A – low cost version
  - No shield, no interleaving, 1-strand pri
  - Pri, 0.5 mm, wound over 2L
  - Sec same as 2
  - Bias – no shielding/CM
- Much lower cost
- Performance difference?
  - $L_{LEAK}$ ~6.4 uH (measured) ~2x version TR#2
  - Efficiency ~ 2.1% worse @ 65 W load vs TR#2 (extra 1.75 W loss)



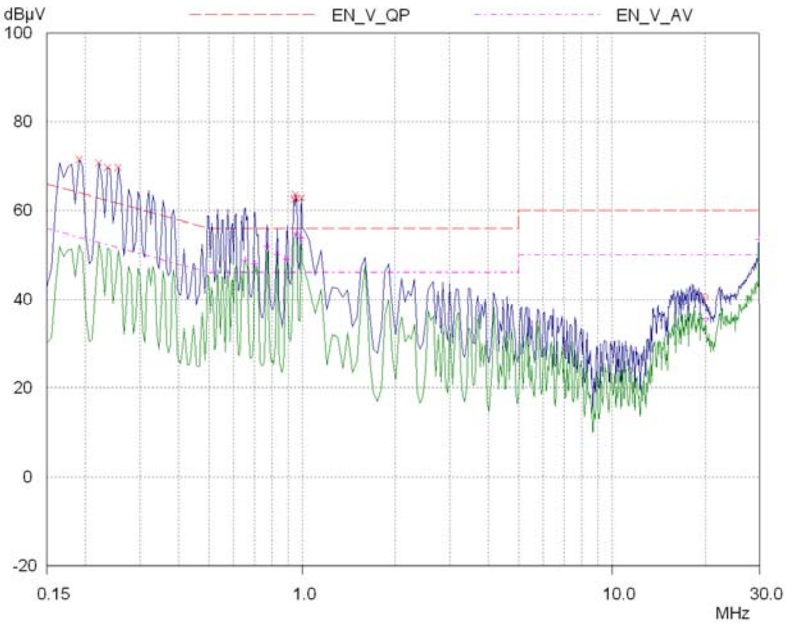
# Leakage inductance and efficiency comparison

| Transformer Version | Winding Summary | Relative Cost | $L_{leak}$ | Full-load Eff | Full-load Pdiss | Power saved or lost |
|---|---|---|---|---|---|---|
| 1 | Standard EVM572;<br>twisted multi-strand windings; thin wire diameters; interleaved, shield layer, multi-filar bias | $$$ | 4.51 uH | 87.71% | 9.11 W | - |
| 2 | Flat multi-strand windings; medium wire diameters; interleaved, shield layer, multi-filar bias | $$$ | 3.24 uH | 89.03% | 8.01 W | **1.10 W** |
| 5A | Single-strand primary; large wire diameter; non-interleaved; no shield | $ | 6.41 uH | 86.94% | 9.76 W | **-0.65 W** |

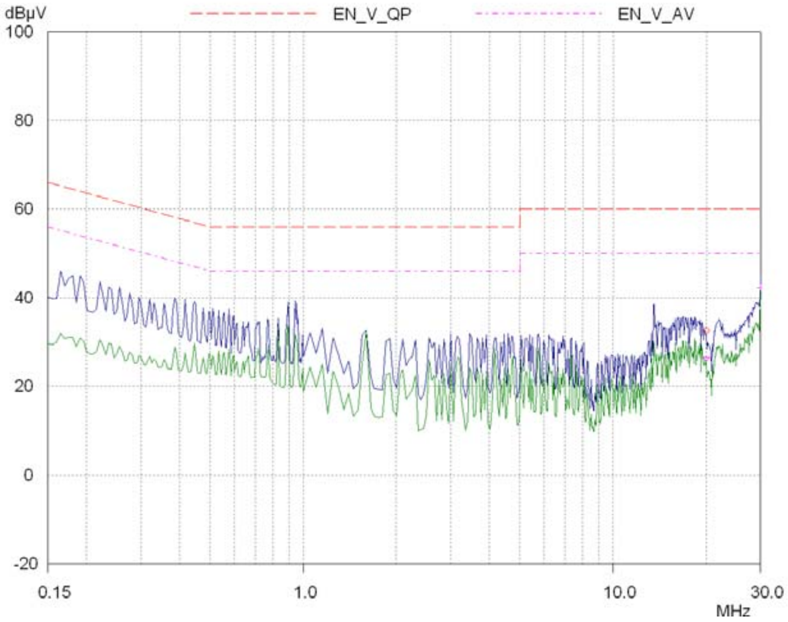
- All measurements taken at 115 V ac, full load (65 W) – worst case line for efficiency *[after warm-up/settling time (>1 hour)]*
- More data and more transformer variations covered in full paper

# Conducted EMI performance comparison

EMI tested at 230 V ac, 65 W earthed load – worst case configuration



- No outer flux-band, no shield, no CM balance winding



- GND-ed outer flux-band, shield connected to CM balance winding

# Summary – flyback transformer best practices

- Core loss – cannot neglect DC bias and duty cycle effects
- Typically maximize $A_E$ and $B_{PK}$ => minimize turns – minimize Cu loss
    - o *Beware of core loss – usually OK at low frequency*
- Choose core and bobbin with wider winding width to height ratio
    - o *Minimize layers, lower leakage inductance, less proximity loss!*
- Interleave primary and secondary layers for lower leakage
- Avoid partial layers – always fill window width fully and neatly for all layers
- Choose wire diameter and number of strands carefully
    - o Target 1 skin depth for main frequency of interest, parallel multiple strands to reduce DCR
- Beware of setting snubber clamp level too low
- Consider EMI shield(s) and CM cancellation winding(s) – save losses and cost in external EMI filter

# References and Further Reading

1. *“A New Core Loss Model for Rectangular AC Voltages”, Mingkai Mu, Fred C. Lee, CPES, Virginia Tech, ECCE 2014*
2. *“High Frequency Magnetic Core Loss Study”, PhD Dissertation, Mingkai Mu, Virginia Tech, 2013*
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4. *“Transformers and Inductors: Theory, Design & Applications”, PEI Training Course, Dr. W. G. Hurley, NUI Galway, 1996*
5. *“Optimizing the AC Resistance of Multilayer Transformer Windings with Arbitrary Current Waveforms”, Hurley, Gath, Breslin, IEEE Trans. Power Elect., 2000*
6. *UCC28630 EVM –* http://www.ti.com/tool/UCC28630EVM-572
7. *“The Magnetics Design Handbook For Switching Power Supplies”, Lloyd H. Dixon, slup132 (slup123/4/5/6/7/8)*
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8. *“Under the Hood of Flyback SMPS Design”, Jean Picard, TI Power Supply Design Seminar 2010 SEM1900, slup261.*
   http://www.ti.com/lit/slup261
9. *“Fundamentals of Power Electronics”, Robert W. Erickson, Dragan Maksimovic*
   **Fundamentals of Power Electronics [FUNDAMENTALS OF POWER ELECTRON] [Hardcover]**

Further references listed in full paper

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