Under the hood of a noninverting buck-boost converter

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Innovative topology and control with optimized PCB layout enables highly efficient, synchronous buck-boost converter designs

When it comes to designing buck-boost converters, there is a huge gap between the simple inverting buck-boost converter in textbooks, which actually produces a negative output voltage, and real-world buck-boost applications that require a positive output. This paper fills a gap in buck-boost literature by presenting various topologies used in noninverting buck-boost designs.

Practical noninverting buck-boost solutions, for example those needed in automotive battery stabilization, industrial computers, USB power delivery, and variable supplies for amplifiers, often consist of a two-stage approach, a boost followed by a buck, or a two-winding approach such as the single-ended primary-inductor converter (SEPIC), Zeta or flyback. Single-stage, single-inductor buck-boost converters offer smaller solution size, higher power and greater efficiency. This paper compares different buck-boost topologies, with a focus on a four-switch, noninverting buck-boost converter design. A practical design example illustrates a four-switch buck-boost application design including the printed circuit board (PCB) layout and the performance achievable with this topology.

Introduction

Converting a positive input voltage into a regulated output voltage is considerably more challenging when the input voltage varies from a level below to a level above the desired output voltage. The converter must be capable of functioning as a boost converter at low input voltages and as a buck (step-down) converter at high input voltages. Topologies that produce a negative output from a positive input such as the Ćuk and common buck-boost support a wide input voltage range, but do not deliver the positive regulated output required in most applications [1].

It is not difficult to find applications requiring a noninverting DC/DC converter that steps the input voltage up or down. Equipment that uses a battery for the main power or backup power source must maintain regulated internal rails as the battery voltage drops during discharge or dips with heavy loads, such as the cold-cranking condition in an automobile. Conversely, some systems such as USB Type-C™ ports have a variable output voltage that can be higher or lower than the input voltage. USB Type-C has port voltages selectable from 5 V to 20 V.

This paper presents several DC/DC converter topologies that satisfy the noninverting buck-boost requirement of a regulated positive output from a higher or lower positive voltage input. Currently, a number of converter topologies address

this challenge. However, these topologies vary widely in their solution size, complexity, maximum power capability and efficiency. We compare topology complexity and efficiency, along with practical output-power capability.

The remainder of this paper focuses on a four-switch buck-boost topology that provides the highest power capability and efficiency. The power stage component choices and control loop compensation must serve both buck and boost operation with a single set of values. A practical design example illustrates the flow of design decisions leading to a high-performance converter solution. The design example includes PCB layout considerations for the four-switch buck-boost that are critical to achieving the desired performance.

Topology comparison

Commonly used solutions for the noninverting buck-boost fall into one of three groups based on the number of magnetic windings and feedback control loops required:

1. Cascaded boost plus buck using two inductors and two controllers.
2. SEPIC, Zeta or flyback with one controller and two inductors or coupled windings.
3. Single-inductor buck-boost using one inductor and one control loop.

We will discuss and compare DC/DC topologies from each of these groups.

Cascaded boost plus buck

When new system requirements extend the input operating range to a much lower operating level than the typical input voltage, designers often add a boost stage in front of a buck stage. **Figure 1** shows this cascaded two-stage configuration, a popular approach when the boost is seldom required and activates only during dips in the input-supply voltage. One example is an automotive infotainment system that must maintain constant signal reception and sound levels during battery dips that occur when cranking the engine in cold conditions.

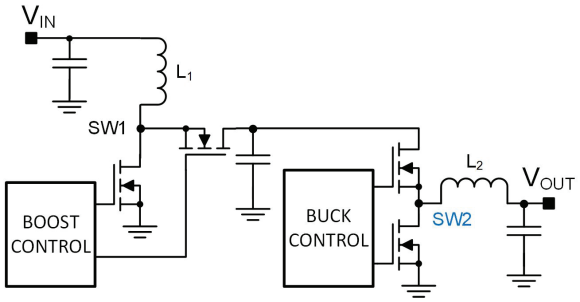

Figure 1. *Cascaded boost and buck converters.*

The cascaded two-stage solution offers a few advantages but a larger number of disadvantages. It provides flexibility to retrofit a boost stage into a buck design only when needed, and to select from a wide array of available buck and boost controller devices. It also has relatively low noise at the input and the output because the two inductors provide nonpulsating current flow at both terminals. Finally, a single boost stage can feed several buck stages operating in parallel to provide multiple regulated output voltages, all derived from the pre-regulated output of one boost converter.

The disadvantages of the solution are mostly self-evident. A cascaded two-stage solution costs more and has a larger total solution size than alternatives because it requires two separate converters, each with its own inductor and regulation control loop. The pre-boost also increases losses which reduces efficiency because the buck input current must be fed through the boost inductor L1 and the series boost rectifier. **Figure 1** includes a synchronously controlled field-effect transistor (FET) as the boost rectifier. A boost controller that does not support synchronous rectification necessitates the use of a diode in place of the FET, which significantly increases power loss. The cost of thermal

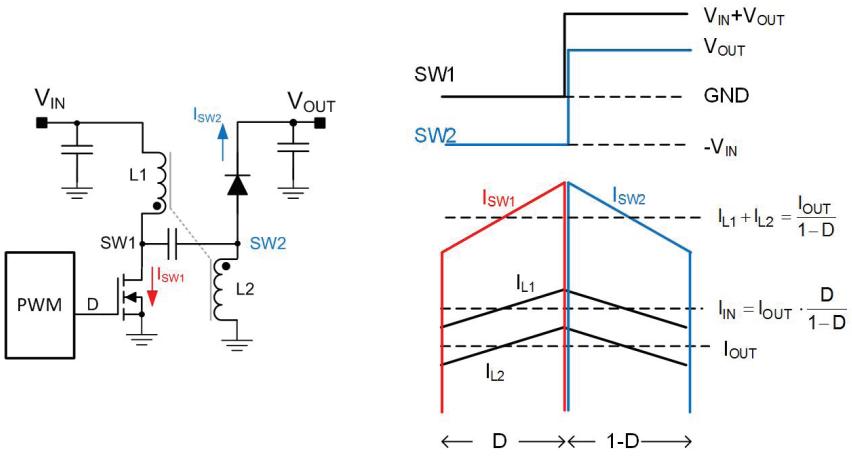

Figure 2. *SEPIC converter diagram and current and voltage waveforms.*

management under worst-case ambient and power-loss conditions typically determines the maximum power range of a topology. The losses and cost of the two series inductors and boost diode restrict the cascaded boost plus buck to moderate or low-power (<40-W) applications.

SEPIC, Zeta and flyback solutions

Systems requiring a noninverting buck-boost commonly use the SEPIC topology [2]. **Figure 2** shows a simplified SEPIC schematic, along with current and voltage waveforms.

The SEPIC requires only one low-side power switch and the two inductors, L1 and L2, can be separate or magnetically coupled on a single core. The pulse-width modulation (PWM) controller can be chosen from a large selection of single-ended switching-regulator controllers. Higher-power applications typically use uncoupled inductors because the required inductance is lower, and large coupled inductors are not commonly available. If using coupled inductors, the two windings should have an equal number of turns and loose coupling (enhanced leakage inductance) to reduce circulating currents [3] [4]. A high-quality coupling or flying capacitor between the two inductors conducts a circulating current that resets the inductor core and also eliminates voltage spikes when the FET switch turns off.

The input side of a SEPIC has relatively low noise because inductor L1 conducts continuously. The current flowing to the output is discontinuous since the output rectifier is off when SW1 switches low, forcing the SW2 voltage to negative V_{IN}. The output rectifier is typically a diode. Replacing the diode with a synchronous-rectifying FET requires a level-shifted gate drive to control the FET when the SW2 voltage swings to a negative V_{IN}. The voltage stress on the SEPIC switch and rectifier are V_{IN} + V_{OUT} and current stress is I_{OUT}/(1-D), similar to the boost converter.

A transfer function that changes abruptly at lower input voltages complicates a SEPIC regulator compensation design [5]. Consider the impact of a right-half-plane (RHP) zero. Some designers avoid the SEPIC topology completely because of difficulty in compensating the loop, while others have achieved success after thorough analysis and testing [6].

The Zeta topology is also known as the inverse SEPIC. As shown in **Figure 3**, interchanging the switch and inductor on the input and output side of the capacitor converts a SEPIC into a Zeta. The input current is discontinuous but the output current is continuous, which provides lower output noise for a given filter capacitor. The voltage stress on the switches (V_{IN} + V_{OUT}) and maximum current I_{OUT}/(1-D) are the same as they are for a SEPIC.

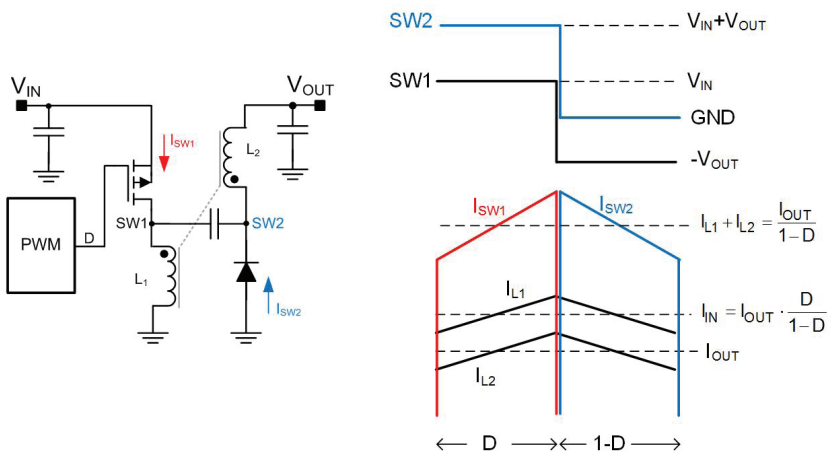

Figure 3. *Zeta converter diagram and current and voltage waveforms.*

Besides lower output ripple, another advantage that a Zeta has over a SEPIC is compatibility with synchronous rectification. The SW2 terminal does not swing below ground, which allows the PWM-controller integrated circuit (IC) to directly drive a synchronous-rectifier FET. SW1 swings to negative V_{OUT}, however, which complicates the drive of the high-side FET.

The Zeta topology commonly uses a P-channel field-effect transistor (PFET), shown in **Figure 3**, to avoid negative gate-drive voltages while supporting the negative voltage swing at terminal SW1 [7] [8]. Zeta compensation is complicated, with multiple real and complex poles and zeros, but it is easier to analyze than a SEPIC. You can avoid the RHP zero with properly selected loop parameters [9].

To satisfy buck-boost requirements, designers use flyback converters with either isolated or nonisolated outputs more often than SEPIC or Zeta.

The electrical behavior and compensation differ from a SEPIC, but it is possible to create a flyback topology with only a minor change to the SEPIC schematic. By simply removing the flying capacitor, tightly coupling the inductor windings, and providing a clamp for the leakage-inductance spike, you can convert a SEPIC into a flyback (**Figure 4**).

The primary advantages of the flyback versus the SEPIC are in the magnetics (transformer) and the loop compensation [10]. The flyback transformer windings can have an unequal turns ratio to step the voltage and current up or down between the input and output. Turns-ratio flexibility supports a wider range of input/output voltage ratios for practical duty-cycle values. The flyback transformer can be somewhat smaller than the SEPIC-coupled inductor or separate inductors because the windings do not conduct additional recirculating current flowing in

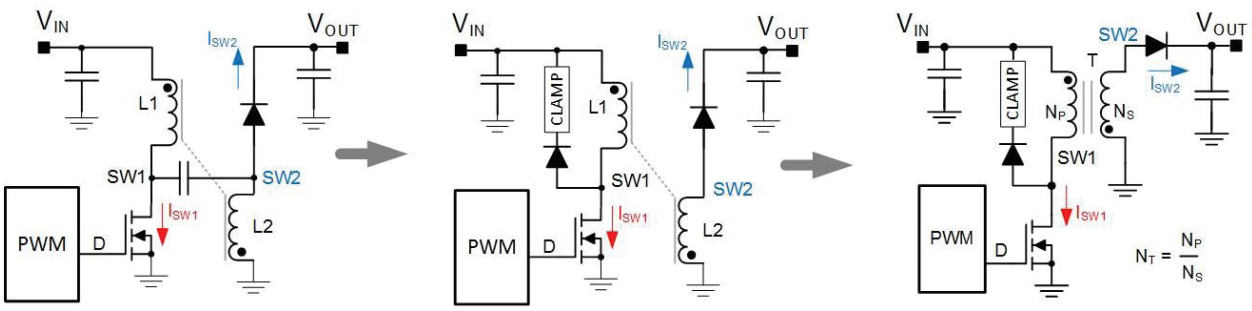

Figure 4. *Deriving a flyback converter from a SEPIC.*

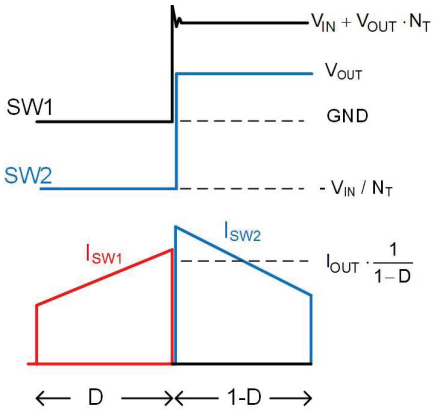

Figure 5. *Flyback current and voltage waveforms.*

the flying capacitor. The smaller magnetic element and elimination of the flying capacitor allow the flyback to serve higher-power applications with reasonable solution size and cost.

Compensating the feedback loop of a flyback is relatively simple; many DC/DC and alternating current (AC)/DC applications use the flyback. Synchronous rectification easily enhances the nonisolated flyback (the focus of this discussion) for improved efficiency at high output power. A PWM-controlled IC intended for the synchronous boost topology can directly drive the synchronous-rectifier FET of a flyback [11].

The current and voltage waveforms in **Figure 5** illustrate the primary disadvantages of the flyback. The voltage stresses on SW1 and SW2 are higher and a function of the turns ratio of the transformer (N_T). The transformer leakage inductance produces a voltage spike at the rising edge of SW1 that must be clamped by a snubber circuit, creating power loss and reducing efficiency. Leakage inductance transients also contribute to SW1 voltage stress and produce high-frequency ringing at the input. The input and output currents are discontinuous, which increases noise at both terminals and stress on the filter capacitors.

Single-inductor buck-boost solutions

Merging and simplifying cascaded buck and boost converters creates a single-inductor buck-boost. If you eliminate the intermediate buck output and merge the two inductors into a single inductor, as shown in **Figure 6**, the result is a single-inductor noninverting buck-boost.

You will need four switches: two on the buck side of the inductor (input) and two on the boost side (output). A single PWM controller can drive the power switches in all operating modes including buck, boost and the transition region, during which the input and output voltages are nearly identical.

When the input is higher than the desired output, the buck switches operate and the boost switches are static. Similarly, when the input is below the desired output, the boost switches operate and the buck switches are static. In the transition region, all four switches must operate with a blend of buck and boost action at the inductor to maintain the desired regulated voltage across the load. **Figure 7** illustrates current and voltage waveforms in all three modes.

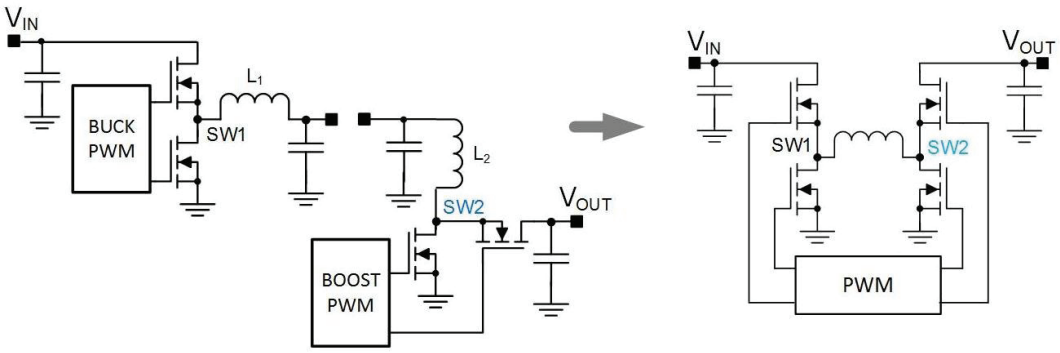

Figure 6. *Derivation of single inductor buck-boost converter.*

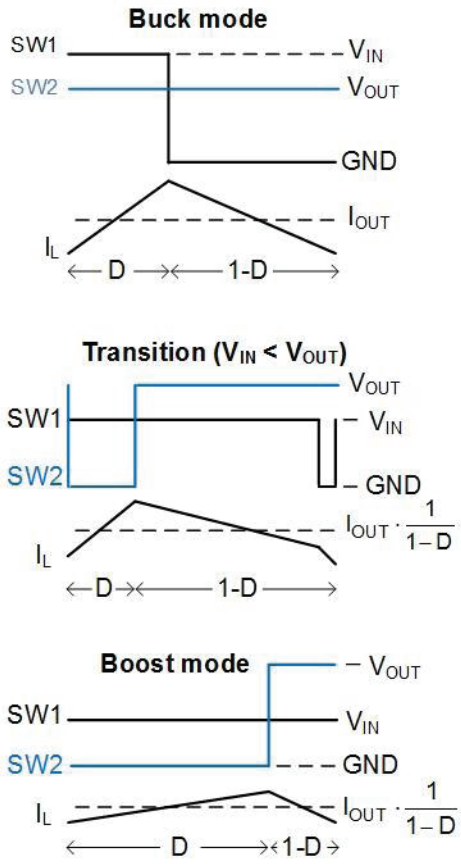

Figure 7. *Current and voltage waveforms in three operating modes.*

Merging a buck and boost converter that share an inductor and PWM controller is not particularly challenging until you consider the transition region [12] [13] [14]. Controlling the buck and boost duty cycles with a single-error amplifier and compensation design during transitions when both legs are active creates many potential problems. Discontinuity of the transfer function and interaction between opposing buck and boost-induced current changes requires architectural and circuit implementation trade-offs. We will address many of these special challenges later.

Of the topologies we consider in this paper, the single-inductor four-switch buck-boost converter yields the smallest solution with the highest efficiency and output power. Eliminating one inductor or transformer winding offers a size and efficiency advantage that typically outweighs the impact of two additional switches. Voltage stress on the switches is another advantage. The two FETs in the buck leg must be rated to block the maximum input voltage, while the two FETs in the boost leg are rated based on the output voltage. Selecting boost-leg FETs based on the output voltage instead of the input voltage allows selection of smaller devices with a lower gate charge without adversely affecting conduction loss.

N-channel FETs represent the four switches of the single-inductor buck-boost in **Figure 6**. However, this topology can be attractive in some applications with nonsynchronous rectifiers (diodes) in the low side of the buck leg and the high side of the boost leg. The nonsynchronous or two-switch single inductor buck-boost converter serves lower-power applications with simplified designs and natural transitions to discontinuous conduction mode (DCM) with light loads [15]. Losses in the diode rectifiers – especially the boost rectifier, which is always in series – limit output power for this configuration and should compel designers to consider the four-switch topology when converter performance is critical.

Topology comparison tables

Table 1 summarizes the strengths, weaknesses and common power range of the noninverting buck-boost solutions presented in the previous sections. Each topology offers some merit, so compare your application's prioritized requirements.

Table 2 provides a brief summary of voltage and current stresses of various topologies as a function of V_{IN}, V_{OUT} and I_{OUT}.

Topology	Strengths	Weaknesses	Power Range	Relative Efficiency
Cascaded boost + buck	+ Boost optional: add when required	– Two inductors and two compensated controllers	< 40 W	86%
	+ Wide choice of controllers for buck and boost stage	– High conduction and switching losses limit efficiency	< 60 W with sync FET	
	+ Low input and output noise	– Larger size and higher cost		
SEPIC	+ Only one switch plus diode	– Flying capacitor required	< 50 W	92% [10]
	+ Wide choice of controllers for a low-side switch	– Two inductors or coupled inductor		
	+ Low input noise	– Efficiency degrades at higher power	< 75 W with sync FET	
		– Switch voltage: $V_{IN} + V_{OUT}$		
		– Higher switch current, $I_{IN} + I_{OUT}$–		
		– Right half plane zero		
Zeta	+ Only one switch plus diode	– Flying capacitor required	< 40 W	90% [8]
	+ Low output noise	– Two inductors or coupled inductor		
	+ Direct drive for synchronous rectifier from PWM IC	– Efficiency degrades at higher power	< 60 W with sync FET	
		– Switch voltage: $V_{IN} + V_{OUT}$		
		– Higher switch current, $I_{IN} + I_{OUT}$		
		– Limited choice of PWM controllers for PFET switch		
Flyback	+ One switch plus diode	– Requires tightly-coupled transformer windings	< 50 W	88% [10]
	+ Wide choice of controllers	– Switch voltage: $V_{IN} + N_T*V_{OUT}$		
	+ Smaller transformer than SEPIC	– Efficiency degrades at high power / low V_{IN}	< 75 W with sync FET	
		– High input and output noise		
		– High frequency ringing on SW node		
2-Switch buck-boost	+ Simple design	– Diode rectifiers limit power	< 25 W	90%
	+ Single inductor	– Limited choice of controllers		
	+ Only buck operates at high V_{IN}	– High switch current for $V_{IN} < V_{OUT}$		
	+ Lower voltage FETs (V_{IN} for buck leg, V_{OUT} for boost)	– Shared compensation for buck and buck-boost		
4-Switch buck-boost	+ Single inductor / high density	– Limited choice of controllers	25–250 W	96%
	+ Sync rectifiers / high efficiency	– Challenging PCB layout		
	+ Only two switches operate at high and low V_{IN}	– Shared compensation for buck and buck-boost		
	+ Lower voltage FETs (V_{IN} for buck leg, V_{OUT} for boost)	– High buck-mode input noise / boost-mode output noise		

Table 1. *Strengths and weaknesses of noninverting buck-boost solutions.*

	Boost + buck	SEPIC & Zeta	Flyback ($N_T = N_P/N_S$)	2-Sw buck-boost	4-Sw buck-boost
Max V_{SW}	SW1, SW2: V_{IN}	$V_{IN} + V_{OUT}$	$V_{IN} + \frac{N_P}{N_S} V_{OUT}$	SW1: V_{IN} SW2: V_{OUT}	SW1: V_{IN} SW2: V_{OUT}
Max I_{SW}	$I_{OUT}\left(\frac{V_{OUT}}{V_{IN}}\right)$	$I_{IN} + I_{OUT}$	$I_{IN}\left(1 + \frac{N_S}{N_P}\frac{V_{IN}}{V_{OUT}}\right)$	$I_{IN} + I_{OUT}$	$I_{OUT}\left(\frac{V_{OUT}}{V_{IN}}\right)$
I_{L1}	$I_{OUT}\left(\frac{V_{OUT}}{V_{IN}}\right)$	$I_{OUT}\left(\frac{V_{OUT}}{V_{IN}}\right)$	$I_{OUT}\left(\frac{V_{OUT}}{V_{IN}} + \frac{N_S}{N_P}\right)$	$I_{OUT}\left(\frac{V_{OUT}}{V_{IN}} + 1\right)$	$I_{OUT}\left(\frac{V_{OUT}}{V_{IN}}\right)$
I_{L2}	I_{OUT}	I_{OUT}	$I_{OUT}\left(1 + \frac{N_S}{N_P}\frac{V_{OUT}}{V_{IN}}\right)$	–	–

Table 2. *Maximum current and voltage stresses of various power stages.*

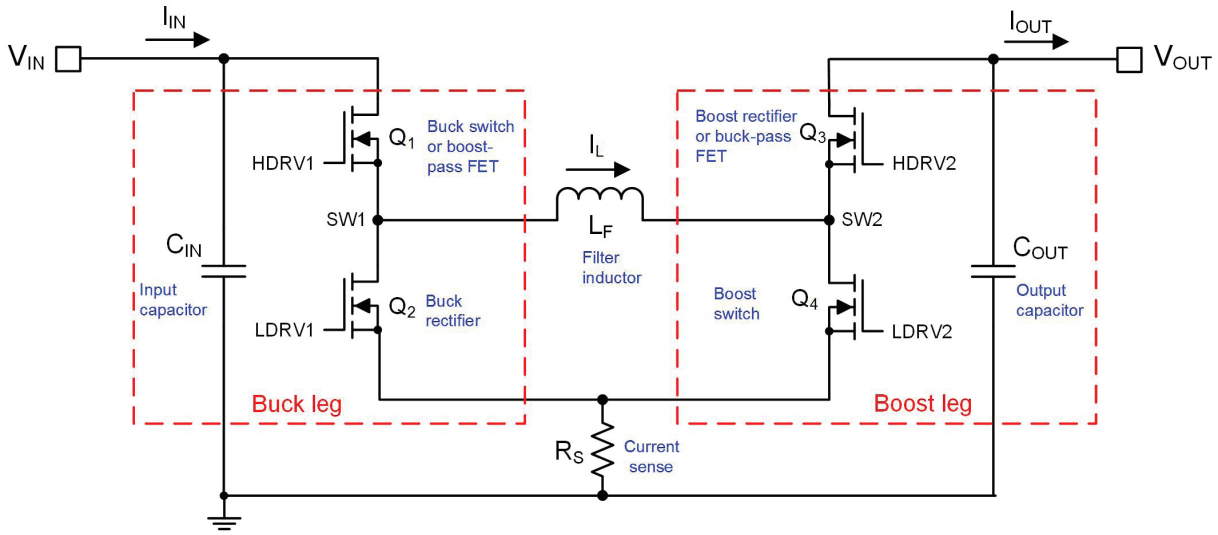

Figure 8. *Four-switch buck-boost converter power stage.*

Four-switch buck-boost operation

Four-switch buck-boost converter power stage

The four-switch buck-boost power stage consists of a buck leg (MOSFETs Q1, Q2 and switch-node SW1), a boost leg (MOSFETs Q3, Q4 and switch-node SW2), an inductor connecting the two switch nodes, and capacitors at the input and output (**Figure 8**).

Four-switch buck-boost operation

The four-switch buck-boost operation has three operating modes depending on the relative levels of input and output voltages: buck mode, buck-boost (transition) mode and boost mode.

In buck mode, the buck-leg MOSFETs (Q1, Q2) are switching and the boost high-side MOSFET (Q3) is in pass-through mode (100 percent duty cycle). The switching pattern is identical to a buck converter (**Figure 9**).

In boost mode, the buck high-side MOSFET (Q1) is always on (100 percent duty cycle) and the boost-leg MOSFETs (Q3, Q4) are switching. The switching pattern is identical to a boost converter (**Figure 10**).

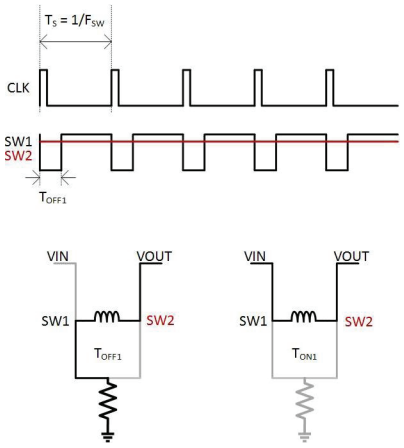

Figure 9. *Buck-mode switching.*

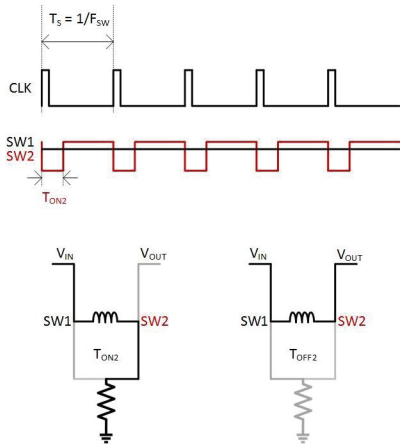

Figure 10*. Boost-mode switching.*

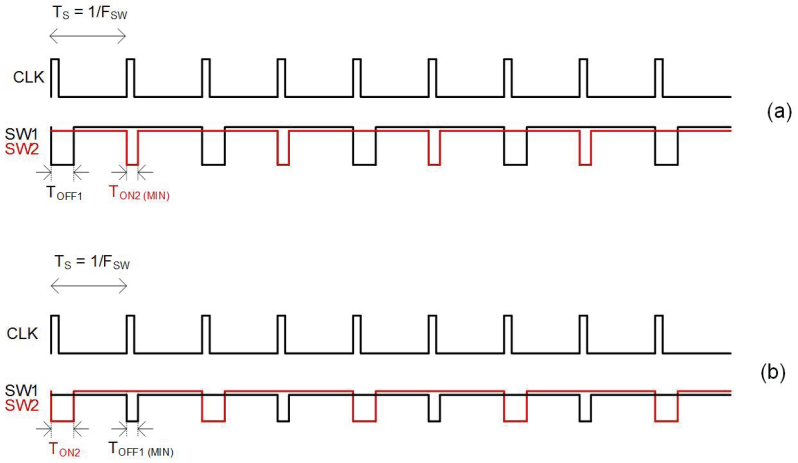

Figure 11. *Buck-boost switching waveforms ($V_{IN} > V_{OUT}$) (a); and ($V_{IN} < V_{OUT}$) (b).*

The buck-boost mode consists of alternating buck and boost cycles (**Figure 11**).

Current-mode control

You can implement a four-switch buck-boost converter with the switching pattern presented in the previous section using either voltage or current-mode control, but current-mode control results in a relatively simple power-stage model that is easier to compensate across a wide input-voltage range.

The current-mode control scheme implementation shown in **Figure 12** uses a low-side sense resistor, designated R_S, for sensing the inductor current. Low-side sensing conveniently provides information for valley modulation in buck mode and peak modulation in boost mode. Let us briefly describe peak and valley modulation.

Peak-current modulation in boost mode

The boost mode uses peak current-mode control. In peak current-mode control, the low-side gate drive LDRV2 turns on at the start of the switching cycle (**Figure 13a**). In this subinterval, V_{IN} appears across the inductor and the inductor current ramps up. The low-side gate drive (LDRV2) terminates when the sensed inductor current exceeds the target current reference (COMP) set by the controller. At this point Q2 turns off, and the inductor current starts flowing through the body diode of Q3. The high-side gate drive is the complement of the low-side gate drive and keeps the high-side MOSFET Q3 on for the remainder of the switching period. Slope compensation is required in a peak current-mode boost converter when $V_{IN} < ½\ V_{OUT}$ to prevent subharmonic oscillation in continuous conduction mode (CCM) and to provide added noise immunity.

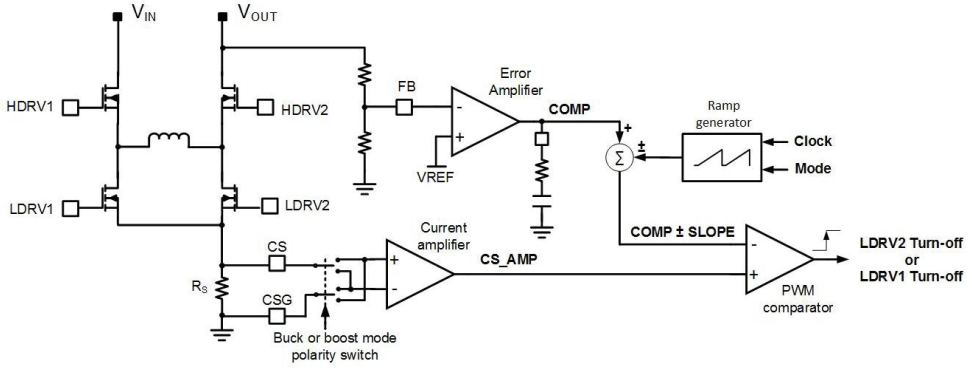

Figure 12. *A conceptual schematic of a current-mode control implementation in a four-switch buck-boost converter.*

Valley-current modulation in buck mode

The buck-mode operation of the four-switch buck-boost is based on valley current-mode control. In valley current-mode control, the low-side gate drive LDRV1 turns on at the start of every switching cycle (**Figure 13b**). In this subinterval, the V_{OUT} is applied across the inductor and the inductor current ramps down. The low-side gate drive (LDRV1) terminates when the sensed inductor current falls below the target current reference (COMP) set by the controller error amplifier. At this point Q2 turns off and the inductor current starts flowing through the body diode of Q2. The high-side gate drive HDRV1 is the complement of the low-side gate drive and turns on the high-side MOSFET Q1 for the remainder of the switching period. As reported in references [16] [17], slope compensation is necessary in a valley current-mode-controlled buck converter operating in CCM when $V_{IN} > 2\ V_{OUT}$.

Buck-boost transition-mode operation

Buck-boost mode consists of alternating buck and boost switching cycles. The individual buck cycles are valley-current modulated in the same way as pure buck mode. The boost cycles in the buck-boost mode are peak-current modulated in the same way as pure boost mode. Due to interleaving buck and boost cycles, the buck-boost mode exhibits a distinct switching pattern (see SW1/SW2 in **Figure 11**).

The inductor current waveform in buck-boost mode consists of four segments: two segments for each of the interleaved buck and boost cycles (**Figure 13c**). For simplicity, **Figure 13c** does not include the slope compensation component.

Buck-boost design example

Application requirements

This section discusses the component selection for a four-switch buck-boost converter using a practical design example. Table 3 lists the design specifications.

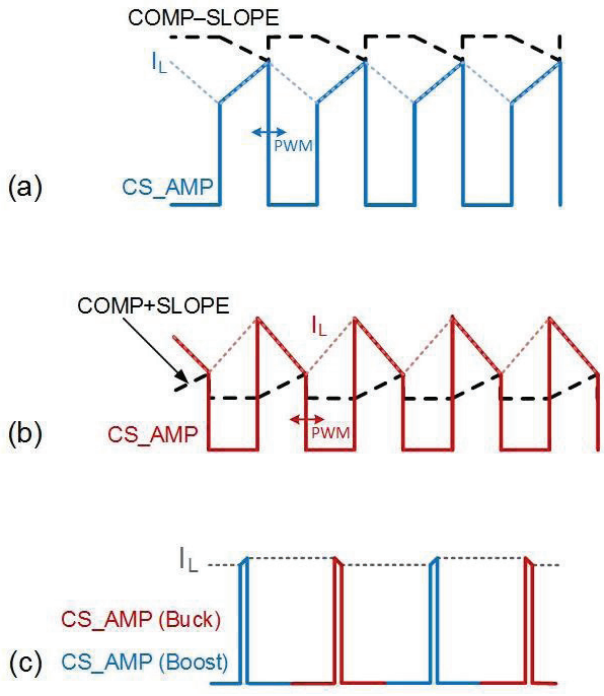

Figure 13. *Current modulation in a four-switch buck-boost converter: peak-current modulation in boost mode (a); valley-current modulation in buck mode (b); interleaved valley and peak-current modulation in buck-boost mode ($V_{IN} = V_{OUT}$) (c).*

Design parameters	Target specifications
Input voltage range, $V_{IN(min)}$-$V_{IN(max)}$	6 V-42 V
Output voltage, V_{OUT}	12 V
Maximum load current, $I_{OUT(max)}$	6 A
Switching frequency, F_{SW}	300 kHz

Table 3. *Design example specifications.*

Inductor selection

Typically, you should base inductor selection on three factors:

- Target peak-to-peak inductor ripple current.
- Root-mean-square (RMS) and saturation current.
- Size and cost.

Set the ripple-current ratio at the minimum input voltage (deepest boost operating point) between 20 to 40 percent of the boost-mode inductor current using Equation 1:

$$L_F = \frac{V_{IN(min)}^2 \left(V_{OUT} - V_{IN(min)}\right)}{0.2 I_{OUT(max)} F_{sw} V_{OUT}^2} = 4.2\mu H \quad (1)$$

Equation 2 calculates the inductor saturation current rating at a minimum input voltage:

$$I_{L(SAT)} \geq 1.3 \times \left(\frac{V_{OUT} \times I_{OUT(MAX)}}{0.9 \times V_{IN(MIN)}} + \frac{\Delta I_L}{2} \right) = 17.3A \quad (2)$$

Equation 2 assumes 90 percent conversion efficiency and 30 percent margin between the peak inductor current and saturation rating. Based on this calculation, select a 4.7-µH inductor rated for greater than 18 A. For applications requiring operation in sustained overload conditions, the RMS current rating should be higher than the saturation current calculated in Equation 2.

Table 4 shows the inductor current ripple for different input voltages. The 4.7-µH inductor selected for this design results in relatively high ripple at the maximum input voltage (100 percent of I_{OUT}). A higher inductance provides smaller ripple current at the expense of inductor size, cost and DC resistance.

V_{IN}	ΔI_{L1}
6 V	2.1 A
24 V	4.3 A
36 V	6.1 A

Table 4. *Inductor ripple current versus input voltage.*

Output capacitor selection

Select the output capacitor based on the maximum RMS current in the capacitor during the boost mode of operation and the output voltage ripple specification. The maximum RMS current flows in the output capacitor when operating at the minimum input voltage with the maximum load, as given by Equation 3.

$$I_{COUT(rms)} = I_{OUT} \sqrt{\frac{V_{OUT}}{V_{IN}} - 1} = 6A \quad (3)$$

The output ripple has capacitive and capacitor equivalent series resistance (ESR)-based components. Equation 4 expresses ESR-based ripple as:

$$\Delta V_{RIPPLE(ESR)} = \frac{I_{OUT} V_{OUT}}{V_{IN(min)}} ESR \quad (4)$$

An ESR of 5 mΩ, for example, results in an ESR-based ripple of 60 mV. Equation 5 gives the capacitive ripple as:

$$\Delta V_{RIPPLE(C_{OUT})} = \frac{I_{OUT}}{C_{OUT} F_{sw}} \left(\frac{V_{OUT} - V_{IN}}{V_{OUT}} \right) \quad (5)$$

The maximum capacitive ripple occurs at the minimum input voltage. Under these conditions, an output capacitance of 330 µF results in a capacitive ripple of 30 mV. **Figure 14** shows the current flow in the output capacitor.

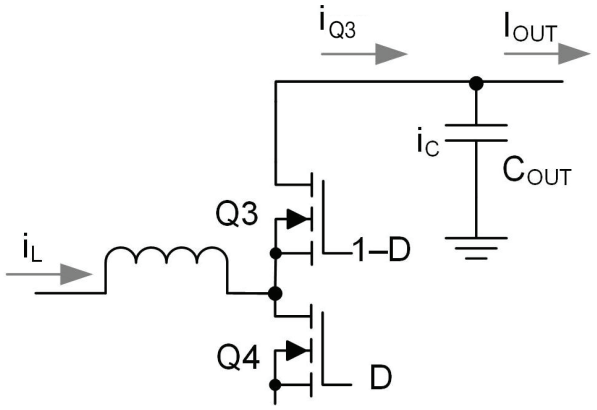

Figure 14. *Current flow in the output capacitor.*

The total output-voltage ripple is the sum of capacitive and resistive ripple components (**Figure 15**).

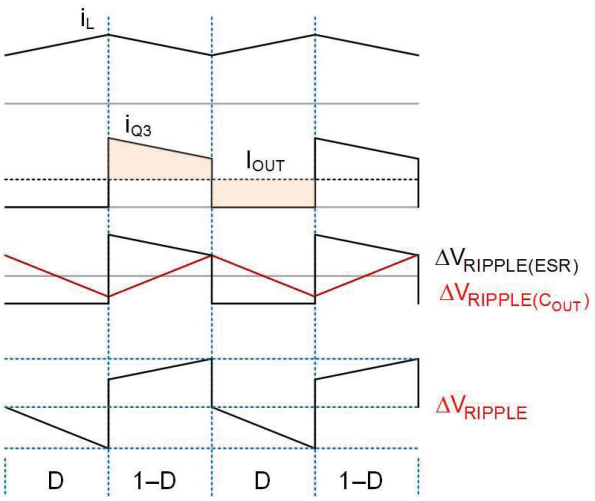

Figure 15. *Capacitive and ESR-based ripple at the output capacitor.*

Typically, you will need a combination of ceramic and bulk capacitors to meet the C_{OUT}, ESR and ripple-current requirements. Aluminum polymer-type capacitors typically have large bulk capacitance and low ESR values.

Input capacitor selection

Input capacitor selection closely follows the method used for the output capacitor. The maximum RMS current flowing in C_{IN} occurs in buck mode. Referring to **Figure 16**, Equation 6 gives the RMS current as:

$$I_{CIN(rms)} = I_{OUT}\sqrt{\frac{V_{OUT}}{V_{IN}}\left(1-\frac{V_{OUT}}{V_{IN}}\right)} \quad (6)$$

The worst-case input RMS current flows when the buck V_{OUT} is half of V_{IN} (50 percent duty cycle). Using 12 V and 24 V for V_{OUT} and V_{IN}, respectively, Equation 6 calculates the maximum I_{CIN}(rms) as 3 A.

The input-voltage ripple is a combination of capacitive and ESR-based ripple, as explained in Figure 17. Equation 7 gives the ESR-based ripple at the input as:

$$\Delta V_{RIPPLE(ESR)} = I_{OUT}ESR \quad (7)$$

An ESR of 25 mΩ results in approximately 150 mV of input-voltage ripple. Equation 8 calculates the capacitive ripple:

$$\Delta V_{RIPPLE(C_{IN})} = \frac{I_{OUT}\frac{V_{OUT}}{V_{IN}}\left(1-\frac{V_{OUT}}{V_{IN}}\right)}{C_{IN}F_{sw}} \quad (8)$$

A capacitance of 68 µF results in approximately 75 mV of capacitive ripple at the input.

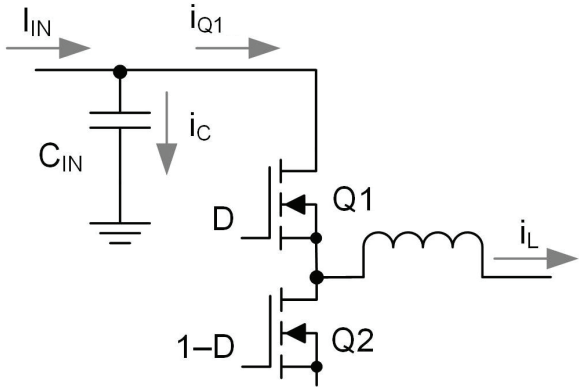

Figure 16. *Current flow in the input capacitor.*

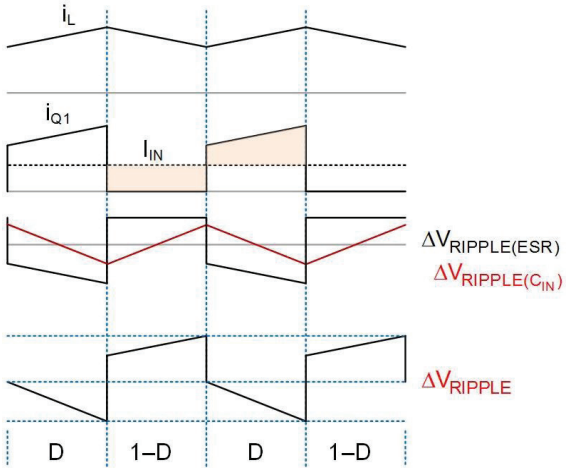

Figure 17. *Capacitive and ESR-based voltage ripple at the input capacitor.*

Again, you will need a combination of ceramic and bulk capacitors to achieve the required ripple current, ESR and capacitance.

Slope compensation

For ideal slope compensation, select a slope capacitor that provides a slope equal to the inductor current slope during boost off-time (Q3 on) or buck on-time (Q1 on) (Equation 9):

$$C_{SLOPE} = g_{m(slope)} \frac{L_F}{R_S A_{CS}} = 2\mu S \times \frac{4.7\mu H}{8m\Omega \times 5} = 235pF \quad (9)$$

Theoretically, a C_{SLOPE} twice the ideal value (per equation 9) is sufficient to prevent subharmonic oscillations. In practice, a lower slope capacitor (higher slope compensation) is almost always necessary to provide sufficient noise immunity. A very small C_{SLOPE} (in other words, high slope compensation) causes the converter to exhibit voltage-mode-like behavior, with subsequent phase-margin degradation. For this design, a 100-pF capacitor proved satisfactory.

Compensation and Bode plot

A four-switch buck-boost converter contains the power stages for both buck and boost converters. **Table 5** summarizes the power-stage poles and zeros for buck and boost stages.

Due to the RHP zero of the boost-mode power stage, the boost mode usually limits the practically achievable bandwidth. A recommended maximum crossover frequency in boost converters is one-third to one-fourth the RHP zero frequency. **Table 6** shows the compensation design steps for a target bandwidth of 4 kHz.

Small-signal parameters	Boost stage	Buck stage
Load pole	$f_{p1(boost)} = \frac{1}{2\pi}\left(\frac{2}{R_{OUT}C_{OUT}}\right) = 398\ Hz$	$f_{p1(buck)} = \frac{1}{2\pi}\left(\frac{1}{R_{OUT}C_{OUT}}\right) = 199\ Hz$
ESR zero	$f_{z1} = \frac{1}{2\pi}\left(\frac{1}{R_{ESR}C_{OUT}}\right) = 79.6\,kHz$	$f_{z1} = \frac{1}{2\pi}\left(\frac{1}{R_{ESR}C_{OUT}}\right) = 79.6\ kHz$
RHP zero	$f_{zRHP} = \frac{1}{2\pi}\left(\frac{R_{OUT}\left(1-D_{Boost(max)}\right)^2}{L_F}\right) = 16.9\ kHz$	–

Table 5. *Converter small-signal model equations.*

Compensation Parameter	Equations/Value
Compensator zero	f_{zc} = 1 kHz to prevent excessive phase loss due to load pole
Set crossover using Rc1	$R_{c1} = \frac{2\pi F_c}{gm_{EA}} \times \frac{R_{FB1}+R_{FB2}}{R_{FB1}} \times \frac{A_{CS}R_S C_{OUT}}{1-D_{max}} = 10.9k\Omega$
Select Cc1 for compensator zero location	$C_{c1} = \frac{1}{2\pi f_{zc} R_{c1}} = 15.9nF$
High-frequency pole	$C_{c2} = \frac{1}{2\pi f_{zESR} R_{c1}} = 106pF$

Table 6. *Summary of loop-compensation equations and values.*

Place the high-frequency pole at a lower frequency to suppress switching-frequency noise and ripple. **Figure 19** shows Bode plots with the selected values at 6-V and 18-V input voltages. The phase axis on the right is the cumulative phase shift through the compensation and power stage. Loop phase differs from phase margin by 180 degrees; that is, a loop phase of –180 degrees corresponds to a phase margin of 0 degrees. Power designers typically target a phase margin of 60 degrees or higher.

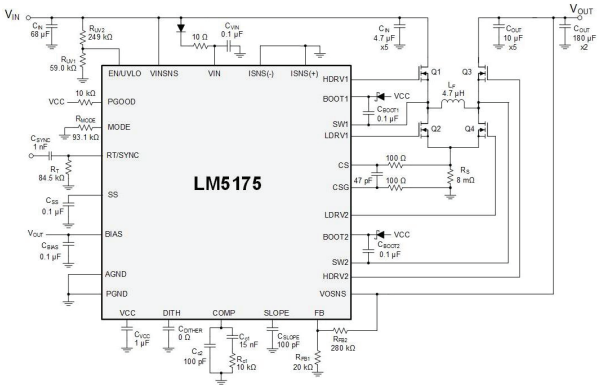

Figure 18. Four-switch synchronous buck-boost converter schematic.

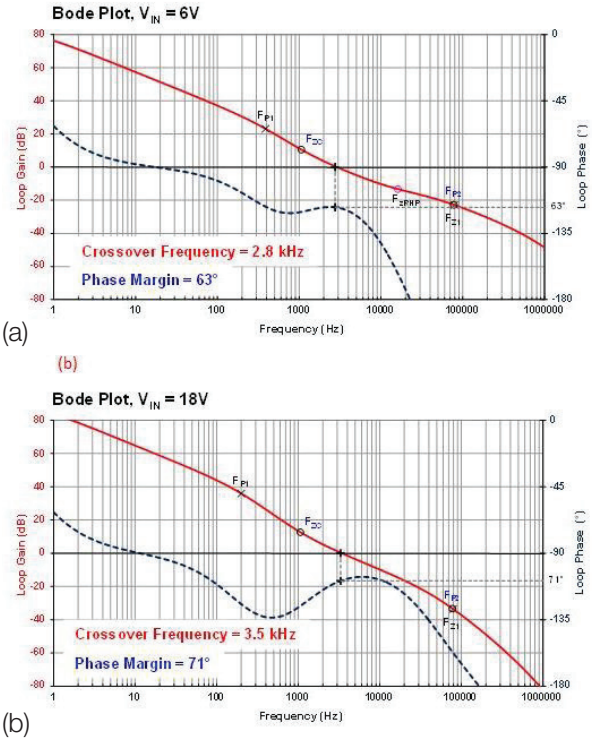

Figure 19. Bode plot at V_{IN} = 6 V, I_{OUT} = 6 A (a); and at V_{IN} = 18 V, I_{OUT} = 6 A (b).

Four-switch buck-boost converter PCB layout

A well-planned PCB layout is fundamental to careful system design of any DC/DC power converter. An optimized layout leads to better performance, lower cost and faster time to market. It can also improve reliability (lower component temperatures), simplify regulatory compliance (lower conducted and radiated emissions), and improve space utilization (reduced solution volume and footprint). Let us review the PCB design procedure for the four-switch buck-boost converter in reference [18].

Critical steps include identification of the converter switching loops, power-stage component floorplanning, connection routing, and polygon plane design of the multilayer PCB's outer and inner layers.

Figure 20 shows the four-switch buck-boost converter schematic with components for the power stage, a controller that includes integrated gate drivers, V_{CC} bias supply, current sensing, output voltage feedback, loop compensation, programmable undervoltage lockout (UVLO) and a dither option for a lower noise signature. **Figure 20** also distinguishes by color high current traces, noise-sensitive traces such as feedback and current sense paths, and circuit nodes with high dv/dt.

Step 1: Identify the high-slew-rate current loops

With an eye toward understanding the layout-induced parasitic inductances that cause excessive noise, overshoot, ringing and ground bounce, it is imperative to identify the high-slew-rate current loops, or "hot loops," from the converter schematic. As **Figure 21** illustrates, loops 1 and 2, shaded in red, are classified as high-frequency switching power loops for the buck and boost legs, respectively. During a MOSFET switching event where the slew rate of the commutating current can exceed 5 A/ns, just 2 nH of parasitic inductance

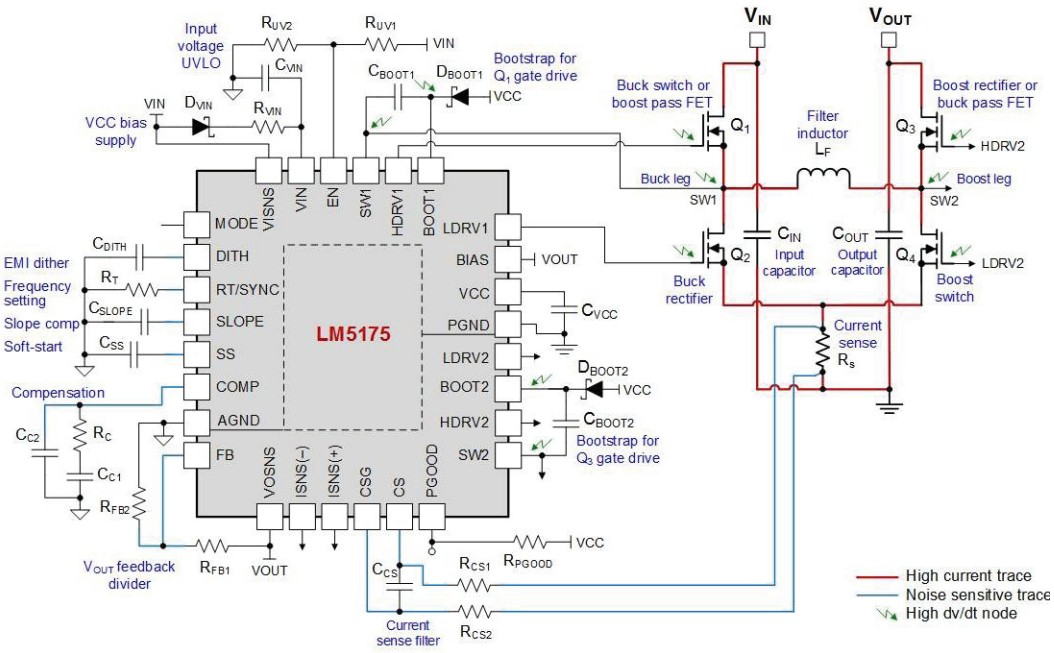

Figure 20. *Four-switch buck-boost converter schematic highlighting high current traces, noise-sensitive nets and high dv/dt circuit nodes.*

results in a voltage spike of 10 V. Insofar as the rectangular current waveforms in the identified power loops are rich in harmonic content, a severe threat of magnetic-field coupling and radiated electromagnetic interference (EMI) exists. Clearly, it is vital to minimize the effective loop length and enclosed area of loops 1 and 2. This reduces parasitic inductance and enables magnetic field self-cancellation [19], and also reduces the radiated energy emanating from what are effectively loop antenna structures.

In contrast, the current flowing in the filter inductor is largely DC, with a superimposed triangular ripple. The inductance inherently limits the current rate of change. Any parasitic inductive component contributed by the series connections is essentially benign.

Loops 3 through 6 in **Figure 21** are classified as gate loops for the buck and boost-leg MOSFETs. Specifically, loops 3 and 4, outlined in green, represent the high-side MOSFETs' gate driver circuits supplied by their respective bootstrap capacitors. Loops 5 and 6, denoted in blue, designate the low-side MOSFETs' gate drivers supplied by the V_{CC} rail. Each case delineates the turn-on and turn-off current paths, denoted by solid and dashed lines, respectively. To charge and discharge the MOSFETs' effective gate capacitance during turn-on and turn-off transitions, an instantaneous current up to 5A peak (a function of gate driver strength, series gate resistance and inductance, and MOSFET capacitance) flows briefly in each gate loop.

You can minimize the low-side gate driver loop's enclosed areas by placing the V_{CC} decoupling capacitor very close to the VCC and PGND pins. Similarly, you can diminish the high-side gate driver loop enclosed areas by positioning the bootstrap capacitors close to their respective SW and BOOT pins [20]. Keeping the gate driver trace runs from the controller to the MOSFETs as short and direct as possible minimizes gate-loop parasitic inductance.

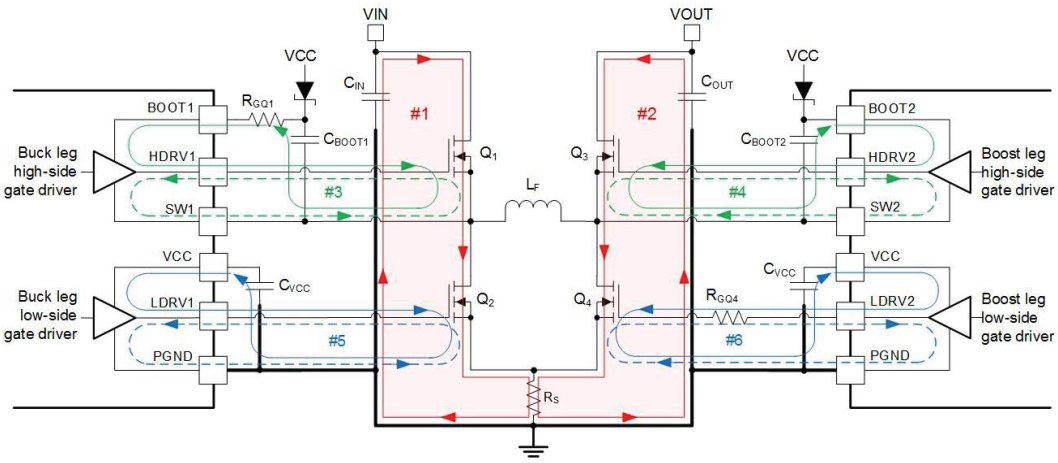

Figure 21. *Buck-boost converter schematic with critical loops categorized for high-slew-rate currents. Loops 1 and 2 are high-frequency switching power loops for the buck and boost legs, respectively. Loops 3, 4, 5 and 6 denote gate-driver loops during MOSFET turn-on and turn-off switching transitions.*

Step 2: Place power-stage components (MOSFETs, inductor, capacitors, shunt)

Based on the high di/dt current loops identified in **Figure 21**, thoughtful and strategic placement of the power-stage components is essential. **Figure 22** illustrates the placement of power MOSFETs, a wide-aspect-ratio footprint current shunt, and input and output ceramic capacitors on the PCB's top layer.

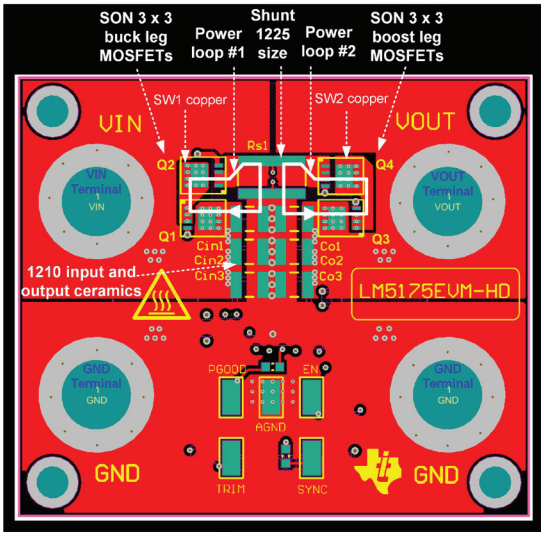

Figure 22. *The PCB top layer with power-stage component layout shows tight AC current-loop conduction paths. A schematic of the powertrain serves as a caption.*

In **Figure 22**, the low-profile MOSFETs (small outline no-lead (SON) 3 mm by 3 mm) and ceramic capacitors (1210 footprint) are purposely located on the top side of the PCB, whereas the taller components (inductor and bulk capacitors) are placed on the bottom side. Input capacitors are located close to buck-leg MOSFETs. Similarly, output capacitors are located adjacent to boost-leg devices, resulting in a tight, symmetric layout for both switching legs.

Note that the shunt resistor increases the area of both switching loops. A shunt resistor with a wide aspect ratio (for example, 1225 footprint) shortens the conduction path, lowers parasitic inductance, and reduces the length of power loops 1 and 2, denoted with white current paths in **Figure 22**.

H-field self-cancellation

Switching-loop parasitic inductance increases MOSFET switching loss and the peak drain-to-source voltage spike. It also exacerbates SW node voltage ringing, increasing broadband EMI in the 50- to 300-MHz range. While minimizing the physical size of the loop by paying attention to component placement is important to reduce loop inductance, noise

coupling also depends on field distribution/orientation, making the design of the PCB's inner layers also noteworthy. Establish a passive shield layer by placing a ground plane as close as possible to the switching loop using the minimum dielectric thickness [21] [22] [23] [24] [25]. The horizontal current flow on the top layer sets up a vertical flux pattern, and the resulting magnetic field induces a current in the shield layer opposite in direction to the current in the switching loop. By Lenz's law, the current in the shield layer generates a magnetic field to counteract the original power-loop magnetic field. The result is that H-field self-cancellation that reduces magnetic flux and effective parasitic inductance. Having an uninterrupted, continuous shield plane on layer 2 at the closest possible proximity to the switching loop offers the best performance. You can achieve a narrow intralayer spacing in the PCB stack-up using a 6-mil core dielectric, for example.

Power stage thermal design and SW node EMI considerations

To maximize thermal performance with convective airflow, MOSFETs placed on the top side of the PCB are not airflow-shadowed by taller components like the inductor and electrolytic capacitors. Depending on the application, it may be viable to locate the inductor on the bottom side of the PCB as it may impede heat transfer if placed on top. Owing to its size, the inductor intrinsically acts as its own heat sink.

For the four-switch buck-boost converter described in this paper, the low-side MOSFET of the nonswitching leg is held off in pure buck or boost modes, thus offsetting the adjacent high-side device that conducts the inductor current continuously with concomitant power loss. Conversely, with deep buck or boost operation (in other words, low buck duty cycle or high boost duty cycle), switching-leg MOSFET selection tilts toward managing low-side power loss and temperature rise. As shown in **Figure 22**, the high-side MOSFET drains are connected with short traces to the V_{IN} or V_{OUT} power terminals through heat-spreading copper planes. Numerous thermal vias join the drain tabs to corresponding copper planes on the bottom layer. Thus, the high-side MOSFETs have adequate heat sinking.

The thermal challenge of this design is the low-side MOSFETs, whose drain tabs are attached to SW node copper polygons with via connections to the inductor below. The wild card here is the SW node copper area. Provisioning for EMI places an emphasis on a small SW node copper area to reduce capacitive coupling related to high dv/dt SW node voltage transitions and decrease e-field radiated emissions. Nevertheless, a larger SW node copper area assists thermal conduction related to dissipation from the inductor and low-side MOSFETs. To mitigate thermal issues, you can achieve a PCB layout for larger SON 5-mm by 6-mm footprint MOSFETs with lower thermal impedance by making relatively minor edits to the placements in **Figure 22**.

Step 3: PWM controller IC location and bottom-side layout

If the PWM controller IC has integrated gate drivers, it is imperative to locate the IC as close as possible to the power MOSFETs. If closely located, keep the gate-driver traces from the controller to the MOSFETs as short and direct as possible to minimize parasitic gate inductance. On a single-sided PCB design, the only option is to place the control IC on the top (component) side, close to the power devices. However, the power-stage layout often complicates achieving short gate-drive connections.

The necessary signal-level components, connecting traces and vias that typically surround the IC also make its placement more difficult. It is often advantageous in a two-sided layout to place the IC on the bottom (solder) side of the PCB. This placement helps gate-drive circuit performance,while shielding the sensitive analog circuits from the switching noise and high operating temperatures of power devices. **Figure 23** illustrates the use of this strategy in a bottom-side layout.

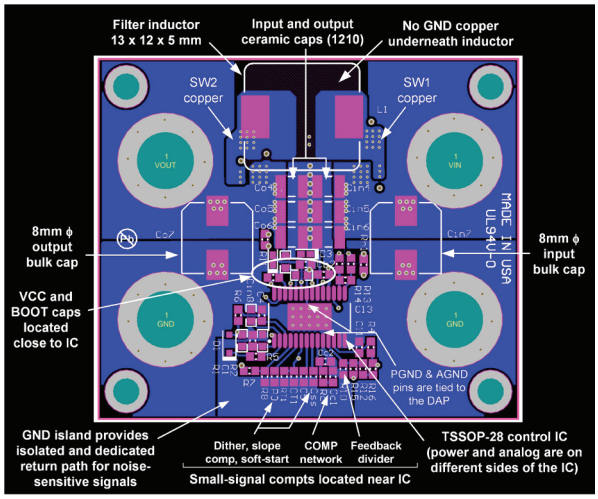

Figure 23. *Bottom layer of PCB (layer 6) viewed from below. Small-signal components surrounding the control IC are located on a separate GND island.*

There are three reasons to locate higher-profile electrolytic capacitors on the bottom side. First, the capacitors are of a similar height as the banana connections for the power terminals in this design and thus, impose no height penalty. Second, the capacitors conduct low- to mid-frequency current harmonics, making close placement to the MOSFETs superfluous. Third, airflow shadowing from the capacitors is largely inconsequential, as the lower-profile heat-dissipating MOSFETs are seated on the top side of the PCB.

The noise-sensitive small-signal components for the compensation network, feedback resistors, frequency-set resistor, soft-start capacitor and current-sense filter are located close to their respective pins (COMP, FB, RT, SS, CS-CSG) and have a dedicated analog ground (AGND) plane connected to the IC AGND pin. Power ground (PGND) connects to the exposed pad of the IC with thermal vias to the inner ground planes. PGND connects to AGND locally there (specifically, single-point grounding).

Step 4: Route the MOSFET gate drives, current sense, feedback and other critical traces

Figures 24 on page 20 show the inner-layer artwork for this PCB design example. The gate-driver traces running from the control IC to the four MOSFETs, which are located on layers 3 and 4, are as short and direct as possible to reduce gate inductance. Kelvin-connecting the gate drive return traces directly to the respective MOSFET source terminals minimizes common-source inductance. The return currents for the low-side MOSFET gate drivers flow on the GND plane back to the PGND pin of the IC. To minimize gate-loop area, gate and source traces are routed side by side as differential pairs using 20-mil trace widths.

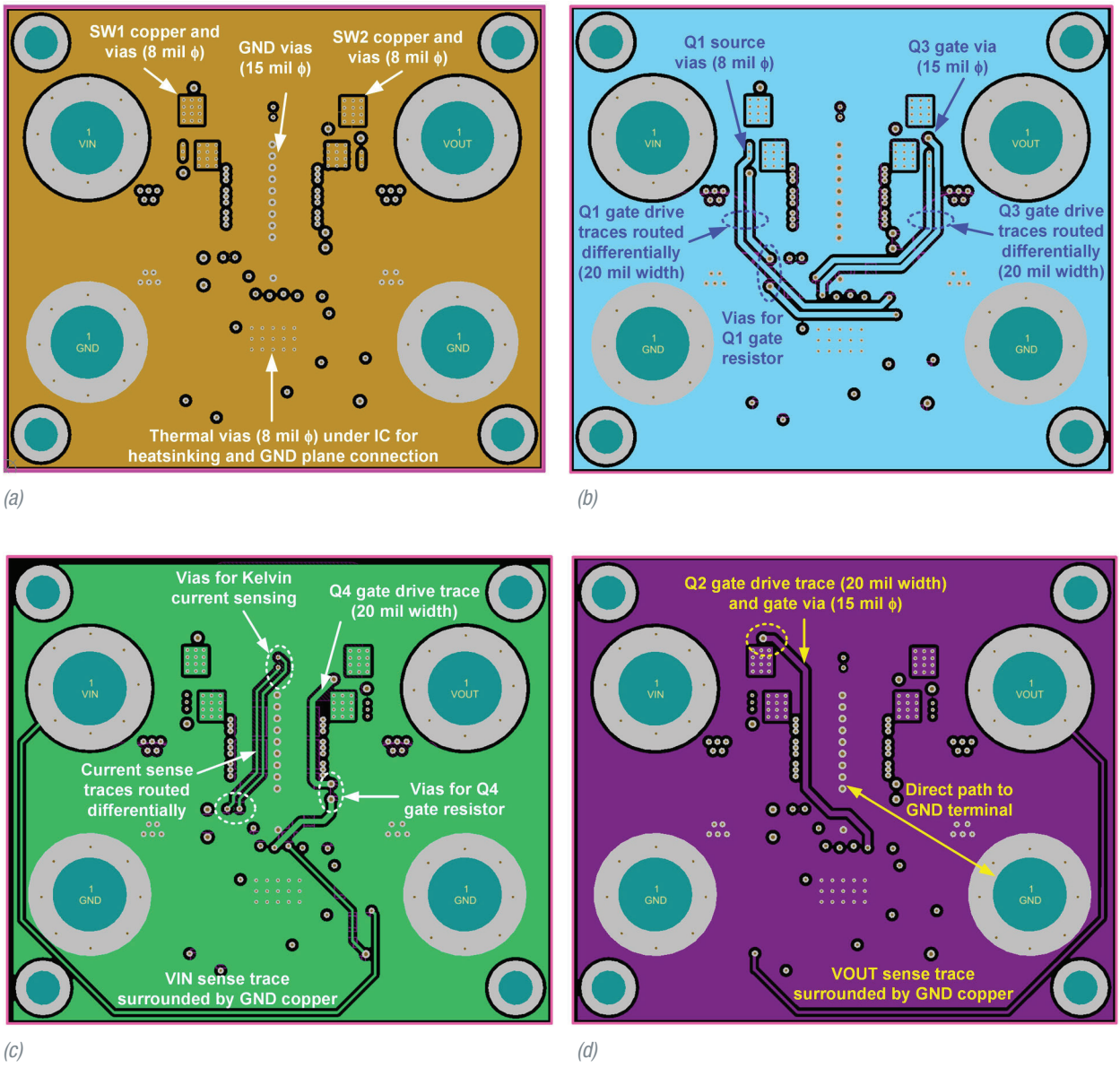

Figure 24. *PCB artwork for layers 2, 3, 4 and 5 (24a, b, c and d, respectively).*

Figure 24a shows the traces for current sense routed as a tightly coupled differential pair from the shunt resistor to the IC current-sense inputs. Kelvin sensing at the shunt is essential for accuracy. Use keep-outs to ensure isolation of the vias associated with the sense-return trace from GND planes. Locate current-sense filter components close to the IC.

Figure 24d shows the V_{OUT} sense location at the most accurate regulation point, typically on the lowest layer in the stackup before current flows to the load. V_{IN} and V_{OUT} sense traces, routed on layers 4 and 5, are low impedance to GND but are still susceptible to the converter's high di/dt loops.

Step 5: Power and GND plane design; single-point grounding

Given that all capacitors decouple effectively only up to their frequency of self-resonance, it is difficult to realize a wide spectral distribution of decoupling from V_{IN} and V_{OUT} to PGND. Stacking V_{IN} and V_{OUT} planes above or below PGND planes leverages the multilayer PCB as a low equivalent series inductor (ESL) capacitor. In this buck-boost converter example layout, locating the V_{IN} and V_{OUT} copper polygons on the top and bottom layers provides low-resistance conduction paths to the power terminals. Then, the inner layers of the PCB are filled with as much copper at GND potential as possible, as shown in **Figure 24**. Two different ground symbols commonly denote AGND and PGND in the schematic. Only one connection point between AGND and PGND is required, usually at the IC's exposed thermal pad.

PCB layout summary

A four-switch buck-boost topology facilitates a discussion of power converter PCB layout, starting with an understanding of the key converter switching loops from the schematic. Diligently minimizing these loop areas during PCB layout is imperative to abating parasitic inductance, magnetic field coupling and radiated EMI. Other considerations include:

- Power-stage component floorplanning
- Thermal design
- Strategic PWM controller placement
- Routing critical traces for gate drives, current sense and feedback
- Small-signal component placement and routing
- Polygon plane design of the multilayer PCB

Overall summary and conclusions

Many practical applications require noninverting buck-boost conversion. Noninverting buck-boost conversion is possible by cascading boost and buck converters or by using a multiwinding topology such as SEPIC, Zeta or flyback. These approaches are usually bulky and less efficient because of multiple windings and higher voltage and current stresses.

The four-switch buck-boost is the topology of choice when you need high power and high efficiency. The four-switch buck-boost maintains high efficiency over its working range by operating in buck, boost or buck-boost mode, depending on the input and output voltages.

Board layout is critical to the success of a buck-boost design. It begins with the identification of high dv/dt nodes and high di/dt loops. You can achieve the best performance by keeping current loops small and sensitive nodes spaced away from noisy switching traces.

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