Power Supply Design Seminar

Under the hood of a non-inverting buck-boost DC/DC converter

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Under the hood of a non-inverting buck-boost DC/DC converter

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Agenda

• Buck-boost conversion
  o Buck-boost applications and approaches
  o Topology advantages and disadvantages

• 4-switch buck-boost converter
  o Basic converter operation
  o Power loss calculations
  o Converter design example
  o PCB layout case study
Who needs a buck-boost converter?

- **Fixed output / variable input:**
  - Battery input from full to minimum charge
  - Automotive cold-crank
  - AC-powered with battery back-up

- **Variable output / fixed input:**
  - GaN or Silicon power amplifier (PA)
  - Constant current LED drive
  - USB Type-C power delivery (PD)

- **Programmable output / variable input**
  - Automotive USB Type-C PD
  - Adaptive PA powered from a battery
Buck-boost applications

**Industrial PCs**

*Application needs*
- 6 V-36 $V_{IN}$ from AC-powered supply or battery
- 12 V output, 60 W-200 W

**Automotive start/stop & DVRs**

*Application needs*
- 9 V-16 $V_{IN}$, 3.5 V during start
- ~12 V output, 60 W-120 W

**USB power delivery**

*Application needs*
- 12 V bus or battery, 9V–16 $V_{IN}$
- 5/12/20 $V_{OUT}$, 10 W–100 W

**Industrial & battery chargers**

*Application needs*
- 12 V or 24 $V_{IN}$ or DC adapter
- CC/CV up to 200 W+

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Cascaded boost + buck

**Advantages**
- Wide choice of buck and boost controllers
- Two simple topologies
- Low noise at both input and output
- Parallel buck stages for multiple $V_{\text{OUT}}$ rails

**Disadvantages**
- Two inductors
- Two controllers
- Higher cost
- Larger solution size
- Higher losses, lower efficiency
SEPIC converter
Single-ended primary inductance converter

Advantages
• Only one switch plus diode
• Wide choice of controllers for a low-side control switch
• Low input noise

Disadvantages
• DC-blocking capacitor required
• Two inductors or coupled inductor
• Efficiency degrades at higher power
• High switch voltage, $V_{IN} + V_{OUT}$
• High switch current, $I_{IN} + I_{OUT}$
• Right half-plane zero
Zeta converter
Inverted SEPIC

Advantages
• Only one switch plus diode
• Can use low-cost PFET controller
• Low output noise

Disadvantages
• DC-blocking capacitor required
• Two inductors or coupled inductor
• Efficiency degrades at higher power
• High switch voltage, $V_{IN} + V_{OUT}$
• High switch current, $I_{IN} + I_{OUT}$
• Right half-plane zero
Flyback converter

Advantages
• One switch plus diode
• Wide choice of controllers
• Higher power with larger transformer

Disadvantages
• Requires tightly-coupled transformer
• High switch voltages ($V_{IN} + N_T V_{OUT}$)
• Efficiency degrades at high power / low $V_{IN}$
• High input and output noise / ripple
• High frequency ringing on SW1

Note: $N_T = \text{Transformer Turns Ratio} = \frac{N_P}{N_S}$
2-switch single inductor buck-boost converter

Advantages

• Simple design
• Single inductor
• Only buck side operates at high $V_{IN}$
• Lower voltage SW2 FET

Disadvantages

• Non-synchronous design limits power
• High switch current for $V_{IN} < V_{OUT}$
• Output diode power losses
• Single control loop for buck and buck-boost
4-switch single inductor buck-boost

Advantages
• Single inductor / high power density
• Operates in buck mode at high $V_{IN}$
• Sync rectification – no diode drops
• Lower voltage SW2 FETs ($V_{OUT}$)

Disadvantages
• Limited choice of controllers
• Challenging PCB layout
• Single control loop for buck and boost
# Buck-boost solutions

<table>
<thead>
<tr>
<th>Boost + buck</th>
<th>SEPIC &amp; Zeta</th>
<th>Flyback ( (N_T = N_P/N_S) )</th>
<th>2-Sw buck-boost</th>
<th>4-Sw buck-boost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max ( V_{SW} )</td>
<td>SW1, SW2: ( V \downarrow \text{IN} )</td>
<td>( V \downarrow \text{IN} + V \downarrow \text{OUT} )</td>
<td>SW1: ( V \downarrow \text{IN} )</td>
<td>SW1: ( V \downarrow \text{IN} )</td>
</tr>
<tr>
<td>Max ( I_{SW} )</td>
<td>( I_{OUT}(VOUT/VIN) )</td>
<td>( I_{IN} + I_{OUT} )</td>
<td>( I_{IN}(1+NS/NP \text{VIN}/V \downarrow \text{OUT}) )</td>
<td>( I_{IN} + I_{OUT} )</td>
</tr>
<tr>
<td>( I_{L1} )</td>
<td>( I_{OUT}(VOUT/VIN) )</td>
<td>( I_{OUT}(VOUT/VIN) )</td>
<td>( I_{OUT}(VOUT/VIN + NS/NP) )</td>
<td>( I_{OUT}(VOUT/VIN + 1) )</td>
</tr>
<tr>
<td>( I_{L2} )</td>
<td>( I_{OUT} )</td>
<td>( I_{OUT} )</td>
<td>( I_{OUT}(1+NS/NP VOUT/V \downarrow \text{IN}) )</td>
<td>–</td>
</tr>
</tbody>
</table>

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Buck-boost DC/DC converter progression

- **2-Sw buck-boost**
  - < 25 W
  - ~90% efficiency

- **Flyback, SEPIC or Zeta**
  - < 40 W
  - ~90% efficiency

- **Sync flyback, SEPIC or Zeta**
  - < 100 W
  - ~93% efficiency

- **4-Sw buck-boost**
  - 25 W – 200 W
  - > 95% efficiency

Higher power and efficiency
4-switch buck-boost converter power stage
Current-mode control: peak boost and valley buck
Buck-boost mode transitions

- Buck FET off-time < 250 ns ⇒ transition mode
- Boost FET on-time < 250 ns ⇒ transition mode
- Timer hysteresis eliminates chatter at boundary

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4-switch buck-boost design example

<table>
<thead>
<tr>
<th>Design parameters</th>
<th>Target specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range, $V_{IN\text{(min)}}$–$V_{IN\text{(max)}}$</td>
<td>6 V–42 V</td>
</tr>
<tr>
<td>Output voltage, $V_{OUT}$</td>
<td>12 V</td>
</tr>
<tr>
<td>Maximum load current, $I_{OUT\text{(max)}}$</td>
<td>6 A</td>
</tr>
<tr>
<td>Switching frequency, $F_{SW}$</td>
<td>300 kHz</td>
</tr>
<tr>
<td>Operating mode</td>
<td>CCM, hiccup-mode OCP</td>
</tr>
</tbody>
</table>
Inductor selection

Inductance selection is based on
1. Target peak-to-peak ripple current
2. RMS and saturation current ratings
3. Size / cost

Set ripple current ratios in deep boost operating points at 20-40%:

\[ L_{\text{BOOST}} = \frac{V_{\text{IN(min)}}^2 (V_{\text{OUT}} - V_{\text{IN(min)}})}{0.2 \times I_{\text{OUT(max)}} F_{\text{sw}} V_{\text{OUT}}^2} = 4.2 \mu\text{H} \]

Inductor sat current rating:

\[ I_{\text{L(SAT)}} \geq 1.5 \times \left( \frac{V_{\text{OUT}} \times I_{\text{OUT(MAX)}}}{0.9 \times V_{\text{IN(MIN)}}} + \frac{\Delta I_{\text{L}}}{2} \right) = 21.6 \text{A} \]

<table>
<thead>
<tr>
<th>VIN</th>
<th>ΔIL1</th>
</tr>
</thead>
<tbody>
<tr>
<td>6 V</td>
<td>2.1 A</td>
</tr>
<tr>
<td>24 V</td>
<td>4.3 A</td>
</tr>
<tr>
<td>42 V</td>
<td>6.1 A</td>
</tr>
</tbody>
</table>

Select L1 = 4.7\mu\text{H}
**C\text{OUT}** selection

Maximum RMS current in C\text{OUT} occurs in boost mode

\[ I_{\text{COUT}(\text{rms})} = I_{\text{OUT}} \sqrt{\frac{V_{\text{OUT}}}{V_{\text{IN}}}} - 1 = 6\, \text{A} \]

\( V_{\text{OUT}} \) ripple: related to ESR

\[ \Delta V_{\text{RIPPLE(ESR)}} = I_{\text{OUT}} \frac{V_{\text{OUT}}}{V_{\text{IN(min)}}} \text{ESR} \]

ESR (5 mΩ) → 60 mV

\( V_{\text{OUT}} \) ripple: related to C\text{OUT}

\[ \Delta V_{\text{RIPPLE(C\text{OUT})}} = I_{\text{OUT}} D_{\text{boost}} \frac{D_{\text{sw}}}{C_{\text{OUT}}} \]

C\text{OUT} (330μF) → 30mV

Use a combination of ceramic and bulk caps to achieve RMS current rating, ESR & C\text{OUT}

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**C\textsubscript{IN} selection**

Maximum RMS current flowing in C\textsubscript{IN} occurs in buck mode

\[ I_{\text{CIN(rms)}} = I_{\text{OUT}} \sqrt{D(1-D)} = 3A \]

\( I_{\text{IN}} \) ripple: related to ESR

\[ \Delta V_{\text{RIPPLE(ESR)}} = I_{\text{OUT}} \cdot \text{ESR} \]

ESR (25m\( \Omega \)) \( \rightarrow \) 150mV

\( I_{\text{IN}} \) ripple: related to C\textsubscript{IN}

\[ \Delta V_{\text{RIPPLE(CIN)}} = \frac{I_{\text{OUT}} D_{\text{buck}} (1 - D_{\text{buck}})}{C_{\text{IN}} F_{\text{sw}}} \]

C\textsubscript{IN} (68\( \mu \)F) \( \rightarrow \) 75mV

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**Slope capacitance, $C_{\text{SLOPE}}$**

**Peak current-mode boost**

For ideal adaptive slope compensation, select

$$C_{\text{SLOPE}} = \frac{L_1}{g_{m(slope)} R_{\text{SENSE}} A_{\text{CS}}}$$

$$= 2\mu\text{s} \times \frac{4.7\mu\text{H}}{8\text{m}\Omega \times 5} = 235\text{pF}$$

Select a slope cap of 100 pF to 2x calculated above.

Lower $C_{\text{SLOPE}}$ recommended for noise immunity.

<table>
<thead>
<tr>
<th>$S_n$</th>
<th>$V_{\text{in}}$</th>
<th>$V_{\text{out}}$</th>
<th>$S_e$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\frac{V_{\text{in}} - V_{\text{out}}}{L}$</td>
<td>$S_f$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\frac{V_{\text{out}}}{L}$</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

$C_{\text{SLOPE}} = 100 \text{pF}$
Converter small-signal model

Load pole

\[
 f_{p1(\text{boost})} = \frac{1}{2\pi} \left( \frac{2}{R_{\text{OUT}}C_{\text{OUT}}} \right) = 398\text{Hz} 
\]

ESR zero

\[
 f_{z1} = \frac{1}{2\pi} \left( \frac{1}{R_{\text{ESR}}C_{\text{OUT}}} \right) = 79.6\text{kHz} 
\]

RHP zero

\[
 f_{z\text{RHP}} = \frac{1}{2\pi} \left( \frac{R_{\text{OUT}} \left( 1 - D_{\text{Boost(max)}} \right)^2}{L1} \right) = 16.9\text{kHz} 
\]

\[
 f_{p1(\text{buck})} = \frac{1}{2\pi} \left( \frac{1}{R_{\text{OUT}}C_{\text{OUT}}} \right) = 199\text{Hz} 
\]

Target crossover frequency

\[
 F_c = 4\text{kHz} 
\]
Control loop compensation

\[ f_{zc} = 1\text{kHz} \]

\[ R_{c1} = \frac{2\pi f_c}{g_{m_{EA}}} \times \frac{R_{FB1} + R_{FB2}}{R_{FB1}} \times \frac{A_{CS} R_{SENSE} C_{OUT}}{1 - D_{\text{max}}} = 10.9\Omega \]

\[ C_{c1} = \frac{1}{2\pi f_{zc} R_{c1}} = 15.9\text{nF} \]

\[ C_{c2} = \frac{1}{2\pi f_{zESR} R_{c1}} = 106\text{pF} \]

\[ A_{CS} = 5 \text{ (current sense gain)} \]

Also provides \( f_{sw} \) noise suppression
Control loop results

### Boost-mode

**Bode Plot, \( V_{\text{in}} = 6V \)**

- Crossover Frequency = 2.8 kHz
- Phase Margin = 63°

### Buck-mode

**Bode Plot, \( V_{\text{in}} = 18V \)**

- Crossover Frequency = 3.5 kHz
- Phase Margin = 71°
Reference schematic

LM5175

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Identify high di/dt and dv/dt, noise-sensitive traces
4-switch buck-boost converter “hot” loops

Minimizing Power Loop and Gate Loop parasitic inductances is very important. Both $C_{\text{IN}}$ and $C_{\text{OUT}}$ must be carefully placed in the PCB layout.
Top layer power stage routing

1. Place input caps close to buck leg MOSFETs
2. Place output caps close to boost leg MOSFETs
3. Keep shunt close to FETs for tight loop layout
4. VIN and VOUT planes provide heatsinking for high-side FETs
Bottom layer power stage and controller routing

1. Connect PGND and AGND at DAP
2. Locate VCC and BOOT caps close to IC
3. Separate GND island for small-signal components
4. Current sense filter close to IC
Layer 2: Solid GND plane; Layer 3: gate drives

SW1 copper & vias (8 mil $\phi$)

GND vias (15 mil $\phi$)

SW2 copper & vias (8 mil $\phi$)

GND vias (8 mil $\phi$)

Vias for Q1 gate resistor

Q1 gate drive traces routed differentially (20 mil width)

Q1 source vias (8 mil $\phi$)

Thermal vias (8 mil $\phi$) under IC for heatsinking & GND plane connection

Q3 gate via (15 mil $\phi$)

Q3 gate drive traces routed differentially (20 mil width)
Layers 4 & 5: Current sense and gate drives

- **Vias for Kelvin current sensing**
- **Q4 gate drive trace (20 mil width)**
- **Current sense traces routed differentially**
- **Vias for Q4 gate resistor**
- **VIN sense trace surrounded by GND copper**
- **Q2 gate drive trace (20 mil width) & gate via (15 mil $\Phi$)**
- **Direct path to GND terminal**
- **VOUT sense trace surrounded by GND copper**
Summary

• Buck-boost applications with step-up / step down conversion appear in many end-markets.

• Several topologies to choose from for buck-boost conversion.
  o Best fit chosen based on power level, efficiency, solution size and cost goals

• Single-inductor solutions dominate when high efficiency and output power are needed
  o 4-switch buck-boost reduces rectifier losses over entire operating range
  o Transition region switching losses are reduced when controller alternates between buck mode and boost mode.

• Application design example provided a working solution for a 12 V / 72 W converter with wide 6 V to 42 V input range.

• PC board layout design begins with identification of high dv/dt nodes and high di/dt loops. Best performance is achieved when current loops are short and sensitive nodes are spaced well away from noise generating traces.
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