Design review of a 2-kW parallelable power supply module

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Design review of a 2 kW parallelable power supply module

Roberto Scibilia
Agenda

• Introduction

• Topology selection:
  o First stage: PFC, single phase, or interleaved?
  o Second stage: Half-bridge, resonant LLC or full-bridge phase shift?

• Module design
  o EMI filter, PFC and auxiliary power supply
  o Input AC voltage sensing
  o Full-bridge, phase-shift resonant
  o Microcontroller

• Digital parallel: using CAN bus (non-standard) to perform parallel and data interchange

• Test data on 2 kW battery charger module
Typical power module applications

- Electric forklift
- Telecom modules with redundancy
- GEL battery
- Lead-acid battery

Diagram showing the supply and charging cycles for different applications.
Power supply or battery charger?

• The module can be generic power supply or customized as battery charger

• Typical application:
  o Telecom power supply with redundancy
  o Battery chargers for forklift
  o Battery chargers for electric vehicles

• After specializing the module as battery charger, new functions are needed:
  o Hot swap for overcurrent protection
  o Reverse polarity protection
  o Charging profile implementation
Specifications

- Nominal input AC voltage: 230 VAC
- Working AC voltage: 90 VAC…265VAC
- Output voltage: 20 V…32 V @ 62.5 A
- Harmonic limits: EN61000-3-2 Class A
- Output power: 2 kW @ 230 VAC
- Input current limit: 10 A
- Minimum plug-to-plug efficiency: 90% (design to cost – better than “80 Plus Silver”)
- User interface: LCD display, 4 pushbuttons
- Modularity: Parallel with master/slave architecture
- Parallel function: Analog or digital, CAN (non-standard) communications bus
- Settable parameters: Output voltage and current levels, input AC UVLO and OVP, reverse OVP, output short, OTP, master/slave configuration (up to 1 master and 9 slaves)
## Modules / chargers available today

<table>
<thead>
<tr>
<th>Model</th>
<th>Power</th>
<th>$V_{IN}$ Range</th>
<th>Efficiency</th>
<th>Power Density</th>
<th>Cooling</th>
<th>Human Interface</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>720 W at $T_{AMB} &lt; 40^\circ$C</td>
<td>Universal and extended</td>
<td>&gt;85%</td>
<td>106 W / cm³</td>
<td>Temperature controlled fan</td>
<td>Status light-emitting diode (LED)</td>
</tr>
<tr>
<td>B</td>
<td>1 kW</td>
<td>High Line (184 VAC…275VAC)</td>
<td>96% peak</td>
<td>78.7 W / cm³</td>
<td>Natural convection</td>
<td>Charging status indication (LED)</td>
</tr>
<tr>
<td>C</td>
<td>3 kW</td>
<td>High Line (184 VAC…275VAC)</td>
<td>94% peak</td>
<td>116 W / cm³</td>
<td>Forced convection</td>
<td>Charging status indication (LED)</td>
</tr>
<tr>
<td>TI prototype</td>
<td>2 kW at $T_{AMB} &lt; 80^\circ$C</td>
<td>Universal with derating</td>
<td>&gt; 91%</td>
<td>86.8 W / cm³</td>
<td>Variable-speed fan</td>
<td>LCD Pushbuttons</td>
</tr>
</tbody>
</table>
Block diagram

- **EM filter & rectifier**
- **PFC power stage**
- **Full-bridge, phase-shift DC/DC converter**
- **Synchr. rectifier**
- **Output filter**
- **Pre-charging thermistor**
- **Back-to-back E-switch**
- **Battery**
- **VAC input**
- **PFC-out**
- **Rsense**
- **Voltage loop**
- **Current loop**
- **Voltage ref**
- **Current ref**
- **PFC enable**
- **Microcontroller**
- **LDC display**
- **4 pushbuttons**
- **Temperature sensor**
- **Auxiliary flyback**

- **0…32 V @ 62.5 A**
PFC CCM boost: interleaved or single-phase?

**Interleaving advantages**
- Reduced high-frequency current ripple
- Easy EMI filtering
- Easier scalability to higher power
- Low profile possible
- More efficient thermal dissipation

**Single-phase advantages**
- Low overall cost solution thanks to reduced component count
- No current share problems
- Low-cost controller
DC/DC topology selection

Switch driving method

- Half-bridge $\rightarrow$ PWM ($D = 0\ldots50\%$)
- PS FB $\rightarrow$ $D = 50\%, 0..180^\circ$ phase-shift
- LLC $\rightarrow$ $D = 50\%$, frequency modulated
DC/DC topology selection

Half-bridge, switch current

- $I_{SW1} = 11.4A$
- $I_{SW2} = 13A$
- $I_{INPUT} = 5.49A$
- $D = 45\%$

Full-bridge, switch current

- $I_{SW1} = 5.7A$
- $I_{SW2} = 6.5A$
- $I_{INPUT} = 5.49A$
- $D = 45\%$

Low $V_{OUT} \rightarrow$ low gain $\rightarrow$ high $F_{SW}$

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## Auxiliary power supply alternatives

<table>
<thead>
<tr>
<th>Modulation Type</th>
<th>Good standby power</th>
<th>Low cost</th>
<th>Opto-less</th>
<th>Overload protection</th>
<th>Good Eff.</th>
<th>Good V&lt;sub&gt;OUT&lt;/sub&gt; regulation</th>
<th>Good transient response</th>
<th>EMI</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quasi-resonant w/PSR</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>~</td>
<td>~</td>
<td>✓</td>
</tr>
<tr>
<td>Quasi-resonant w/optocoupler &amp; depl. mode FET</td>
<td>✓</td>
<td>~</td>
<td>X</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Constant switching frequency + optocoupler</td>
<td>~</td>
<td>~</td>
<td>X</td>
<td>X</td>
<td>~</td>
<td>✓</td>
<td>✓</td>
<td>~</td>
</tr>
</tbody>
</table>

✓ = Yes, X = No, ~ = average performance

Chose quasi-resonant w/optocoupler for best regulation, efficiency and standby performance.
Block design: EMI filter

- Different L3 and L4 to avoid noise peaking (resonance)
- RT1 NTC is shorted by means of Relay
- Start with L4 arbitrary 1 mH; rate @ maximum input current
- Differential LC filter: leverage L4 leakage inductance (~1%)
- Main differential filter defined by C7, L4 and C12 // C11 (class X2)
- Class-Y capacitors needed for high-frequency and CM noise (C2, C3, C13, C14)
Block design: EMI filter, differential-mode

- $C_7 = 1.54 \mu F$ (use $2.2 \mu F$) by:
  - Allowing 30% inductor current ripple
  - Using 1% $C_7$ voltage ripple

- Greatest ripple current:
  - @ $D=50\% \rightarrow I_r = 4.58 \text{ Apk-pk}$

- Both 1 Vpk square and triangular wave → use only 3rd-harmonic to select filter
  \[
  I_{3H} = \frac{8 \cdot \left( \frac{I_{pp}}{2} \right)}{9 \cdot \pi^2} = 0.206 \text{ A}
  \]

\[
\frac{4V_r}{nT} = 1^{st} \text{ harmonic, square wave } = 122\text{dBuV}
\]
\[
\frac{8V_r}{(nT)^2} = 1^{st} \text{ harmonic, triangular wave } = 118\text{dBuV}
\]

\[
V_r = V\text{ ripple } = 1\text{Vpk}
\]
Block design: EMI filter, differential-mode (cont.)

\[ V_{C7} = I_{3H} \cdot \frac{1}{2 \cdot \pi \cdot (3 \cdot F_{SW}) \cdot C7} = 38 \text{ mV} \]

- \( V_{C7} \) ripple is sinusoidal ~ 92 dBuV
- Voltage sent to receiver: \( V_{Cx} / 2 \)
- Add 3 dBuV margin

\[ \text{Att} = V_{C7}(dB) - \text{Limit}(QP) + \text{Margin} = 36.6 \text{ dB} \]

\[ \text{Limit}(QP) = \text{Quasi-peak CISPR22 limit @ 390 KHz} = 58 \text{ dbuV} \]

- Corner frequency \( F_c \) defined by \( L_s \) and \( C_x \):

\[ F_c = 10^{\frac{-\text{Att}}{40}} \cdot F_{3H} = 47.4 \text{ KHz} \]

\[ C_x = \frac{1}{8 \cdot \pi^2 \cdot L_s \cdot (F_c)^2} = 563 \text{ nF} \]

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Block design: PFC boost

- Hard-switching and CCM:
  - SiC needed
- D1 avoids surge through SiC diode
- 2 FETs in parallel:
  - Spread the heat
  - Use cheaper components
- 4 Al-E caps benefit 100 Hz / 120 Hz ripple and transient response
Block design: inductor value

- Inductor ripple current = 30% @ D=50%
  \( V_{IN(pfc)} = V_{OUT(pfc)}/2 \)
  \[
  L_1 = \frac{V_{OUT(pfc)} \cdot (1 - D) \cdot D}{\Delta I \cdot F_{SW}} = 168 \, \mu H
  \]

- Inductor to support 16 A (peak) and 10 A (RMS)

\[
I_{SW} = K_1 \cdot \sqrt{1 - K_2 \cdot K_3} = 6.9 \, A
\]

\[
I_{D2} = K_1 \cdot \sqrt{K_2 \cdot K_3} = 8.3 \, A
\]

\[
I_c = \frac{P_{OUT(pfc)}}{V_{OUT(pfc)}} \cdot \sqrt{\frac{K_2}{K_3}} - 1 = 6.1 \, A
\]

\[
K_1 = \frac{P_{OUT(pfc)}}{\eta \cdot V_{IN(pfc, \min)}}
\]

\[
K_2 = \frac{8 \cdot \sqrt{2}}{3 \cdot \pi}
\]

\[
K_3 = \frac{V_{IN(pfc, \min)}}{V_{OUT(pfc)}}
\]
Block design: component stress analysis

- Swinging inductor improves EMI and keeps high L
- Allow 0.2% conduction losses
- FET → $R_{DS_{ON}} = 125 \text{ m}\Omega$, 650 V, $C_{OSS} = 53 \text{ pF}$
- Total FET losses → 4.14 W per FET
- SiC → $V_{TH} = 1 \text{ V}$, $Z_D = 0.05 \text{ Ohm}$

\[
R_{DS_{ON}(EQ)} = \frac{2}{1000} \frac{P_{OUT}(pf\text{c})}{\eta \cdot (I_{SW})^2} = 0.087 \Omega
\]

\[
P_{COND(EQ)} = \frac{R_{DS_{ON}(EQ)}}{2} \cdot (I_{SW})^2 = 3.02 \text{ W}
\]

\[
P_{CROSS(EQ)} = \frac{1}{2} \cdot (2 \cdot COSS) \cdot (V_{OUT}(pf\text{c}))^2 \cdot F_{SW} = 1.1 \text{ W}
\]

\[
P_{SW(EQ)} = \frac{1}{2} \cdot V_{OUT}(pf\text{c}) \cdot I_{SW} \cdot (T_R + T_F) \cdot F_{SW} = 4.16 \text{ W}
\]

\[
P(EQ) = P_{COND(EQ)} + P_{CROSS(EQ)} + P_{SW(EQ)} = 8.28 \text{ W}
\]

\[
P_{D2} = V_{TH} \cdot I_{OUT}(pf\text{c}) + Z_D \cdot (I_{D2})^2 = 8.46 \text{ W}
\]
Block design: output bulk capacitor

- Output capacitance supports both hold-up time and RMS current:

\[
C_{OUT}(pfc) = \frac{2 \cdot P_{OUT}(pfc) \cdot T_{HOLD}}{(V_{OUT}(pfc, nom))^2 - (V_{OUT}(pfc, nom) - V_{DROP})^2} = 1.08 \cdot 10^3 \mu F
\]

- Choose ~1300 uF (+ 20% due to tolerance) \(\rightarrow\) select 4 x 330 uF
- Each capacitor should support \(I_{RMS} \geq 1.53 A_{RMS}\) (6.11 A / 4)
- Also check peak-peak ripple voltage @ \(F_{LINE} = 47\) Hz:

\[
V_{RIPPLE}(pfc) = \frac{I_{OUT}(pfc)}{2 \cdot \pi \cdot 2 \cdot F_{LINE} \cdot C_{OUT}(pfc)} = 7.9 V
\]

**DONE! Less than ± 2%**

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Block design: auxiliary power supply

- Nominal power consumption: $P_{\text{NOM}} = 8.5 \, \text{W} \rightarrow \text{design for 10 W}$
- Input voltage range $V_{\text{IN(AUX)}}$: $120 \, \text{V (85 Vac)} \ldots 400 \, \text{V}$
- Switching frequency range: $F_{\text{SW}} = 70 \, \text{kHz} \ldots 120 \, \text{kHz}$
- Select transformer turns ratio to keep $V_{\text{DS_MAX}} \leq 650 \, \text{V}$

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Block design: AC voltage-sensing

$V_{AC}$ measurement needed for:
- Input under-voltage and over-voltage protection
- Limit input current per digital calculation of $V_{OUT(fb)}$, $I_{OUT(fb)}$, $\eta$

Important: Decouple input AC current 50 Hz stray field from $I_1$ loop → it will affect the precision!

$V_{PK} \equiv I_{PK} \cdot R_B$

$0\ldots2\text{Vdc} \rightarrow 0\text{Vac}...300\text{Vac}$

$0V + 3V_{PK}/2$

$\eta \cdot V_{IN(pfc)} = \frac{P_{OUT(fb)}}{I_{IN(pfc)}}$
Block design: PSFB block diagram

- Back-to-back FETs block FET surge and reverse polarity
- CS Xfrm in series w/ bridge prevents x-cond.
  (Also imbalance due to circulating currents)
- Gate drive simplified by 50% D
- 0.2 mΩ shunt thanks to high-precision, low-offset op amp

0..32V DC @ 62.5A
Block design: PSFB circulating currents

$V_{\text{OUT}}(\text{PFC})$

Current loop flowing during:
$T_{\text{ON}} \rightarrow T_{\text{OFF}}$

Diagram showing the circuit layout with components labeled and the flow of current during $T_{\text{ON}}$ and $T_{\text{OFF}}$. The diagram includes components such as $Q_a$, $Q_b$, $Q_c$, $Q_d$, $Q_f$, $C_{\text{SS}}$, $C_{\text{OUT}}$, $L_{\text{OUT}}$, and others.
Block design: PSFB waveforms

- $I_{Qa}(\text{RMS}) \sim I_{Qc}(\text{RMS})$
- Set $(\Delta I_{\text{Out}}) = 20\%$, @ $V_{\text{IN}}(\text{fb,nom}) = 400$ V, $V_{\text{OUT}}(\text{fb,nom}) = 27$ V

$$L_{\text{OUT}} = \frac{V_{\text{OUT}}(\text{fb,nom}) \cdot (1 - D(\text{fb,nom}))}{\Delta I_{\text{OUT}} \cdot F_{\text{SW}}} = 3.7 \, \mu\text{H}$$

- "Leading" switch $Q_a$
- "Lagging" switch $Q_c$
- Sync switch $Q_e$ with overlap

$Q_e_{\text{RMS}}$ switch current: $I_{S_{\text{RMS}}} = 42.7 \, \text{A}$
Block design: PSFB main FET choice

- Select loss budget = 1% of $P_{OUT}$ on $Q_A$ through $Q_D \rightarrow P_{Q_A} = (0.25\% \text{ of } P_{OUT}) = 4.8\text{W}$

$$P_{Qa} = (I_{Qa}(RMS))^2 \cdot RDS_{ON}(Qa) + 2 \cdot Q_G(Qa) \cdot V_{GATE} \cdot \frac{F_{SW}(fb)}{2}$$

- Selected 4 x FETs, $RDS_{ON} = 0.19\ \Omega, \ 17\text{A}, \ 650\text{V}$ ($\geq V_{IN(fb,max)}$)
- Incorporates ultra-fast body diode: no spikes at light load (when ZVS is lost)
- $N = \text{Transformer turns ratio} = 9.5, \ V_{IN(fb,max)} = 440\ \text{V}$
- Sync. rectification $Q_e$ and $Q_f$ must withstand $V_{DS(Qe)}$ according to:

$$V_{DS(Qe)} = \frac{2 \cdot V_{IN(fb,max)}}{N_{PS(fb)}} \cdot 1.5 = 139\ \text{V} \quad (+50\% \text{ due to spikes})$$

Neglect $Q_G(Qa)$ (gate charge loss)

$R_{DS(ON)} \leq 0.21\ \Omega$
Block design: PSFB sync. FET choice

- Select 200 V FET, since we have 139 V clamped spike
- Loss (conduction) budget = 1% of $P_{OUT}$ on Qe and Qf → $P_{BUDGET}(Qe) = (0.5\% \text{ of } P_{OUT}) = 10 \text{ W}$
- Selected 4 x FETs, $RDS_{ON} = 10.5 \text{ m}\Omega$, 84A, 200 V
- Use 2 parallel FETs each for Qe and Qf

\[
RDS_{ON}(EQ) \leq \frac{P_{BUDGET}(Qe)}{(I_{Qe}(RMS))^2} = 5.5 \cdot 10^{-3} \Omega
\]

\[
P_{Qe} = (I_{Qe}(RMS))^2 \cdot RDS_{ON}(Qe) + \frac{P_{OUT}(fb)}{V_{OUT}(fb,\text{nom})} \cdot V_{DS}(Qe) \cdot T_F \cdot F_{SW}(fb) \cdot 2 + 2 \cdot COSS(Qe, \text{avg})
\]

\[
\cdot (V_{DS}(Qe))^2 \cdot \frac{F_{SW}(fb)}{2} + 2 \cdot Q_G(Qe) \cdot V_{GATE} \cdot F_{SW}(fb) = 25.2 \text{ W}
\]
Block design: PSFB resonant inductor

- \( E_{\text{STORE}} \) in \( L_S \) charges total \( C_{\text{OSS}} \) of one leg
- Achieve ZVS down to \( \text{Load}_{\text{MIN}} = 15\% \) of full load →

\[
L_S \geq 2 \cdot \text{COSS}(Qa, \text{avg}) \cdot \frac{(V_{IN}(fb, \text{nom}))^2}{\left[\text{LOAD}(\text{min}) \cdot \left(I_{PP} - \frac{\Delta I_{\text{OUT}}}{N_{PS}(fb)}\right)\right]^2} - L_{LK} = 1.13 \cdot 10^{-5} \text{H}
\]

- Where: \( L_{LK} = 3.5 \text{ uH} \) (0.1% of magnetizing inductance) → \( L_S = 10 \text{ } \mu\text{H} \)
- \( L_S \) RMS current and T1 primary current are the same (have only AC component)
- Select PQ20/20 platform with:
  - \( \Delta B_{PK} = 118 \text{ mT} \), 10 turns Litz wire (160x0.1 mm)
  - N97 EPCOS core, gap 0.77 mm, \( \mu_E = 57 \)
  - Results in copper losses = 0.63 W and core losses = 0.57 W
Block design: PSFB FET drive

- Select turns ratio of $T4 = 1:1$ to get $V_{DRIVE} = 12V$ (AF4779, $L_M = 0.9 \text{ mH}$)
- Add small $R_P (~2…3\Omega)$ to damp primary winding + $C_P = 1 \text{ uF}$ to remove DC comp.
- $C_{f1,2}$ hold $V_{DD} = +12 \text{ V}$ and $V_{EE} = -12 \text{ V}$ voltages during driving peaks (used 22 nF)
- $R_{d1,2}$ are needed to damp the oscillation on $V_{DD}$ & $V_{EE}$
- Select damping factor $\zeta$ in a range of 0.5…1

\[ \zeta := 0.5 \]

\[ \zeta = 0.4 \quad \zeta = 0.6 \quad \zeta = 1 \]

\[ Rd1 = 2 \cdot \zeta \cdot \frac{L_M(T4)}{Ch1} = 94.4\Omega \]

= minimum damping factor

$V_{DD}$

$V_{EE}$

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Block design: PSFB voltage and current loop

- DAC achieved by PWM-to-average → V-REF, I-REF
- Chosen Rfilt1 = 2 * Rfilt2 and Cfilt2 = 2 * Cfilt1 → same FCO
- By selecting FCO = 16 Hz, Rfilt1 = 100 K, Cfilt1 = 100 nF
- RBIAS2 biases current loop → zero current at startup
- 2 x PWM_REF come from μC timer channels
- If PWM_REF is in three-state condition → VOUT=0, IOUT=0
Block design: Leverage a microcontroller

Master-slave architecture

Sets and reads RPM

CAN bus and digital parallel

Reads input voltage

Microcontroller

Sets $V_{\text{OUT}}$ levels

Sets $I_{\text{OUT}}$ and current limit

Internal temperature reading
Block design: Choice of Microcontroller

• Slow voltage and current loops: no need of ultra-high speed microcontroller
• Microcontroller sets $V_{\text{OUT}}$, $I_{\text{OUT}}$, $P_{\text{OUT}}$ + managing all “slow” variables
• Functions:
  o Analog inputs (ADC channels): $V_{\text{OUT}}$, $I_{\text{OUT}}$, $V_{\text{IN-RMS}}$, $T_{\text{AMB}}$ → 4 x ADC
  o Analog outputs (PWM to analog): $V_{\text{OUT}}$ and $I_{\text{OUT}}$ REF → 2 x PWM
  o UART (CAN-bus hardware): Full-duplex → CAN RX & TX
  o General purpose I/O: → 28 GPIO
  o $V_{\text{OUT}}$ and $I_{\text{OUT}}$ precision: 100 ksp is sufficient, ±1% 10-bit ADC
  o $V_{\text{OUT}}$ and $I_{\text{OUT}}$ setting: $F_{\text{CLOCK}} = 16$ MHz and compare$_{FS} = 16000$, PWM = 1 kHz
  o No need for extra-low power consumption

• Selected MSP430F2252:
  o 16 KB + 256 B flash memory
  o 512 B RAM
Block design: Hot-swap + rev-polarity protection

- RT2 and RT3 limit current (PTC)
- Back to back FETs protect DC/DC power stage in all conditions
- Drev1, Drev2 and Rb2 protect Q9A and Q8 against reverse currents
- Current mirror Q9A, Q9B provide voltage-shifting
- “SW” switch node from a buck converter generates 13 V ($V_{FLOAT}$)
- Discrete solution selected due to high nominal current
Paralleling modules: UART with CAN bus interface

Why use digital bus
- Battery charger is “slow” system and digital communication is necessary anyway – hardware interface already implemented
- Fixed M/S assignment – master manages battery-charging, dictates current slaves supply. Slaves simply follow commands and deliver current.
- Only one loop is active – no multi-loop stability problems, nor further parallel loop to stabilize
Module functionality: alarms and warnings

<table>
<thead>
<tr>
<th>#</th>
<th>Alarm Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Mains too low</td>
</tr>
<tr>
<td>1</td>
<td>Mains overvoltage</td>
</tr>
<tr>
<td>2</td>
<td>Output overvoltage</td>
</tr>
<tr>
<td>3</td>
<td>Output shorted</td>
</tr>
<tr>
<td>4</td>
<td>Reverse polarity</td>
</tr>
<tr>
<td>5</td>
<td>Over temperature</td>
</tr>
<tr>
<td>6</td>
<td>Fan failure</td>
</tr>
<tr>
<td>7</td>
<td>DC/DC failure</td>
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<table>
<thead>
<tr>
<th>#</th>
<th>Warning Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Output current limit</td>
</tr>
<tr>
<td>1</td>
<td>Output power limit</td>
</tr>
<tr>
<td>2</td>
<td>Input current limit</td>
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<tr>
<td>3</td>
<td>Low battery voltage</td>
</tr>
<tr>
<td>4</td>
<td>Not used</td>
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<tr>
<td>5</td>
<td>Not used</td>
</tr>
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<td>6</td>
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</tr>
<tr>
<td>7</td>
<td>Not used</td>
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</tbody>
</table>

Module OFF

Normal operation; yellow LED ON
PMP8740 module

**FRONT PANEL**
- EMI Filter & inrush limit

**BACK PANEL**
- PFC
- Boost
- Bridge
- Back-to-back FETs
- Output inductor
- Sync. FETs
- Output caps
- Main transformer

**Main FETs and SiC diode on heatsink**

**Aux. power supply**

**μC**

**Dim: 125 x 170 x 290 mm**

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Test data @ 1.6 KW load (limit of the AC source)

Input voltage and current @ 90 Vac

Bridge voltage and sync. rectifier drain

Input voltage and current @ 230 Vac

PFC FET drain voltage
Module test data

PFC Power Stage Efficiency

DC/DC Power Stage Efficiency

Total Module Efficiency (plug to plug)
Summary

• Complete design of 2 kW module **PMP8740**

• Module employed in master-slave (M/S) architecture
  o Suits lead-acid and Li-Ion battery charging and redundant telecom apps

• In M/S configuration, firmware is open to
  o Master configuration + slave without display (single multi-kW module)
  o M/S architecture with paralleled modules, separable in different modules (one display + pushbuttons for each module)

• Two modules built and tested - parallel operation proven
  o ±1% unbalance

• Future developments
  o Automatic M/S assignment if the master fails: improved reliability
  o Three-phase connection architecture with (Y) and without neutral (Δ)
# TI Worldwide Technical Support

## Internet

**TI Semiconductor Product Information Center Home Page**
support.ti.com

**TI E2E™ Community Home Page**
e2e.ti.com

## Product Information Centers

### Americas

<table>
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<tr>
<th>Country</th>
<th>Phone</th>
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<td>0800-891-2616</td>
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<td>Mexico</td>
<td>0800-670-7544</td>
<td>1(972) 927-6377</td>
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### Europe, Middle East, and Africa

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<th>Phone</th>
<th>Fax</th>
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</thead>
<tbody>
<tr>
<td>Europe Free Call</td>
<td>00800-ASK-TEXAS (00800 275 83927)</td>
<td></td>
</tr>
<tr>
<td>International</td>
<td>+49 (0) 8161 80 2121</td>
<td></td>
</tr>
<tr>
<td>Russian Support</td>
<td>+7 (4) 95 98 10 701</td>
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</tbody>
</table>

**Note:** The European Free Call (Toll Free) number is not active in all countries. If you have technical difficulty calling the free call number, please use the international number above.

### Asia

<table>
<thead>
<tr>
<th>Country</th>
<th>Phone</th>
<th>Fax</th>
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<tr>
<td>Australia</td>
<td>1-800-999-084</td>
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<tr>
<td>China</td>
<td>800-820-8682</td>
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<tr>
<td>Hong Kong</td>
<td>800-96-5941</td>
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<tr>
<td>India</td>
<td>000-800-100-8888</td>
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<td>Indonesia</td>
<td>001-803-8861-1006</td>
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<tr>
<td>Korea</td>
<td>080-551-2804</td>
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<td>Malaysia</td>
<td>1-800-80-3973</td>
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<td>New Zealand</td>
<td>0800-446-934</td>
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<tr>
<td>Philippines</td>
<td>1-800-765-7404</td>
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<tr>
<td>Singapore</td>
<td>800-886-1028</td>
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<td>Taiwan</td>
<td>0800-006800</td>
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<td>Thailand</td>
<td>001-800-886-0010</td>
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**Note:** Toll-free numbers do not support mobile and IP phones.

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<table>
<thead>
<tr>
<th>Products</th>
<th>Applications</th>
<th>Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265</th>
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<td>Audio</td>
<td><a href="http://www.ti.com/audio">www.ti.com/audio</a></td>
<td>Copyright © 2016, Texas Instruments Incorporated</td>
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<td>Amplifiers</td>
<td>amplifier.ti.com</td>
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<tr>
<td>Data Converters</td>
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<tr>
<td>DLP® Products</td>
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<td>DSP</td>
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<td>Interface</td>
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