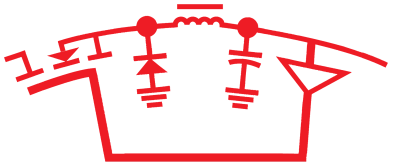

Power Supply Design Seminar

Design review of a 2-kW parallelable power supply module

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Texas Instruments

Design review of a 2 kW parallelable power supply module

Roberto Scibilia

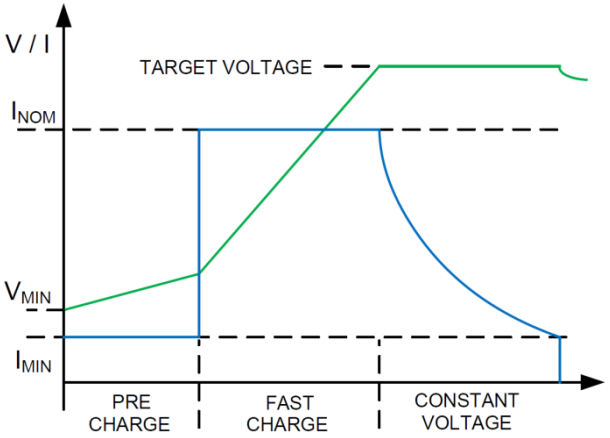
Agenda

- Introduction
- Topology selection:
  - First stage: PFC, single phase, or interleaved?
  - Second stage: Half-bridge, resonant LLC or full-bridge phase shift?
- Module design
  - EMI filter, PFC and auxiliary power supply
  - Input AC voltage sensing
  - Full-bridge, phase-shift resonant
  - Microcontroller
- Digital parallel: using CAN bus (non-standard) to perform parallel and data interchange
- Test data on 2 kW battery charger module

Typical power module applications

Electric forklift

Telecom modules with redundancy



GEL battery

Lead-acid battery

SUPPLYING

CHARGING

Power supply or battery charger?

- The module can be generic power supply or customized as battery charger
- Typical application:
  - Telecom power supply with redundancy
  - Battery chargers for forklift
  - Battery chargers for electric vehicles
- After specializing the module as battery charger, new functions are needed:
  - Hot swap for overcurrent protection
  - Reverse polarity protection
  - Charging profile implementation

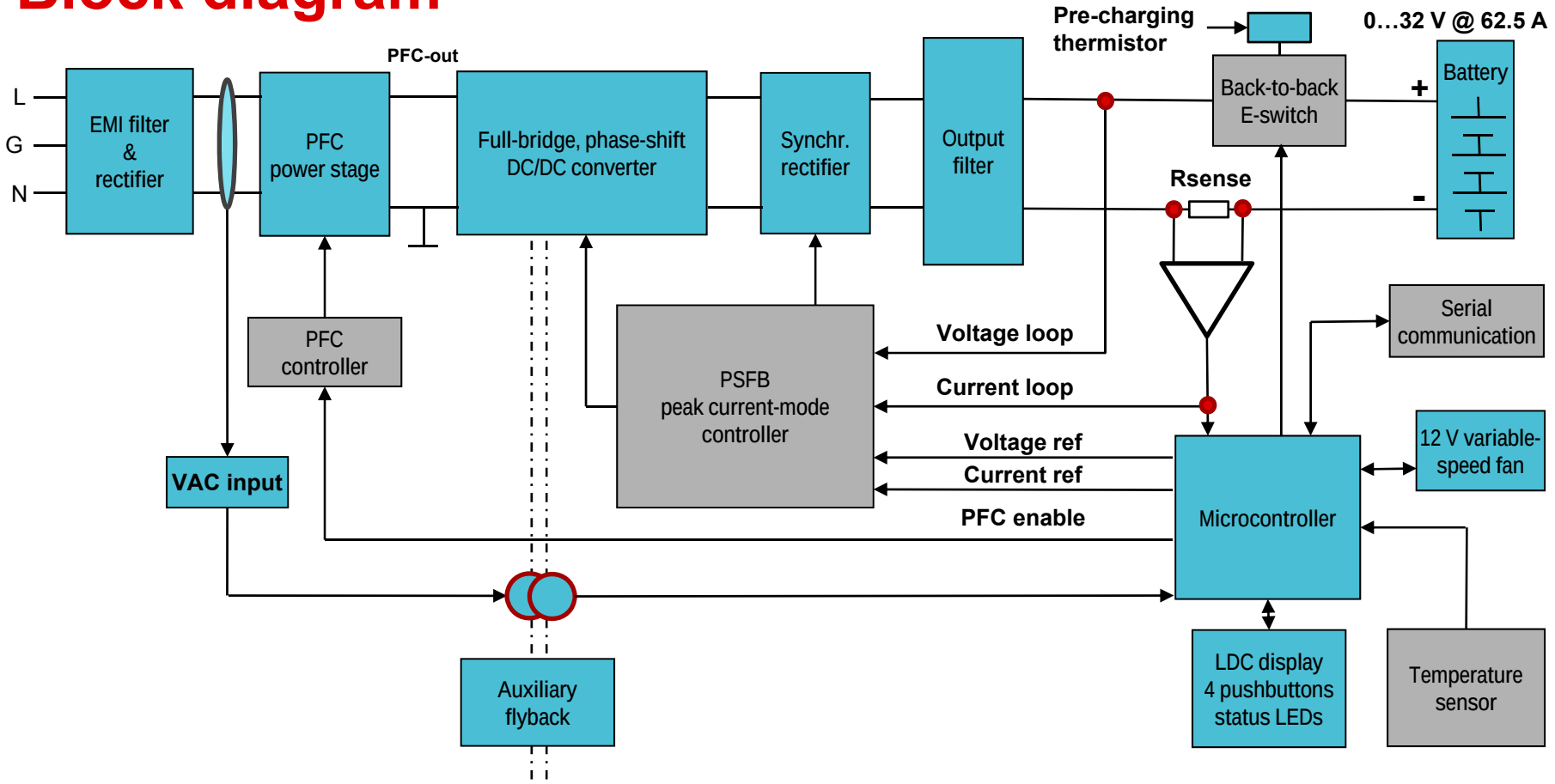
Specifications

- Nominal input AC voltage: 230 VAC
- Working AC voltage: 90 VAC…265VAC
- Output voltage: 20 V…32 V @ 62.5 A
- Harmonic limits: EN61000-3-2 Class A
- Output power: 2 kW @ 230 VAC
- Input current limit 10 A
- Minimum plug-to-plug efficiency: 90% (design to cost – better than “80 Plus Silver”)
- User interface: LCD display, 4 pushbuttons
- Modularity: Parallel with master/slave architecture
- Parallel function: Analog or digital, CAN (non-standard) communications bus
- Settable parameters: Output voltage and current levels, input AC UVLO and OVP, reverse OVP, output short, OTP, master/slave configuration (up to 1 master and 9 slaves)

Modules / chargers available today

Model	Power	V_{IN} Range	Efficiency	Power Density	Cooling	Human Interface
A	720 W at T_{AMB} < 40ºC	Universal and extended	>85%	106 W / cm^3	Temperature controlled fan	Status light-emitting diode (LED)
B	1 kW	High Line (184 VAC…275VAC)	96% peak	78.7 W / cm^3	Natural convection	Charging status indication (LED)
C	3 kW	High Line (184 VAC…275VAC)	94% peak	116 W / cm^3	Forced convection	Charging status indication (LED)
TI prototype	2 kW at T_{AMB} < 80ºC	Universal with derating	> 91% 93.5% peak	86.8 W / cm^3	Variable-speed fan	LCD Pushbuttons

Block diagram



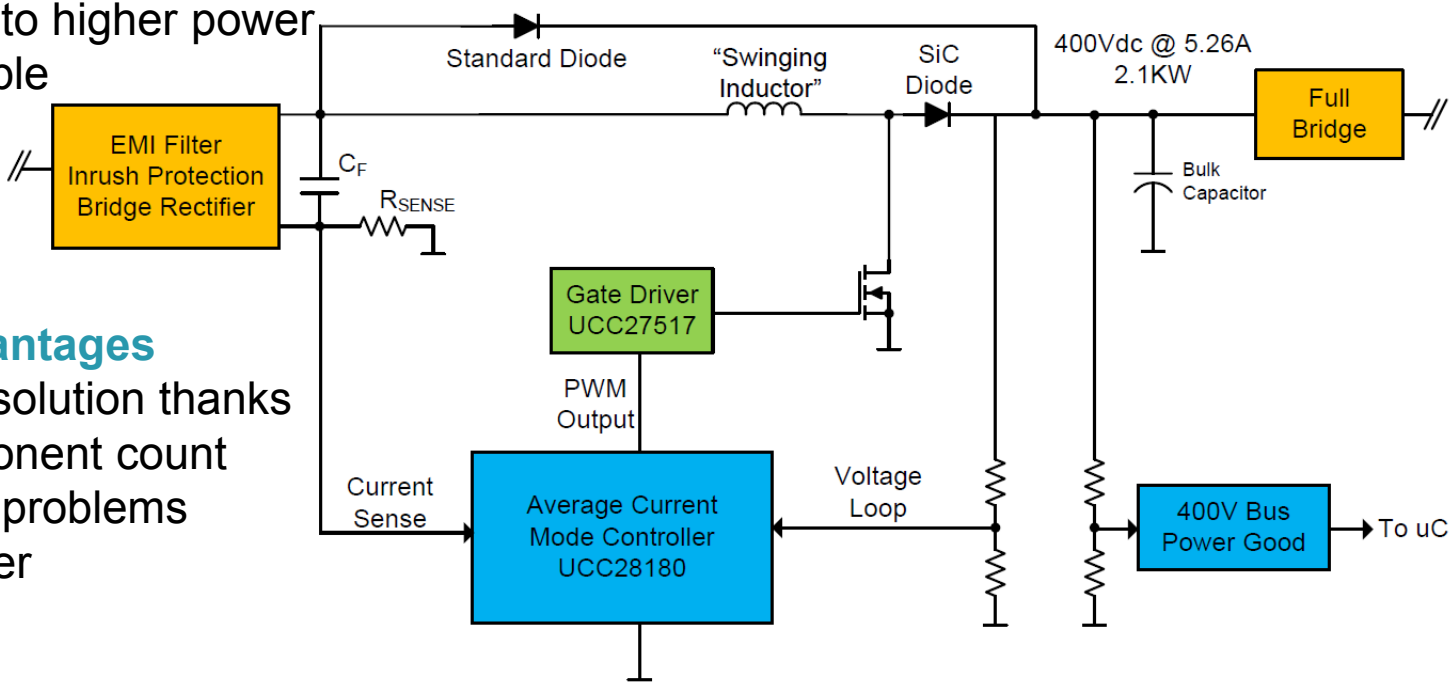
PFC CCM boost: interleaved or single-phase?

Interleaving advantages

- Reduced high-frequency current ripple
- Easy EMI filtering
- Easier scalability to higher power
- Low profile possible
- More efficient thermal dissipation

Single-phase advantages

- Low overall cost solution thanks to reduced component count
- No current share problems
- Low-cost controller

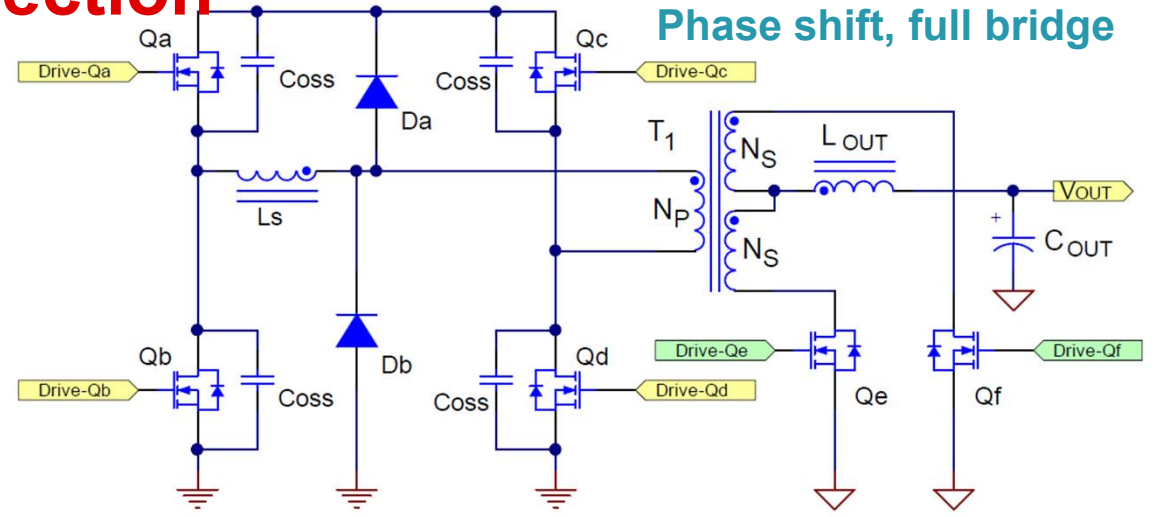


DC/DC topology selection

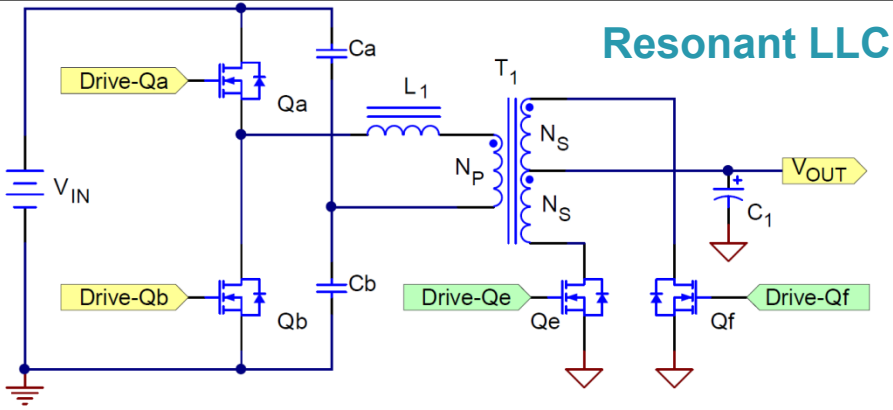
Switch driving method

- Half-bridge → PWM (D = 0…50%)
- PS FB → D = 50%, 0..180º phase-shift
- LLC → D = 50%, frequency modulated

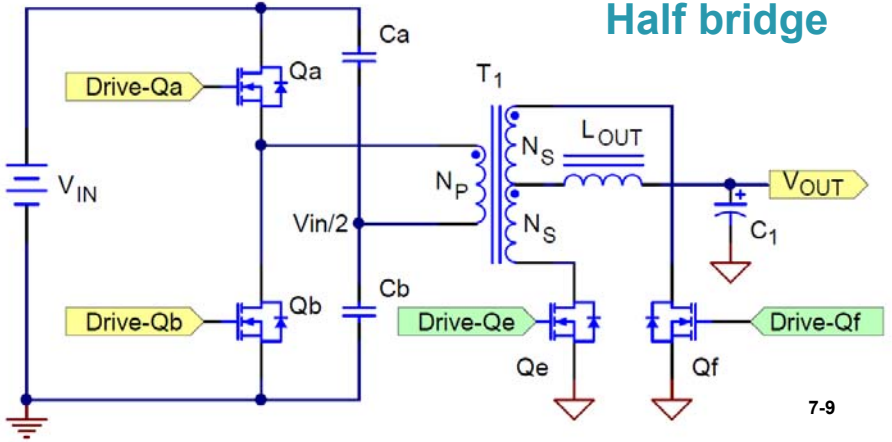
Phase shift, full bridge



Resonant LLC

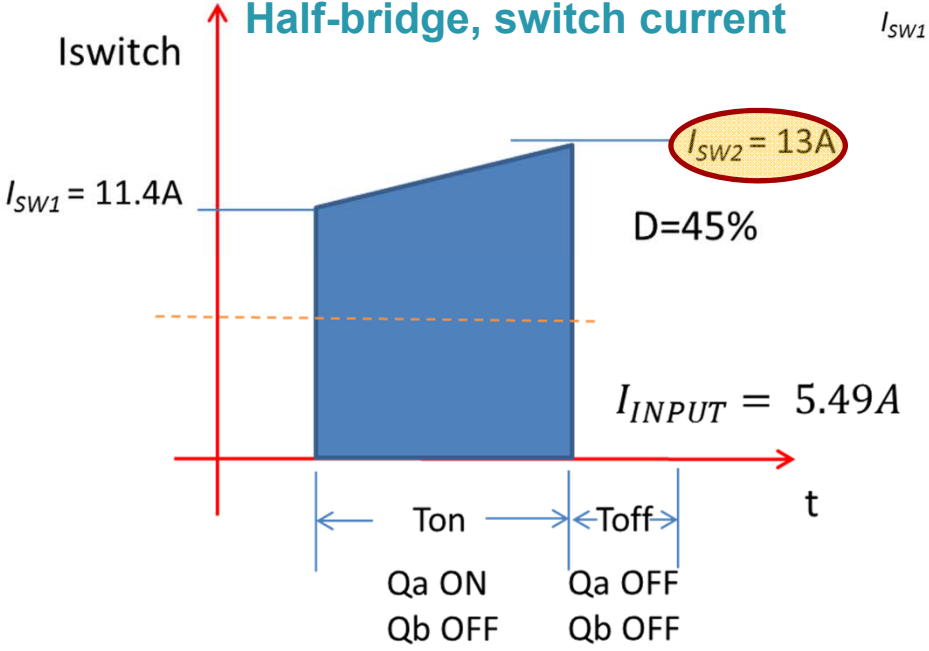


Half bridge



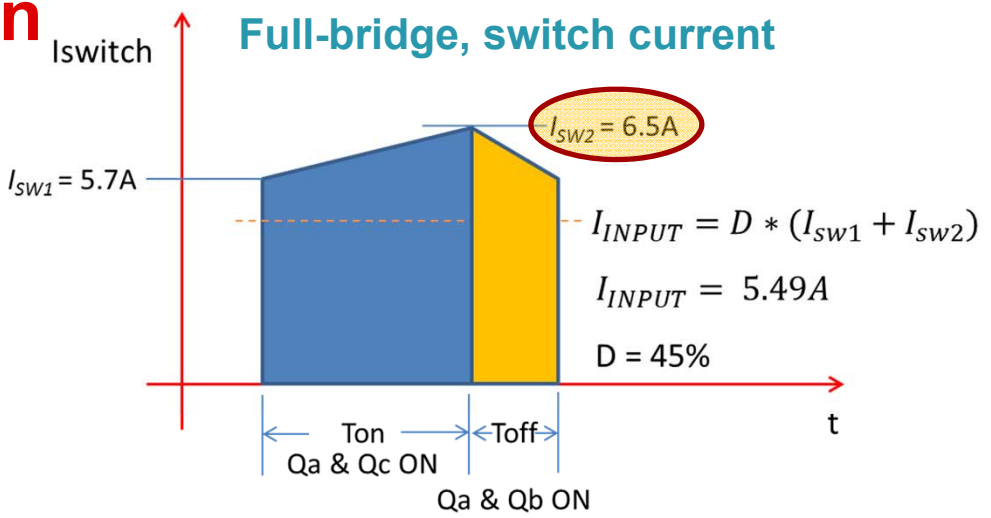
DC/DC topology selection

Half-bridge, switch current

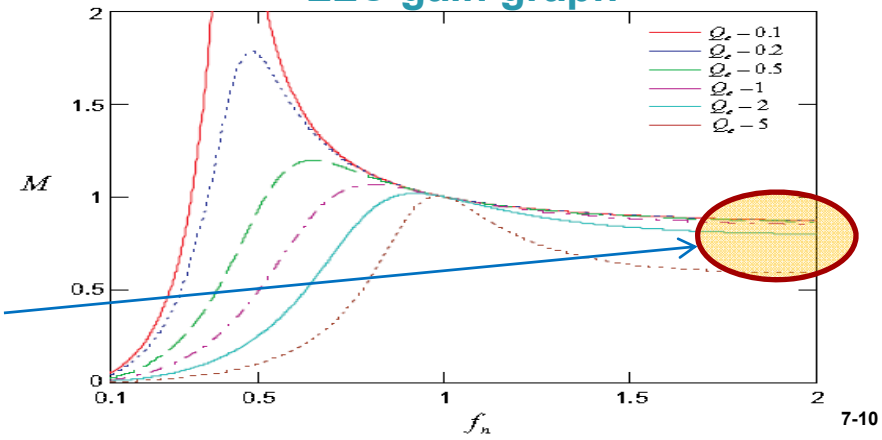


Low V_{OUT} → low gain → high F_{SW}

Full-bridge, switch current



LLC gain graph



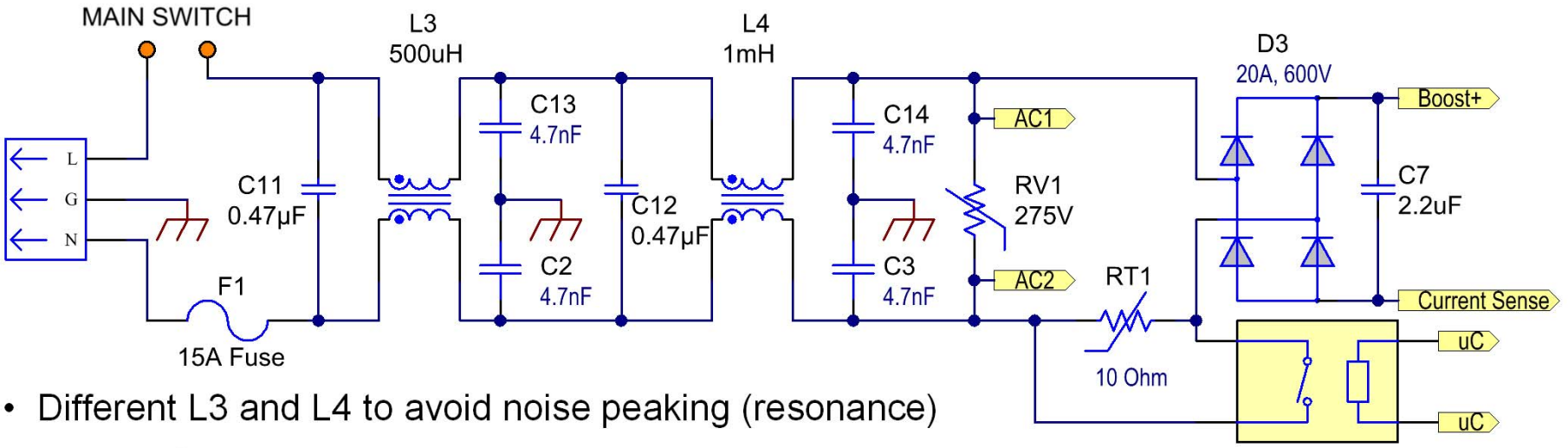
Auxiliary power supply alternatives

Modulation Type	Good standby power	Low cost	Opto-less	Overload protection	Good Eff.	Good V_{OUT} regulation	Good transient response	EMI
Quasi-resonant w/PSR	√	√	√	√	√	~	~	√
Quasi-resonant w/optocoupler & depl. mode FET	√	~	X	√	√	√	√	√
Constant switching frequency + optocoupler	~	~	X	X	~	√	√	~

√ = Yes, X = No, ~ = average performance

Chose quasi-resonant w/optocoupler for best regulation, efficiency and standby performance

Block design: EMI filter



- Different L3 and L4 to avoid noise peaking (resonance)
- RT1 NTC is shorted by means of Relay
- Start with L4 arbitrary 1 mH; rate @ maximum input current
- Differential LC filter: leverage L4 leakage inductance (~1%)
- Main differential filter defined by C7, L4 and C12 // C11 (class X2)
- Class-Y capacitors needed for high-frequency and CM noise (C2, C3, C13, C14)

Block design: EMI filter, differential-mode

- C7 = 1.54 uF (use 2.2 uF) by:
  - o Allowing 30% inductor current ripple
  - o Using 1% C7 voltage ripple
- Greatest ripple current:

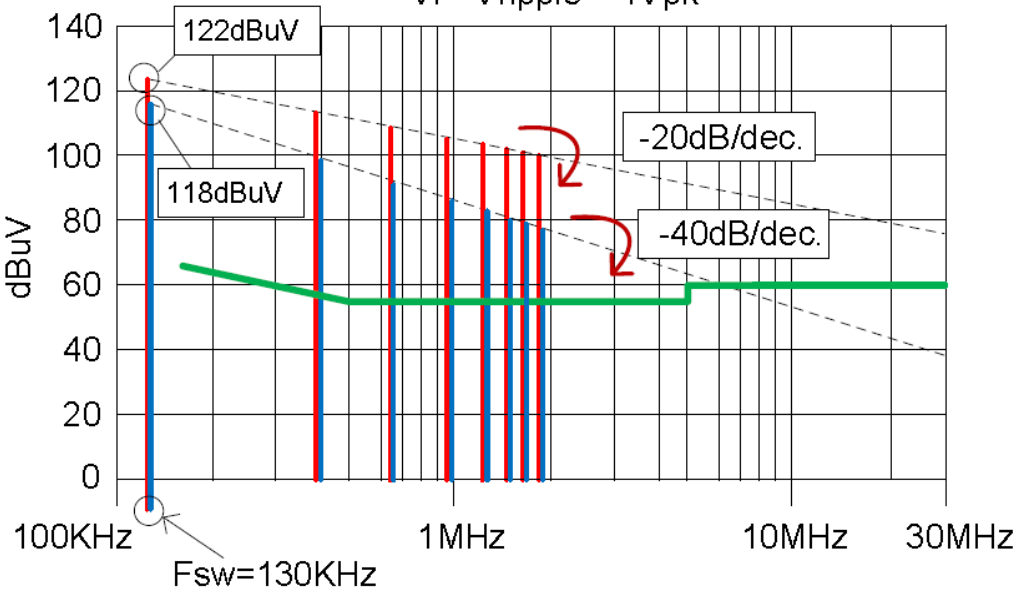
  @ D=50% →Ir = 4.58 Apk-pk
- Both 1 Vpk square and triangular wave → use only 3rd-harmonic to select filter

$$I_{3H} = \frac{8 \cdot (\frac{Ipp}{2})}{9 \cdot \pi^2} = 0.206\ A$$

$\frac{4Vr}{n\pi}$ = 1st harmonic, square wave = 122dBuV

$\frac{8Vr}{(n\pi)^2}$ = 1st harmonic, triangular wave = 118dBuV

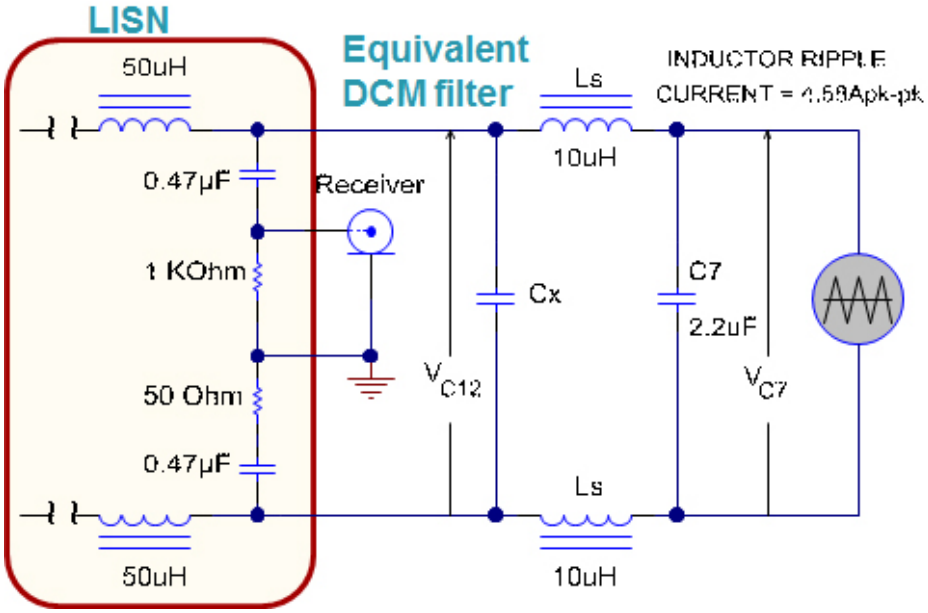
Vr= Vripple = 1Vpk



Block design: EMI filter, differential-mode *(cont.)*

$$V_{C7} = I_{3H} \cdot \frac{1}{2 \cdot \pi \cdot (3 \cdot F_{SW}) \cdot C7} = 38\,mV$$

- V_{C7} ripple is sinusoidal ~ 92 dBuV
- Voltage sent to receiver: V_{Cx} / 2
- Add 3 dBuV margin



$$Att = V_{C7}(dB) - Limit(QP) + Margin = 36.6\,dB$$

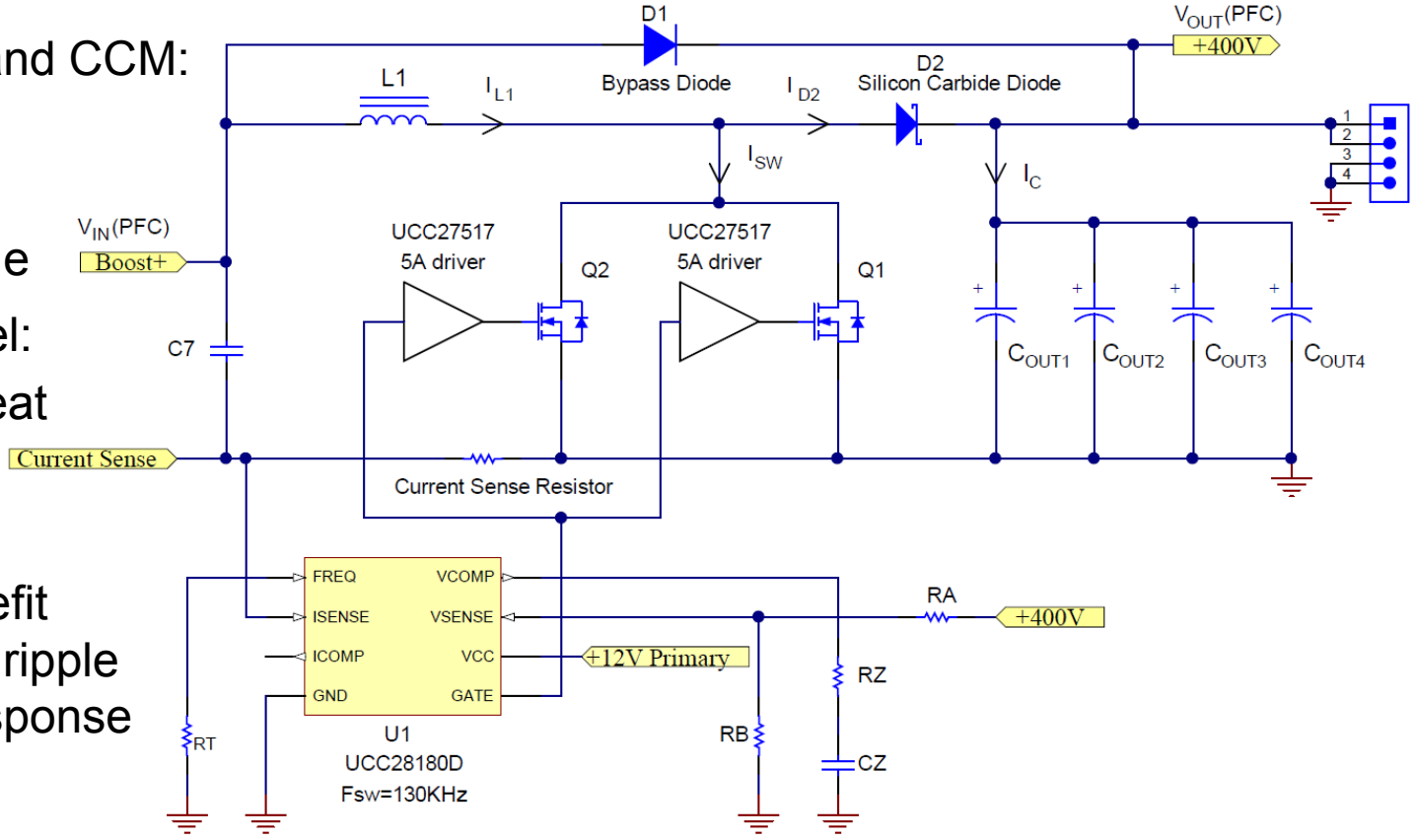
Limit(QP) = Quasi-peak CISPR22 limit @ 390 KHz = 58 dbuV

- Corner frequency Fc defined by Ls and Cx:

$$F_C = 10^{\frac{-Att}{40}} \cdot F_{3H} = 47.4\ \text{KHz} \qquad C_X = \frac{1}{8 \cdot \pi^2 \cdot L_S \cdot (F_C)^2} = 563\,\text{nF}$$

Block design: PFC boost

- Hard-switching and CCM:
  - o SiC needed
- D1 avoids surge through SiC diode
- 2 FETs in parallel:
  - o Spread the heat
  - o Use cheaper components
- 4 Al-E caps benefit 100 Hz / 120 Hz ripple and transient response



Block design: inductor value

- Inductor ripple current = 30% @ D=50%
  ($V_{IN}(pfc) = V_{OUT}(pfc)/2$)

$$L1 = \frac{V_{OUT}(pfc) \cdot (1 - D) \cdot D}{\Delta I \cdot F_{SW}} = 168\ \mu H$$

- Inductor to support 16 A (peak) and 10 A (RMS)

$$K_1 = \frac{P_{OUT}(pfc)}{\eta \cdot V_{IN}(pfc, min)}$$

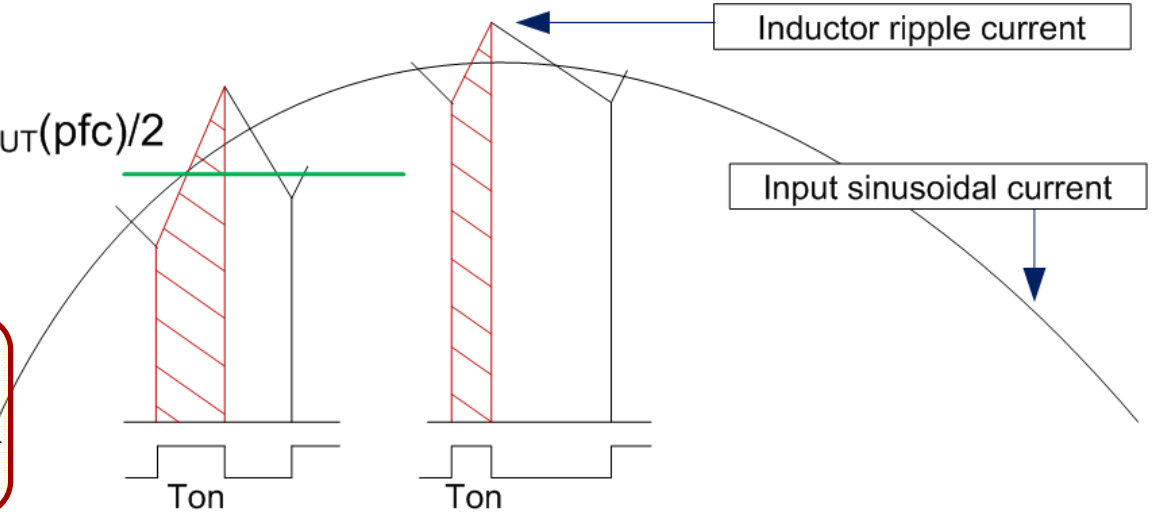
$$K_2 = \frac{8 \cdot \sqrt{2}}{3 \cdot \pi}$$

$$K_3 = \frac{V_{IN}(pfc, min)}{V_{OUT}(pfc)}$$

$$I_{SW} = K_1 \cdot \sqrt{1 - K_2 \cdot K_3} = 6.9\,A$$

$$I_{D2} = K_1 \cdot \sqrt{K_2 \cdot K_3} = 8.3\ A$$

$$I_C = \frac{P_{OUT}(pfc)}{V_{OUT}(pfc)} \cdot \sqrt{\frac{K_2}{K_3} - 1} = 6.1\,A$$



$V_{IN}(pfc) = V_{OUT}(pfc)/2$

Block design: component stress analysis

- Swinging inductor improves EMI and keeps high L
- Allow 0.2% conduction losses
- FET → RDS_{ON} = 125 mΩ, 650 V, C_{OSS} = 53 pF
- Total FET losses → 4.14 W per FET
- SiC → V_{TH} = 1 V, Z_D = 0.05 Ohm

$$RDS_{ON}(EQ) = \frac{2}{1000}\frac{P_{OUT}(pfc)}{\eta \cdot (I_{SW})^2} = 0.087\,\Omega$$

$$P_{COND}(EQ) = \frac{RDS_{ON}(EQ)}{2}(I_{SW})^2 = 3.02\,W$$

$$P_{COSS}(EQ) = \frac{1}{2} \cdot (2 \cdot COSS) \cdot (V_{OUT}(pfc))^2 \cdot F_{SW} = 1.1\,W$$

$$P_{SW}(EQ) = \frac{1}{2} \cdot V_{OUT}(pfc) \cdot I_{SW} \cdot (T_R + T_F) \cdot F_{SW} = 4.16\,W$$

$$P(EQ) = P_{COND}(EQ) + P_{COSS}(EQ) + P_{SW}(EQ) = 8.28\,W$$

$$P_{D2} = V_{TH} \cdot I_{OUT}(pfc) + Z_D \cdot (I_{D2})^2 = 8.46\,W$$

Block design: output bulk capacitor

- Output capacitance supports both hold-up time and RMS current:

$$C_{OUT}(pfc) = \frac{2 \cdot P_{OUT}(pfc) \cdot T_{HOLD}}{(V_{OUT}(pfc,nom))^2 - (V_{OUT}(pfc,nom) - V_{DROP})^2} = 1.08 \cdot 10^3\ \mu F$$

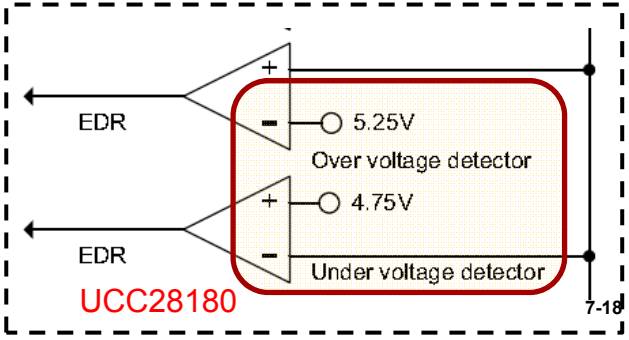
V_{DROP} = 50V

T_{HOLD} = 0.01 s

- Choose ~1300 uF (+ 20% due to tolerance) → select 4 x 330 uF
- Each capacitor should support I_{RMS} ≥ 1.53 A_{RMS} (6.11 A / 4)
- Also check peak-peak ripple voltage @ F_{LINE} = 47 Hz:

$$V_{RIPPLE}(pfc) = \frac{I_{OUT}(pfc)}{2 \cdot \pi \cdot 2 \cdot F_{LINE} \cdot C_{OUT}(pfc)} = 7.9\ V$$

V_{RIPPLE} must be low enough to avoid OVD & UVD



DONE! Less than ± 2%

Block design: auxiliary power supply

- Nominal power consumption:

  P_{NOM} = 8.5 W → design for 10 W

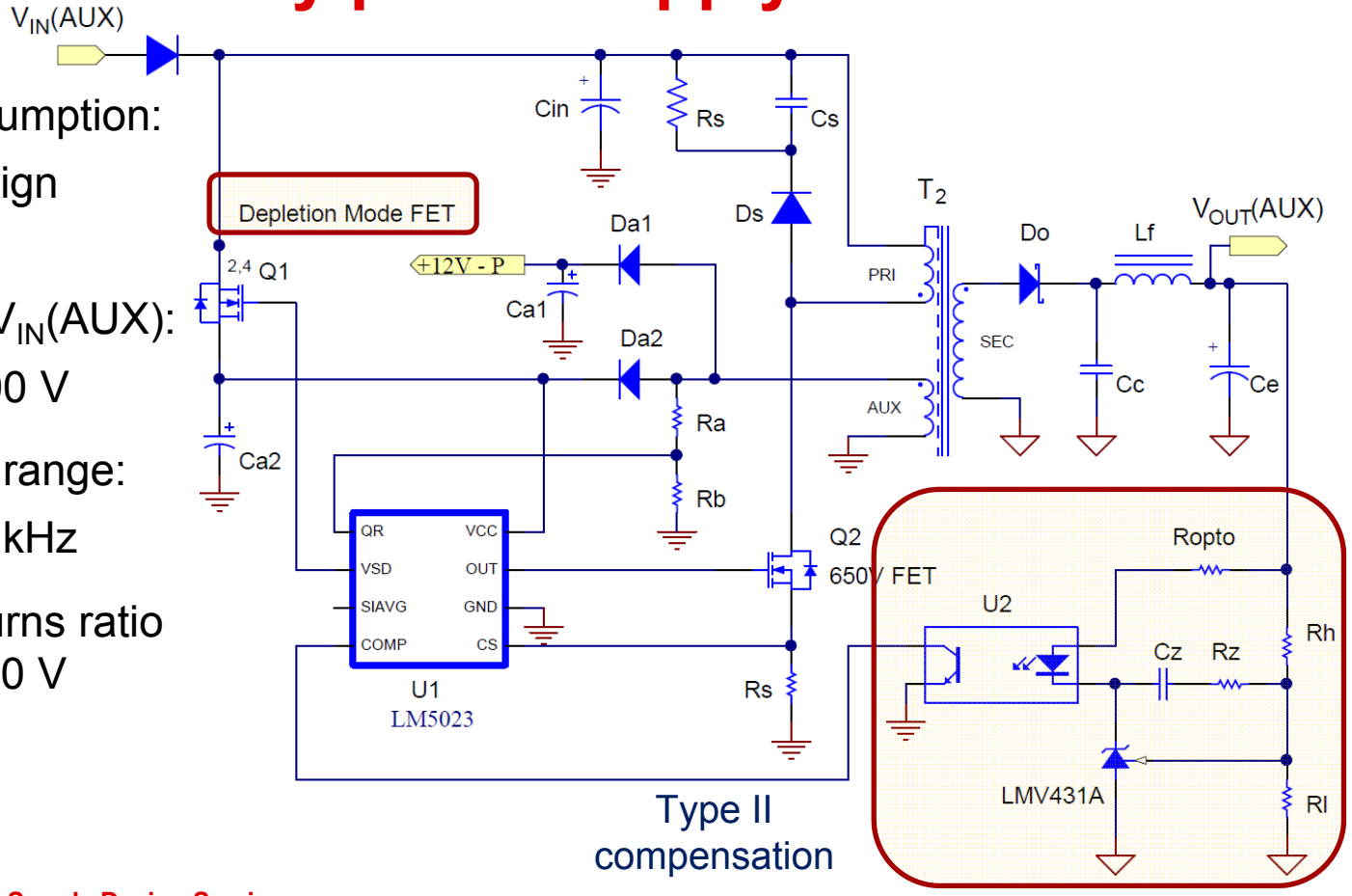
- Input voltage range V_{IN}(AUX):

  120 V (85 Vac) ... 400 V

- Switching frequency range:

  F_{SW} = 70 kHz …120 kHz

- Select transformer turns ratio to keep V_{DS_MAX} ≤ 650 V



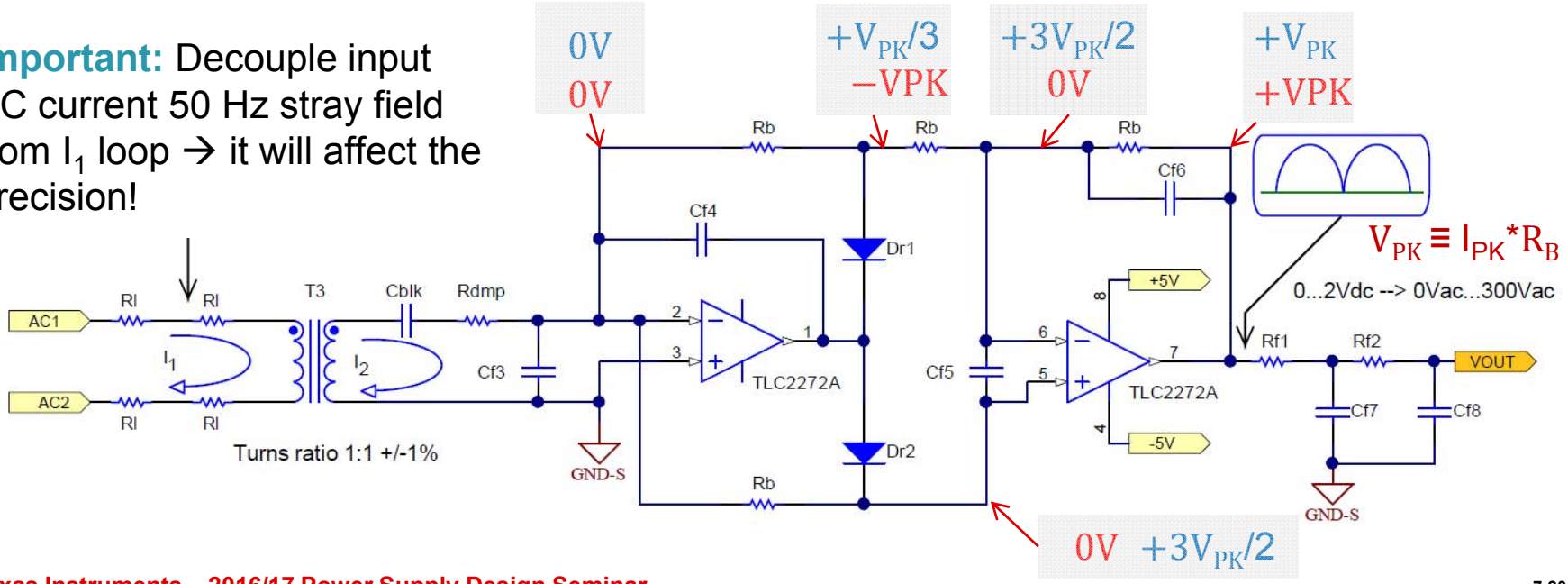
Block design: AC voltage-sensing

$$I_{IN}(pfc) = \frac{P_{OUT}(fb)}{\eta \cdot V_{IN}(pfc)}$$

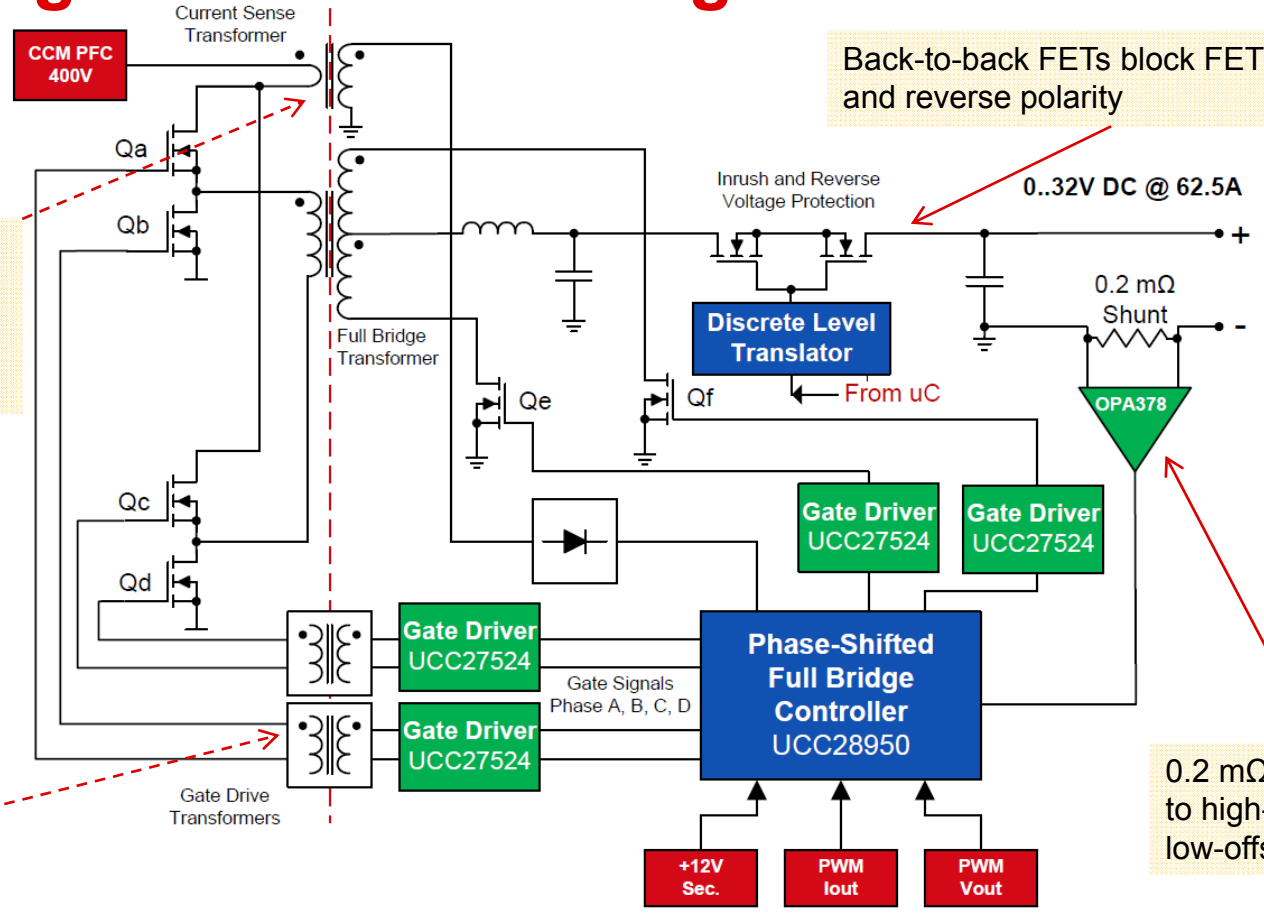
V_{AC} measurement needed for:

- Input under-voltage and over-voltage protection
- Limit input current per digital calculation of $V_{OUT}(fb)$, $I_{OUT}(fb)$, η

Important: Decouple input AC current 50 Hz stray field from I_1 loop → it will affect the precision!



Block design: PSFB block diagram



Back-to-back FETs block FET surge and reverse polarity

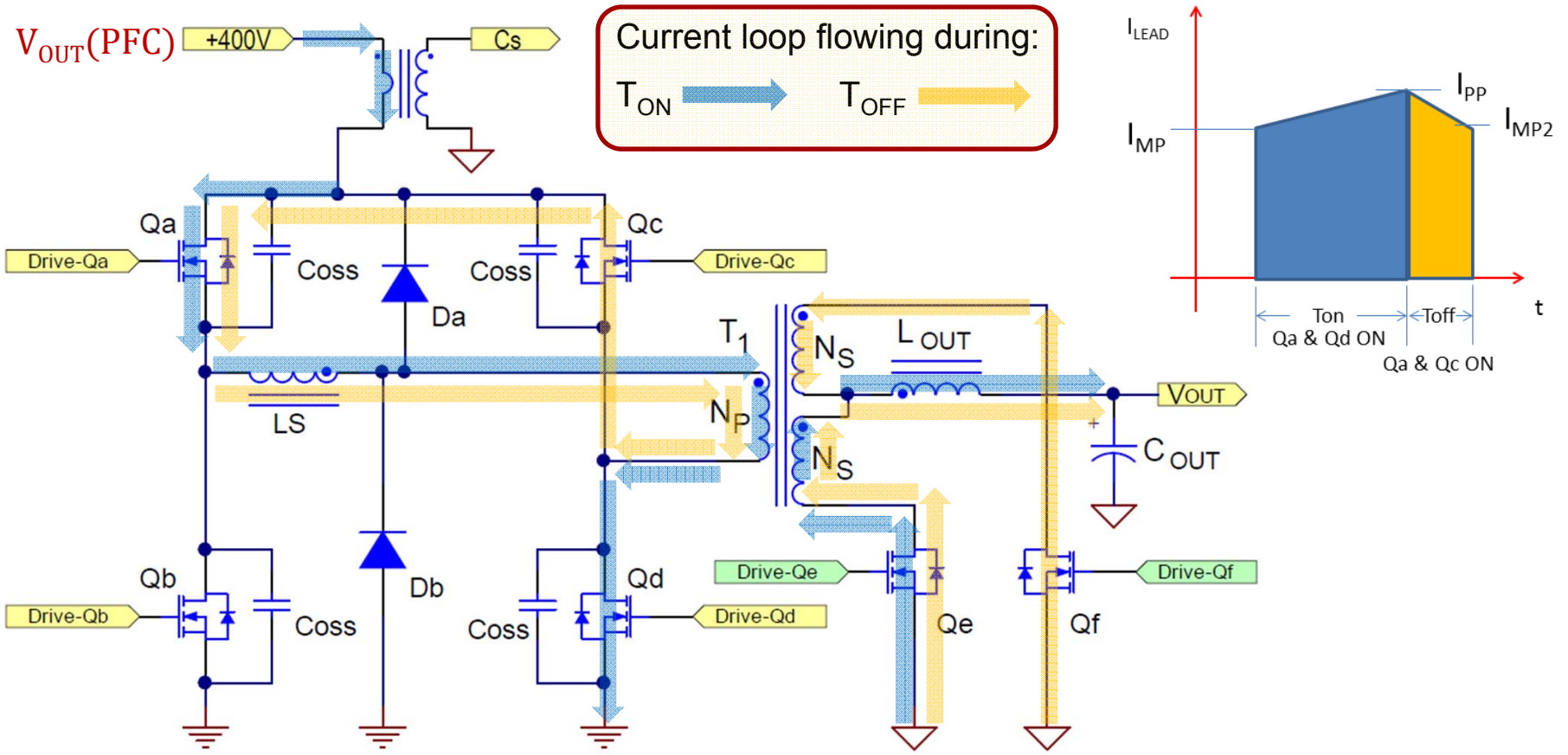
CS Xfrm in series w/ bridge prevents x-cond.

(Also imbalance due to circulating currents)

Gate drive simplified by 50% D

0.2 mΩ shunt thanks to high-precision, low-offset op amp

Block design: PSFB circulating currents

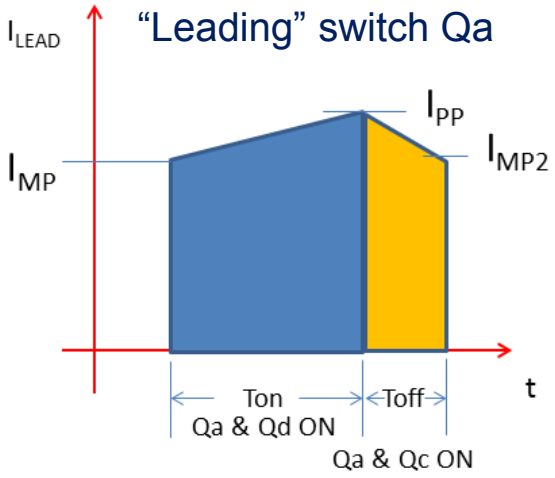


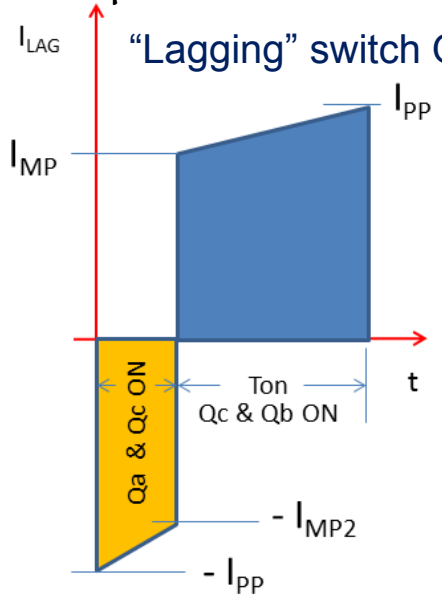
Block design: PSFB waveforms

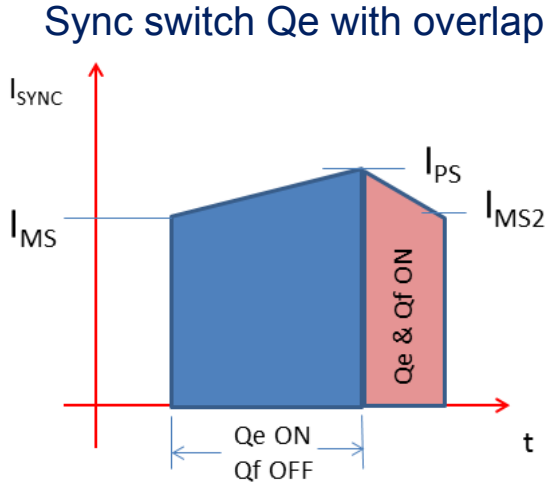
- IQa(RMS) ~ IQc(RMS)
- Set (ΔI_{Lout}) = 20%, @ V_{IN}(fb,nom) = 400 V, V_{OUT}(fb,nom) = 27 V

$$L_{OUT} = \frac{V_{OUT}(fb,nom) \cdot (1 - D(fb,nom))}{\Delta I_{LOUT} \cdot F_{SW}} = 3.7\,\mu H$$

Q_{E_RMS} switch current:
I_{S_RMS} = 42.7 A







Block design: PSFB main FET choice

- Select loss budget = 1% of P_{OUT} on Q_A through Q_D → PQ_A = (0.25% of P_{OUT}) = 4.8W

Neglect Q_G(Qa) (gate charge loss)

$$P_{Qa} = \left(I_{Qa}(RMS)\right)^2 \cdot RDS_{ON}(Qa) + 2 \cdot Q_G(Qa) \cdot V_{GATE} \cdot \frac{F_{SW}(fb)}{2}$$

→ $R_{DS(ON)} \leq 0.21\ \Omega$

- Selected 4 x FETs, RDS_{ON} = 0.19 Ω, 17A, 650V **(≥ V_{IN}(fb,max))**
- Incorporates ultra-fast body diode: no spikes at light load (when ZVS is lost)
- N = Transformer turns ratio = 9.5, V_{IN}(fb,max) = 440 V
- Sync. rectification Qe and Qf must withstand $V_{DS}(Qe)$ according to:

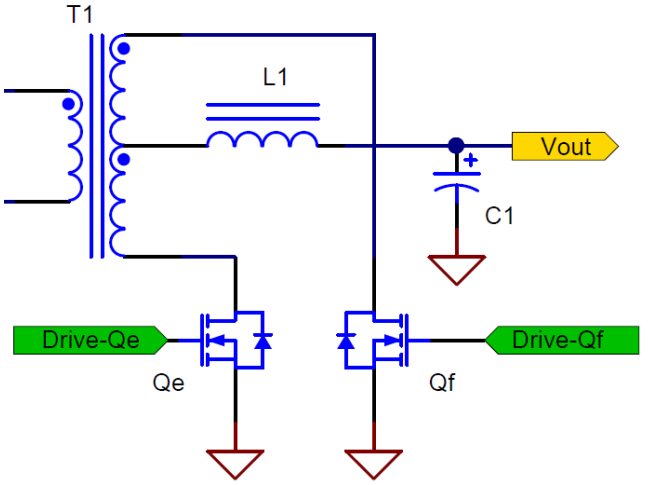
$$\rightarrow \quad V_{DS}(Qe) = \frac{2 \cdot V_{IN}(fb,max)}{N_{PS}(fb)} \cdot 1.5 = 139\ V$$

(+50% due to spikes)

Block design: PSFB sync. FET choice

- Select 200 V FET, since we have 139 V clamped spike
- Loss (conduction) budget = 1% of P_{OUT} on Qe and Qf → $P_{BUDGET}(Qe)$ = (0.5% of P_{OUT}) = 10 W
- Selected 4 x FETs, RDS_{ON} = 10.5 mΩ, 84A, 200 V
- Use 2 parallel FETs each for Qe and Qf

$$RDS_{ON}(EQ) \le \frac{P_{BUDGET}(Qe)}{\left(I_{Qe}(RMS)\right)^2} = 5.5 \cdot 10^{-3}\Omega$$



$$P_{Qe} = \left(I_{Qe}(RMS)\right)^2 \cdot RDS_{ON}(Qe) + \frac{P_{OUT}(fb)}{V_{OUT}(fb,nom)} \cdot V_{DS}(Qe) \cdot T_F \cdot \frac{F_{SW}(fb)}{2} + 2 \cdot COSS(Qe,avg) \cdot \left(V_{DS}(Qe)\right)^2 \cdot \frac{F_{SW}(fb)}{2} + 2 \cdot Q_G(Qe) \cdot V_{GATE} \cdot F_{SW}(fb) = 25.2\,W$$

Block design: PSFB resonant inductor

- E_{STORE} in L_S charges total C_{OSS} of one leg
- Achieve ZVS down to **$Load_{MIN}$ = 15%** of full load →

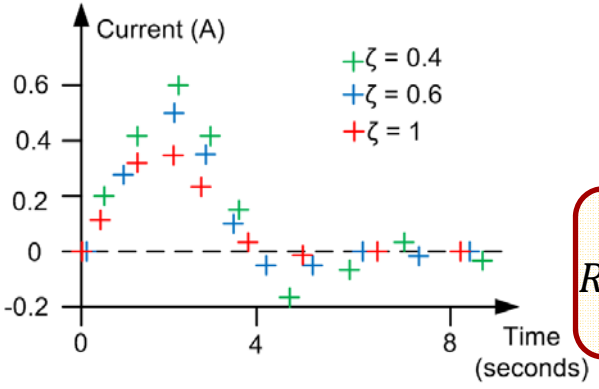
$$L_S \geq 2 \cdot COSS(Qa, avg) \cdot \frac{(V_{IN}(fb, nom))^2}{\left[\mathrm{LOAD(min)} \cdot \left(I_{PP} - \frac{\Delta I_{LOUT}}{N_{PS}(fb)}\right)\right]^2} - L_{LK} = 1.13 \cdot 10^{-5} H$$

- Where: L_{LK} = 3.5 uH (0.1% of magnetizing inductance) → **L_S = 10 µH**
- L_S RMS current and T1 primary current are the same (have only AC component)
- Select PQ20/20 platform with:
  - ΔB_{PK} = 118 mT, 10 turns Litz wire (160x0.1 mm)
  - N97 EPCOS core, gap 0.77 mm, μ_E = 57
  - Results in copper losses = 0.63 W and core losses = 0.57 W

Block design: PSFB FET drive

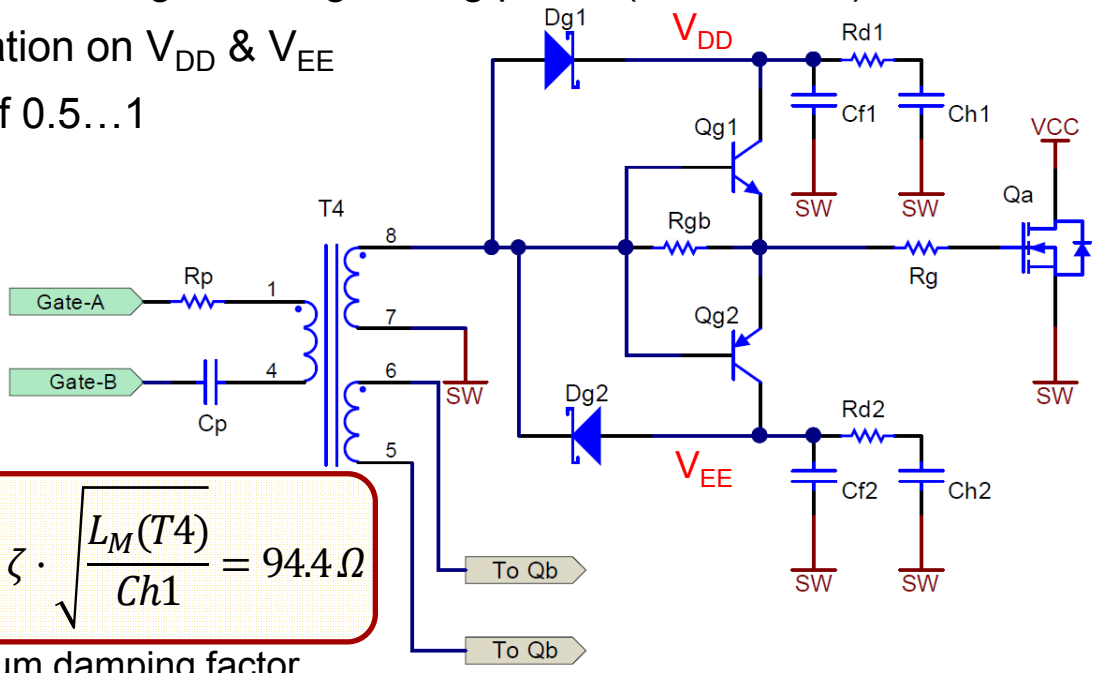
- Select turns ratio of T4 = 1:1 to get V_{DRIVE}=12V (AF4779, L_M = 0.9 mH)
- Add small R_P (~2…3Ω) to damp primary winding + C_P=1 uF to remove DC comp.
- $Cf_{1,2}$ hold V_{DD} = +12 V and V_{EE} = -12 V voltages during driving peaks (used 22 nF)
- $Rd_{1,2}$ are needed to damp the oscillation on V_{DD} & V_{EE}
- Select damping factor ζ in a range of 0.5…1

$$\zeta := 0.5$$



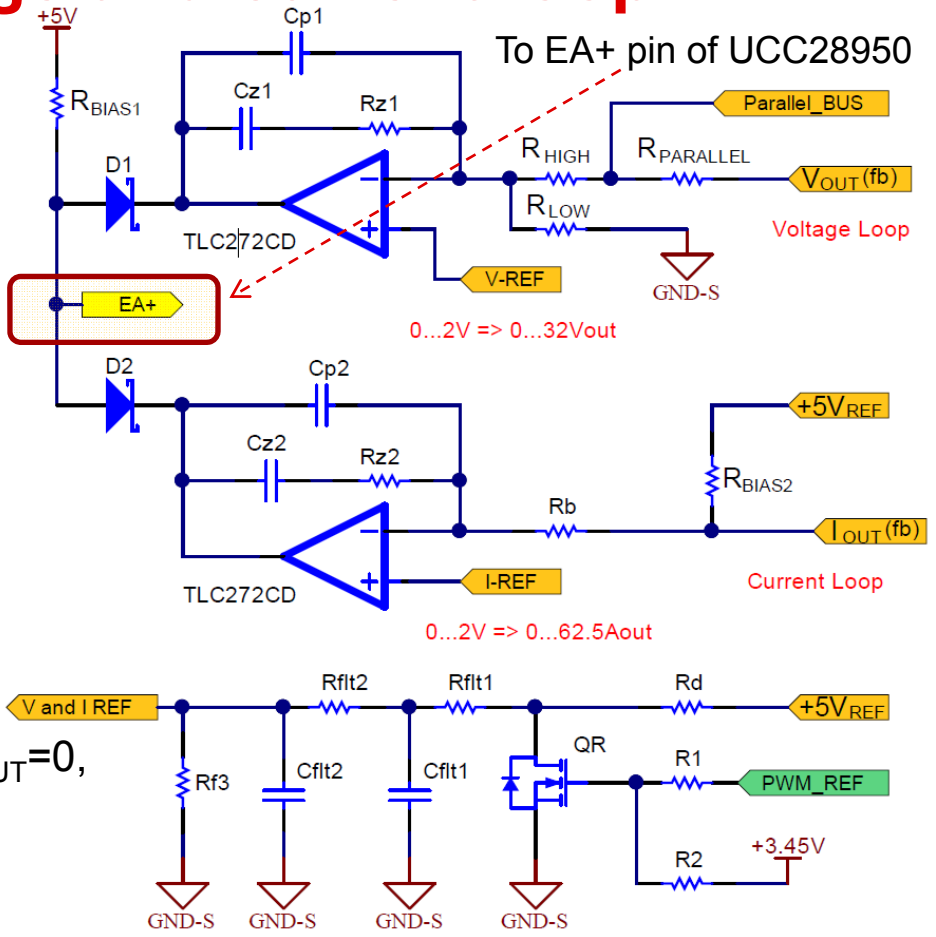
$$Rd1 = 2 \cdot \zeta \cdot \sqrt{\frac{L_M(T4)}{Ch1}} = 94.4\,\Omega$$

= minimum damping factor



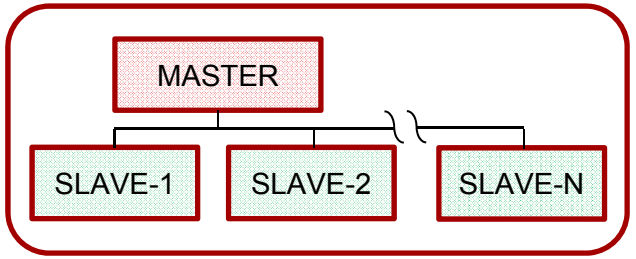
Block design: PSFB voltage and current loop

- DAC achieved by PWM-to-average → V-REF, I-REF
- Chosen Rflt1 = 2 * Rflt2 and Cflt2 = 2 * Cflt1 → same F_{CO}
- By selecting F_{CO} = 16 Hz, Rflt1 =100 K, Cflt1 = 100 nF
- R_{BIAS2} biases current loop → zero current at startup
- 2 x PWM_REF come from µC timer channels
- If PWM_REF is in three-state condition →V_{OUT}=0, I_{OUT}=0

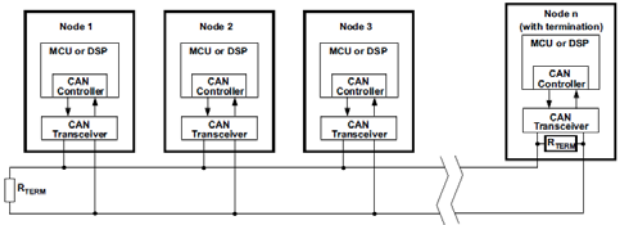


Block design: Leverage a microcontroller

Master-slave architecture



CAN bus and digital parallel



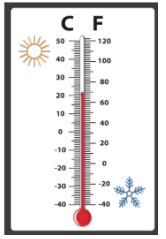
Microcontroller

Sets and reads RPM

Reads input voltage

Sets V_{OUT} levels

Sets I_{OUT} and current limit



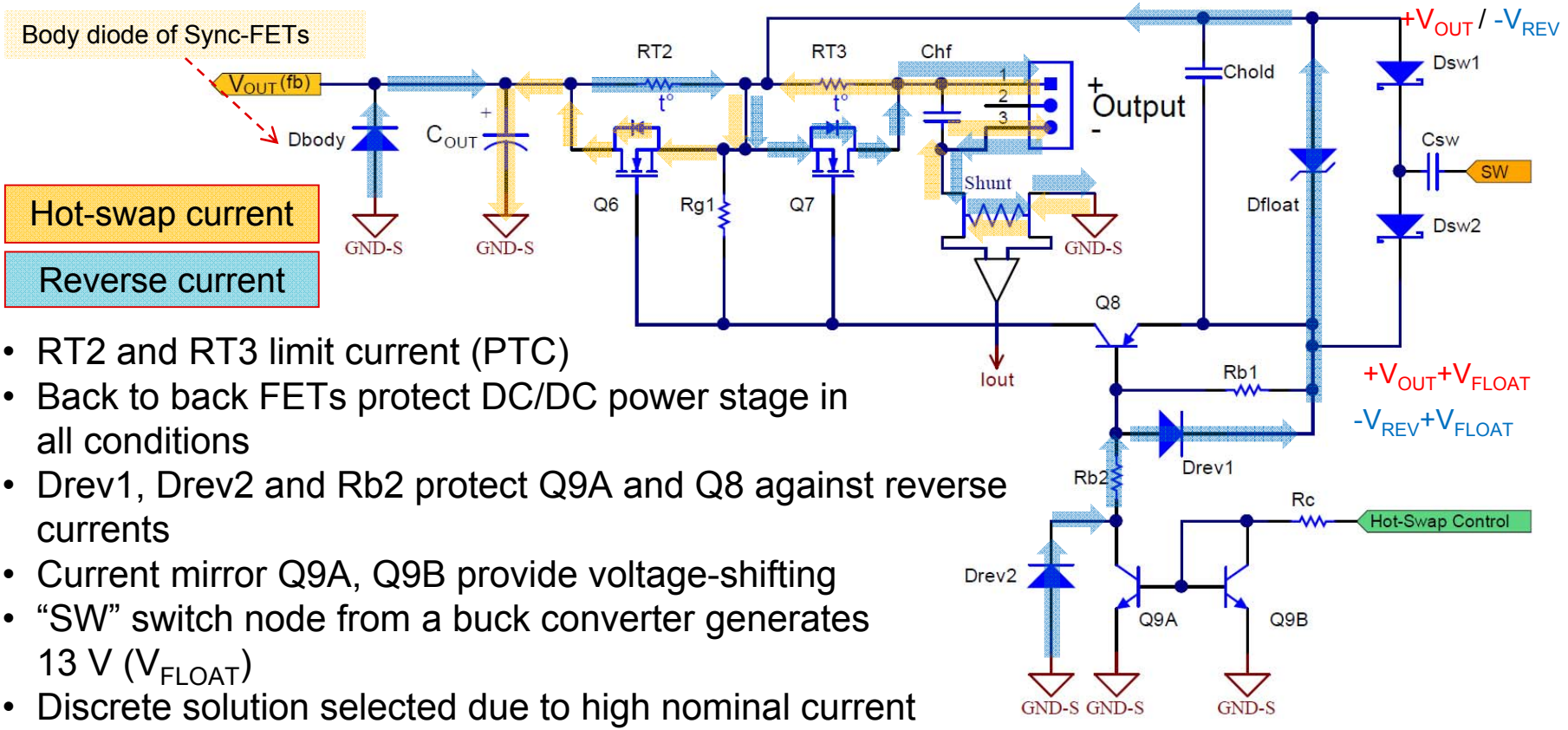
Internal temperature reading

Block design: Choice of Microcontroller

- Slow voltage and current loops: no need of ultra-high speed microcontroller
- Microcontroller sets V_{OUT}, I_{OUT}, P_{OUT} + managing all “slow” variables
- Functions:
  - o Analog inputs (ADC channels): V_{OUT}, I_{OUT}, $V_{IN\text{-}RMS}$, T_{AMB} → 4 x ADC
  - o Analog outputs (PWM to analog): V_{OUT} and I_{OUT} REF → 2 x PWM
  - o UART (CAN-bus hardware): Full-duplex → CAN RX & TX
  - o General purpose I/O: → 28 GPIO
  - o V_{OUT} and I_{OUT} precision: 100 ksps is sufficient, ±1% 10-bit ADC
  - o V_{OUT} and I_{OUT} setting: F_{CLOCK} = 16 MHz and $compare_{FS}$ = 16000, PWM = 1 kHz
  - o No need for extra-low power consumption

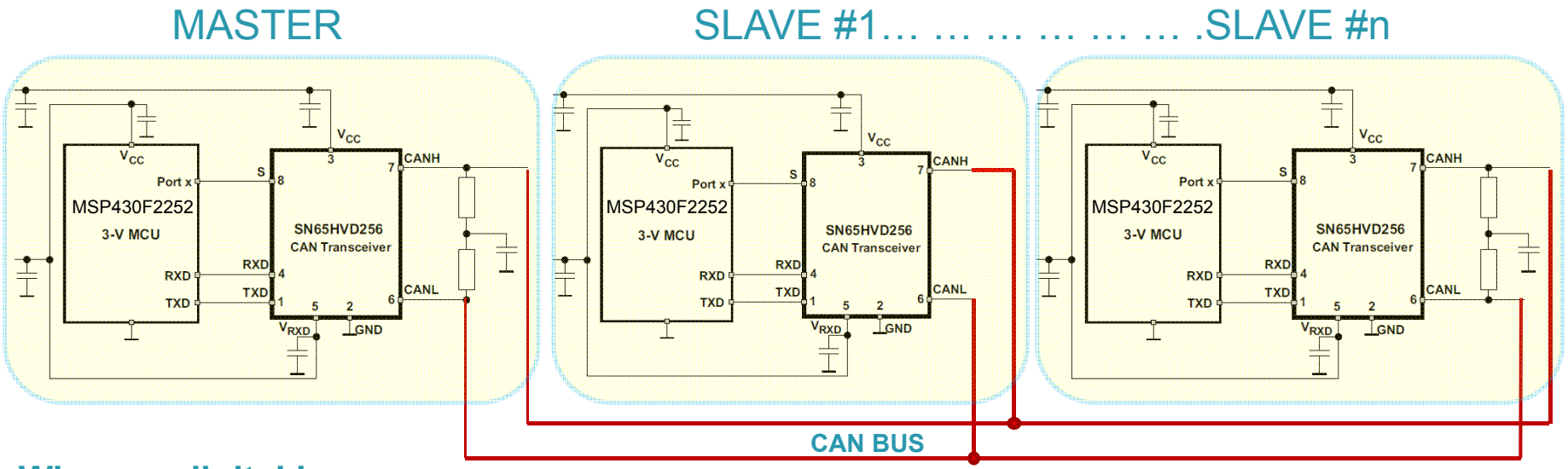
- Selected MSP430F2252:
  - o 16 KB + 256 B flash memory
  - o 512 B RAM

Block design: Hot-swap + rev-polarity protection



- RT2 and RT3 limit current (PTC)
- Back to back FETs protect DC/DC power stage in all conditions
- Drev1, Drev2 and Rb2 protect Q9A and Q8 against reverse currents
- Current mirror Q9A, Q9B provide voltage-shifting
- “SW” switch node from a buck converter generates 13 V (V_{FLOAT})
- Discrete solution selected due to high nominal current

Paralleling modules: UART with CAN bus interface



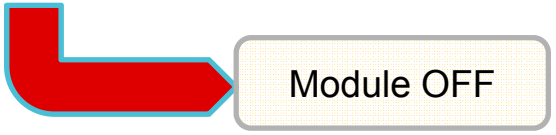
Why use digital bus

- Battery charger is “slow” system and digital communication is necessary anyway – hardware interface already implemented
- Fixed M/S assignment – master manages battery-charging, dictates current slaves supply. Slaves simply follow commands and deliver current.
- Only one loop is active – no multi-loop stability problems, nor further parallel loop to stabilize

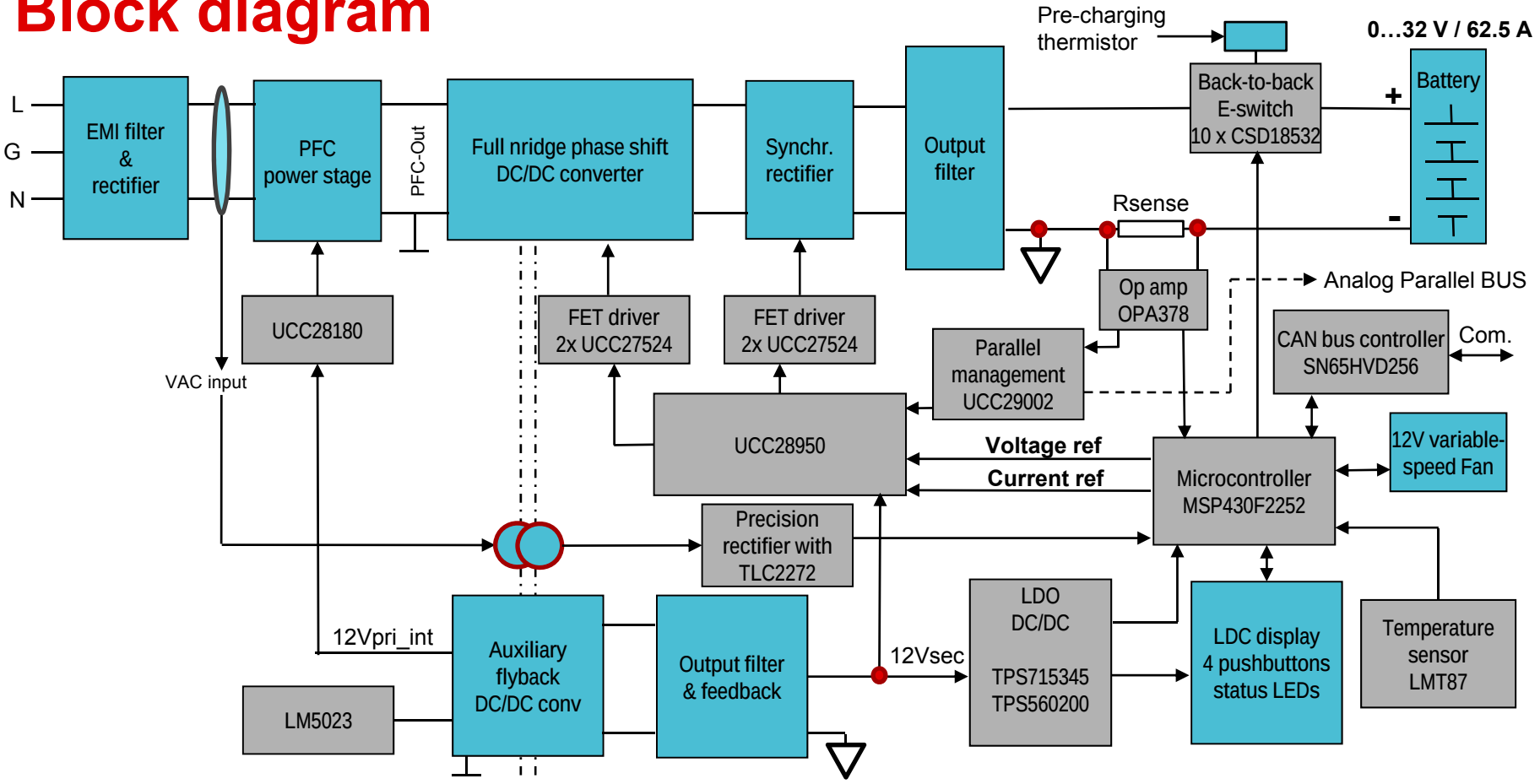
Module functionality: alarms and warnings

#	Alarm Description
0	Mains too low
1	Mains overvoltage
2	Output overvoltage
3	Output shorted
4	Reverse polarity
5	Over temperature
6	Fan failure
7	DC/DC failure

#	Warning Description
0	Output current limit
1	Output power limit
2	Input current limit
3	Low battery voltage
4	Not used
5	Not used
6	Not used
7	Not used



Block diagram

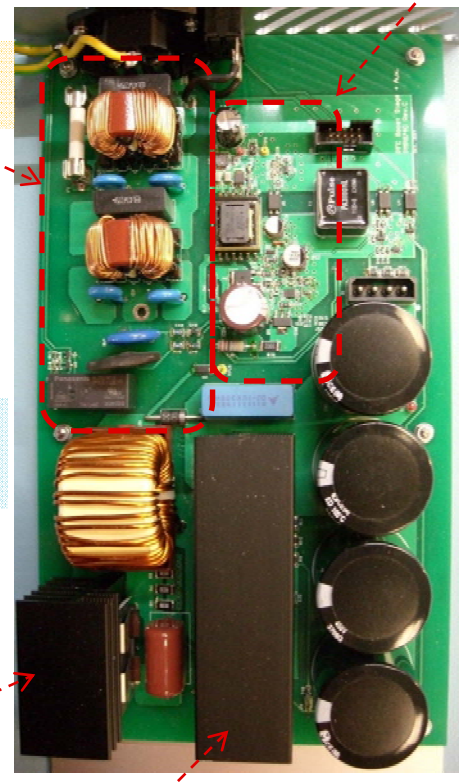


PMP8740 module

FRONT PANEL

BACK PANEL

Dim: 125 x 170 x 290 mm



Aux. power supply

µC

Back-to-back FETs

EMI Filter & inrush limit

Output caps

Sync. FETs

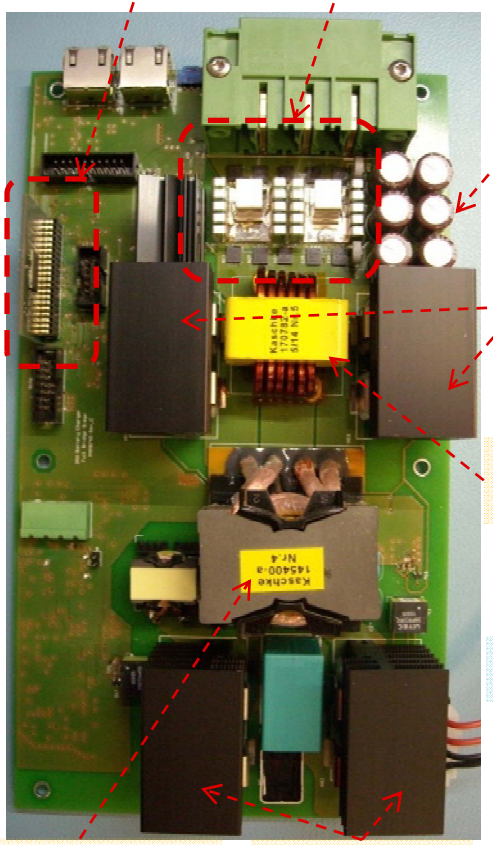
PFC BOOST

Output inductor

DC/DC

Bridge

Main FETs and SiC diode on heatsink

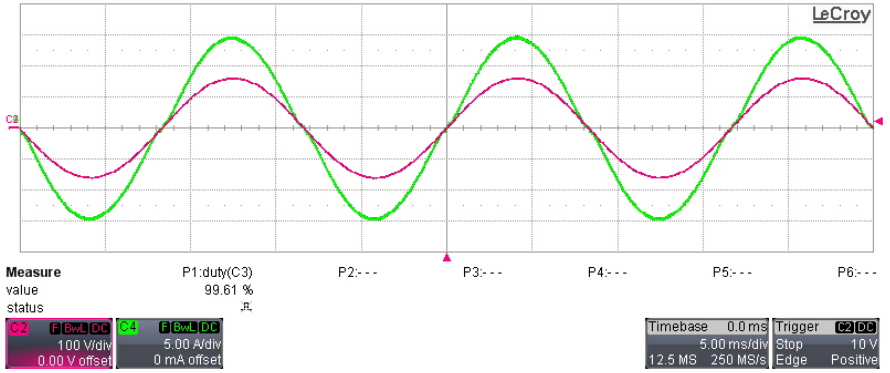


Main transformer

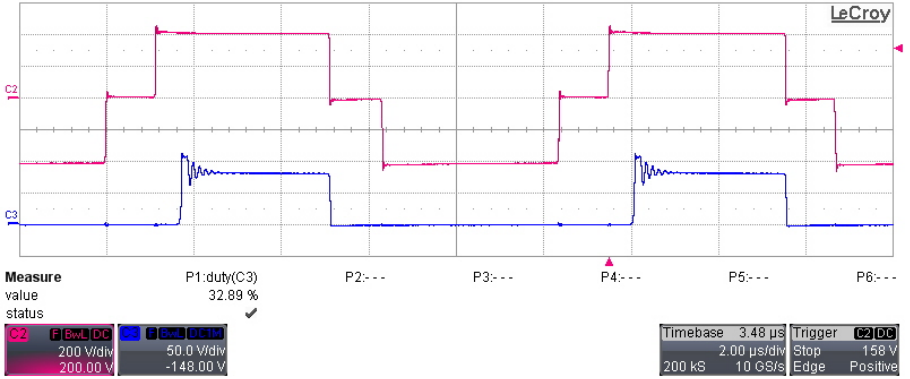
Bridge FETs

Test data @ 1.6 KW load (limit of the AC source)

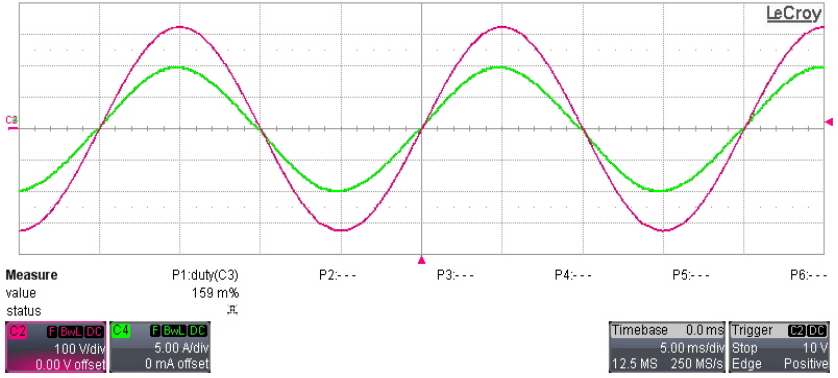
Input voltage and current @ 90 Vac



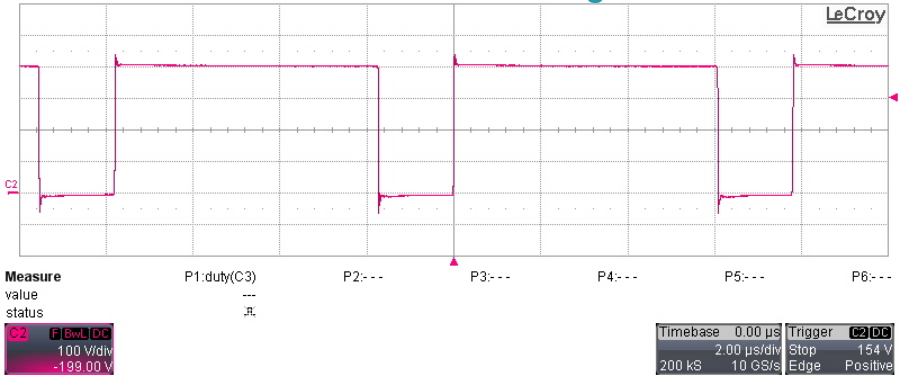
Bridge voltage and sync. rectifier drain



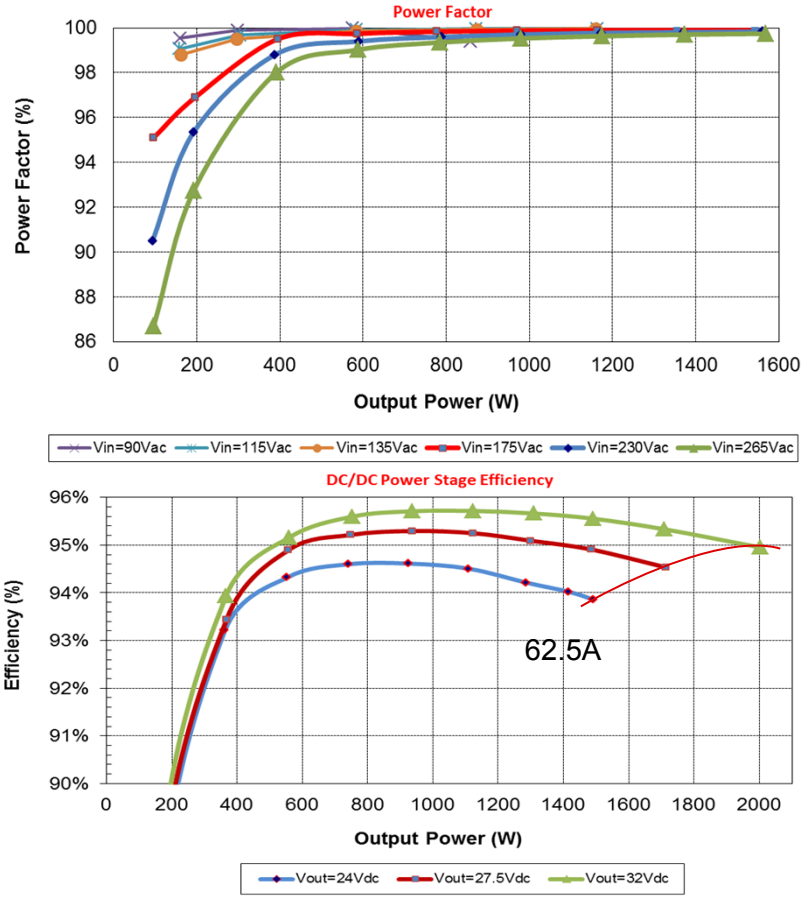
Input voltage and current @ 230 Vac

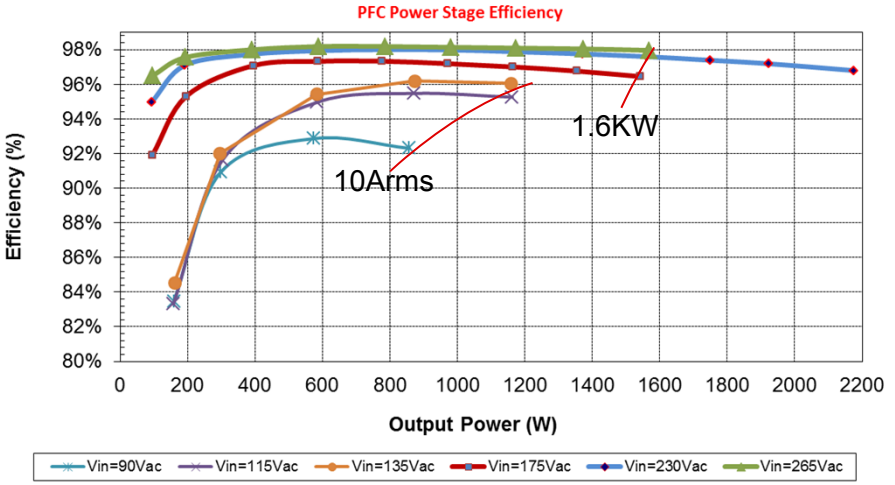


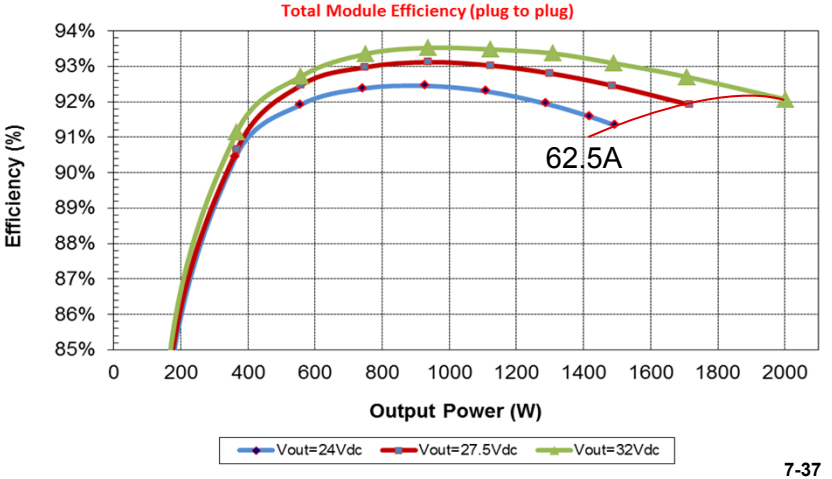
PFC FET drain voltage



Module test data







Summary

- Complete design of 2 kW module **PMP8740**
- Module employed in master-slave (M/S) architecture
  - Suits lead-acid and Li-Ion battery charging and redundant telecom apps
- In M/S configuration, firmware is open to
  - Master configuration + slave without display (single multi-kW module)
  - M/S architecture with paralleled modules, separable in different modules (one display + pushbuttons for each module)
- Two modules built and tested - parallel operation proven
  - ±1% unbalance
- Future developments
  - Automatic M/S assignment if the master fails: improved reliability
  - Three-phase connection architecture with (Y) and without neutral (Δ)

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