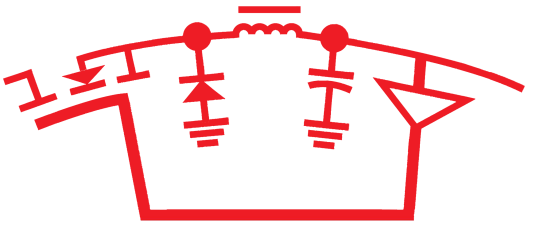

Power Supply Design Seminar

Control and Design Challenges for Synchronous Rectifiers

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Control and Design Challenges for Synchronous Rectifiers

Bing Lu

ABSTRACT

To improve power supply efficiency to meet stringent standards, a synchronous rectifier (SR) often replaces the diode rectifier. Based on loss breakdown, this session explains how to achieve efficiency improvement and presents design criteria for selecting a suitable SR MOSFET, balancing between conduction and switching losses. Also, SR control methods are discussed, including V_{DS} sensing, volt-second sensing and self-driven. The pros and cons of each control method are discussed in detail. Some design challenges, including noise immunity, fast turn off, high-side and low-side SR and special current shapes, such as LLC converters, are also discussed.

I. INTRODUCTION

With the development of telecommunication and mobile technologies, smart phones, tablets and notebook computers became essential parts of everyday life. The more powerful processors, larger screen sizes and longer operating times require the battery sizes to keep increasing. In turn, the power levels of the AC/DC adapters (chargers) are also increasing. While the power of these adapters keeps increasing, the size of the adapters is expected to remain the same or become even smaller (for either branding reasons or better mobility). Due to the smaller size and less surface area, the adapter efficiency must increase to allow an acceptable surface temperature for safe operation. The power supply design industries are searching for different solutions to obtain higher power density AC/DC adapters through better semiconductor devices and topologies. Meanwhile, different countries and organizations have passed legislation for the efficiency standard for these power supplies [1]. The most significant ones are the US Department of Energy (DoE) [2] and the Code of Conduct (CoC) [5] from the European Commission.

A. Efficiency Standards and Power Density Requirements

Most AC/DC adapters fall into the external power supply categories of the efficiency standards. Both the DoE and CoC have regulated the efficiency for many years. As summarized in [1], different countries and organizations are regulating the power supply efficiency. The expected energy efficiency level is becoming higher with the years. According to the DoE requirement, the energy efficiency level is clearly marked on the adapter with a Roman numeral, as shown in Figure 1. The rules of the efficiency marking can be found in [4].

Figure 1 – External power supply marking with efficiency level.

In the latest DoE efficiency standard (Table 1), the basic voltage power supply is defined as a rated output voltage larger or equal to 6 V. For the low voltage power supply, which has a rated output voltage less than 6 V, the required efficiencies are lower due to the higher conduction loss challenges for the lower output voltage. The regulation has been in effect since February 10, 2016. The efficiency measurement method is defined as in [3]. The average efficiency is the average value efficiencies measured at 25%, 50%, 75% and 100% of the rated output current. CoC has very similar regulation levels but it also regulates the 10% rated load efficiency, which further emphasizes the light load efficiency requirement. Besides the average efficiency, the standard also regulates the no-load standby power.

To meet the stringent efficiency standards, the power supply industry implemented different technologies, such as better semiconductor devices as well as better circuit topologies to reduce the conduction and switching losses. Meanwhile, the output rectifier is often addressed with a different method.

Single Voltage External AC/DC Power Supply, Basic Voltage		
Nameplate Output Power (P_{OUT})	**Minimum Average Efficiency in Active Mode (Expressed as a Decimal)**	**Maximum Power in No-Load Mode (W)**
$P_{OUT} \leq 1$ W	$\geq 0.5 \times P_{OUT} + 0.16$	≤ 0.100
1 W < P_{OUT} ≤ 49 W	$\geq 0.071 \times \ln(P_{OUT}) - 0.0014 \times P_{OUT} + 0.67$	≤ 0.100
49 W < P_{OUT} ≤ 250 W	≥ 0.880	≤ 0.210
$P_{OUT} > 250$ W	≥ 0.875	≤ 0.500

Single Voltage External AC/DC Power Supply, Low Voltage		
Nameplate Output Power (P_{OUT})	**Minimum Average Efficiency in Active Mode (Expressed as a Decimal)**	**Maximum Power in No-Load Mode (W)**
$P_{OUT} \leq 1$ W	$\geq 0.517 \times P_{OUT} + 0.087$	≤ 0.100
1 W < P_{OUT} ≤ 49 W	$\geq 0.0834 \times \ln(P_{OUT}) - 0.0014 \times P_{OUT} + 0.609$	≤ 0.100
49 W < P_{OUT} ≤ 250 W	≥ 0.870	≤ 0.210
$P_{OUT} > 250$ W	≥ 0.875	≤ 0.500

Table 1 – DoE efficiency standard for external power supply.

A simple flyback converter is show in Figure 2. The secondary side current is rectified and filtered as the load current. The rectifier is directly in series with the load.

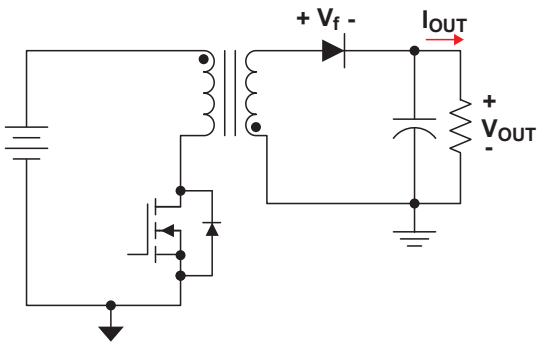


Figure 2 – Flyback converter and its output rectifier.

The flyback converter as well as most of the power conversion topologies have similar architecture, such as forward or LLC converters. Since the diode forward voltage drop is roughly a fixed voltage of V_f, the conduction loss on the diode can be calculated using Equation 1.

$$P_{DIODE} = V_f \cdot I_{OUT} \quad (1)$$

From this equation, the diode conduction loss is directly proportional to the forward voltage drop of the diode rectifier. Lowering the diode's forward voltage drop can help reduce the loss and improve efficiency. As shown in Figure 3, the forward voltage drop for a Schottky diode is much lower than the PN junction diode. Therefore, a Schottky diode is often used to reduce the conduction loss.

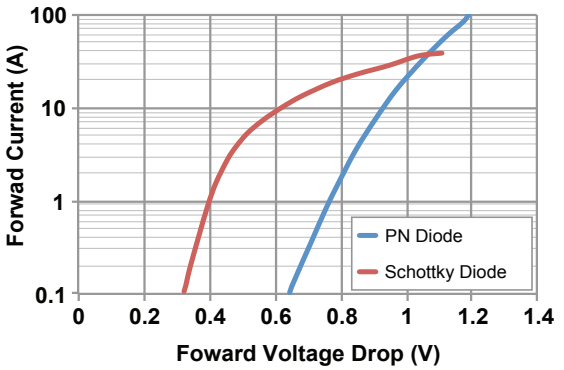


Figure 3 – Forward voltage drop comparison between PN diode and Schottky diode.

Besides the absolute value of the conduction loss, the conduction loss can be normalized with the output power, so the efficiency impact can be directly calculated. Due to the other losses in the converter, the efficiency impact is approximately the ratio between the diode loss and the output power.

$$\eta_{DIODE} \approx \frac{P_{DIODE}}{P_{LOAD}} = \frac{V_f \cdot I_{OUT}}{V_{OUT} \cdot I_{OUT}} = \frac{V_f}{V_{OUT}} \quad (2)$$

According to Equation 2, at lower output voltage, the diode drop has a higher impact on the efficiency. This is part of the reason why the efficiency standard is lower for a low voltage power supply.

Furthermore, beyond the efficiency impact, the designers often face the issue of thermal management. For example, at 10 A output, the 0.5 V diode drop causes a 5 W loss and the thermal management could be an issue. A large and expensive heatsink is required.

Even though the Schottky diode can help reduce the conduction loss, its forward voltage drop is still relatively high. Besides this, the Schottky diodes are also limited by the voltage ratings. When the breakdown voltage is above 100 V, the improvement of the Schottky diode becomes less significant.

To further reduce the conduction loss, a synchronous rectifier was proposed to replace the diode rectifier and reduce the conduction loss [6]. If a MOSFET is turned on and off in synchronization with the diode rectifier, it can be used to replace the diode. Instead of a fixed voltage drop, when the MOSFET conducts, its voltage drop is proportional to its on-state resistance ($R_{DS(ON)}$) and the instantaneous current. When the resistance is low enough, the MOSFET can achieve much lower conduction loss. As shown in Figure 4, the MOSFET's (CSD18532KCS) [8] forward voltage drop is much lower compared to the Schottky diode SBRT20M60SP5 [7]. Much lower conduction loss and heat is generated if the SR is implemented.

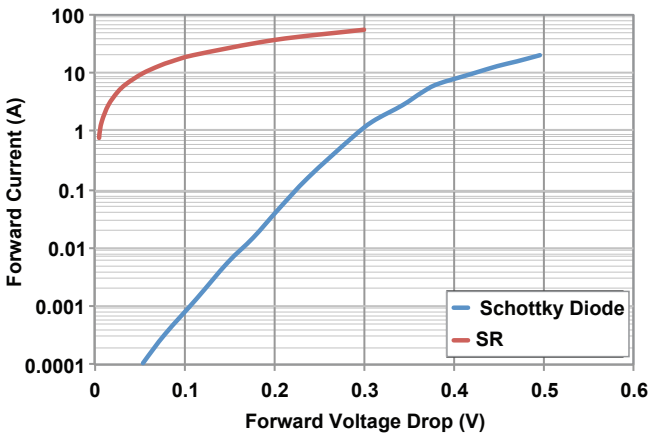
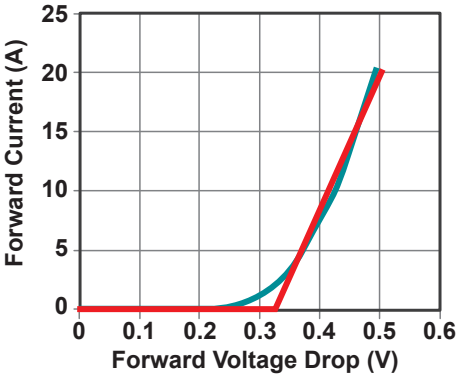


Figure 4 – Forward voltage drop comparison of MOSFET and Schottky diode.

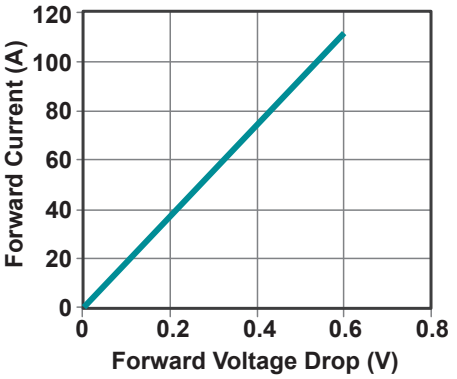
B. Loss Comparison of Diode and SR

The loss improvement can be calculated based on the loss models of the diode and SR. The conduction loss models of the diode and SR are shown in Figure 5.

For the diode, the blue line is its forward voltage drop versus the forward current. It can be approximated by a fixed voltage drop with a straight line as shown with the red line. This simple piecewise linear approximation models the diode conduction loss as a fixed voltage drop in series with a resistor, as shown in Figure 6(a).



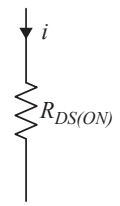
(a) Diode conduction loss model



(b) SR conduction loss model

Figure 5 – Conduction loss model of diode and SR.

(a) Diode conduction loss



(b) SR MOSFET conduction loss

Figure 6 – Equivalent circuit for conduction loss.

$$V_{DIODE}(I) = V_f + I \cdot R_{EQ} \quad (3)$$

As for the SR, if it is ideally controlled in synchronization with the current flowing, the SR can be simplified as a resistor and its forward voltage drop can be replaced by

$$V_{SR}(I) = R_{DS(ON)} \cdot I \quad (4)$$

For the previously mentioned Schottky diode (SBRT20M60SP5), its forward voltage drop is V_f = 0.328 V, while its equivalent series resistance is R_{EQ} =8.7 mΩ. For the SR (CSD18532KCS), we can set the loss model parameter as $R_{DS(ON)}$ = 5.3 mΩ.

If we use a DCM flyback as the test circuit, the secondary side current waveform is shown in Figure 7.

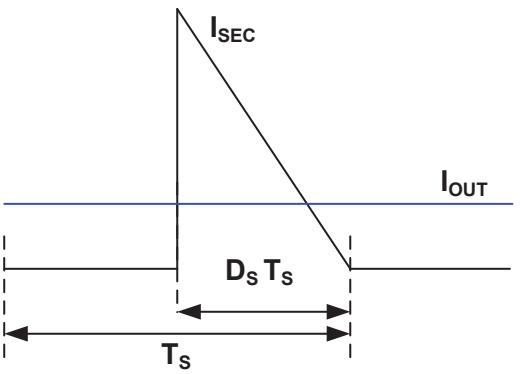


Figure 7 – DCM flyback secondary side current.

For the diode, the conduction loss is calculated as

$$P_{DIODE} = V_f \cdot I_{AVG} + R_{EQ} \cdot I_{RMS}^2 = \frac{1}{2} V_f \cdot I_{PK} \cdot D_S + R_{EQ} \cdot \frac{I_{PK}^2}{3 \cdot D_S} \quad (5)$$

For the SR, the conduction loss is calculated as

$$P_{SR} = R_{DS(ON)} \cdot I_{RMS}^2 = R_{DS(ON)} \cdot \frac{I_{PK}^2}{3 \cdot D_S} \quad (6)$$

In these equations I_{PK} is the secondary side peak current and D_S is the secondary side conduction duty-cycle. For a flyback converter with 50% secondary side conduction duty-cycle, the losses are shown in Figure 8. The conduction loss of the SR is significantly less than the Schottky diode. With the loss model, the SR conduction loss is calculated for other conditions and topologies.

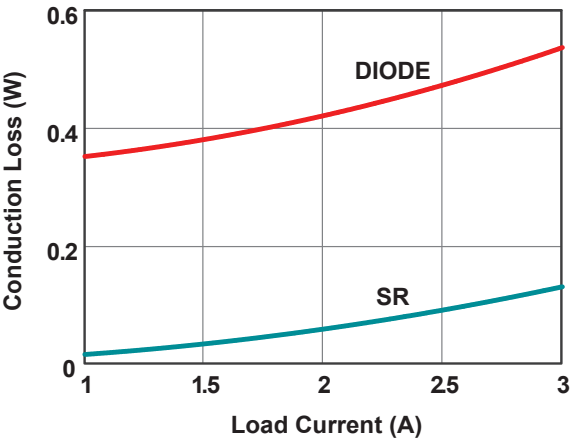


Figure 8 – Conduction loss of diode and SR.

II. SR Control Methods

Even though a diode has higher conduction loss, it is essentially a passive device. The turn-on and -off of the diode is automatic, no dedicated control is needed. For the SR, the MOSFET needs to be turned on and off in sync with the diode conduction. Due to the different topologies and rectifier operation principles, the SR can be controlled with different methods.

A. Controlled-Driven and Self-Driven

In some topologies the SR control can be quite straightforward. For example, in the synchronous buck converter, convert the freewheeling diode into the SR, as shown in Figure 9, the SR Q_{Sync} can turn on and off in complement to the control switch $Q_{Control}$.

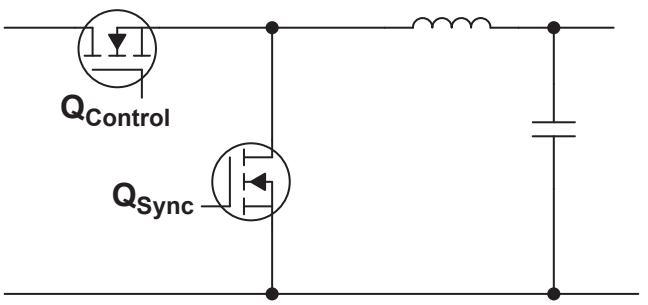


Figure 9 – Synchronous buck converter.

As soon as the control switch $Q_{Control}$ turns off, the inductor flows through the body diode of SR Q_{Sync} as the freewheeling diode. The SR is turned on as soon as its body diode starts conducting, normally a short delay after turning off the control switch. Before turning on the control switch, the SR needs to turn off so that the control switch can force the SR body diode to turn off. Therefore, the control of the synchronous buck converter's SR does not need complicated control schemes except to use the simple dead-times between control and sync switches. To optimize the SR performance, there should be appropriate dead-time between the two switches to prevent shoot-through current and minimize the body diode conduction time [9].

When moving from the non-isolated topologies into an isolated topology, such as active clamp forward, not only is the control straight forward, SRs might be able to be driven directly from the transformer (self-driven). As shown in Figure 10, the SR control is automatic and no extra control IC is required.

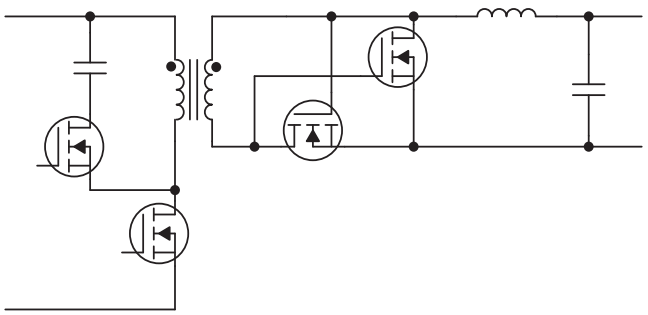


Figure 10 – Active clamp forward with self-driven SR.

Although these controls are simple and straight forward, the control method is basically complementary. Therefore, the inductor current is kept as continuous conduction. At light load, the continuous inductor current flows positively and negatively to give the equivalent low load current. This causes large circulating energy, decreasing the efficiency. At light load, the circulating current causes large conduction loss and decreases the light load efficiency. As the emphasis is on the light load efficiency for different efficiency standards, these simple control methods need to be improved [10][11].

B. V_{DS} Sensing

To prevent the negative current, and be useful for more topologies, the SR control based on drain-to-source voltage sensing (V_{DS} sensing) is proposed [12]. The principle of operation for the V_{DS} sensing SR control can be simplified as in Figure 11.

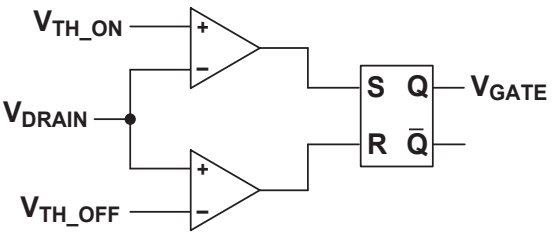


Figure 11 – Simplified SR control diagram.

The V_{DS} control can be illustrated as in Figure 12. When the current starts to flow into the SR body diode, the voltage drop across the SR source-to-drain is the body diode forward voltage drop of a few hundreds of mV. A simple turn-on threshold V_{TH_ON} can be used to detect the body diode conduction and turn on the SR MOSFET. As shown in the waveforms, a short turn-on delay is observed due to the comparator and gate driver delays. After the SR turns on, its voltage drop changes from body diode forward voltage drop into the $R_{DS(ON)}$ voltage drop. Or, in other words, the MOSFET on-state resistor becomes a current sense resistor and its voltage drop directly represents the SR current. Ideally, setting up a comparator to compare this voltage drop to zero allows the SR to be turned off at exactly the time when the current is at the zero crossing. However, due to the tolerance on reference, the comparator delay, gate driver delay, etc., SR is always turned off later than the instance when the voltage crosses the threshold. Therefore, the turn-off threshold V_{TH_OFF} is often set slightly below zero. This way the $\bar{S}R$ can be turned off slightly earlier than the current zero crossing. In a later section, this paper will cover how the threshold impacts the turn-off timing of the SR.

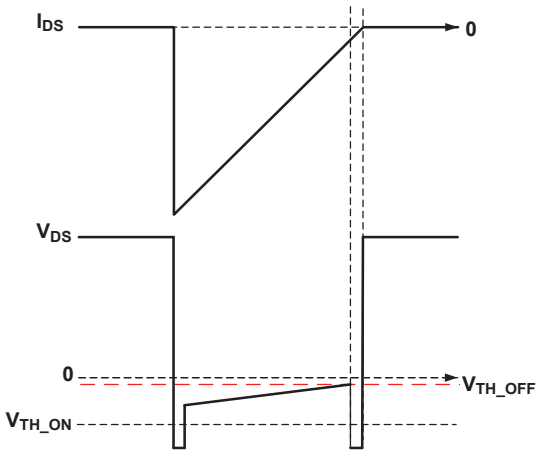


Figure 12 – SR operation waveforms based on V_{DS} sensing.

The V_{DS} sensing method is the most versatile control method, however, it still has many challenges. Firstly, the sensing circuit needs to handle the high voltage (SR voltage rating) and measure very low voltage (a few mV of SR conduction voltage). This makes the sensing circuit design costly and challenging. Secondly, the turn-off threshold needs to be very close to zero. The SR voltage sensing and the comparator offset voltage have to be designed accurately. Furthermore, the comparator speed needs to be fast. SR needs to operate in sync with the diode conduction. If the SR turns off too late, there could be shoot-through current or circulating current, which will decrease the efficiency of the converter.

C. Based on Volt-Second Balancing

Instead of sensing very low voltage, some topologies can use volt-second balancing to achieve SR control [13]. One example would be a DCM flyback converter.

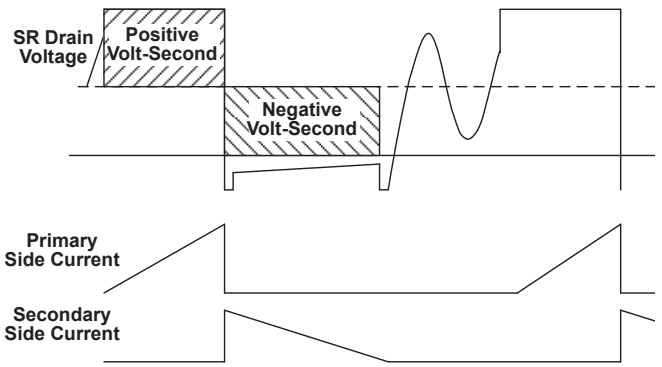


Figure 13 – DCM flyback SR control based on volt-second sensing.

DCM flyback converter operation waveforms are shown in Figure 13. In each switching cycle, the transformer inductor current rises from zero to its peak value and falls back to zero. Because the flyback transformer is a coupled inductor, its current represents the volt-second applied to it. Therefore, in each switching cycle, the volt-second also starts from zero and reaches its maximum value when the primary side switch turns off. During the secondary side conduction, the volt-second keeps reducing and turns back to zero when the secondary side current reaches zero. The transformer volt-second can be used to detect the turn-off of the SR. The volt-second can be captured through the voltage across the SR drain to source [13].

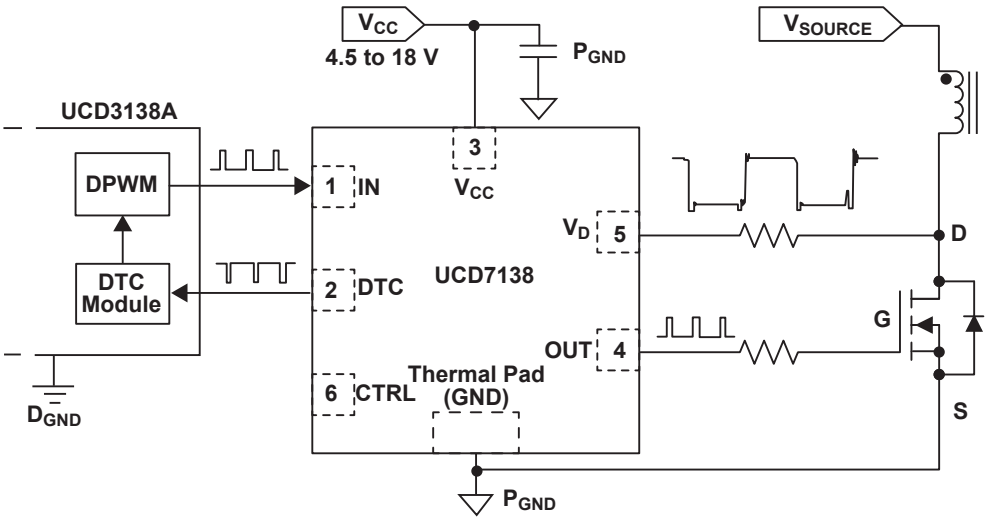
By using the volt-second balancing, the SR can be turned off at its current zero crossing. It senses the voltage across the SR drain-to-source during the off state to calculate the volt-second. Therefore, it does not require sensing of mV levels and is much less sensitive to the noise. The controller design challenges in this case are fewer.

However, it also has some limitations. The volt-second balance can only be used for certain topologies, such as the DCM flyback, the freewheeling diode in a DCM buck or DCM forward converter. In other topologies, such as a LLC resonant converter or active clamp flyback, the volt-second is not balanced. In addition, the volt-second can only be guaranteed to be balanced in DCM operation. In CCM operation, the volt-second balancing is only achieved in steady state. During line or load transients, the volt-second is not balancing and the SR control cannot be guaranteed. Since V_{DS} sensing does not have these limitations, it is a much more versatile control method.

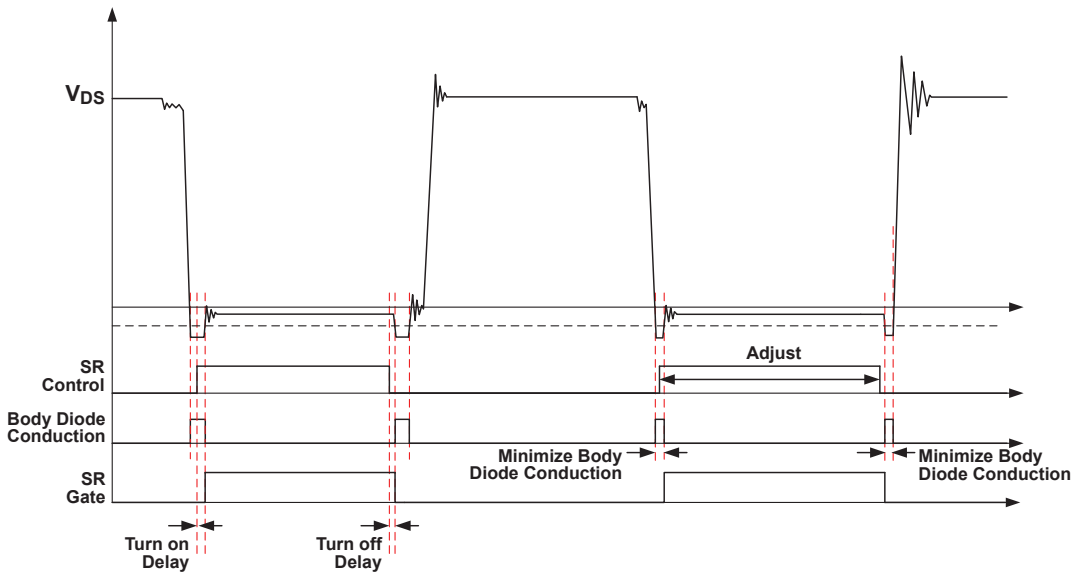
D. Adaptive Control

For V_{DS} sensing control, as mentioned earlier, to prevent the SR current from flowing negative at turn-off, the turn-off threshold needs to be set slightly negative. Considering the component tolerances, the SR is always turned off before its current reaches zero. After the SR turns off, the current continues to flow through its body diode. Because the body diode voltage drop is significantly higher than the SR drop, much higher loss is expected. This gets worse for higher switching frequency designs, when the total SR conduction time is short.

To minimize the body diode conduction time, an adaptive control method is proposed. Reference [14] gives one example. As shown in Figure 14, the SR driver measures the body diode conduction time and feeds it back to the digital controller UCD3138A. The digital controller can adjust the SR conduction time according to the body diode conduction time information and minimize the time. In this way, the SR is controlled very closely to the ideal synchronization with the diode conduction and achieves the best efficiency possible.



(a) Circuit diagram



(b) Operation waveforms

Figure 14 – Adaptive control for SR.

III. Design Challenges for SR Control

SR is an effective way of reducing the conduction loss of power converters, improving efficiency and thermal management. Detailed consideration and trade-offs are required to allow correct SR operation, optimize the performance and cost, as well as power management and EMI handling. In this section, the design challenges are discussed in detail.

A. SR MOSFET Selection

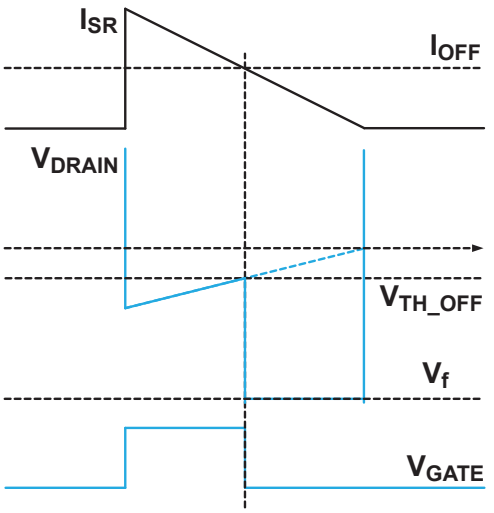
From the loss analysis, the conduction loss reduction is significant. The SR conduction loss is proportional to its on-state resistance ($R_{DS(ON)}$). Based on the equation, if the SR $R_{DS(ON)}$ becomes zero, the conduction loss is zero and the converter efficiency is maximized. Unfortunately, the reality is that this is not the right solution. Not only does the extremely low $R_{DS(ON)}$ device require much higher costs, it also introduces other issues and eventually hurts the efficiency [15].

The first issue is the body diode conduction. As mentioned earlier, to prevent negative current and in consideration of the component tolerances, the SR controller often sets the turn-off threshold slightly lower than zero, instead of right at zero. This forces the SR to turn off before its current reaches zero. Without considering other effects, the turn-off current can be calculated as

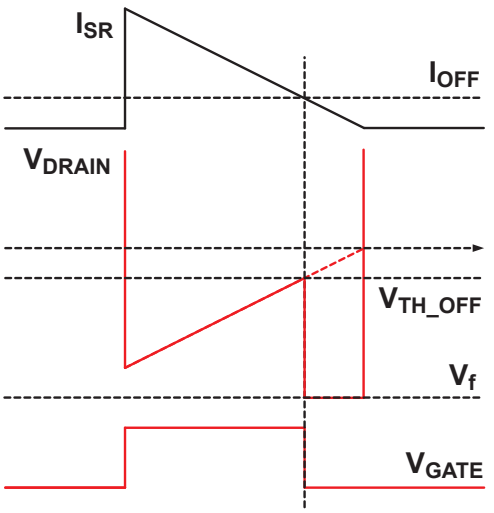
$$I_{OFF} = \frac{V_{TH(OFF)}}{R_{DS(ON)}} \tag{7}$$

In this equation, for a selected SR controller, the turn-off threshold $V_{TH(OFF)}$ is a fixed value. Lowering the $R_{DS(ON)}$ causes higher turn-off current. Figure 15 is an example of a DCM flyback converter using different $R_{DS(ON)}$ SRs.

For the lower $R_{DS(ON)}$ SR, with the same turn-off threshold, the turn-off current is much higher compared to the higher $R_{DS(ON)}$ SR. The conduction loss at the SR turn-on portion is lower because of the early turn-off and the body diode conduction time being longer. The SR overall conduction loss could be higher.



(a) Lower $R_{DS(ON)}$ SR



(b) Higher $R_{DS(ON)}$ SR

Figure 15 – DCM flyback using different SRs.

Let's use a 3 A DCM flyback design with a 50% secondary side conduction time as an example. The circuit parameters are summarized in Table 2. The lower $R_{DS(ON)}$ MOSFET causes higher conduction loss, even though it gets much less conduction loss when the SR is on.

	High $R_{DS(ON)}$ SR	High $R_{DS(ON)}$ SR
SR peak current	12 A	12 A
Turn-off threshold	-5 mV	-5 mV
SR $R_{DS(ON)}$	5 mΩ	1 mΩ
Body diode forward voltage drop	0.5 V	0.5 V
Turn-off current	1 A	5 A
Body diode conduction duty	4.2%	20.8%
$R_{DS(ON)}$ conduction loss	0.12 W	0.022 W
Body diode conduction loss	0.01 W	0.26 W
Total conduction loss	0.13 W	0.282 W

Table 2 – Design examples of different SR for DCM flyback.

The curve in Figure 16 shows the relationship between the conduction loss and different $R_{DS(ON)}$. At the beginning, when reducing the $R_{DS(ON)}$, the conduction loss gets lower, while the body diode conduction loss keeps increasing. There should be an optimal design point, based on the minimum conduction loss, that gives the tradeoff between the SR conduction and body diode conduction, for a given design.

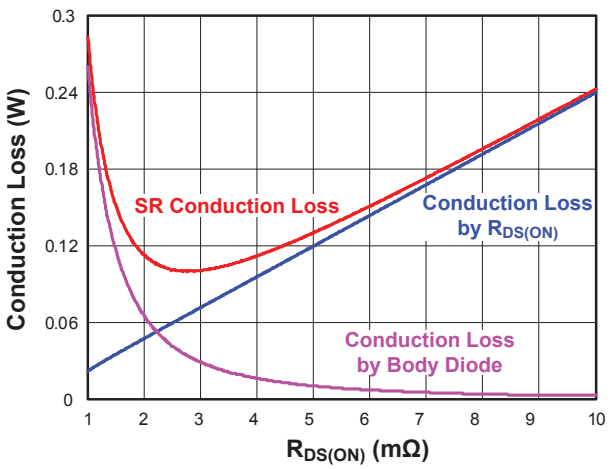


Figure 16 – Conduction loss for different $R_{DS(ON)}$ (assuming 3 A output current, 50% secondary side conduction duty-cycle, -5 mV turn-off threshold and 0.5 V body diode voltage drop).

The design optimization shown in Figure 16 only considers the conduction loss. The overall loss of the SR can be summarized in Equation 8.

$$P_{SR} = P_{CON} + P_{SW} + P_{DRV} \quad (8)$$

In this equation, P_{CON} is the conduction loss, P_{SW} is the switching loss, including the junction capacitor loss and the reverse recovery loss, and P_{DRV} is the driving loss.

The conduction loss portion was discussed earlier in this paper. The selection of the MOSFET needs to consider both the conduction loss of the SR conduction and body diode conduction.

For the switching loss, it includes the capacitive loss and reverse recovery loss, if the converter is operating in CCM. If the converter is operating in DCM condition, the loss can be simplified as the capacitive loss (C_{OSS} loss). For a flyback converter, due to the hard switching turn-on of the primary side switch, every time the switch turns on, it discharges the switch node capacitor. In the meantime, it charges the SR drain-to-source voltage to its maximum value. Therefore, the switching loss associated with a SR junction capacitor is calculated as

$$P_{SW} = \frac{1}{2} C_{OSS(eq)} \cdot V_{DS}^2 \cdot f_{SW} \quad (9)$$

In Equation 9, the worst case is considered where the SR voltage is charged from zero to full drain-to-source voltage. For a flyback converter operating in DCM mode, if the DCM ring is completely damped out, the SR voltage is charged from output voltage to its maximum voltage and Equation 9 changes into Equation 10.

$$P_{SW} = \frac{1}{2} C_{OSS(eq)} \cdot \left(\left(\frac{V_{IN}}{N_{PS}} + V_{OUT} \right)^2 - V_{OUT}^2 \right) \cdot f_{SW} \quad (10)$$

In this equation, $C_{OSS(eq)}$ is the energy based equivalent output capacitance, V_{IN} is the flyback input voltage, N_{PS} is the flyback transformer primary to secondary side turns ratio, V_{OUT} is the output voltage and f_{SW} is the switching frequency.

It is clear that the switching loss is directly proportional to the SR equivalent output capacitance. Larger SR MOSFETs (lower $R_{DS(ON)}$) have higher capacitance and in turn create higher switching losses. Depending on the ratio between conduction loss and switching loss at heavy loads, often the conduction loss dominates. At lighter loads, the switching loss becomes a more significant portion of the loss. Simply reducing the $R_{DS(ON)}$ of

the SR could result in less conduction loss at a heavy load but more switching loss on the lighter load.

Furthermore, the SR loss also includes the driving loss. Unlike a diode, the MOSFET needs to be turned on and off in each switching cycle as the SR gate voltage is charged and discharged. The loss associated with a gate driver is calculated in Equation 11. As with the C_{OSS}, the input capacitance also gets bigger with a lower $R_{DS(ON)}$ MOSFET.

$$P_{DRV} = C_{ISS} \cdot V_{DRV}^2 \cdot f_{SW} \tag{11}$$

When considering all the losses, conduction, switching and driving losses as illustrated in Figure 17, the overall performance has higher efficiency at a heavy load, but less efficiency at a lighter load for the low $R_{DS(ON)}$ MOSFET.

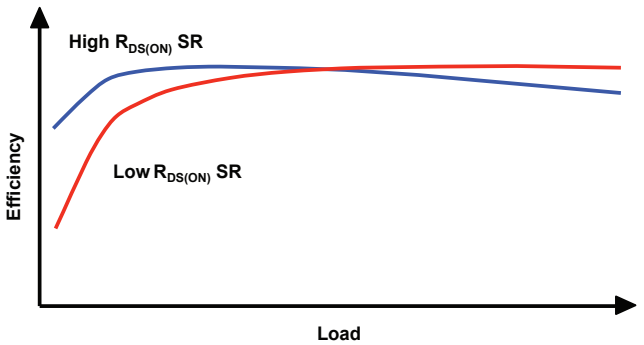
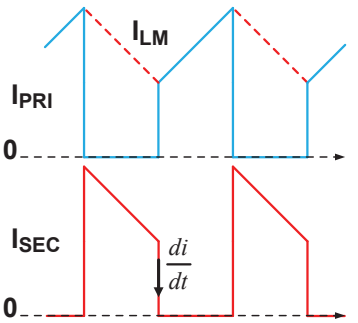


Figure 17 – Converter efficiency with different SRs.

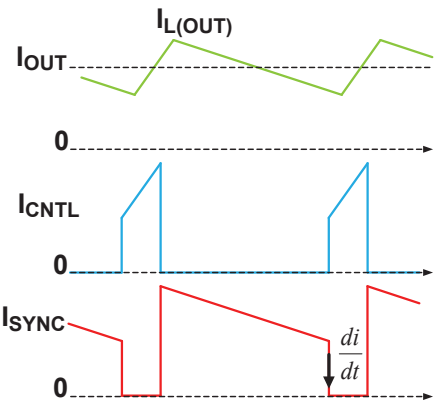
When the power supply is designed, efficiency has two significant constraints, thermal considerations and standards requirements. The converter must be efficient enough to manage the thermals and be higher than the efficiency standard requirement. As described in the introduction, the efficiency standard regulates the average efficiency, instead of full load efficiency alone. The power supply designer should optimize the design to deliver the lowest cost solution while meeting the standard. Even though the lower $R_{DS(ON)}$ MOSFET gives better efficiency at a heavy load, if it results in less efficiency at lighter loads and gives similar average efficiency, the higher $R_{DS(ON)}$ MOSFET should be chosen to get lower system costs. The selection of the SR is an iteration process that looks at the trade-off between cost and performance, instead of just simply assuming the lower $R_{DS(ON)}$ MOSFET gives the better performance [15].

B. Handling CCM Operation

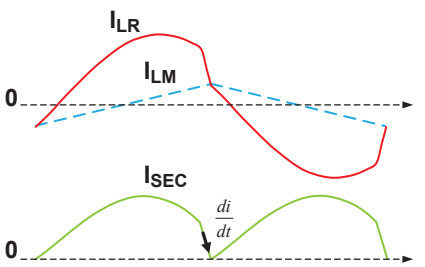
Previous discussions have mainly focused on the DCM operation and the reverse recovery loss is ignored. Converters operating in CCM mode help to reduce the conduction loss and achieve a smaller transformer size, and it is widely used in different designs. Before the SR turns off, the CCM operation mode gives a much higher current slew rate in comparison to the DCM operation. As a result, the V_{DS} sensing based SR control often encounters the shoot-through issue.



(a) Flyback converter



(b) Forward converter



(c) LLC converter

Figure 18 – Current slew rate for different converters operating in CCM mode.

Converter	Slew Rate
Flyback converter	$\frac{di}{dt}=\frac{V_O+\frac{V_{IN}}{N_{PS}}}{L_{LK}}$
Forward converter	$\frac{di}{dt}=\frac{\frac{V_{IN}}{N_{PS}}}{L_{LK}}$
LLC converter	$\frac{di}{dt}=\frac{V_O+\frac{V_{IN}+V_{CR}}{N_{PS}}}{\frac{L_R}{N_{PS}^2}}$

Table 3 – Slew rates for different converters operating in CCM mode.

Figure 18 summarizes the current slew rating in CCM conditions for different circuit topologies. It is observed that all the slew rates (di/dt) are determined by the leakage or the resonant inductance. Normally, the circuit designer tries to minimize the leakage to improve the transformer efficiency. A smaller leakage inductor forces the di/dt higher and introduces extra design challenges. Using CCM flyback as an example, the issue associated with the high current slew rate is illustrated in Figure 19. Before the primary side switch turns on, the SR keeps conducting and the magnetizing inductor discharges with the slew rate as shown in Equation 12 and in (a) of Figure 20. In this equation, L_M is the magnetizing inductor and N_{PS} is the transformer primary to secondary side turns ratio. It should be noted that the current decreasing rate is determined by the output voltage and the magnetizing inductor reflected to the secondary side.

$$\frac{di}{dt}=\frac{V_{OUT}}{L_M/N_{PS}^2} \qquad (12)$$

Once the primary side switch turns on, the secondary current is still positive and it takes time for the current to reach zero. During this period, the current slope changes to Equation 13. In this equation, the voltage increases to the summation of the output voltage and the reflected input voltage and the inductor changes into the leakage inductor reflected on the secondary side. Due to the higher voltage and much lower inductance, the current slew rate is much higher.

$$\frac{di}{dt}=\frac{V_{OUT}+V_{IN}/N_{PS}}{L_{LK}/N_{PS}^2} \qquad (13)$$

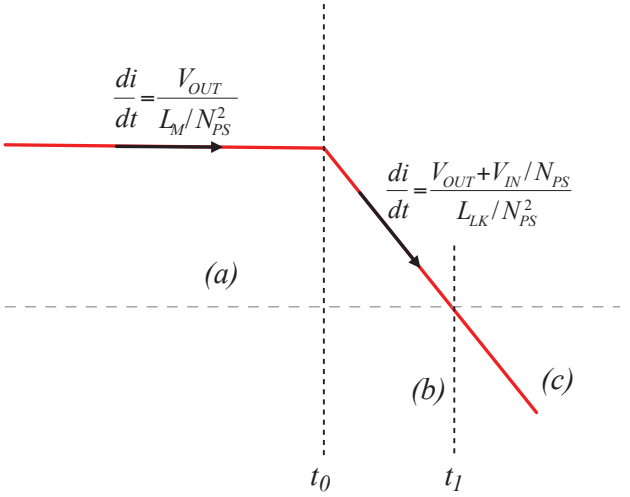


Figure 19 – Zoom in details of SR operation in CCM.

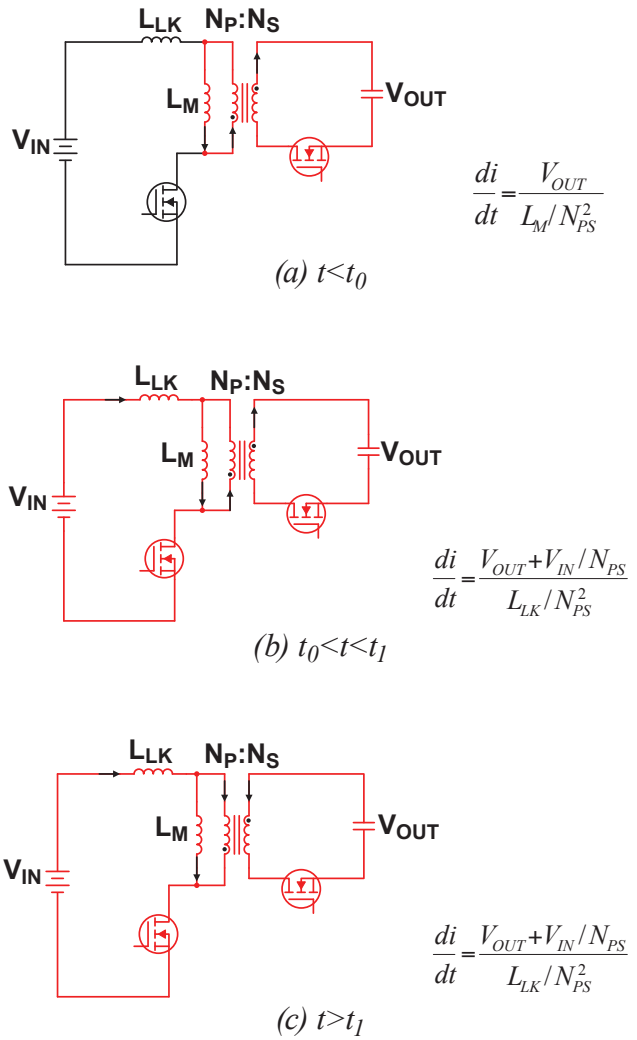


Figure 20 – Equivalent circuit at different stages of SR operation in CCM.

For example, a 15 W, 5 V/3 A output design with a 1 mH magnetizing inductor and 3% leakage, N_{PS}=15, at 165 V_{DC} input, equivalent to the peak of the 115 V_{AC} line, at the inductor discharge portion, the current slew rating is only 1.125 A/µs. During the CCM transition edge, the current slew rate becomes 120 A/µs, which is more than 100 times higher than the inductor discharge portion.

The issue associated with the high di/dt is the SR controller turn-off delay. In CCM operation, during the inductor discharge portion, due to the large conduction current, the SR turn-off threshold is not reached yet. SR is turned off at the fast transition edge. Because of the comparator and gate driver propagation delay, the SR can only be turned off 10 to 20 ns later after the V_{DS} crosses the turn-off threshold. With 120 A/µs current slew rate, the 10~20 ns delay means 1.2 A~2.4 A reverse current. This is quite similar to the reverse recovery of a diode. The reverse recovery behavior of a diode is shown in Figure 21. During the reverse recovery time, T_{RR}, diode current flows negatively and causes the shoot-through current [16]. When the diode current is positive, the voltage drop across the diode is its forward voltage drop. When the diode current crosses zero, it cannot block the voltage immediately. During the t_A portion of the reverse recovery time, T_{RR}, the diode voltage drop is still its forward voltage. The diode can only start to block the voltage during the t_B portion of the reverse recovery time. The t_A portion of the diode reverse recovery is equivalent to the SR turning off late for same amount of time.

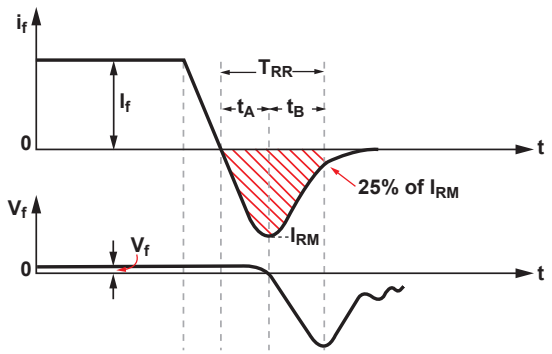


Figure 21 – Diode reverse recovery current.

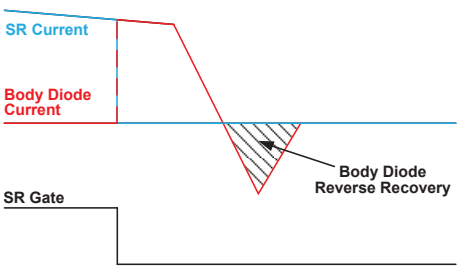
The loss caused by the diode reverse recovery can be quantified based on its reverse recovery charge Q_{RR}. Table 4 summarizes two different diodes with different Q_{RR} and different voltage during shoot through. The reverse recovery loss is calculated based on Equation 14. In this equation, Q_{RR} is the reverse recovery charge, V_{ST} is the shoot-through voltage, which in the flyback case is the output voltage plus the reflected input voltage, and f_{SW} is the switching frequency. To minimize the reverse recovery loss, the only choice is to choose a diode with less reverse recovery charge or a short reverse recovery time.

$$P_{RR} = Q_{RR} \cdot V_{ST} \cdot f_{SW} \tag{14}$$

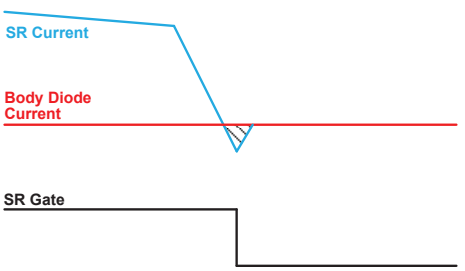
Since the delayed SR turn-off is equivalent to the diode reverse recovery, to minimize this effect there are several choices. As shown in Figure 22(a), after SR turns off, because the current is still flowing in the same direction, the current automatically shifts from the SR channel to its body diode. This way, even though it avoids the shoot-through caused by the delayed turn-off, the reverse recovery of the body diode still introduces a large amount of loss. Another option is to have the SR controller turn off the SR as fast as it can, as shown in Figure 21(b). In this case, the reverse recovery is caused by the SR turn-off delay. Due to the slow SR body diode, the fast turn-off often provides better performance.

	Q_{RR}	Reverse Recovery Loss
Diode 1 @ 30 V V_{DS}	127 nC	0.381 W
Diode 2 @ 75 V V_{DS}	385 nC	2.887 W

Table 4 – Diode reverse recovery loss estimation.



(a) SR turns off too early



(b) SR turns off too late

Figure 22 – Different SR timing in CCM operation.

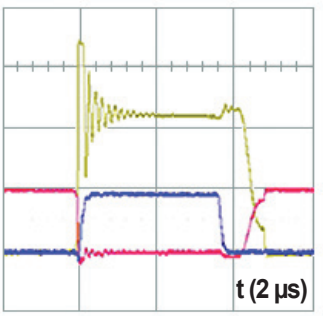
C. Dealing with Noise

The V_{DS} sensing-based SR control senses the voltage across the drain-to-source and detects the current direction. Because the SR $R_{DS(ON)}$ is used as a current sensing resistor, the turn-on and -off threshold is quite low. The low threshold makes the controller more sensitive to the noise and some blanking times are required for proper SR operation [12].

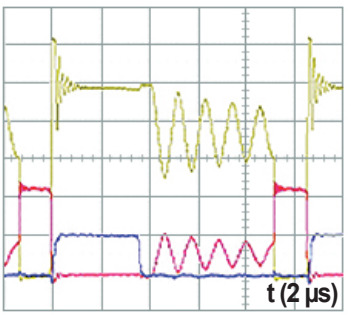
Continuing to use a flyback converter as an example, Figure 23 shows that at the SR turn-on edge the primary side leakage is resetting and large voltage ringing can be observed on the primary side switch node and SR drain voltages. Without proper blanking, the SR voltage could reach the turn-off threshold with this ringing and cause short SR conduction.

During the DCM operation, after the SR turns off, large voltage ringing is observed on both the primary side switch node and SR drain. If there is no damping, the SR drain voltage should resonate centered at the output voltage with the output voltage as the resonant amplitude. This large resonance could potentially pass the SR control turn-on threshold on the first or second resonant ring. If the SR turned on at the DCM ring, not only does it discharge the output energy into the transformer, causing extra efficiency loss, it will also extend the ringing duration and make the EMI noise worse.

To prevent false turning on and turning off, the blanking times are essential. Figure 24 illustrates the operation principles of blanking times. After the SR turns on, the turn-off of SR is prohibited until after the turn-on blanking time expires. If the turn-on blanking time is longer than the leakage reset time, or allows the ringing voltage to dampen out, the SR control can avoid the false turn-off. Following the same principle, the turn-off blank time can be used to avoid false turn-on at the DCM ring. After the SR is turned off, it cannot turn on again during the turn-off blanking time. The turn-off blanking time should be at least one DCM ring cycle to avoid the false turn-on. The turn-off blanking time should not be so big that it cuts into the SR normal conduction time. Some ICs allow the user to adjust this blanking time and achieve the balance between noise immunity and normal operation [12].



(a) SR turn-on noise



(b) SR turn-off noise

Primary Switch Node (100 V/div)
SR Drain (10 V/div) **SR Gate (5 V/div)**

Figure 23 – Noise associated with SR turning on and off.

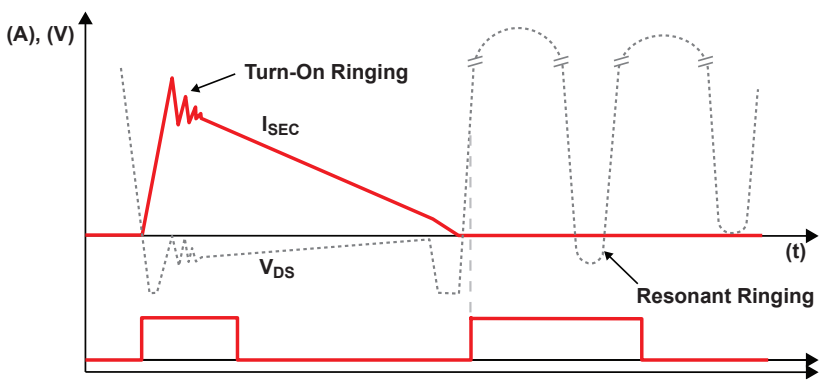


Figure 24 – Blanking times for proper SR control.

D. Special Current Shape

Besides avoiding the false turn-off at the beginning of the SR conduction, the minimum on-time also helps to deal with the special current shape, such as is observed in LLC resonant coverters. As shown in Figure 25, the SR current has a sinusoidal shape. Following the operation principle of V_{DS} sensing, after the current flows through the body diode, the SR control turns on the SR with a short delay. After that, the SR starts to conduct and due to the sinusoidal current shape, the SR current remains low. Since the SR current is small, the voltage drop could reach the turn-off threshold easily and causes the SR to prematurely turn off. To allow SR conduction with a full conduction angle, the minimum on-time can be used to force the SR on until the SR current reaches the high level. In this way, premature turn-off can be avoided.

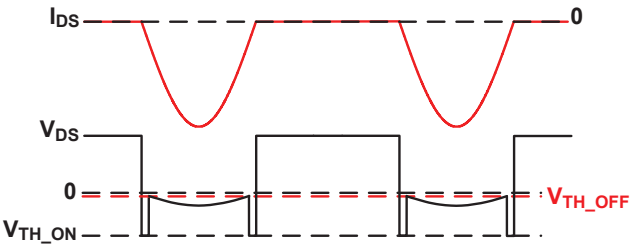


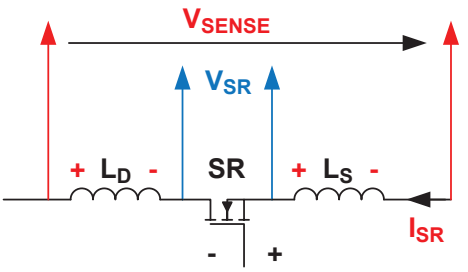
Figure 25 – LLC resonant SR waveforms.

E. Parasitic Inductor Impact

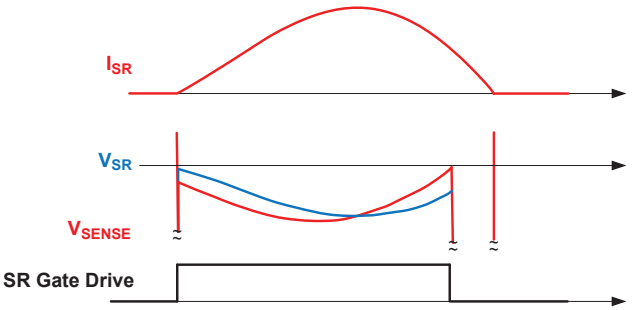
In the previous discussion, after the SR turns on, the voltage drop across the SR is considered as pure IR drop from the SR MSOFET $R_{DS(ON)}$. Depending on the SR MOSFET package, the voltage across the SR not only includes the voltage from the resistive drop, but also from the voltage drop across the parasitic inductance. The parasitic inductance can be the contribution from both the trace inductance from the layout and the package inductance. The inductor caused by the trace inductance can be eliminated with a proper layout. However, the package inductance cannot be eliminated [17][18].

Figure 26(a) shows the SR voltage drop with the package inductances. For the SR controller, it senses the voltage, V_{SENSE}, which is the combination of voltage across the $R_{DS(ON)}$ (V_{SR}) and the voltage across the drain inductance (L_D) and source inductance (L_S). The sensed voltage is calculated using Equation 15.

$$V_{SENSE} = V_{SR} + V_{LD} + V_{LS} = -\left[I_{SR} \cdot R_{DS(ON)} + \left(L_D + L_S\right) \cdot \frac{dI_{SR}}{dt} \right] \quad (15)$$



(a) SR with parasitic inductor



(b) SR voltage and controller sensed voltage

Figure 26 – Parasitic inductor impact on the V_{DS} sensing.

From Equation 15, the effects of the parasitic inductance are seen. When dI_{SR}/dt is positive, the voltage drop across the inductor is of the same polarity as the resistive drop, and the voltage across SR appears as higher current flowing through the SR. On the other end, when the dI_{SR}/dt is negative, the voltage drop across the inductor adds onto the offset voltage in reverse polarity, compared to the resistive drop, and the sensed voltage appears to have less current flowing through the SR.

As illustrated in Figure 26(b), for a LLC resonant converter SR, when the current slew rate is positive, the sensed SR voltage appears to have more voltage drop and when the current slew rate is negative, the sensed SR voltage appears to have less voltage drop. The decreased voltage drop could cause the SR controller to make the wrong decision and turn on the SR early.

Let's look at an example. For a LLC resonant converter, assuming it operates at the resonant

frequency and the SR current can be approximated as a sinusoidal waveform, the SR current in each SR can be written as in Equation 16.

$$I_{SR}(t) = \frac{\pi}{2} \cdot I_{OUT} \cdot sin(2\pi t) \quad (16)$$

For a 10 A output current, at 100 kHz switching frequency, the current slew rate varies from -10 A/µs to 10 A/µs. If we choose 5 A/µs as the operation point, for a typical TO-220 package with an inductance of about 12 nH, the di/dt could cause 60 mV offset. This is much higher than the turn-off threshold and would cause the SR to turn off much too early. This offset gets much worse if the di/dt is higher, such as in higher power or higher frequency designs. To avoid the SR early turn-off caused by the package inductor, a MOSFET package with less package inductance is preferred. Besides, the smaller package inductance MOSFETs can be used in parallel with the high package inductance MOSFET as a sensing FET to reduce the impact from the package inductance.

MOSFET Package	Drain Inductance (L_D)	Source Inductance (L_S)
TO-220 [19]	4.5nH	7.5nH
D2PAK [20]	3.5nH	7.5nH
DPAK [21]	0.0164nH	2.85nH
SO-8FL [22]	0.005nH	1nH

Table 5 – Typical SR MOSFET package inductance.

F. Proportional Gate Drive

Besides using smaller package inductance, the early turn-off can also be mitigated by using the proportional gate drive.

When the SR is driven with voltages much higher than its threshold voltage, its voltage drop is proportional to its on-state resistance. When the gate driver voltage is reduced, the voltage drop across the SR could be much higher for the same drain current, as shown in Figure 27.

Instead of fully turning on the SR all the time, the SR gate voltage can be reduced when the SR current level is low. The SR gate voltage is controlled so that the voltage across the SR becomes a fixed voltage drop, instead of an I-R

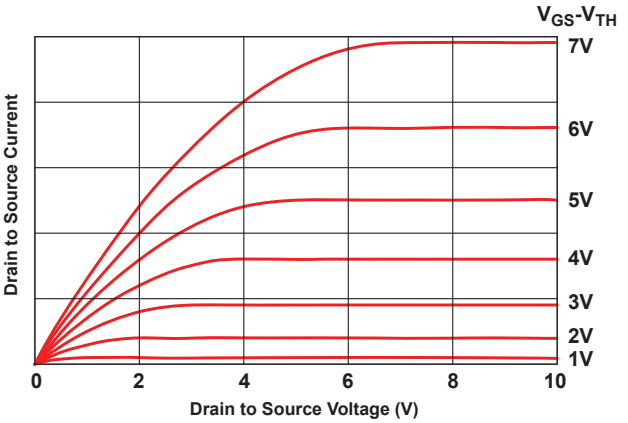


Figure 27 – SR MOSFET V-I characteristic curves.

drop. The SR behaves likes a diode with a much lower voltage drop in this period. Since the voltage drop is fixed, it becomes higher than the resistive drop and causes more loss. However, the sacrifice on the conduction loss brings a few benefits. The SR control with proportional gate drive is shown in Figure 28. First, this regulation allows longer conduction time for the lower $R_{DS(ON)}$ SR MOSFET, even with the offset voltage caused by the package inductance. Because of reduced body diode conduction time, it could help the converter efficiency. Second, during the proportional gate drive activated region, the SR gate voltage is very close to its threshold. For CCM operation, this allows the SR to be turned off fast without considering the time delay from discharging the gate voltage to the threshold voltage. This helps to minimize the shoot-through and improve the performance in CCM operation [23].

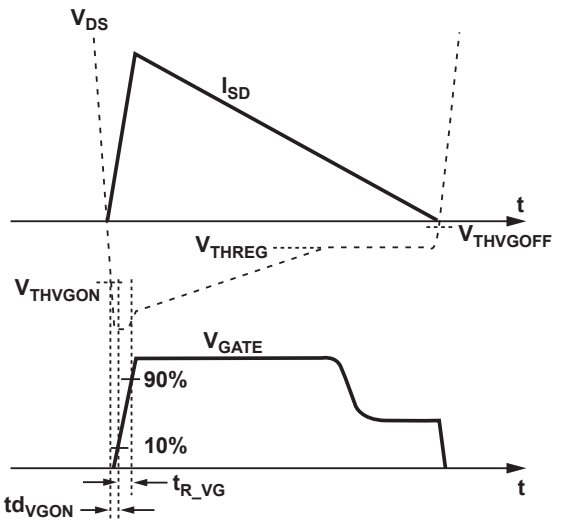
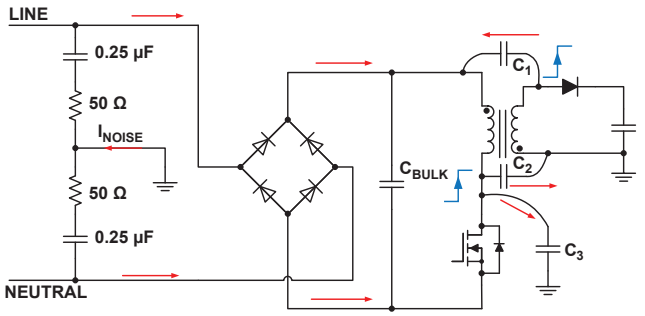


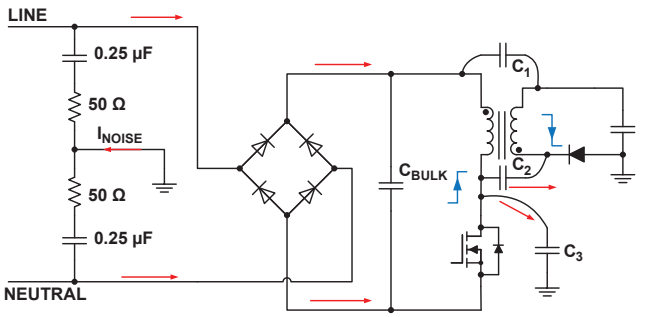
Figure 28 – Proportional gate drive.

G. EMI Noise Considerations

For a simple flyback converter, the output rectifier can be located on the positive side, as shown in Figure 29(a), or the negative side, as shown in Figure 29(b). From the operational point of view, these two rectification methods make no difference, but they have EMI noise behaviors.



(a) Flyback with high-side rectification



(b) Flyback with low-side rectification

Figure 29 – Natural EMI noise cancellation of flyback converter.

The EMI noise, especially the common mode EMI noise, is largely affected by the circuit parameters. As shown in Figure 29(a), the common mode noise measured by the LISN 50 Ω resistor is generated by the primary side switch node voltage fluctuation. For the rectifier located on the positive side, when the switch node steps high, the positive dv/dt causes a pulse current flowing from the primary to secondary side through the parasitic capacitor C_2. At the same time, when the switch node steps up, the node on the rectifier anode also steps high. This causes a pulse current flowing from the secondary side to primary side through the parasitic capacitor C_1. Since the currents flowing through C_1 and C_2 are in reverse polarity, they cancel each other and result in less common mode EMI noise.

When the rectifier is in the negative path, as shown in Figure 29(b), there is no current flowing through C_1 because both sides of C_1 have a stable voltage potential. In this case, the primary side node steps up and the secondary side rectifier cathode steps down. This causes much higher current flowing through C_2. With higher capacitor current and no current to cancel it out, the common mode EMI noise is expected to be worse.

The same analysis can be applied to the SR case and draws the same conclusion. Even though the common mode EMI noise performance for the SR located in the negative path is worse, because the SR controller can be easily powered up and drive the SR MOSFET, it is still an attractive solution. The power supply designers need to use other EMI mitigation methods, such as the cancelation winding, EMI filters, etc., to address the EMI noise challenge [24].

H. Bias Power Considerations

Unlike the diode rectifier, the SR MOSFET needs to be actively controlled. How to power up the controller and drive the SR MOSFET becomes a new challenge for power supply designers.

As shown in Figure 30, the SR can be directly driven when it is on the negative path; this is also called low-side configuration since the SR is located on the low-side. In this way, the SR source, controller ground and output negative bus are sharing the same node. Because of the common ground, the IC is less sensitive to noise. Furthermore, the SR controller can be directly powered by the output voltage, if the output voltage is within the IC power supply range. This provides the most efficient path to power up the controller IC. However, as mentioned in the previous section, when SR is located on the positive path (high-side configuration), there is some common mode EMI noise benefit.

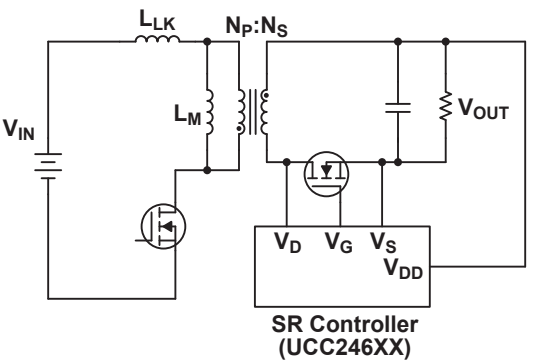
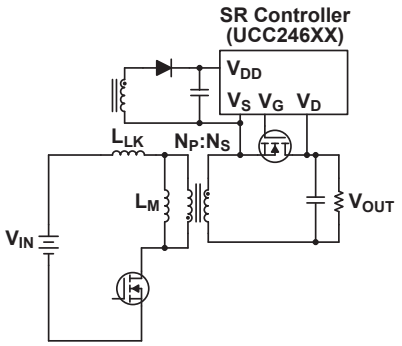


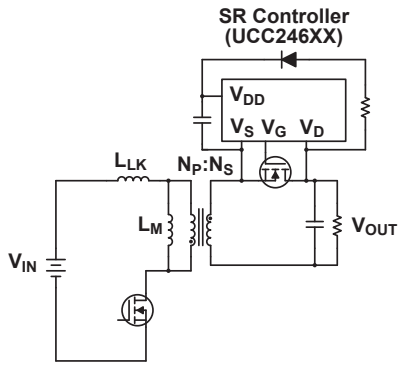
Figure 30 – Low-side SR configuration.

The first challenge of the high-side configuration design is the SR controller ground is now connecting on the secondary side switch node. The high dv/dt can cause noise and affect the IC operation. The design needs to be carefully done and the copper area of the IC ground path needs to be minimized.

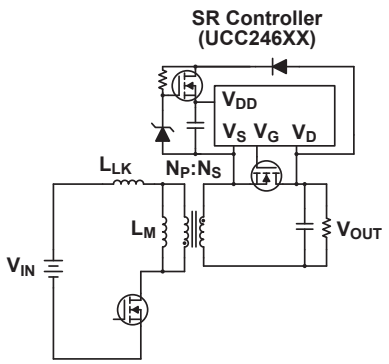
Besides the switch node noise, powering up the IC also becomes a challenge. As illustrated in Figure 31, the SR controller can be powered through the auxiliary winding, the RCD circuit or the pulse linear regulator.



(a) Aux winding



(b) RCD circuit



(c) Pulse linear regulator

Figure 31 – Different methods of powering high-side SR.

The auxiliary winding voltage is basically the output voltage reflected on it. Therefore, the controller operates very similarly to be directly powered from the output voltage.

Another method is to power the controller from the SR drain. The drain voltage is filtered out as a voltage source and powers up the controller. There are several limitations to this method. First, the voltage level changes with the input voltage and load condition. For a flyback converter, the SR drain voltage is the sum of the output voltage and the reflected input voltage. When the input voltage changes, especially for the universal input voltage range, the drain voltage has large variations. The RC filter could also get the average voltage across the SR drain, and reduces the voltage variation. In the meantime, the average voltage is largely affected by the converter load condition. Often, the circuit needs a Zener clamp to help limit the voltage range. The voltage variation is addressed through the pulse linear regulator shown in Figure 31(c). Since the pulse linear regulator gate is clamped by the Zener voltage, its output is a well-regulated voltage regardless of line and load conditions.

In addition to the voltage variation, the power conversion efficiency is worse when the SR controller is powered from the SR drain. For a typical 20 V output flyback converter, assume 4:1 transformer turns ratio, 1 mA of controller current and 23 nC of gate charge switching at 100 kHz. When the input voltage is 325 V, which is equivalent to 230 V AC peak, the total charge required for the SR operation in each switching cycle is

$$Q_{CYC} = \frac{I_{IC}}{f_{SW}} + Q_G = \frac{1\ mA}{100\ kHz} + 23\ nC = 33\ nC \tag{17}$$

The total power consumed from the SR drain is

$$\begin{aligned} P_{CNTL} &= Q_{CYC} \cdot V_{DS} \cdot f_{SW} \\ &= Q_{CYC} \cdot \left(\frac{V_{IN}}{N_{PS}} + V_{OUT} \right) \cdot f_{SW} = 0.334W \end{aligned} \tag{18}$$

At the same time, if the SR is located on the low-side and the IC is powered from the output, the IC power consumption is

$$P_{CNTL} = Q_{CYC} \cdot V_{OUT} \cdot f_{SW} = 66mW \tag{19}$$

Comparing Equations 18 and 19, the low-side configuration gives much lower power consumption and better efficiency. The power supply designers have to pick the trade-off between EMI noise and the power consumption.

I. Standby Mode

As discussed earlier, the efficiency standard not only demands higher average efficiency, it also limits how much power the power supply consumes in standby mode when there is no load connected. Even though the standard is quite loose, 75 mW for CoC and 100 mW for DoE for power supplies less than 75 W, some other applications, such as cell phone chargers, are demanding much lower standby power. As shown in Figure 32, the cell phone industry is looking for solutions that provide less than 30 mW standby power to achieve a five-star rating [25]. In general, when the analog IC is in active mode, it consumes roughly 1~2 mA of current. With a 5 V output, that is 5~10 mW, which is a big portion of the 30 mW standby power. This is the same for other applications, such as notebook adapters: for a 20 V output, 1 mA of IC current consumption results in a 20 mA load that makes meeting the 75 mW standby power mode a challenge.

To lower the SR controller power consumption, the SR controller needs to have built-in intelligence and enters low power mode during standby mode to consume minimum current. The SR controller needs to maintain its intelligence so that it can resume normal operation when the load is back to the normal level.

The load level detection can be implemented through the SR conduction time-based or SR switching frequency-based methods.

Figure 33 illustrates the SR conduction time-based standby mode detection, as implemented in

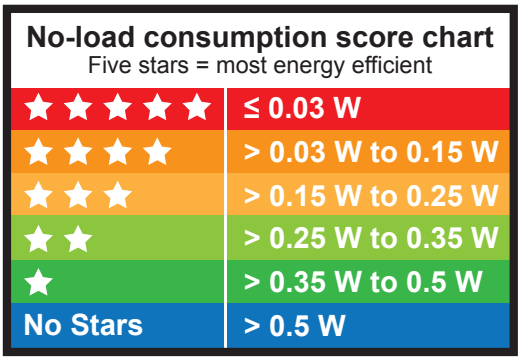


Figure 32 – Five-star standby power.

UCC24610. The SR conduction time is compared with a fixed time. If the SR conduction time is smaller than the minimum conduction time, the controller detects it as a low load condition and puts the SR controller into low power mode, reducing its power consumption. It continuously monitors the SR conduction time and resumes normal operation when the SR conduction time becomes longer than the pre-set minimum conduction time. The key design consideration of this control method is that the controller cannot be woken up in the middle of a switching cycle.

The time-based standby mode detection works well when the conduction time is proportional to the load. With the higher efficiency requirement for the light load, the latest controllers use burst mode to improve the light load efficiency. The burst mode forces the converter to operate in the on/off mode. During the on-period, the converter operates with higher power and higher efficiency. During the off-period, the converter consumes no power. In this way, the converter maintains higher efficiency at a lighter load. The converter power is adjusted through the ratio between the on-period and off-period. Because of the burst mode control, the SR conduction time is no longer related to the load level at burst mode.

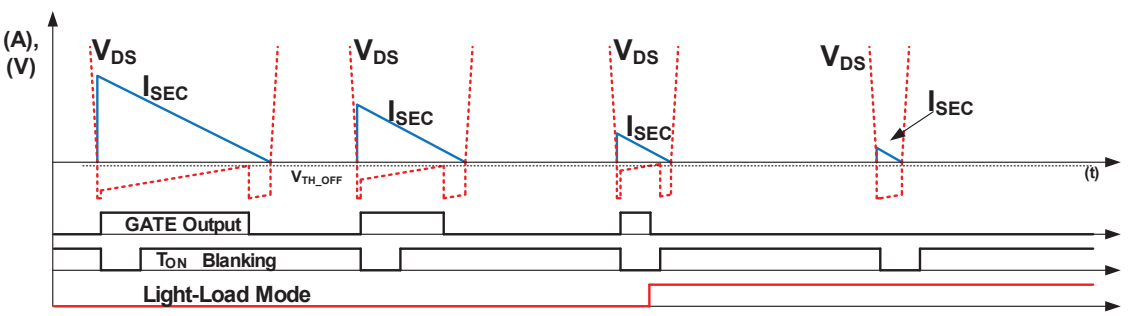


Figure 33 – SR conduction time-based standby mode detection.

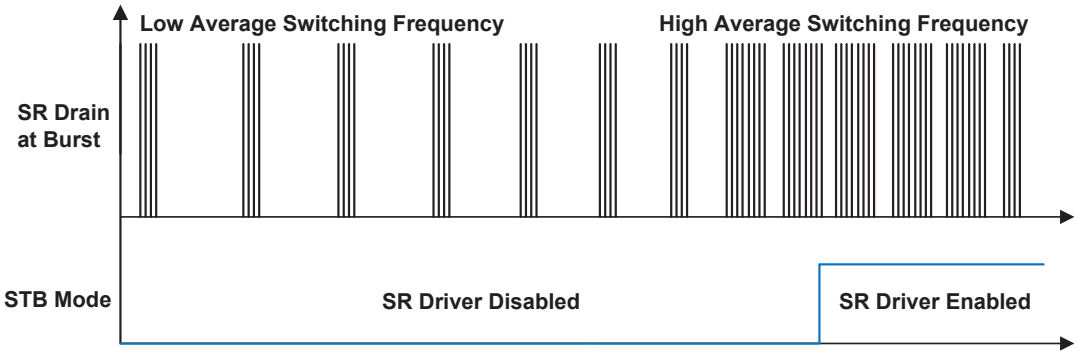


Figure 34 – Switching frequency-based standby mode detection.

To allow the standby mode detection without using the SR conduction time, the switching frequency-based method was proposed and implemented in UCC24630. The control principle is based on the average switching frequency of the converter. When the average switching frequency is lower than the preset threshold, the converter power level is low enough to enter the standby mode. In burst mode, the power level is related more to the average switching frequency than the SR conduction. The switching frequency-based standby mode detection works more reliably for the burst mode control.

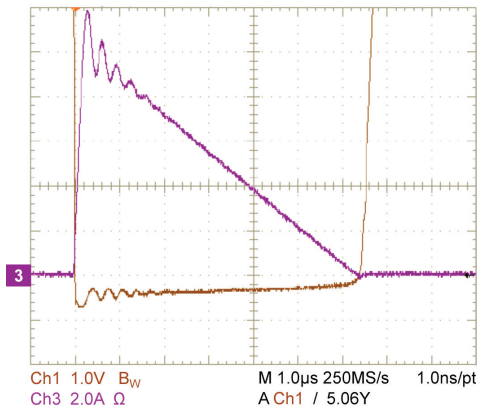
IV. Design Example

The UCC28740 EVM was used to demonstrate the efficiency improvement by using a synchronous rectifier. The key circuit parameters of UCC28740EVM-525 [26] are summarized in Table 6. The original EVM used two SBR10U45SP5 diodes in parallel as the output rectifier. The SR MOSFET CSD19531Q5A has 5.3 mΩ $R_{DS(ON)}$ at 10 V V_{GS}.

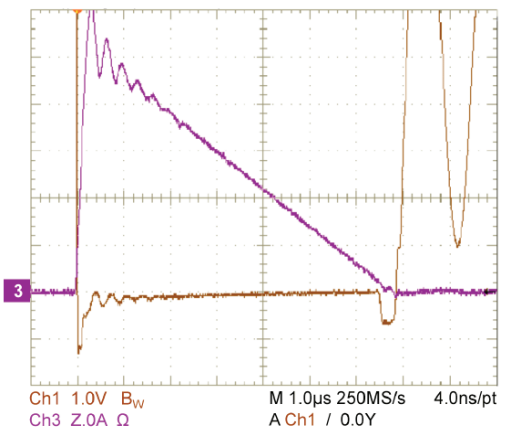
Parameter	Test Conditions	Min	Nom	Max	Units
Input Characteristics					
Voltage range, V_{IN}		85	115/ 230	265	V_{RMS}
Line frequency		47	60/ 50	63	Hz
Output Characteristics					
Output voltage, V_{OUT}	$V_{INmin} \le V_{IN} \le V_{INmax}$, 0 A $\le I_{OUT} \le I_{OUTmax}$	4.85	5	5.15	V
Output load current, I_{OUTmax}	$V_{INmin} \le V_{IN} \le V_{INmax}$	1.995	2.1	2.205	A

Table 6 – UCC28740EVM-525 electrical performance specifications.

Using analysis on different control methods and design considerations, Figure 35 shows the voltage drop and current for the diode rectifier and the SR rectifier. From these waveforms, the turn-on ringing, the early turn-off and the loss reduction are observed by comparing the SR with the diode.



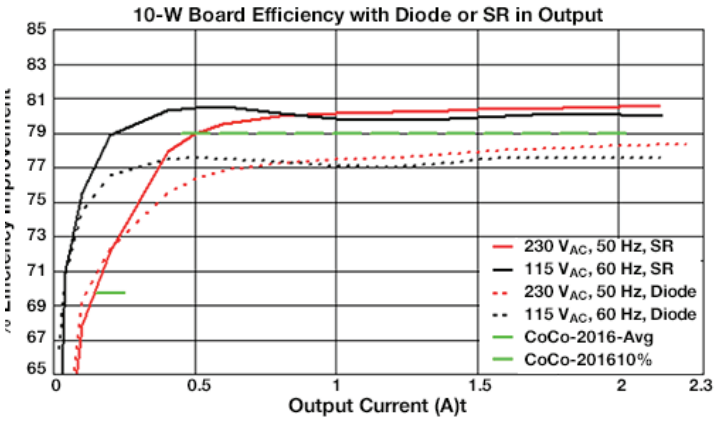
(a) Diode rectification



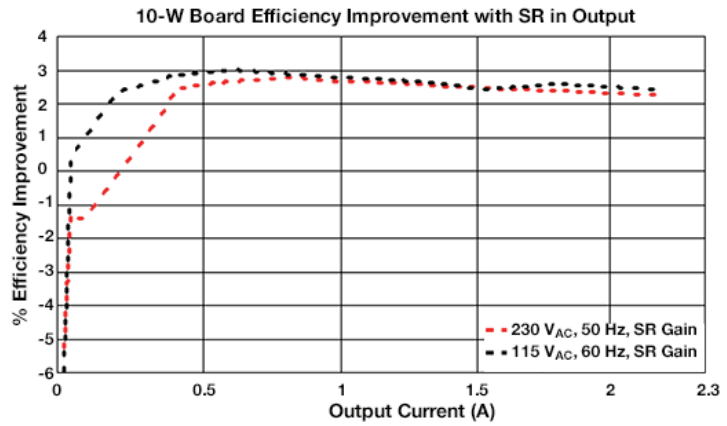
(b) SR rectification

Figure 35 – Voltage and current for different rectification methods.

The efficiency performance using the diode rectifier and synchronous rectifier are summarized in Figure 36. Around a 3% efficiency gain as well as much higher overall efficiency is observed by using a synchronous rectifier.



(a) Efficiency performance comparison



(b) Efficiency gain by using SR

Figure 36 – Efficiency performance summary.

V. Summary

With the demand for higher efficiency and higher power density, replacing the rectifier diode with a synchronous rectifier provides an easy and straight forward method to reduce the conduction loss and improve the efficiency. With different control methods, the V_{DS} sensing-based control method is the most popular one. This paper discussed the different design challenges of SRs and SR control, including the SR FET selection, noise immunity, standby mode detection, etc. All this analysis helps to pick the correct SR and SR control for more efficient power supplies.

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