Power Solutions for Class-D Audio Amplifiers

Reproduced from
2018 Texas Instruments Power Supply Design Seminar
SEM2300,
Topic 4
TI Literature Number: SLUP382

© 2018 Texas Instruments Incorporated

Power Supply Design Seminar resources
are available at:
www.ti.com/psds
Power Solutions for Class-D Audio Amplifiers

Roberto Scibilia and Matthias Ulmann

ABSTRACT

Today, the most popular medium and high power audio amplifiers employ a Class-D working scheme due to high efficiency and excellent linearity. Compared to traditional analog amplifiers, Class-D uses high frequency pulse width modulation, similar to a switch mode power supply. Even though Class-D amplifiers incorporate negative feedback on supply voltage, the reality is that the output impedance of the power supply has an impact on audio quality. This topic describes how to properly design a power supply for a high power Class-D amplifier based on the output impedance requirements as well as on typical requirements like average and peak power demands. Two different built and tested power reference designs are introduced. The first is for a universal AC/DC input suitable for home theatre, monitor and soundbar applications. The second solution covers high power automotive applications rated to several hundred watts.

I. Audio Basics

For a long time, audio amplifiers have been pure analog, using different configurations. The simplest configuration is the Class-A (Figure 1) with a positive supply voltage, using a single bipolar transistor operated in the linear region. It is heavily biased so that it conducts the positive and the negative part of the waveform. To avoid damage of the input source and the speaker, coupling capacitors are needed on the input as well as on the output of the amplifier to remove the DC part of the signal which is added by the biasing circuit. This circuit provides the lowest distortion as well as the lowest efficiency and is typically used in low-power applications. It is also important to mention that the output signal is inverted (phase-shifted 180 degrees) to the input signal.

To overcome the problem of low efficiency, an NPN- and PNP-transistor are used in the Class-B amplifier (Figure 2). It is a “push-pull” configuration where the upper transistor conducts for the positive and the lower transistor for the negative part of the waveform. This is possible because it is supplied by a positive and negative supply voltage. This configuration does not need any biasing, but the transition at zero-crossing causes distortion. When an audio signal is applied which is not high enough to bias the transistor to make it conduct, this part is not amplified and therefore not present at the output. This missing part causes a distortion of the overall audio signal and has a negative impact on the audio quality. Compared to a Class-A amplifier, efficiency is much better and the signal is not inverted.

Figure 1 – Class-A.

Figure 2 – Class-B “push-pull”.
The Class-AB amplifier is a combination of Class-A and Class-B to overcome the drawbacks, like low efficiency and distortion issues. The Class-B amplifier is extended by adding a biasing circuit to make both transistors conduct for slightly more than half of the waveform. Distortion at zero-crossing is eliminated because the transistors are slightly biased to get them to the beginning of the linear region. Biasing is achieved with several methods such as resistor dividers or diodes. Class-AB is the standard for medium and high power analog amplifiers as they provide high linearity and good efficiency at the same time.

![Figure 3 – Class-AB “push-pull”](image)

A big jump in efficiency is achieved with a Class-D amplifier (Figure 4).

![Figure 4 – Class-D](image)

Compared to the previously shown amplifier configurations, the Class-D amplifier is based on a switched approach almost identical to a synchronous buck converter. The only difference is that instead of a fixed reference voltage, the input audio signal is compared to the triangle waveform of the pulse width modulator (Figure 5).

![Figure 5 – Class-D waveforms](image)

The duty-cycle changes with the input signal, but the average is 50%. That means the output voltage is the amplified audio signal plus one half of the supply voltage. To keep DC from the speaker, a coupling capacitor is needed on the amplifier output. Class-D amplifiers incorporate negative feedback to compensate for supply voltage variations and to improve the linearity. The main part of the losses is caused by the switching losses of the FETs, especially at high supply voltages. Modern Class-D amplifiers can achieve an efficiency of 90% or even more. If this type of amplifier is supplied by a variable input voltage, it is called a Class-G amplifier. The purpose of Class-G amplifiers is to increase the efficiency at low power. The switching losses due to $C_{\text{oss}}$ (output capacitance of switching FETs) are always constant and just dependent on the supply voltage. Even if no signal is applied to the input, these switching losses are the same as at full load. Now, if only low power is needed, the supply voltage can be reduced significantly to reduce the losses while still maintaining the audio level on the output.

Dependent on the power range, different Class-D configurations are used. Multi-channel systems with moderate power typically use the single-ended (SE) configuration (Figure 6) in which one speaker is connected to each half-bridge. One-half of the supply voltage is seen after the LC filter, therefore the maximum voltage swing of the audio signal is also only half of the supply voltage.
The parallel bridge-tied load (PBTL) configuration (Figure 8) is almost identical to the BTL configuration, but in this case two outputs are connected in parallel. The voltage swing remains the same, but the current capability is doubled. It offers eight times the power compared to the SE configuration and is mainly used for high power subwoofers with 2 Ω impedance.

The configuration of the amplifier depends not only on the power but also on the impedance of the speaker. Typical impedances are 4 to 16 Ω for home audio applications and 2 to 4 Ω for car Hi-Fi. The impedance is an indication of the speaker’s AC resistance and the nominal impedance is usually determined at the lowest point after resonance as shown in Figure 9.

A speaker’s impedance curve is not linear, which can cause problems. It is important to match the amplifier and speaker impedance to avoid a non-linear frequency response as well as to avoid overloading the output stage of the amplifier. For example, when using passive crossovers in multi-way speakers the impedance reaches minimum values below 2 Ω, which needs to be compensated. This is done by a so called “Zobel” network (Figure 10) to achieve a flat impedance curve for the required frequency range of the speaker.
There is a trend to use higher speaker impedances to reduce the weight of the wire harness. For the same amount of power, a high impedance speaker needs lower current but higher voltage compared to a low impedance speaker. Typically, the maximum supply voltage of a Class-D amplifier is around 50 V to stay below dangerous voltage levels without the need for special isolation and protection. With 50 V supply voltage in BTL mode, the peak power is 156 W on 16 Ω impedance and 625 W on 4 Ω impedance.

But the peak power is only one parameter of an audio amplifier. Another important parameter is the continuous RMS power capability. Both parameters are connected by the crest factor (C). Figure 11 shows the crest factor visually. The RMS audio level is relatively low compared to the large peaks.

As can be seen in the picture and table above, the difference between the RMS and peak value can be quite large and one speaks of a large dynamic range. In some areas, for example broadcast, it is essential to have a rather uniform volume for good audibility. This is achieved by using audio compression to decrease the dynamic range of an audio signal by reducing the peaks. Thereby the crest factor is reduced which in turn balances the volume. As now the dynamic range of the audio signal itself is reduced, it is increased to fill the dynamic range of the audio channel again. With these two steps, the peaks are reduced and the RMS value is increased, therefore the signal itself sounds louder. This is an effect one can often hear if an older recording without compression is compared with a modern recording using audio processing techniques.

The crest factor plays a very important role in the design of a power supply for an audio amplifier and corresponds directly to its average and peak power capabilities. The average power of the power supply corresponds to the RMS power capabilities of the amplifier. The peak power needs to be identical. The average and peak power impacts the part selection of the power stage as well as other parameters like those shown in Table 2.

![Figure 11 – Crest factor.](image)

The crest factor is either specified as a ratio or in dB.

\[
C = \frac{P_{\text{peak}}}{P_{\text{RMS}}} \quad \text{and} \quad C_{\text{dB}} = 20 \cdot \log_{10} \frac{P_{\text{peak}}}{P_{\text{RMS}}} \tag{1}
\]

Typical crest factors for various signal types are shown in Table 1.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Crest Factor</th>
<th>C_{dB}</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ambient noise</td>
<td>3 : 1</td>
<td>10 dB</td>
</tr>
<tr>
<td>Speech</td>
<td>4 : 1</td>
<td>12 dB</td>
</tr>
<tr>
<td>Music with peak level compression</td>
<td>4 : 1 to 8 : 1</td>
<td>12 to 18 dB</td>
</tr>
<tr>
<td>Music without peak level compression</td>
<td>8 : 1 to 10 : 1</td>
<td>18 to 20 dB</td>
</tr>
<tr>
<td>Movie audio</td>
<td>&gt;10 : 1</td>
<td>&gt; 20 dB</td>
</tr>
</tbody>
</table>

![Table 2 – Impact of crest factor on power supply design.](image)
II. IMPACT OF POWER SUPPLY ON AUDIO PERFORMANCE

There are several key parameters that define the quality of an audio amplifier, and in particular Class-D. The four main parameters are: transient distortion, frequency response, power supply (PSU) output impedance matching with audio amplifier input impedance and power supply ripple rejection (PSRR).

The transient distortion is an unwanted behavior of closed-loop Class-D amplifiers, due to non-ideal loop compensation. The top picture of Figure 12 shows an underdamped transient response which ideally should be a square wave. The frequency response should be, of course, wider than the audible frequency band, which nowadays is fairly easy to achieve thanks to high switching frequency. The PSRR is directly related to the output impedance of the power supply. All of the previous parameters impact what is probably the most important one: THD (total harmonic distortion), which is defined as the ratio of the contribution all the harmonic components to the value at the fundamental frequency:

$$THD = \sqrt{\frac{V_2^2 + V_3^2 + V_4^2 + \cdots + V_N^2}{V_1}}$$

Even though speakers in cheap systems are usually the bottleneck regarding the total THD of an audio system, Class-D amplifiers showing THD values lower than 0.025% are considered high-quality, while 0.1% can be accepted as maximum performance degradation due to low-cost optimization.

The scope of this topic is to find a relationship between the output impedance of the power supply, which energizes the Class-D audio amplifier and THD. The main question is: how does this impedance impact the quality and, in this case, the THD of such an amplifier?

To figure it out, a set of measurements was performed on a Class-D amplifier, connected in BTL (bridge-tied load) mode. The ability of the amplifier to reject the noise, present on its own VDD, was measured by superimposing a noise frequency (in this case e(s) = 250 Hz) directly to the power VDD of the amplifier, according to Figure 13.
The main audio signal was set to 1 kHz \( (f_{\text{AUDIO}}) \) and the result is shown in Figure 14. The fundamental is named “1” and shows the \( f_{\text{AUDIO}} \) signal. The harmonics “2” and “3” show the noise due to modulation. The impact of the power supply impedance is seen by the presence of harmonics “4” through “7”. The harmonic “6” is due to twice the audio signal frequency, therefore at \( 2 \cdot f_{\text{AUDIO}} \). In fact, since a resistive load, supplied by a sinusoidal voltage, absorbs a sinusoidal current, according to Figure 15, the ripple voltage present on \( V_{\text{DD}} \) of the amplifier has a main ripple component at twice \( f_{\text{AUDIO}} \). Even intermodulation between the fundamental and \( 2 \cdot f_{\text{AUDIO}} \) frequency generates the harmonics 5, 6 and 7 (and beyond), therefore worsening THD.

Figure 14 – Output frequency spectrum of Class-D amplifier: 1 kHz audio + 250 Hz noise.

In the real world, the best practice is to design a power supply suitable to supply the load; therefore, we decided to analyze how the output impedance of the supply section impacts the THD of the audio section. For this reason, we tested a TPA3251 evaluation board (EVM) connected in BTL, supplied at 36 V and tested at 0.4 kHz, 2.5 kHz and 5 kHz audio signal.

We measured the THD when the audio amplifier was supplied by (see Figure 16):

1) A very high quality bench power supply, with negligible output impedance (compared to the input impedance of the audio amplifier)

2) The same bench supply with a 2 Ω series impedance

The purpose of this test was to quantify the ability of closed-loop Class-D amplifiers to reject \( V_{\text{DD}} \) power supply ripple.

![Figure 15 – Output voltage, current and power of a Class-D amplifier.](image)

Since the audio EVM is equipped with high values of electrolytic capacitance on the power \( V_{\text{DD}} \), we removed those capacitors and added only 2, each one 120 µF, just to avoid excessive ripple voltage at switching frequency. The results are shown in Table 3.

![Figure 16 – Test bench setup to measure the THD of the audio amplifier.](image)
The fourth column of Table 3 shows the RMS ripple measured on the $V_{DD}$ voltage, which directly impacts the THD on both channels. A comparison between a 0 Ω and 2 Ω resistor is necessary to understand what the contribution of the impedance itself is. We put all numbers into the graph shown in Figure 17. We can see that even with 2 Ω impedance in series with the power $V_{DD}$, the THD stays below 0.016% until an audio frequency of 5 kHz.

Another cause of audio quality degradation comes from clipping: when the duty-cycle of the

Class-D audio amplifier approaches 0 or 100% it can no longer regulate the audio signal and strong clipping occurs, as seen in Figure 18.

Heavy clipping of a sinusoidal waveform generates high harmonic content, which can damage the speakers (mainly the tweeters). Figure 19 shows the behavior (slope of amplitude versus frequency) of each harmonic of a 1 kHz square waveform. At low frequency, the distortion can also be dangerous for woofers because of its mechanical and thermal limits, mainly due to the limited swing amplitude of the coil.
Even though such cases happen only at very high output power levels, the so-called Class-G modulation (where a Class-D amplifier is supplied at a reduced voltage to reduce the switching losses of the power stage) decreases the audio level where clipping occurs. Therefore a “smart” way to detect clipping should be added to the whole system to avoid these issues.

If we now look at the output impedance of a PSU, it is well known that closing the loop improves not only the regulation but also greatly reduces the output impedance, according to Equation (3), where \( L(s) \) is the open-loop gain:

\[
Z_{OUT(ClosedLoop)}(s) = \frac{Z_{OUT(OpenLoop)}(s)}{1+L(s)} \tag{3}
\]

At the crossover frequency, \( f_{CO} \), the closed-loop and open-loop impedances match. Since we verified that even with a 2 \( \Omega \) series impedance, the THD of our audio amplifier still shows more than acceptable performance (see Figure 17), we can accept that our hypothetical PSU can have 2 \( \Omega \) output impedance at \( f_{CO} \) frequency. Figure 20(a) shows how this PSU output impedance and open-loop gain looks for voltage mode control.

It can be noted that the closed-loop output impedance remains flat in the frequency range 1 kHz - 10 kHz and for frequencies <1 kH; the high open-loop gain reduces it greatly. This is why we selected the impedance at \( f_{CO} \) (in this case 5 kHz) to calculate it. From the graph of Figure 20(b), a voltage mode converter would have even lower impedance below 1 kHz compared to current mode. But, at the end of the day, current mode is the most used modulation technique because of its characteristic of cycle-by-cycle limiting the peak current in an isolated converter.

We will see later that according to the minimum output capacitance (\( C_{OUT} \)) requirement to satisfy 2 \( \Omega \) impedance, a very small \( C_{OUT} \) should be selected. It must be noted that such a small \( C_{OUT} \) has to also comply with the high-demanding transient response capability of the isolated converter. For this reason we have to calculate the overshoot and undershoot of a peak current mode isolated converter. The related formulas are sorted in Table 4.

![Figure 20(a) – Open-loop graph and output impedance of target PSU.](image)

![Figure 20(b) – Output impedance of target PSU for voltage mode and current mode.](image)
The values in Table 4 are calculated according to the definitions of ΔV_{UNDERSHOOT} and ΔV_{OVERSHOOT} shown in Figure 21:

\[
C_{OUT} \geq \frac{\Delta I}{e \cdot \pi \cdot f_{CO} \cdot \sqrt{\Delta V_{UNDERSHOOT}^2 - (R_{ESR} \cdot \Delta I)^2}}
\]

\[
C_{OUT} \geq \frac{\Delta I}{8 \cdot f_{CO} \cdot \sqrt{\Delta V_{UNDERSHOOT}^2 - (R_{ESR} \cdot \Delta I)^2}}
\]

\[
C_{OUT} \geq \frac{L_{OUT} \cdot \Delta I^2}{(V_{OUT} + \Delta V_{OVERSHOOT})^2 - V_{OUT}^2}
\]

The limits are defined by the absolute maximum PV_{DD} of the audio Class-D amplifier (PV_{DD} is the supply voltage of the power stage) and are named PV_{DD(ABSMAX)} (for TPA3251 is 38 V) and PV_{DD(CLIPPING)} (to be calculated later). In practice, it is mandatory that during an extremely heavy output current transient of the PSU, its output voltage never goes beyond those two values to avoid failure or clipping. R_{ESR} represents the series resistance of C_{OUT} while the ESL (equivalent series inductance) is neglected because of its small contribution in the transient response performance.

The values in Table 4 are calculated according to the definitions of ΔV_{UNDERSHOOT} and ΔV_{OVERSHOOT} shown in Figure 21:

- ΔV_{UNDERSHOOT} (current mode, critically damped)
- ΔV_{UNDERSHOOT} (voltage mode)
- ΔV_{OVERSHOOT} (both)

The limits are defined by the absolute maximum PV_{DD} of the audio Class-D amplifier (PV_{DD} is the supply voltage of the power stage) and are named PV_{DD(ABSMAX)} (for TPA3251 is 38 V) and PV_{DD(CLIPPING)} (to be calculated later). In practice, it is mandatory that during an extremely heavy output current transient of the PSU, its output voltage never goes beyond those two values to avoid failure or clipping. R_{ESR} represents the series resistance of C_{OUT} while the ESL (equivalent series inductance) is neglected because of its small contribution in the transient response performance.

\[f_{CO} \] was selected to be 5 kHz because typically a low cost optocoupler is employed in isolated DC/DC converters. The optocoupler introduces a pole in the transfer function in the range of 10 kHz - 40 kHz. Since this frequency is not always exactly known, or varies in production and due to aging, it is better to close the feedback loop earlier, typically at 5 kHz.

**III. AC/DC Power Supply**

The specification of the AC/DC power supply is driven by a mix of the high-demanding transient response of the TPA3251 Class-D audio amplifier and by the desire for a low cost custom solution. In Table 5 we summarize the main specifications:

<table>
<thead>
<tr>
<th>Input voltage range</th>
<th>85 V_{AC} to 264 V_{AC}</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal output voltage</td>
<td>36 V, 18 V in Class-G mode</td>
</tr>
<tr>
<td>Output current</td>
<td>5.5 A (thermal protected) 11 A (short time, thermal protected) 22 A (overcurrent protected)</td>
</tr>
<tr>
<td>Target efficiency</td>
<td>85% minimum (50% - 100% load), 87% peak</td>
</tr>
</tbody>
</table>

**Table 4 – C_{OUT} minimum requirements versus undershoot and overshoot values.**

**Table 5 – Main specifications of AC/DC power supply.**
Depending on the final application of such a system (PSU + Class-D amplifier), it might be necessary to add a PFC (power factor correction) stage in order to comply with EN61000-3-2 Class-A norm, which specifies a maximum harmonic content in the input current of the PSU. This is mandatory if the continuous input power is higher than 75 W. In consumer applications like audio-video (A/V receivers), home theater, TV or low-cost audio amplifiers, the average input power is seldom higher than 75 W. But in other applications like monitors (active speakers for studios), high-end A/V receivers and high-quality and high power audio amplifiers, mainly a PFC stage is always considered as in our case. Another characteristic of a high-quality PSU is light-load efficiency. It is pretty clear that an A/V receiver is operated at low-volume (typically 1 W – 10 W) most of the time, by listening to background music. Therefore both the PFC and DC/DC stage must have the capability to consume the least power possible at a light load. One method is to reduce the output voltage to enter Class-G mode. In this way the audio amplifier will also consume less power and the overall efficiency will increase. In Figure 22 the block diagram of the PSU is shown.

Figure 22 – Block diagram of the complete AC/DC and auxiliary power supplies.

A. PFC Stage Selection

The average output power of this PSU is 200 W. For the PFC stage we consider four different types of boost converters as seen in Table 6.

For this application both interleaved transition mode (I-TM) and single-phase continuous conduction mode (S-CCM) are suitable for a 200 W average output power level. The S-CCM has the advantage that it can be up-scaled to a higher power; therefore, we selected a UCC28180 controller.

<table>
<thead>
<tr>
<th>PFC Boost Modulation Type</th>
<th>Power Level</th>
<th>Suitable Controllers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single-phase transition mode</td>
<td>80 W to 200 W</td>
<td>UCC28050/51</td>
</tr>
<tr>
<td>Interleaved transition mode</td>
<td>200 W to 600 W</td>
<td>UCC28060/61/63</td>
</tr>
<tr>
<td>Single-phase continuous conduction mode</td>
<td>400 W to 1 kW</td>
<td>UCC2817A/18A UCC28019A UCC28180</td>
</tr>
<tr>
<td>Interleaved continuous conduction mode</td>
<td>&gt; 1 kW</td>
<td>UCC28070</td>
</tr>
</tbody>
</table>

Table 6 – Suitable controllers according to modulation type and power range.

The bandwidth of the PFC stage must satisfy several constraints. It should not be too high, because otherwise the controller will “try” to follow the output ripple voltage, which has a 100/120 Hz component. The consequence is an increased distortion of the AC current waveform and worse THD and power factor. It should not be too small though; otherwise load transients can bring the output voltage (V_{PFC}) regulation outside boundaries (overvoltage → danger for active components, under-voltage → high peak current due to V_{AC(PEAK)} ≥ V_{PFC}). It can be demonstrated that an attenuation of the closed-loop gain at 100/120 Hz ≥ 20 dB is already enough to avoid increasing THD beyond the EN61000-3-2 limits. A similar constraint comes from the interaction between the minimum frequency of an audio signal, which is 20 Hz, and twice the line frequency. Since the frequency of the absorbed current in an audio amplifier doubles, if the PFC has to regulate at 40 Hz, the equivalent peak input current will be proportional to the peak output power. This causes the PFC stage to deliver twice the nominal output power and all active and passive components have to be dimensioned accordingly. As a rule of thumb that satisfies the transient response, THD, power factor and peak power capability, the bandwidth should be selected according to the following formula:

\[ f_{CO} \leq \frac{2 \cdot f_{\text{min}}}{3}, \]  

where \( f_{\text{min}} = 20 \text{ Hz} \) is the minimum audio frequency.
Figure 23 shows a screenshot of three waveforms: $V_{\text{OUT}}$, $I_{\text{OUT}}$ (DC/DC output voltage and current) and $V_{\text{PFC}}$.

![Waveforms](image)

Figure 23 – $V_{\text{OUT}}$, $I_{\text{OUT}}$, $V_{\text{PFC}}$ of proposed converter at full load and 20 Hz audio signal.

Care must be taken when selecting the output capacitors of this PFC stage. The value should be high enough to avoid triggering the UCC28180 enhanced dynamic response (EDR), which is set internally to ± 5%. The “acceleration” in the voltage loop can increase THD and worsen PF, which may happen at very high peak output power. Figure 24 shows the simulated open-loop gain and phase for this converter.

![Bode Plot](image)

Figure 24 – Open-loop gain and phase Bode plot of the PFC stage.

B. Isolated DC/DC Topology Selection

There are several possibilities for designing such a DC/DC converter. After discarding a flyback topology, suitable for continuous power levels up to 100 W, we analyzed half-bridge (HB), 2-switch forward and LLC resonant topologies. It is beyond the scope of this paper to discuss all the advantages/disadvantages of every topology, but in the end we selected a 2-switch forward topology based on the following pros and cons:

**PROs:**
- Low cost solution
- The power switch stress voltage is $V_{\text{PFC}}$, (400 V nominal)
- During demagnetization of the transformer magnetizing current, two diodes clamp both switch nodes to $V_{\text{PFC}}$; therefore, if the maximum duty-cycle is less than 50%, the transformer resets automatically

**CONS:**
- The maximum duty-cycle is < 50%; the output inductor must have a higher inductance value compared to half-bridge topology
- High-side drive is needed, even though that is also true in HB and LLC

The high-side driving of the FET is accomplished with: (1) transformer or (2) HB driver (with floating section). With (1), due to the transformer impedance (mainly resistance and leakage inductance) it is not possible to reach high peak driving currents. Therefore we decided to use a HB driver, capable of 4 A sink and 4 A source, thus improving the efficiency and reducing switching losses on both FETs. The block diagram of such a converter is shown in Figure 25.

The floating section (HS driver) takes its own power source by means of a “bootstrap” circuit, $D_{\text{BOOT}}$, $C_{\text{BOOT}}$. In practice $C_{\text{BOOT}}$ is recharged by $D_{\text{BOOT}}$ at every PWM cycle only if the switch node $SW_1$ reaches the ground potential. Both diodes $D_1$ and $D_2$ in normal conditions discharge the energy stored in the magnetizing inductance ($L_M$) of $T_1$, therefore they are clamping the magnetizing current back to +400 V bus ($V_{\text{PFC}}$). In CCM mode, this always happens because the duty-cycle range is defined by $V_{\text{OUT}}$, $V_{\text{PFC}}$ and the transformer turns ratio. At very light load, the relationship between the former parameters is not valid anymore and the duty-cycle is reduced to zero as the load decreases. At some load-level, the magnetizing current is insufficient to charge $Q_{1 COSS}$, $D_2$ capacitance and $T_1$ interwinding capacitance, and the $SW_1$ switch node swings from +400 V towards zero without reaching the ground, according to Figure 26.
The teal line is the switch node SW\(_1\) voltage when the energy is sufficient, while the first two top red dashed lines show that C\(_{\text{BOOT}}\) will not be recharged. To overcome this issue, we added a recharge network, comprised of inexpensive, small signal FET + SOT223 600 V FET, as shown in Figure 27.

The signal “Delayed Signal” is the gate voltage of Q\(_{12}\), while the “FET\(_{\text{BOOT}}\) Driver” is the gate voltage of Q\(_{11}\). This network and the associated delay, force SW\(_1\) to reach ground potential when the voltage swing reaches the valley. In this way Q\(_1\) C\(_{\text{OSS}}\) losses are further reduced. The delay needed to switch at the valley is calculated using the following formula:

\[
R_{68} \cdot C_{51} \geq \frac{\pi}{2} \cdot \sqrt{L_M \cdot 2C_{\text{OSS}}}
\]  

(5)

where \(L_M = T_1\) magnetizing inductance and C\(_{\text{OSS}}\) is from Q\(_1\), Q\(_2\).
The only disadvantage of such a network is even though Q₂ has zero-voltage transition during T_ON, Q₁ “sees” the whole V_PFC voltage, therefore there is some 20% to 30% unbalance between Q₁ and Q₂ regarding switching losses.

C. Output Capacitor Requirements

As previously anticipated, we assume as a starting point f_CO = 5 kHz. Dependent on the output ripple current requirement, by selecting 200 kHz as the switching frequency, we used an output inductor with L_OUT = 50 µH. To keep the THD of a Class-D audio amplifier below 0.016%, we calculate a minimum value of C_OUT according to:

\[
C_{OUT} (l) \geq \frac{I}{2 \cdot \pi \cdot 2\Omega \cdot 5kHz} = 16 \mu F
\]  

(6)

where 2 Ω is the maximum allowed impedance in series between the audio amplifier and PSU. The other two constraints are overshoot and undershoot voltages on V_OUT (see Table 4 in Section II). If we consider that the nominal PV_DD(NOM) of the TPA3251 EVM is 36 V, the maximum absolute value is 38 V and the maximum duty-cycle, just before clipping, is 95%, we arrive at the following values for ΔV_OVERSHOOT and ΔV_UNDERSHOOT:

\[
\Delta V_{OVERTSHOOT} \leq PV_{DD(ABSMAX)} - PV_{DD(NOM)} = 38.0 \text{ V} - 36.0 \text{ V} = 2.0 \text{ V}
\]  

(7)

\[
\Delta V_{UNDERSHOOT} \leq PV_{DD(NOM)} - PV_{DD(CLIPPING)} = 36.0 \text{ V} \cdot (1-95\%) = 1.8 \text{ V}
\]  

(8)

Using these values, we can calculate the minimum C_OUT requirements for current and voltage mode, respectively:

\[
C_{OUT} (1) \geq \frac{1}{2 \cdot \pi \cdot 2\Omega \cdot 5kHz} = 16 \mu F
\]  

(9)

\[
C_{OUT} (2) \geq \frac{22.0 A}{8 \cdot 5 kHz \cdot \sqrt{(1.8 V)^2 - (25 m\Omega \cdot 22 A)^2}} = 321 \mu F
\]  

\[
C_{OUT} (3) \geq \frac{50 \mu H \cdot (22.0 A)^2}{(36.0 V + 2.0 V)^2 - (36.0 V)^2} = 164 \mu F
\]  

(10)

The output capacitance should be selected from the highest values of C_OUT(1,2,3), which in our case is 321 µF. As a first assumption when the ESR = 25 mΩ, we predicted a 300 µF capacitor. After selecting C_OUT and the ESR, it is possible to choose the poles and zeroes of the compensation network. The selected controller works in peak current mode, so a type II compensation is sufficient. After analyzing the poles and zeroes of the power stage, we used the components described in Figure 29.

A zero was placed at 184 Hz and a pole at 184 kHz. This way enough phase margin (60 degrees) is measured, as visible in the Bode plot measurement (Figure 30).
The Class-G circuit is also useful regarding over-temperature protection. We placed a temperature sensor with digital output, set to 80°C, close to the main heat sink. It enters Class-G mode when triggering instead of switching the whole power supply off, thereby letting the audio amplifier run at low power. This is sufficient to cool down the PSU. At this point $C_{OUT}$, $L_{OUT}$ and the compensation network are defined. The whole converter was built and tested and the load transient response verified. $C_{OUT}$ was selected by using 3 electrolytic capacitors in parallel, each 100 µF, with an ESR = 74 mΩ. One 10 µF ceramic capacitor was added to reduce high frequency spikes due to ESL. The following formulas calculate the output impedance, both the reactive and the active part:

$$X_{OUT} \approx \frac{1}{8.3 \cdot C_{OUT(SINGLE)} \cdot f_{CO}} = 92.6 \text{ mΩ} \quad (11)$$

$$ESR_{C(OUT)} = \frac{ESR_{C(OUT), SINGLE}}{3} = 24.7 \text{ mΩ} \quad (12)$$

$$Z_{OUT} = \sqrt{X_{C(OUT)}^2 + ESR_{C(OUT)}^2} = 95.8 \text{ mΩ} \quad (13)$$

According to these values, we expect the load transient response might show a $\Delta V$ of:

$$V = \Delta I \cdot Z_{OUT} = 9.0 \text{ A} \cdot 95.8 \text{ mΩ} = 862 \text{ mV}, \quad \Delta V = 2.4 \% \quad (14)$$

We measured the response on the real prototype and, as shown in Figure 31, there is sufficient correlation.

According to this measurement, if we double the load transient from 9 A to 22 A, we should obtain $\Delta V \leq 1.8 \text{ V}$. The difference in the calculation comes from the difference between the simulated bandwidth (5 kHz) and the measured one (4.5 kHz).

Before writing this article, we tested the whole system (Class-D audio amplifier + PSU) in different conditions, at different frequencies, with the same power supply but with higher output capacitance (3000 µF), according to the specifications from a customer. The results are shown in Figures 32, 33 and 34 with the Class-D amplifier switching at 600 kHz.

![Figure 32 – Complete system efficiency curves (amplifier + PSU), fixed 36 V and Class-G.](image)

![Figure 33 – Performance comparison between reference lab supply and proposed PSU.](image)

![Figure 34 – THD performance of audio amplifier versus frequency and power.](image)
IV. AUTOMOTIVE POWER SUPPLY

In automotive Hi-Fi, the maximum power capability of an amplifier plays a very important role because that parameter is often solely used for comparison of different amplifiers and systems. This is not limited to only aftermarket amplifiers; car manufacturers also emphasize having large numbers in their audio specification. It is arguable if the declaration of peak or RMS power without the corresponding THD makes any sense, but typically this relationship does not play a role. This section of the white paper describes the design of a power supply for a car amplifier which is capable of providing 700 W of audio power.

First, we will take a detailed look into the power specifications of a TPA3251 Class-D amplifier to understand the different output power specifications and which power supply demands arise from that. The amplifier system contains one power supply and two TPA3251 amplifiers. Amplifier #1 is configured in BTL mode and provides the full audio spectrum to the left and right channels with 4 Ω speakers. Amplifier #2 is configured in PBTL mode and contains an 80 Hz low pass filter on the input to drive a subwoofer with 2 Ω impedance. It is also possible to connect two 4 Ω subwoofers in parallel to gain the same amount of power.

<table>
<thead>
<tr>
<th>TPA3251 #1 in BTL Mode</th>
<th>TPA3251 #2 in PBTL Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Left and right channel with full audio bandwidth</td>
<td>Subwoofer with 80 Hz low pass</td>
</tr>
<tr>
<td>2x175 W&lt;sub&gt;RMS&lt;/sub&gt; / 2x 350 W&lt;sub&gt;PEAK&lt;/sub&gt; into 4 Ω load @ 10% THD</td>
<td>1x350 W&lt;sub&gt;RMS&lt;/sub&gt;/1x700 W&lt;sub&gt;PEAK&lt;/sub&gt; into 2 Ω load @ 10% THD</td>
</tr>
<tr>
<td>2x120 W&lt;sub&gt;RMS&lt;/sub&gt; / 2x240 W&lt;sub&gt;PEAK&lt;/sub&gt; into 4 Ω load @ 0.1% THD</td>
<td>1x240 W&lt;sub&gt;RMS&lt;/sub&gt;/1x480 W&lt;sub&gt;PEAK&lt;/sub&gt; into 2 Ω load @ 0.1% THD</td>
</tr>
<tr>
<td>0 dBu (-2.2 dBV) input level for full power (standard for European pro audio)</td>
<td>2.2 V&lt;sub&gt;PEAK-Peak&lt;/sub&gt; / 0.775 V&lt;sub&gt;RMS&lt;/sub&gt; @ 600 Ω (1 mW)</td>
</tr>
<tr>
<td>2.2 V&lt;sub&gt;PEAK-Peak&lt;/sub&gt; / 0.775 V&lt;sub&gt;RMS&lt;/sub&gt; @ 600 Ω (1 mW)</td>
<td>Power source is the car battery (9 to 16 V nominal for full load, 6 to 16 V operating)</td>
</tr>
</tbody>
</table>

Table 7 – General system specification.

When reading the specification of a Class-D amplifier it is very important to understand the relationship between RMS power, peak power and THD. At the beginning of this paper we stated that 0.1% THD is a value most people will not be able to hear. For this amplifier in BTL mode we can achieve a maximum power of 2x 120 W<sub>RMS</sub> / 2x 240 W<sub>PEAK</sub> with 0.1% THD for the left and right channel on 4 Ω speakers. For the same THD and a single 2 Ω speaker, the total power for the subwoofer channel is identical. If we increase the THD to 10%, the RMS and peak power levels are around 46% higher. So it is always very important to check if an amplifier is specified either with RMS or peak power and at which THD. In this example, the complete system can be specified either with 480 W (RMS power @ 0.1% THD) or with 1400 W (peak power @ 10% THD) – almost three times higher.

Aftermarket amplifiers generally provide a low as well as a high input for the audio signal. If the head unit provides a pre-amplifier output on the RCA connectors (typically 2.0 up to 6.0 V<sub>PEAK</sub>), this is preferably used to feed the amplifier. If such an output is not available, the head unit’s speaker signal (up to 20.0 V<sub>PEAK</sub>) is used and connected to the high inputs of the amplifier. The pre-stage of this audio system is designed to provide the full power at 10% THD with an input level of 0 dBu. 0 dBu is the standard for European pro audio applications and equals 2.2 V<sub>PEAK-Peak</sub> / 0.775 V<sub>RMS</sub> at 600 Ω (1 mW). The input power source for the amplifier is the car battery and must provide full power between 9 and 16 V and be operable down to 6 V with reduced power.

For the design of the power supply 0.1% THD is taken into account, which equals 480 W<sub>RMS</sub> and 960 W<sub>PEAK</sub> audio power. Considering a crest factor of 1:8 for this kind of application results in 120 W<sub>RMS</sub> continuously. Because that is the audio power directly on the speakers, the efficiency of the Class-D amplifiers and the power supply itself have to be taken into account. Assuming 90% efficiency for the amplifiers and 95% efficiency...
for the power supply, the output current of the power supply is 3.9 A average and 31.2 A peak at 36.0 V. It is unlikely that both amplifiers need maximum peak power at the same time, therefore the current limit of the power supply is limited to 20.0 A. This is the current which all components of the power stage must be able to provide for a short time in the range of a few seconds. Thermally the power supply and its power stage, including the thermal interface, need to be designed to provide 3.9 A continuously without any limitations.

<table>
<thead>
<tr>
<th>Audio power @ 0.1% THD</th>
<th>240 W_{RMS} / 480 W_{PEAK} per amplifier → 480 W_{RMS} / 960 W_{PEAK} total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Crest factor 1:8</td>
<td>120 W_{RMS} continuous</td>
</tr>
</tbody>
</table>
| Current consumption at 36.0 V supply voltage | Class-D efficiency: 90%  
Power supply efficiency: 95%  
\[
I_{AVG} = \frac{120 \ W_{RMS}}{0.9 \cdot 0.95 \cdot 36.0 \ V} = 3.9 \ A
\]
\[
I_{PEAK} = \frac{960 \ W_{PEAK}}{0.9 \cdot 0.95 \cdot 36.0 \ V} = 31.2 \ A
\]
| Topology              | Interleaved synchronous boost with 2x LM25122-Q1 as no galvanic isolation is needed and it supports high efficiency over a wide load range |

Table 8 – Power supply specification.

The component selection of the boost converter is driven by several factors, but the main one is the peak current demand. That is also the reason for using a two-phase approach instead of a single-phase boost converter, which would be sufficient to provide the average current of 3.9 A continuously. For the high peak current, which is limited to 20.0 A, the low-side FETs are put in parallel to enable peak power capabilities and to spread the heat. As the output current is relatively low compared to the input current of the booster, a single FET for the high-side can be utilized. This design uses flatwire inductors with ferrite core to maximize the efficiency while providing a very high saturation current. A more cost sensitive approach would utilize inductors based on iron power, which reduces the mechanical footprint too.

The input capacitance is 2x 1200 µF (25 V) per phase, so 4800 µF in total. It is important to stay below the negative impedance of the power supply to ensure stability and avoid any resonances. As the inductor of a boost converter is connected to the input voltage, the input current is continuous with a ripple on top. This leads to low AC current stress for the input capacitors and theoretically no need for expensive low ESR and
high ripple current capacitors. Nevertheless, this design uses low ESR capacitors (Nichicon UPA1E122MHDANE) to provide long-life reliability and low ESR even at cold temperatures. At the output of a boost converter, the current is pulsed as energy is only delivered during the off-time. Additionally, the Class-D amplifiers, which are connected to the output of the booster, work like a synchronous buck converter at 50% duty-cycle average. On a buck converter, the situation is opposite: large AC current stress on the input, low AC current stress on the output. Finally, the booster output capacitors have to cover not only the AC current stress from the power stage itself, but also the pulsed input current of the amplifiers.

To reduce this effect, a post-filter is used on the output of the boost converter (Figure 36) which not only reduces the current stress for the electrolytic capacitors but also provides a very clean supply voltage for the amplifiers. Directly connected to the synchronous rectifiers are only 8x 4.7 µF (50 V) ceramic capacitors which are capable of handling AC current in the range of several amperes per capacitor. The disadvantage is the low capacitance which results in a voltage ripple around 570 mV Peak-Peak (1.6%) at 13.8 V input voltage and 10.0 A load.

For post filters with a high quality factor, a damping resistor in parallel to the inductor might be necessary to avoid resonances. The inductor used has a DCR of only a few mΩ, but even together with the relatively low ESR of the electrolytic capacitors the simulation showed no resonance and that a damping resistor is actually not necessary.

As described earlier, the capacitance on the supply voltage for the TPA3251 Class-D amplifier is quite small while still ensuring a very good THD. On the other hand, the bandwidth of the booster is below 1 kHz due to the right half plane zero. That means a relatively large capacitance on the amplifier’s supply voltage is needed to support load steps. This actual design uses 12x 560 µF (40 V) low ESR capacitors (Nichicon UPW1G561MHDANE), which is much more than necessary to ensure a THD below 0.1%. This decision was driven by customer demands and for a design with a comparable audio performance as the previously shown AC/DC solution, half of the capacitance is sufficient.

Figure 37 shows the efficiency of the boost converter at 36.0 V output voltage and 10.0 A load. The measurements show an almost flat curve over a wide load range with a peak efficiency of 95.5% at 13.8 V input voltage. At 9.0 V input voltage, the efficiency is around 3% lower, caused by increasing conduction losses due to the higher input current.
The bandwidth of the converter at 10.0 A load (Figure 38) does not show any surprises and is a bit below 1 kHz. Electrolytic capacitors can have significant changes of ESR over temperature and lifetime, therefore compensation was designed to provide a generous phase and gain margin of 81 degrees and -21 dB, respectively, at a crossover frequency of 830 Hz with a 13.8 V input voltage.

The system audio performance is excellent and the THD is well below 0.1% over the whole frequency range from 20 Hz up to 20 kHz for 12.0 V input voltage. Figure 39 shows the measurement results for 25, 50, 75 and 100 W\textsubscript{RMS} at 4 Ω load.

The THD vs. power measurement (Figure 40) shows that at up to 120 W\textsubscript{RMS}, the THD of the system is below 0.1%. This fits exactly with the specification of the TPA3251 Class-D amplifier datasheet, which guarantees 0.1% THD at 120 W\textsubscript{RMS} per BTL channel at 4 Ω load. The measurement proves that the power supply has no negative impact on the audio performance and it is comparable with the lab reference supply which was used to specify the Class-D amplifier IC.

Heat sinks with a spring-pressure setup are used to cool the Class-D amplifier as well as the FETs of the booster. As the average power dissipation is moderate, relatively small ribbed aluminum heat sinks can be used. The mechanical setup is shown in Figure 41.
In this solution, a thermal foil equalizes minimal height differences (planarity) as a single heat sink is used for both Class-D ICs. Heat-conductive paste can also be used, as long as the same height for both ICs is ensured. The springs apply a constant pressure to the device and reduce the mechanical stress compared to a solution where the heat sink is directly screwed to the PCB.

V. CONCLUSION

This white paper explained the influence of the power supply on the audio performance of a Class-D audio amplifier. A method based on output impedance was described detailing how to estimate the output capacitance of a switch mode power supply while keeping in mind the audio performance degradation with regards to THD. An AC/DC power supply with PFC as well as an automotive solution have been presented showing that for both cases there is almost no difference between the reference power supply, which has been used to characterize the Class-D IC, and these two solutions.

Figure 42 – PMP10215 & TPA3251 EVM.

Figure 43 – PMP11769.

VI. REFERENCES


Information on both reference designs, including the schematic, bill of material, test report, gerber and CAD data, are available on ti.com:

PMP10215 - AC/DC Power Supply
http://www.ti.com/tool/PMP10215

PMP11769 - Complete Automotive Audio System
http://www.ti.com/tool/PMP11769
**TI Worldwide Technical Support**

**TI Support**
Thank you for your business. Find the answer to your support need or get in touch with our support center at

www.ti.com/support

China:  http://www.ti.com.cn/guidedsupport/cn/docs/supporthome.tsp
Japan:  http://www.tij.co.jp/guidedsupport/jp/docs/supporthome.tsp

**Technical support forums**
Search through millions of technical questions and answers at TI's E2E™ Community (engineer-to-engineer) at
e2e.ti.com

China:  http://www.deyisupport.com/
Japan:  http://e2e.ti.com/group/jp/

**TI Training**
From technology fundamentals to advanced implementation, we offer on-demand and live training to help bring your next-generation designs to life. Get started now at

training.ti.com

Japan:  https://training.ti.com/jp

---

**Important Notice:** The products and services of Texas Instruments Incorporated and its subsidiaries described herein are sold subject to TI's standard terms and conditions of sale. Customers are advised to obtain the most current and complete information about TI products and services before placing orders. TI assumes no liability for applications assistance, customer's applications or product designs, software performance, or infringement of patents. The publication of information regarding any other company's products or services does not constitute TI's approval, warranty or endorsement thereof.

The platform bar and E2E are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.
IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ("TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI’s provision of TI Resources does not expand or otherwise alter TI’s applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT. AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include, without limitation, TI’s standard terms for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2018, Texas Instruments Incorporated