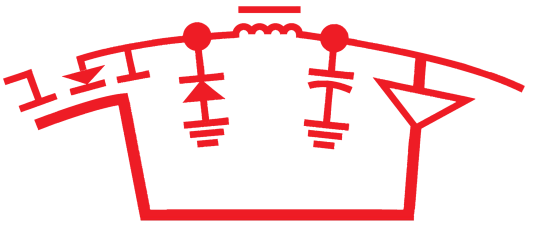

Power Supply Design Seminar

Common Mistakes in DC/DC Converters and How to Fix Them

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Common Mistakes in DC/DC Converters and How to Fix Them

Pradeep Shenoy and Anthony Fagnani

ABSTRACT

If you want to learn from the mistakes of others, this session is for you. This practical presentation goes through a number of common mistakes in point-of-load DC/DC converter design and testing. With an engaging, interactive format, this session covers issues found in converter capabilities, component selection, control design, board layout and measurement techniques. The causes of the design mistakes and how to avoid them in future designs are explained.

I. INTRODUCTION

No one likes to make mistakes. While we are bound to make them in our engineering journey, it is better if we can learn from the mistakes of others. This paper aims to highlight common mistakes in DC/DC converters. To remain simple and succinct, this paper overviews the most frequently seen errors and how to avoid them. References are provided for more detailed learning and information when possible. Let's begin with a brief review of the buck converter.

The buck converter is the most widely used DC/DC converter topology in point-of-load (POL) switching regulators. It is a simple and effective mechanism to step down the input voltage to a lower voltage level and to regulate the output voltage efficiently. Diagrams of the two buck converter switching states in continuous conduction mode are shown in Figure 1. A simplified switch node voltage (V_{SW}) and inductor current waveform are shown in Figure 2. While other converter topologies, like the boost converter, buck-boost converter, series capacitor buck converter [1][2] and many others may also be used, this discussion focuses on the buck converter for simplicity.

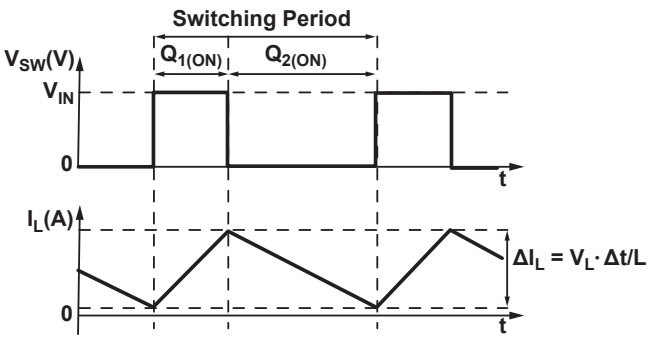

Figure 2 – Buck converter switching waveforms depicting the switch node voltage and the inductor current.

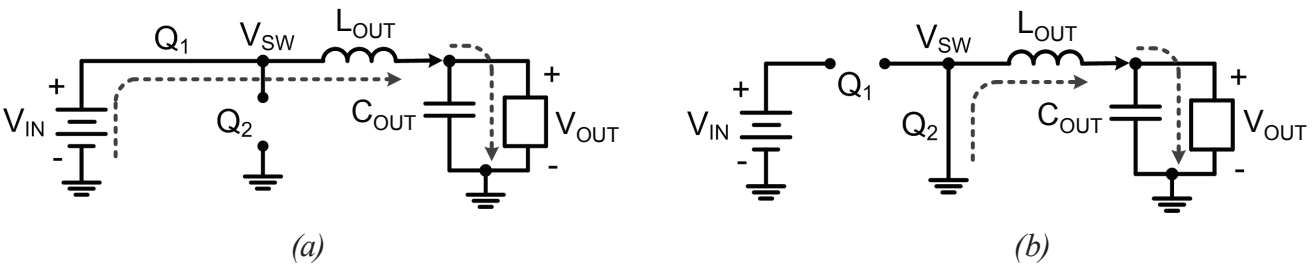

Figure 1 – Buck converter switching states with (a) high-side switch on and (b) low-side switch on.

II. Minimum On-Time Violation

When designing a buck converter, selecting the switching frequency (f_{SW}) is typically one of the first design choices to be made. The f_{SW} is selected based on the input voltage, output voltage and other specifications of the buck converter IC. Figure 3 shows an example V_{SW} and V_{OUT} ripple for a buck converter in normal operation. The converter is operating with the following conditions: V_{IN} = 11 V, V_{OUT} = 1.2 V, I_{OUT} = 0 A, f_{SW} = 1.2 MHz and forced continuous conduction mode (FCCM). In Figure 4, V_{IN} is increased to 12 V and the V_{OUT} ripple increases. Why does the V_{OUT} ripple increase?

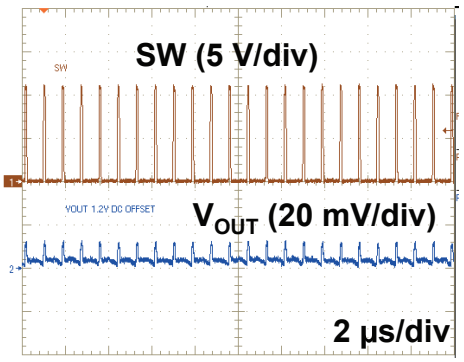

Figure 3 – 11 V input switching node and output voltage ripple waveforms.

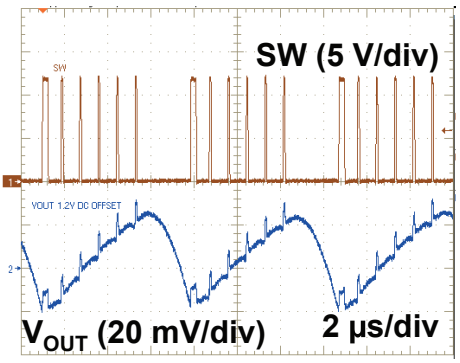

Figure 4 – 12 V input switching node and output voltage ripple waveforms.

The increased output voltage ripple in this waveform is a result of a violation of the minimum on-time of the buck converter IC. Equation (1) is a simple equation to estimate the on-time of the converter. This equation ignores losses in the converter for simplicity. When there is no load, the losses are low so this equation is an accurate estimation for no load. When the output is loaded and there are more losses in the converter, the on-time increases. The calculated on-time required for V_{IN} = 12 V, V_{OUT} = 1.2 V and f_{SW} = 1.2 MHz is 83 ns. The estimated on-time is below the typical 90 ns minimum on-time for the converter [3].

$$t_{ON} = \frac{1}{f_{SW}} \cdot \frac{V_{OUT}}{V_{IN}} \qquad (1)$$

$$t_{ON} = 83\ ns$$

The converter used in this example is a fixed frequency converter. When the on-time required is less than the minimum on-time, the converter skips switching pulses to keep V_{OUT} regulated. The converter outputs a series of 90 ns minimum on-time pulses that charge V_{OUT} above the target regulated voltage. The control loop responds to the overcharged V_{OUT} with a skipped pulse to regulate V_{OUT} to the correct DC voltage. Other converters may respond differently when the minimum on-time is violated. For example, the f_{SW} may begin to decrease or V_{OUT} may become regulated to a higher voltage.

To avoid potential problems related to the minimum on-time, the switching frequency should be selected considering the maximum input voltage and maximum minimum on-time listed in the datasheet. The maximum minimum on-time should be used because the minimum on-time typically varies with temperature, with output current and between parts. Figure 5 shows an example of how the minimum on-time can vary with temperature and load [3]. Typically, a number for the maximum minimum on-time is given in the electrical specifications of the datasheet. Using this number is the most conservative approach.

After the maximum minimum on-time is found, Equation (2) can be used to calculate the maximum f_{SW}. The part used in this example is specified for a maximum minimum on-time of 130 ns [3]. Using this with the V_{IN} and V_{OUT} in this example, the f_{SW} should be set below 769 kHz to always avoid pulse-skipping.

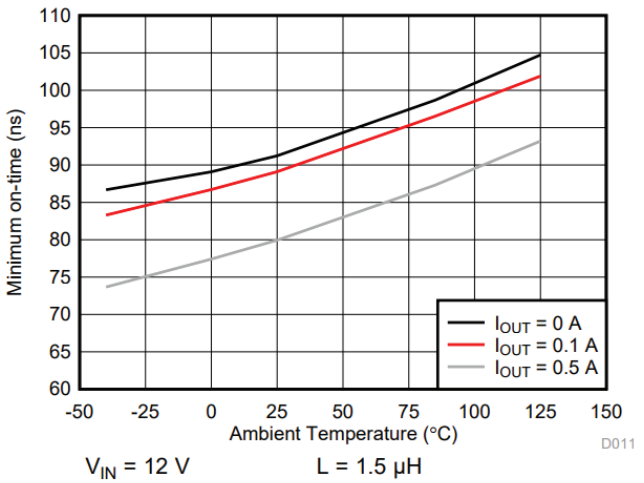

Figure 5 – Example variation in minimum on-time with temperature and load.

$$f_{SW} \le \frac{1}{t_{ON(MIN)}} \cdot \frac{V_{OUT}}{V_{IN(MAX)}} \quad (2)$$

Violation of the minimum on-time is not the only possible cause of increased output voltage ripple. For example, an unstable control loop or poor PCB layout are other possible causes. Some of these different causes will be discussed in later sections of this paper.

III. Thermal Derating

Another important consideration when selecting a part for an application is thermal performance. It is best to keep the operating temperature of the part as low as possible. In extreme cases, high operating temperature may cause a part to operate above its rated junction temperature and reach thermal shutdown. It can also reduce the lifetime of an IC as higher temperature accelerates failures.

Figure 6 shows the thermal image of two different converters both operating with the following conditions: V_{IN} = 12 V, V_{OUT} = 1.8 V, I_{OUT} = 8 A, and f_{SW} = 700 kHz. Part A has a case temperature T_C = 59.6 °C and Part B has T_C = 82.4 °C. In addition to a higher T_C, the thermal image for Part B shows higher PCB temperature and a larger thermal footprint. Part B would have little thermal margin in an application requiring operation up to an ambient temperature of 85 °C. Which of these two parts are rated for 8 A?

It turns out, both Part A and Part B are rated for 8 A! Table 1 gives a full comparison of the specifications for these two parts. Part A and Part B have similar specifications except for one important parameter; Part B is designed with higher $R_{DS(ON)}$ MOSFETs than Part A resulting in more power dissipation in Part B. Higher $R_{DS(ON)}$ MOSFETs can be advantageous in applications where optimizing cost is more important than optimizing efficiency.

Spec	Part A (TPS54824)	Part B (TPS54821)
V_{IN} range	4.5 – 17 V	4.5 – 17 V
Current	8 A	8 A
Size	3.5 x 3.5 mm	3.5 x 3.5 mm
$R_{DS(ON)}$	14/6 mΩ	26/19 mΩ
Modeled P_{LOSS}	1.69 W	2.38 W
Simulated die temp	64 °C	81 °C
Price	$$	$

Table 1 – Specification comparison between Part A and Part B.

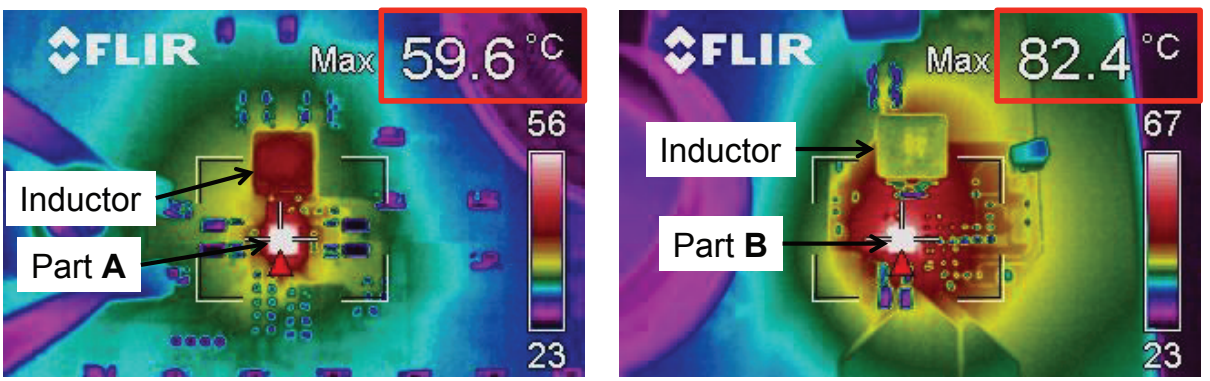

Figure 6 – Thermal image for two parts operating in the same load conditions.

Topic 5

Why is Part B rated for 8 A? Part B may be a good choice for applications which do not require operation in higher ambient temperatures. There are also two possible application specific details which allow Part B to better support an 8 A application.

First, to reduce the operating temperature of Part B, the power loss could be reduced by designing for a lower f_{SW}. However lower f_{SW} comes with a tradeoff of increased total solution size and increased cost for external components.

Second, this example has only considered an application requiring the converter to operate at its rated load of 8 A continuously for a period of time on a scale of seconds or longer. Many applications do not require the part to operate at its full load continuously. The full load of 8 A may only be for a short transient on the scale of milliseconds or shorter. With a short transient, the die and package may thermally saturate but the PCB and ambient air may not. In a case where the rated 8 A load is only needed for a short period of time, Part B may be sufficient. When evaluating the thermal performance of a part, the effective average load current should be considered.

TI's WEBENCH® software is a useful tool to account for thermal performance while selecting a part for an application. Table 1 includes rows for modeled P_{LOSS} and simulated die temperature taken from WEBENCH. The modeled P_{LOSS} number comes from the efficiency model in WEBENCH. The simulated die temperature is from a WebTHERM™ simulation from within WEBENCH. The thermal simulation is based on TI's standard EVM so it is important to remember variations in the PCB layout affect the thermal performance.

IV. Poor Inductor Selection

Inductor selection is an important part of converter design. Inductors impact efficiency, transient response and control loop stability. The image in Figure 7 shows what can happen when an improper inductor is selected. Can you see what is wrong with the inductor current waveform?

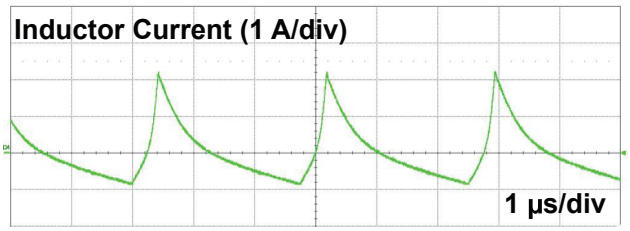

Figure 7 – Inductor current waveform exhibiting saturation.

The inductor current waveform should look similar to Figure 8. The inductor current should have a constant slope during the switch intervals. The inductor current waveform in Figure 7 exhibits a peaking waveform. This indicates that the inductor's magnetic core is saturating. When the core saturates, its permeability decreases significantly. The slope of the inductor current is increasing within the switch interval because the effective inductance of the inductor is decreasing.

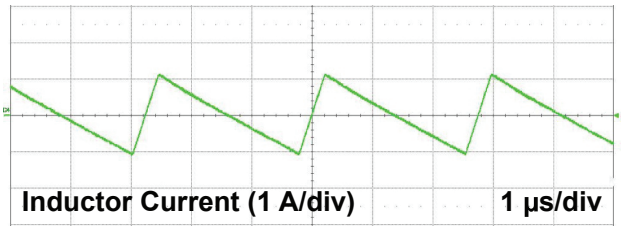

Figure 8 – Inductor current waveform (non-saturating).

Generally speaking, inductor saturation should be avoided. It can cause damage to the converter, lead to premature overcurrent protection and limits the output current from the converter. The peaking seen in Figure 7 can be observed in inductors made from a hard saturating magnetic material like ferrite and operated above their saturation current limit. Other magnetic core materials that offer soft saturating profiles can be more forgiving in these situations. It is also recommended to check how the inductor saturation profile changes with temperature and design for the worst case.

Another undesirable situation that can occur is shown in Figure 9. In this case, the converter is only running at 10% of its full rated load current yet the inductor is exhibiting a very large temperature rise (about 30°C above ambient temperature). What would cause the inductor to get so hot?

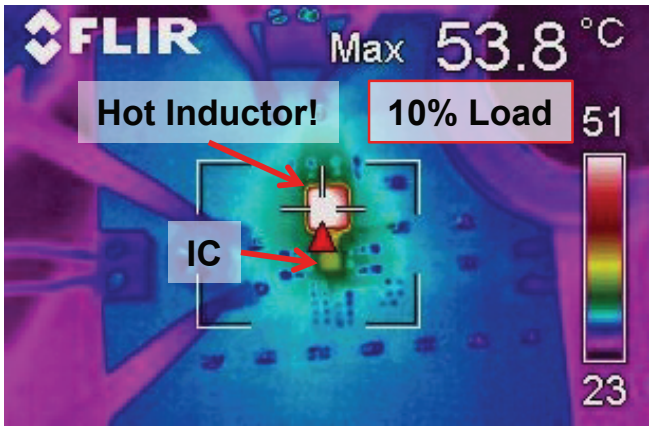

Figure 9 – High inductor temperature rise despite operating at 10% rated load current.

The inductor in Figure 9 is hot because there is a large amount of core loss. This happens because the inductance value selected is too low. With a low inductance value selected, very large peak-to-peak inductor current ripple (ΔI_L) results. Large current ripple can lead to excessive core loss. A simplified Equation (3) for estimating core loss is

$$P_{CORE} \approx k_0 f_{SW} B_{PK}^2 \propto k_0 f_{SW} \Delta I_L^2 \qquad (3)$$

where k_0 is a material constant and B_{PK} is peak flux swing. Core loss increases approximately quadratically with increases in inductor current ripple. A good design is shown in Figure 10. In this case, the current ripple is 30% of the full load current unlike the previous case where the ripple was over 100% of the full load current.

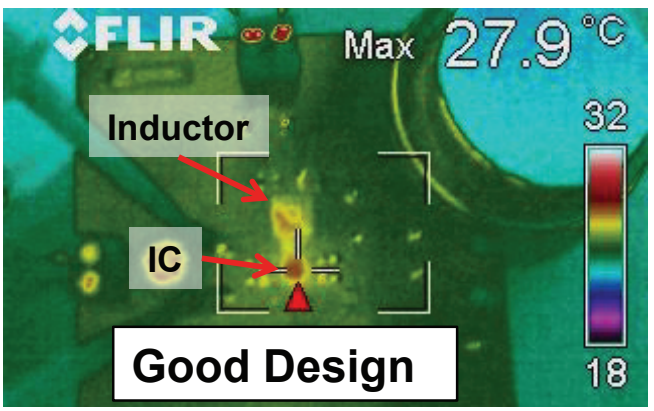

Figure 10 – A well designed converter where the inductor temperature is low at 10% load.

Typically, the inductance value is selected to keep the current ripple between 15% and 40% of the full load current level. For a converter with integrated MOSFETs, the inductance should be selected using the rated I_{OUT} of the converter. A good starting point for inductor selection is 30%. In the below Equation (4), the value for K would be 0.3 for this case.

$$L = \left(\frac{V_{IN(MAX)} - V_{OUT}}{K \cdot I_{OUT}} \right) \left(\frac{V_{OUT}}{V_{IN(MAX)} \cdot f_{SW}} \right) \qquad (4)$$

There is some flexibility when it comes to inductance selection. The efficiency graph of a converter can be shaped based on the inductance selected as shown in Figure 11. Assuming the same physical size inductors, higher inductance tends to increase peak efficiency. This is because there is less current ripple, core loss and RMS current. The tradeoff is that it increases inductor DC resistance (DCR) and tends to slow the transient response. Lower inductance values tend to result in higher full load efficiency due to lower DCR and have faster inductor current slew rates.

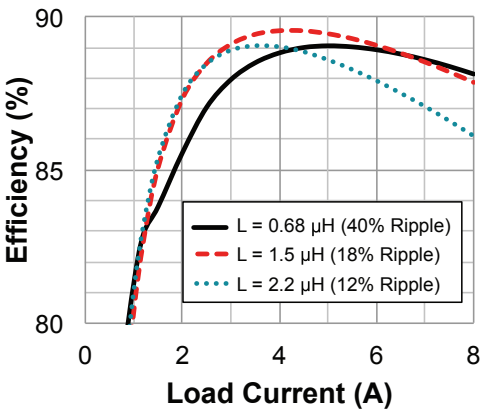

Figure 11 – Efficiency comparison of a converter designed with three different inductor values with the same physical size.

V. Insufficient Capacitance

Mistakes in capacitor selection can cause problems. For example, observe the output voltage ripple shown in Figure 12. The output voltage measurement shows the converter's response to a large load step increase. As expected, the output voltage initially drops but quickly recovers. The potentially undesirable aspect of Figure 12 is the oscillations on the output voltage after the transient. Sometimes these oscillations are interpreted as low phase margin in the control loop. What is the real cause of these oscillations?

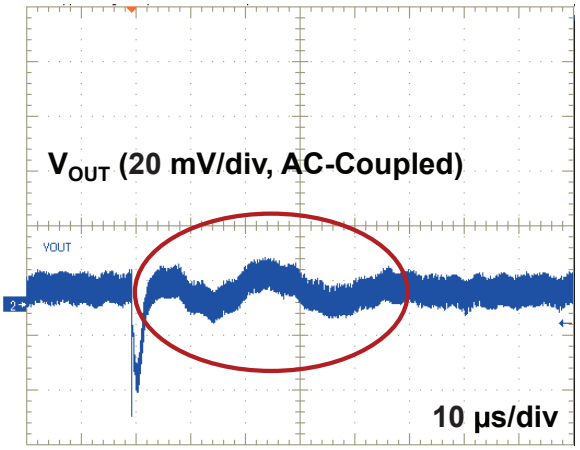

Figure 12 – Output voltage oscillation after a load step-up.

Figure 13 shows why the oscillations are occurring. The converter's input voltage has large variations due to the load step (on the order of hundreds of mV). For the most part, the converter rejects these input perturbations and only disturbs the output by a few mV.

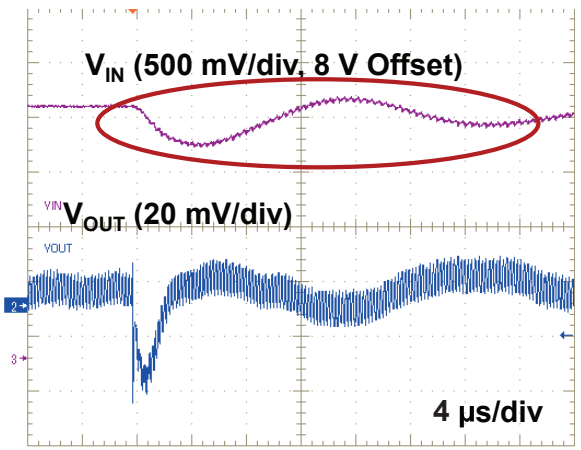

Figure 13 – Input voltage perturbations are impacting the output voltage.

This situation often arises when testing converter evaluation modules (EVMs). If the input supply to the converter is not properly bypassed with input capacitance or there are long bench power supply leads, the input disturbances like those shown in Figure 13 can result in incorrect inferences about the performance of the device under test. One possible solution is to connect a bulk input decoupling capacitor to the input of the EVM to avoid the perturbations. The response to the load step with a bulk decoupling capacitor is shown in Figure 14. In this case, the response to the load transient is clean without any oscillations on the input or output of the converter.

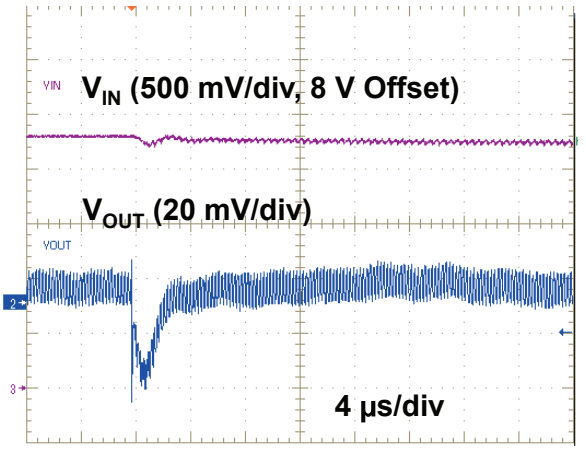

Figure 14 – Input voltage perturbations are eliminated with sufficient input decoupling capacitance.

Another problem that can occur with insufficient input decoupling is shown in Figure 15. In this situation, the converter is running close to its minimum input voltage when a load step-up occurs. The input voltage waveform is similar to the waveform show in Figure 13 except it occurs at a lower DC voltage. After the load step-up, the input voltage dips below the input undervoltage lockout (UVLO) level which results in the converter turning off. The output voltage collapses due to the perturbation on the input voltage. Once the input voltage recovers, the converter restarts and the output comes back in to regulation.

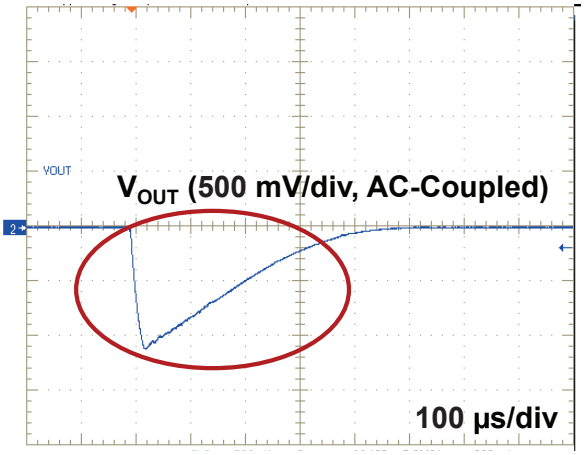

Figure 15 – Input voltage dips below the undervoltage lockout threshold during a load step-up and causes the converter to shut down and then restart.

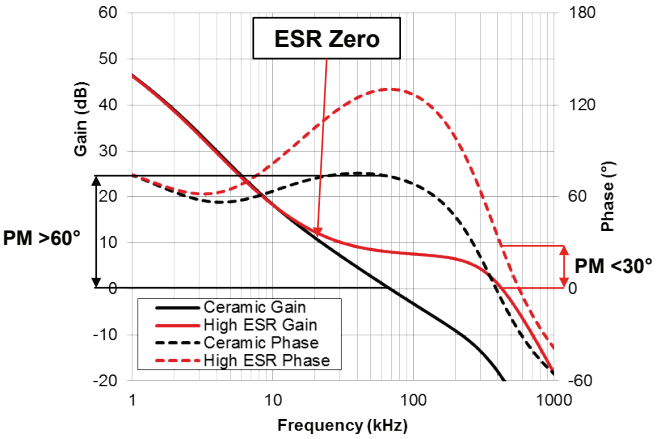

Figure 16 – Replacing a ceramic output capacitor with a high ESR capacitor can unexpectedly lead to low phase margin (PM).

There are several design guidelines to consider for input and output capacitors. You must ensure sufficient input and output decoupling capacitance; design equations located in the applications section of a converter datasheet can help. Typically, the "worst case" scenario to be designed for is large load transients. Capacitance also impacts steady state ripple and control loop bandwidth [7][8].

It is important that parasitic resistance and inductance of capacitors is taken into account. For example, do not design a converter with a low equivalent series resistance (ESR) ceramic output capacitor and later replace it with a (potentially cheaper) high ESR capacitor. This can cause low phase margin and potential instability as shown in Figure 16. This simulation had a fixed output capacitance and the ESR was varied from 3 mΩ to 30 mΩ. Many capacitor's ESR can also change dramatically with temperature and change the control loop dynamics. For example, an aluminum electrolytic capacitor can exhibit the same 10x increase in ESR from room temperature to cold temperature as simulated in Figure 16. It is also recommended to estimate the RMS current of the capacitor and check to see what the temperature rise due to self-heating will be.

VI. Poor Control Loop Compensation

After the key power components are selected for the converter, it is important that the control loop is properly compensated. Figure 17 shows the switching node of a converter operating with V_{IN} = 17 V and V_{OUT} = 1.8 V. The switching node shows alternating narrow and wide pulses. What causes this behavior?

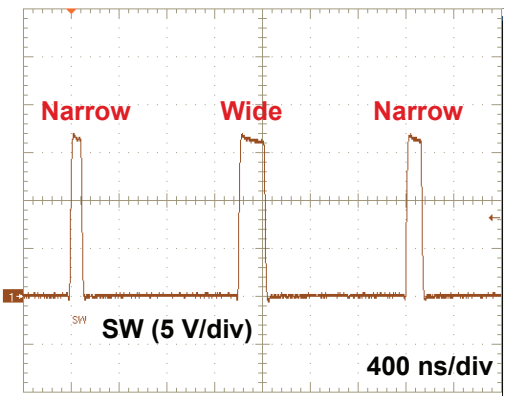

Figure 17 – Switching node of converter with wide and narrow pulses.

This behavior appears to be subharmonic oscillations that can occur with the peak current mode control converter at >50% duty-cycle if there is insufficient slope compensation [4]. This waveform was taken with a peak current mode

control converter but the duty-cycle is only 11%. With a duty-cycle <50%, insufficient slope compensation is not the cause. The cause instead is a poorly compensated design that has too little gain margin. The measured loop Bode plot is shown in Figure 18 and the gain margin is less than 5 dB.

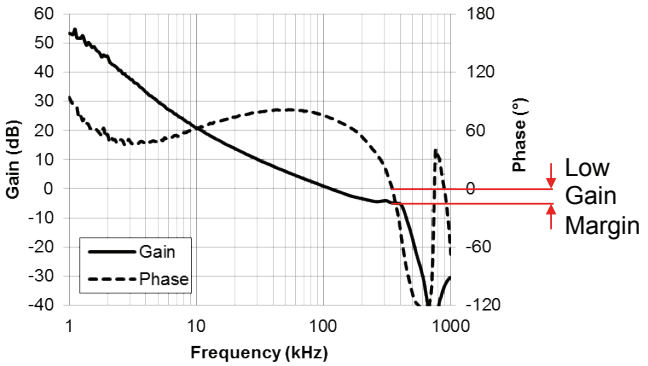

Figure 18 – Bode plot of converter with low gain margin.

To improve the gain margin, the compensation was modified to remove a zero previously in the loop near 100 kHz. Removing this zero reduces the high frequency gain but comes with a tradeoff of reduced phase. Figure 19 shows the resulting switching node and Figure 20 shows the Bode plot. The switching node is stable, the gain margin is improved to 13 dB and the phase margin is sufficient at 55°.

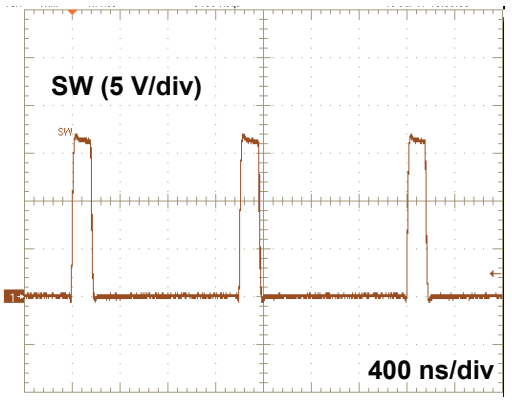

Figure 19 – Switching node of converter with good gain margin.

For a stable control loop, the typically recommended design goals are to have a minimum phase margin of 45° and gain margin of -10 dB [5]. When variations between components and variations across operating conditions are considered, the margin of a nominal circuit may need to be higher to always meet these recommended minimum values. For example, a more conservative design target of 60° phase margin and -16 dB gain margin may be used. The amount of added margin depends on the characteristics of the components and the range of operating conditions in an application.

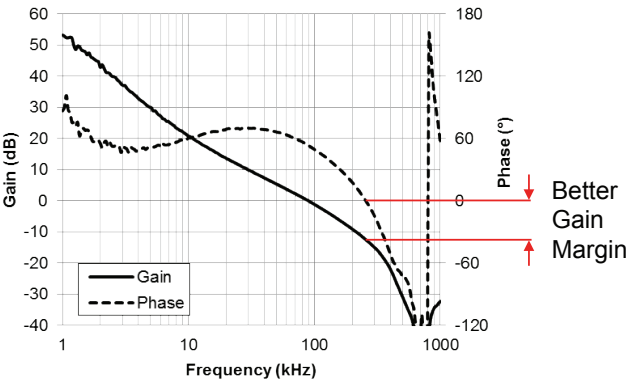

Figure 20 – Bode plot of the converter with good gain margin.

Sometimes even if a converter is designed with sufficient margin on paper, it may be unstable in the final application. Figure 21 shows a simulated Bode plot for a circuit after the initial calculation of the compensation values. It shows sufficient phase margin of 60° and gain margin of -16.7 dB. However, when the circuit was built and tested in the final application, the output voltage had an oscillation at 40 kHz as shown in Figure 22. Why does the output oscillate even when the simulation shows sufficient margins?

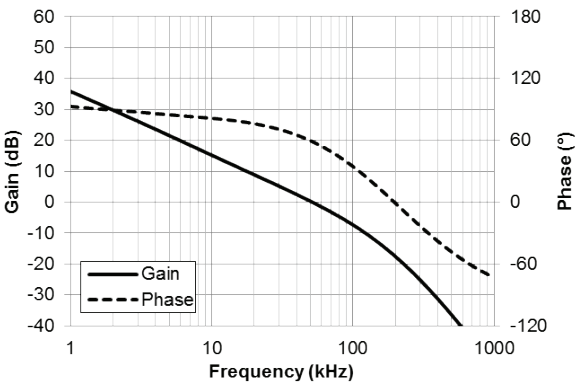

Figure 21 – Simulated Bode plot of a converter with good phase and gain margin.

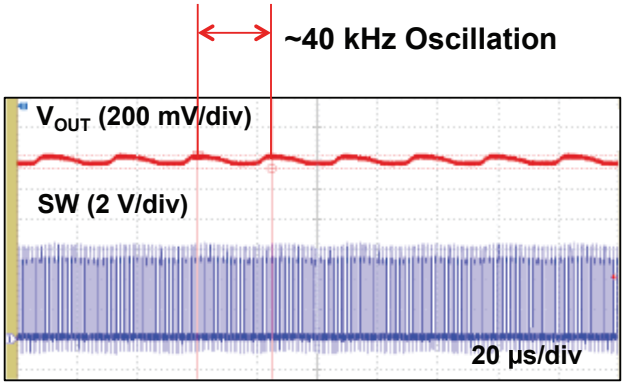

Figure 22 – Output voltage oscillation.

After a review of the circuit schematic that was built and tested, it was found that a second stage LC filter was used in the design but was not included in the compensation calculations or the initial simulation. The second stage was created with a ferrite bead in the output filter as shown in Figure 23. Figure 24 shows the simulated Bode plot when the entire output filter is included. This second stage adds a double pole that causes a -180° drop in phase and peaking in the gain at the LC resonance frequency. This results in the phase dropping below 0° before the 0 dB gain crossover frequency. The loop is unstable so the output oscillates.

When selecting compensation, it is important to make sure the entire output filter is included. In addition to any second stage filtering, all capacitance connected to the output voltage on the entire board must be included, not only the capacitance in this local to the POL converter. To

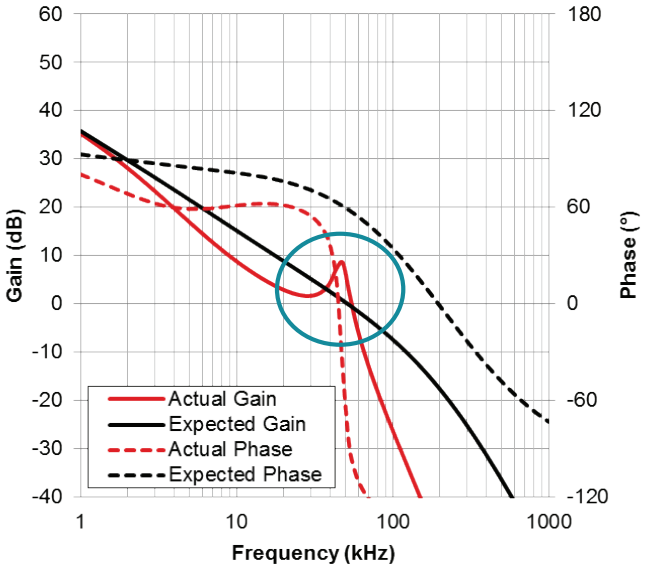

Figure 24 – Expected Bode plot vs. actual Bode plot with second stage LC filter.

stabilize the loop specific example, it is recommended to adjust the compensation so that the crossover frequency is less than 1/3rd the LC resonance frequency [5]. If the quality factor (Q factor) of the second stage is relatively high, it may require a lower crossover frequency to increase the gain margin or some damping resistance may be needed to reduce the Q factor.

This example has a second stage created by a ferrite bead in the output filter. However, if the load is located relatively far from the POL converter, a second stage could also be created by parasitic PCB inductance. The further away the load is from the POL converter, the more the parasitic PCB inductance.

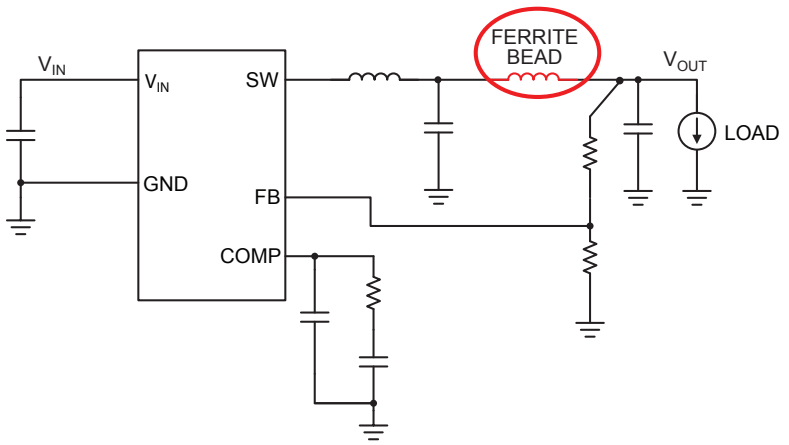

Figure 23 – Simplified schematic of circuit tested.

VII. Wrong Soft Start Time

You may come across a case where a DC/DC converter does not start up. A situation like what is shown in Figure 25 could be happening. The output voltage starts to increase but then the converter stops suddenly. The converter then tries to start again after waiting some time. In this example, the overcurrent protection was triggered during start up. This can be caused by large output capacitance, a heavy load during start up and/or a short circuited output. Many converters have a "hiccup" auto restart feature where the converter continually attempts to restart. This is the behavior being exhibited in Figure 25.

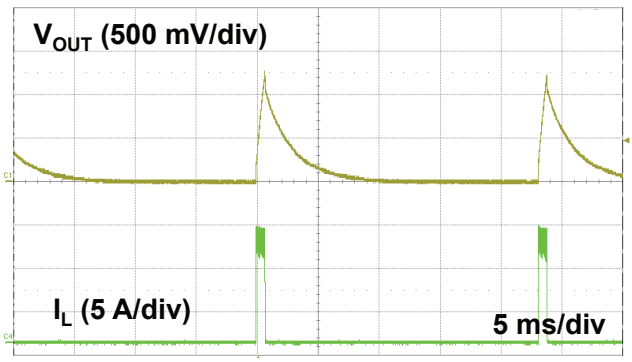

Figure 25 – A converter keeps hitting its overcurrent limit when attempting to start up.

One way to avoid this situation is to have an appropriate start up time. Most converters have programmable soft start times. If the soft start time is too fast, the input voltage can sag, overcurrent protection can be tripped or the input bus converter can hit its current limit. An appropriate soft start time avoids these issues and reduces inrush current.

Some simple equations can be used to estimate converter input and output current during soft start. If either input or output current is too high, increase the soft start time. During soft start, the converter needs to charge the output capacitance and bring the output voltage up to the target regulation voltage. The converter also needs to supply any current the load is demanding. This is depicted in Figure 26.

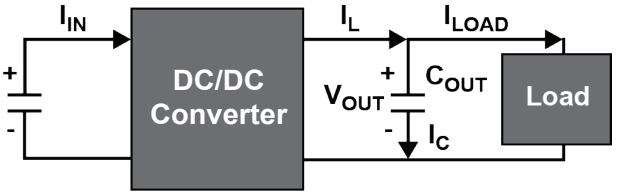

Figure 26 – A converter charges the output capacitors and provides any load current demand during start up.

The following Equation (5) can be used to estimate the current used to charge the output capacitance during start up.

$$I_C = C\frac{\Delta V}{\Delta T} \tag{5}$$

where C is the output capacitance, ΔV is the change in output voltage, ΔT is the soft start time and I_C is the DC current flowing into the capacitor. This equation assumes a straight line start up waveform which is a fairly good approximation of most start up profiles. A diagram showing the output voltage profile during start up is shown in Figure 27.

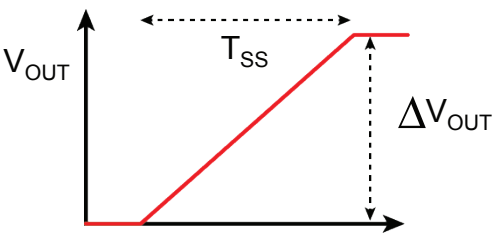

Figure 27 – Converter output voltage rise during soft start.

The output current from the converter supplies the capacitor charging current as well as any load current. Therefore, the converter output current during start up is

$$I_L = I_{LOAD} + I_C \tag{6}$$

where I_L is the converter output current and I_{LOAD} is the load current during start up. Take care to ensure the converter output current stays well below the overcurrent protection threshold during start up.

The following Equation (7) can be used to estimate converter input current in a buck converter

$$I_{IN} \approx D(I_{LOAD} + I_C) \tag{7}$$

where D is the duty ratio. For a buck converter, the duty ratio is V_{OUT}/V_{IN}. If many converters are supplied from the same intermediate bus, the current demand on the bus converter can be large if they all start up simultaneously. A technique commonly used to address this issue is to sequence the start up intervals of the converters. This spreads out the current demanded on the bus converter and avoids hitting its current limit.

VIII. Poor PCB Component Placement

Switching power converters are fairly easy to lay out on a printed circuit board (PCB). Sometimes simple layout mistakes can cause big problems, however. For example, consider the converter design shown in Figure 28.

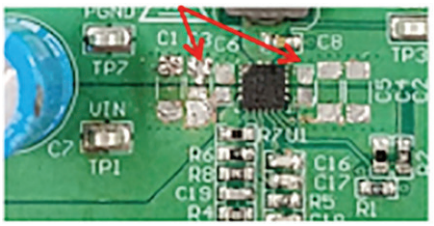

Figure 28 – Converter layout with no nearby input decoupling capacitor populated.

Because there are no input decoupling capacitors anywhere near the V_{IN} and GND terminals of the converter, the switch node of the converter exhibits large ringing, as shown in Figure 29. The switch node rings to about 10 V higher than the input voltage. This can cause additional stress to the converter, increase power loss, increase EMI and potentially damage the power MOSFETs and other internal circuitry.

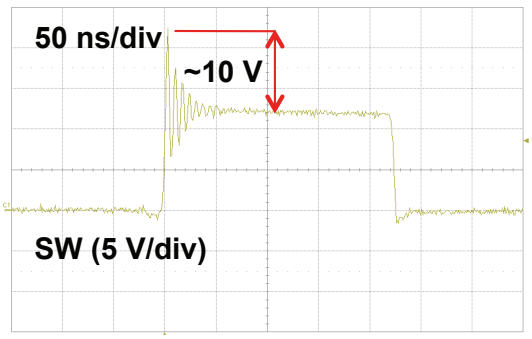

Figure 29 – Switch node waveform with no nearby input decoupling capacitor populated.

If input decoupling capacitors are placed right next to the converter, the switch node ringing is reduced. An example placement is shown in Figure 30. A 10 µF, 1206 size capacitor and a 0.1 µF, 0603 size capacitor are connected in parallel and adjacent to the converter input.

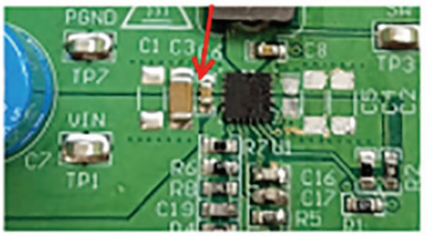

Figure 30 – Converter layout with two input capacitors populated right next to the IC.

The switch node waveform with this input capacitor placement is shown in Figure 31. As you can see, the switch node rings to about 5 V greater than the input voltage. This is a significant reduction from the previous layout because there is less parasitic inductance in series with the input capacitors.

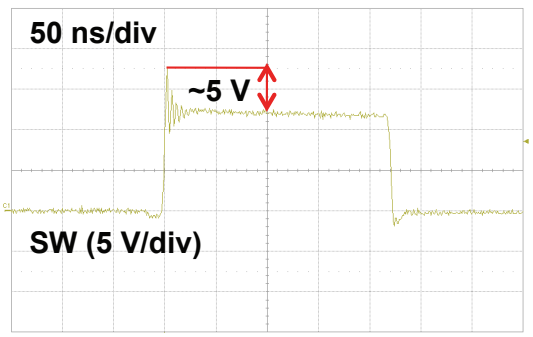

Figure 31 – Switch node waveform with two input capacitors populated right next to the IC.

A third layout is shown in Figure 32. In this case, input capacitors are populated on both sides of the IC. This converter has V_{IN} and GND pins on both sides of the IC which enables this layout approach [3].

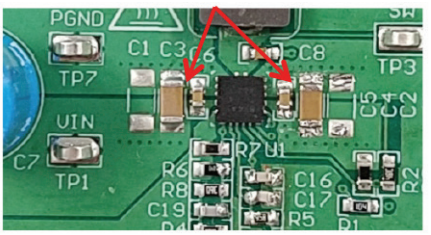

Figure 32 – Converter layout with two input capacitors populated on each side next to the IC.

The switch node waveform associated with this layout is shown in Figure 33. The switch node ringing is reduced to approximately 2 V higher than the input voltage. This reduced ringing is due to effective input decoupling capacitor placement that limits parasitic inductance.

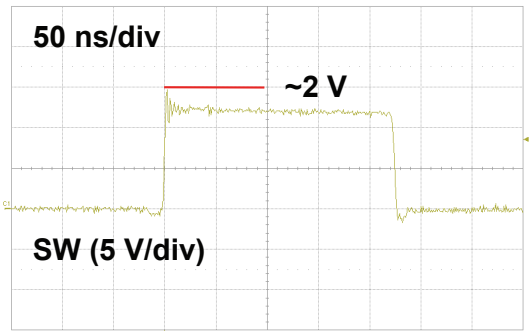

Figure 33 – Switch node waveform with two input capacitors populated on each side next to the IC.

There are several general guidelines to follow with a converter layout. It is important to minimize the switching loop area. This is highlighted in the pink box in Figure 34. A tight layout reduces parasitic elements, improves efficiency and limits the noise disturbances' impact on the system. Special care should be taken to optimize current return paths through the ground plane. Make these returns as short and wide as possible. Avoid having a large switch node to reduce EMI. Keep sensitive analog pins/traces like feedback and compensation away from noisy switching pins/traces like the switch node or bootstrap capacitor. A snubber circuit or a boot resistor can be added to slow down the switch node slew rate but these approaches tend to increase power loss [9][10].

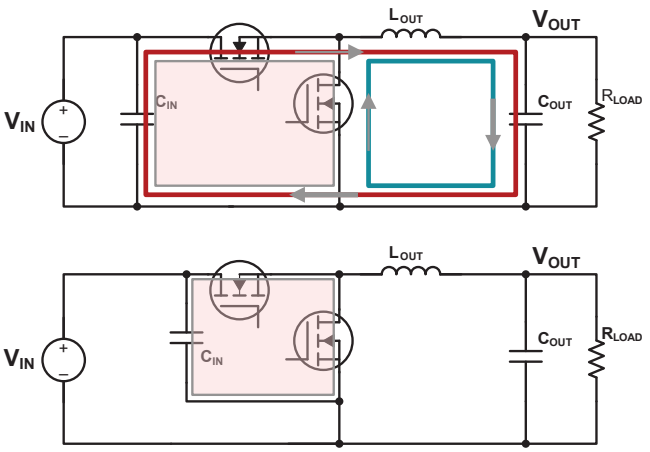

Figure 34 – Understand current flows (red and blue lines) and minimize the switching loop area (pink box).

IX. Poor Thermal Design

PCB layout is important not only for electrical performance but also thermal performance. Besides IC specific parameters, PCB layout is a very important, if not the most important, variable in a design affecting the thermal performance of an IC. The PCB layout is important because it is a strong determining factor for the junction to ambient thermal resistance of the IC. As mentioned in Section III, thermal performance matters because poor layout can result in a part not working as expected in an application or it can reduce the lifetime of the IC.

Figure 35 shows the thermal images of the same part with two different PCB layouts. The thermal image for both the top-side and bottom-side are shown. Both boards are 2-layer boards with 2 ounce copper. On Board A the IC temperature is 86 °C and the maximum temperature on the bottom layer is 62.6 °C. On Board B the IC temperature is 66 °C and the maximum temperature on the bottom layer is 52.2 °C. Why is the operating temperature of the IC higher on Board A?

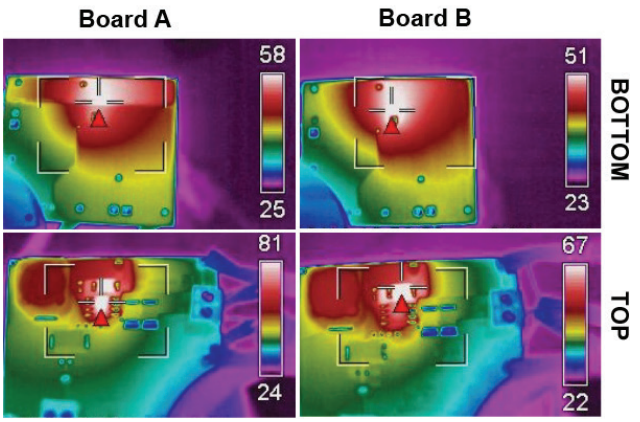

Figure 35– Thermal images of two different PCBs.

The IC operates at a higher temperature on Board A because of a horizontal trace cutting through the bottom-layer of the PCB. This is the only difference between Board A and Board B. This trace reduces how effectively the heat spreads across the entire bottom layer. Because of this trace affecting the thermal performance, this trace is visible in the thermal image of the bottom layer of Board A.

When laying out the PCB, thermal dissipation should be kept in mind. Figure 36 illustrates how heat transfers from the IC into the PCB and the ambient air. Transferring heat from the IC into the PCB is typically the most effective way to get heat out of the IC, however some heat will also transfer to the ambient air through the top of the IC. There are multiple standard thermal parameters which quantify how effective each path is at getting heat out of the IC. For more details, see reference [6].

To maximize thermal dissipation in the layout it is important to minimize cuts in the copper planes and to allow the heat to effectively spread laterally across the board. Copper planes of the PCB provide the lowest thermal resistance to spread the heat throughout the PCB, so cuts in the copper planes will increase the thermal resistance. The ground plane is typically used for spreading the heat because this is typically the largest copper area in a PCB layout. Thermal vias should be used and placed to spread heat vertically in the PCB to other layers. The bottom and top layers of the PCB are important for thermal dissipation because this is where the heat transfers from the PCB to the ambient air [10].

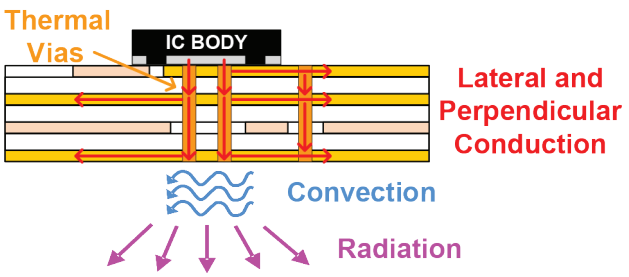

Figure 36 – Example heat transfer paths from the IC to the PCB to the ambient air.

ICs with thermal pads can more effectively transfer heat from the IC into the PCB in comparison to a part without a thermal pad, in general. To maximize the heat transfer, vias should be placed in the thermal pad's PCB footprint to provide a path for the heat to conduct vertically to other layers. A recommended via pattern, like what is shown in Figure 37, can be found in the PCB footprint recommendation at the end of each datasheet.

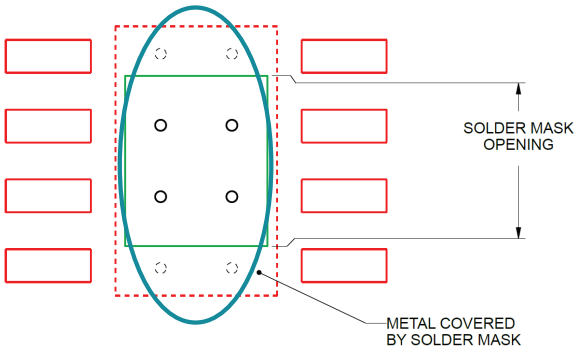

Figure 37 – Example thermal pad package PCB footprint with a recommended via pattern.

X. Poor Voltage Measurement

After you have built your converter, it comes time to test its performance. One common waveform to measure is the output voltage ripple. If care is not taken with this measurement, it is easy to get erroneous results. This is especially important when millivolts matter in low output voltage applications. See Figure 38, for example.

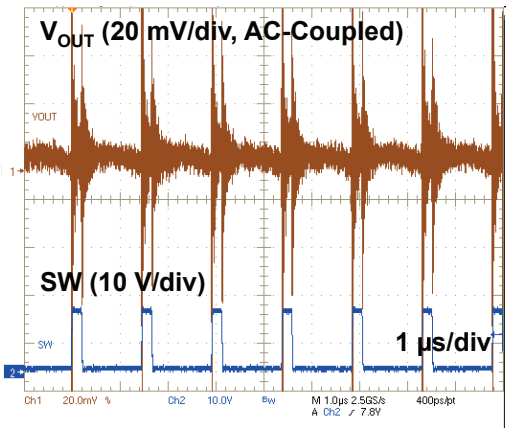

Figure 38 – Noisy output voltage measurement.

The output voltage waveform in Figure 38 is AC-coupled and zoomed in at an appropriate scale. This is good. However, the waveform measurement is not clean. Switching noise is being picked up from the switch node measurement on channel 2. There also is no bandwidth limit set on the output voltage measurement. Limiting the bandwidth to 20 MHz helps to focus on the lower frequency output voltage ripple and not on higher frequency radiated noise that is being picked up. Compare Figure 38 to a clean output measurement shown in Figure 39.

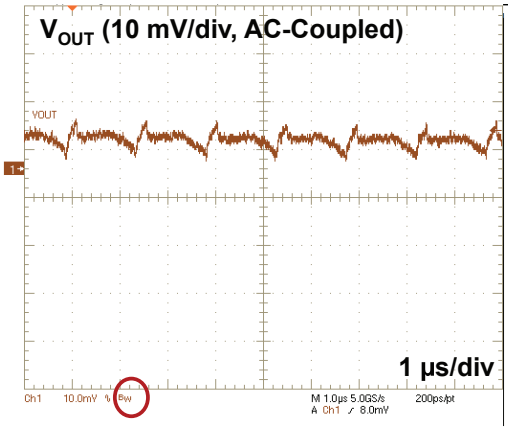

Figure 39 – Clean output voltage measurement.

In Figure 39, a more accurate output voltage measurement is observed. The output ripple due to the output capacitors and their parasitic elements (ESR and ESL) is clearly visible. The Y-axis scale is zoomed in to its maximum of 10 mV/div. The 20 MHz bandwidth filtering is active which helps to remove unrelated noise. The switch node measurement has also been removed as it is not needed.

There are a few recommendations to follow when probing key voltage waveforms. Measure the output voltage directly across the output capacitor. Consider using a "tip and barrel" approach shown in Figure 40 instead of having a flying ground lead. This will reduce the amount of radiated noise picked up (the flying ground lead acts like an antenna). There are also other techniques using probe sockets that may be useful to reduce the measurement loop area. Limiting the scope probe bandwidth to 20 MHz helps to focus the time domain measurement. Set the Y-axis scale to take up as much of the oscilloscope viewing area as possible. Using 1:1 passive probes or active probes may also be useful [11]. They enable sub-10 mV range measurements with an oscilloscope.

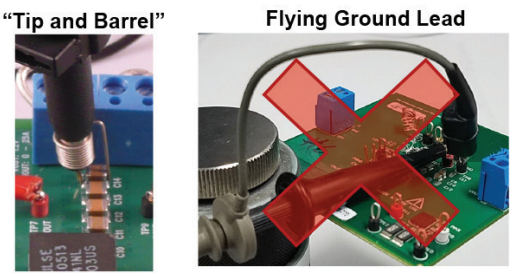

Figure 40 – Try using a "tip and barrel" approach instead of a flying ground lead when taking output voltage measurements.

XI. Poor Bode Plot Measurement

Evaluating the stability of a POL converter is an important part of validating a design. To evaluate the stability, the Bode plot can be measured by injecting a signal into the control loop between V_{OUT} and the top feedback resistor as shown in Figure 41. Practically this is done by adding a 10 to 50 Ω resistor into the feedback path then injecting a signal across this resistor using a transformer.

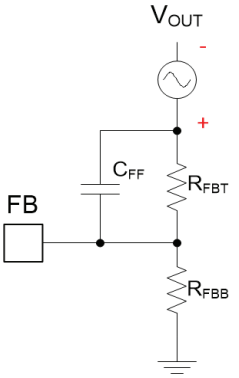

Figure 41 – Simplified schematic for Bode plot measurements.

There are some mistakes that can be made when taking the measurement that result in an inaccurate measurement. Figure 42 shows a loop measurement where the Bode plot is not smooth from about 50 kHz and higher. What can cause this?

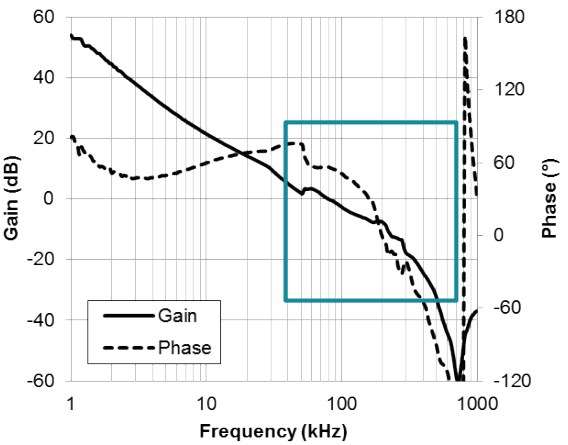

Figure 42 – Bode plot with poor measurement for high frequencies.

For this measurement, the signal injected into the loop was too large. This caused some large signal characteristics of the IC to affect the control loop. Figure 43 shows the switching node and output voltage of the converter with a 100 kHz signal injected into the loop. This signal is the same amplitude as the one used to measure the Bode plot in Figure 42. Injecting too large of a signal caused the converter to skip pulses at the switching node. When the converter skips pulses, the loop measurement is no longer valid because it is no longer a small signal measurement. Generally, a POL converter will be sensitive to too large of signal injection at frequencies above the crossover frequency because the loop does not attenuate the signal amplitude.

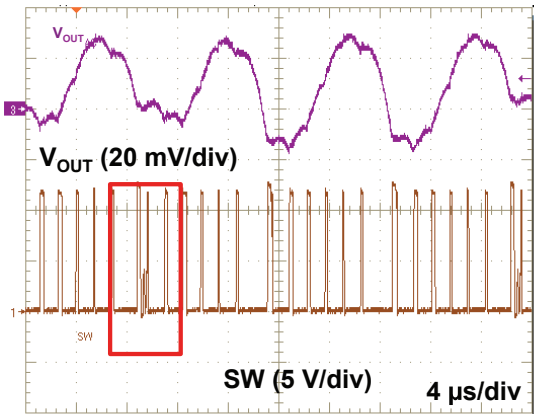

Figure 43 – Converter pulse-skipping due to too large signal injection.

Figure 44 shows a loop measurement where the Bode plot is not smooth for frequencies less than 10 kHz. What can cause this?

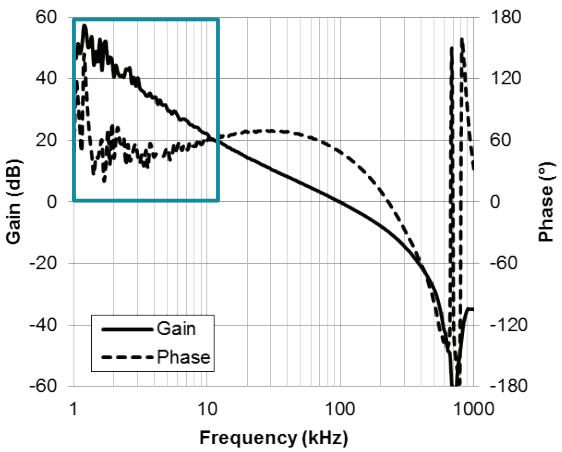

Figure 44 – Bode plot with poor measurement for low frequencies.

For this measurement, the amplitude of the signal injected into the loop was too small. The equipment used to measure the loop is unable to get an accurate measurement at lower frequencies because the signal-to-noise ratio was too low. A larger amplitude signal is typically needed at frequencies below the crossover frequency because the loop will attenuate the injected signal. Alternatively, equipment used to take frequency response measurements usually have settings that can be adjusted to filter out some of the noise. For example, some equipment can increase the integration time or decrease the IF filter bandwidth.

Figure 45 shows a loop measurement where more optimal signal injection amplitude was used across the entire frequency range giving a smooth Bode plot. For this measurement, the signal injection amplitude was varied versus frequency. Larger amplitude was used below the crossover frequency and smaller amplitude was used above the crossover frequency. Monitoring the waveform at the output and at the switching node can aid in optimizing the signal injection amplitude. Figure 46 shows the switching node and output voltage with good signal injection amplitude. The switching node is regular and the output voltage has visible ripple at the injection frequency.

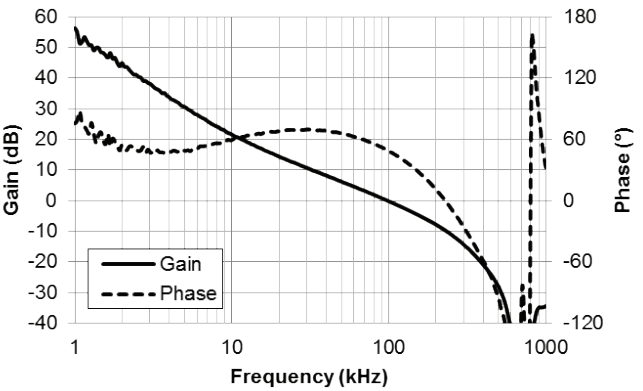

Figure 45 – Bode plot with proper measurement for low frequencies.

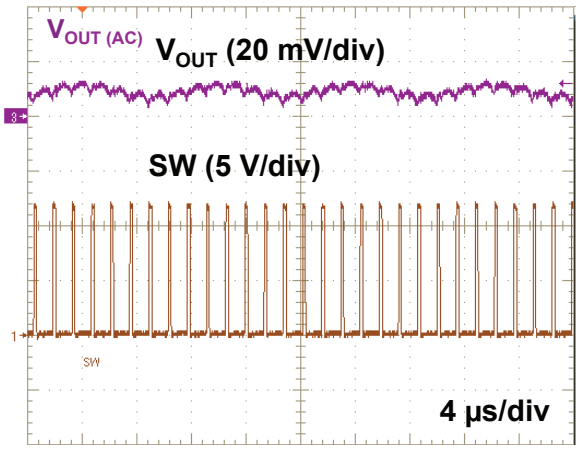

Figure 46 – Converter output voltage and switching node with optimal signal injection.

XII. Summary

When designing a POL regulator, there are multiple stages in the design where a mistake may be made. These mistakes can occur when selecting the regulator, selecting the external components around the regulator, designing the PCB layout and testing the final design. This paper covered ten common mistakes we have seen made throughout the entire design process. The cause of each mistake was explained along with how to fix them. This paper can be used to learn from others' mistakes so that you can avoid making them. It can also be used as a reference to aid in debugging an issue you are currently having with a regulator. The cause of the problem may not be exactly the same as shown in this paper but these examples can be useful to brainstorm possible causes.

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