

Power Supply Design Seminar

Voltage Regulator Design and Optimization for High-Current, Fast-Slew-Rate Load Transients

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Voltage Regulator Design and Optimization for High-Current, Fast-Slew-Rate Loads

Carmen Parisi

ABSTRACT

Designing to the tight voltage tolerances of today's modern central processing units and field-programmable gate arrays (FPGAs) is becoming more difficult as their current draw increases and becomes more dynamic. Getting the correct output capacitance mix to ensure first-time power-delivery success is no small feat with >100-A steps and slew rates in excess of 100 A/μs. Standard point-of-load design techniques no longer hold true; we need new methods to choose the output capacitance.

This topic breaks down regulator transient response, the effects of load slew rate on C_{OUT} selection and two methods of calculating C_{OUT} in processor power applications. The first method is a charge-based approach in the time domain, while the second method calculates a target impedance across a range of frequencies. When used in conjunction with one another, these approaches meet the transient specifications of a high-current FPGA core voltage rail. This topic also includes an overview of regulator output impedance, load lines and the effect of control topology on transient response.

I. INTRODUCTION

With every new processor generation, the demand placed on voltage regulators for ever better performance increases. Modern CPUs and FPGAs can now draw peak currents in excess of 400 A with greater than 100 A transients at slew rates exceeding 1000 A/μs. As the speed and size of these transients increase, the allowable tolerance on the core output voltage shrinks to ±3% or lower. If the voltage rails to these CPUs exceed their r limits, then issues such as clock drift or timing skews inside the processor can occur and cause processing errors. In the worst case, physical damage to the processor, board or regulator can happen as well.

Designing a regulator output filter and laying out a motherboard to power these processors is no easy task. First time success of a design is often crucial to hitting product release targets. A prototype run of ten 12" x 12" 14-layer printed circuit boards with impedance controlled traces and micro-vias can run more than \$5,000 just for the PCB fabrication. Too many board spins can quickly cause a project to go over budget and be cancelled.

The standard regulator design techniques called out in most application notes and introductory textbooks are no longer enough when faced with high-performance, high-current loads. An approach combining transient performance in the time domain as well as a power network's output impedance in the frequency domain is needed. This paper will discuss the shortcomings of standard design techniques while introducing the concepts needed to hit the tolerances of today's demanding applications such as target impedance, DC load lines and converter output impedance.

A. Modern Processor Specifications

In Figure 1, several current processor power specifications are shown for a variety of applications. Regardless of the end equipment, all the examples feature load steps ≥50% of the maximum current at slew rates typically in excess of 100 A/μs. Each set of specs offers its own complexities but designing a regulator to meet the necessary requirements is certainly achievable with the proper design techniques.

Processor	Nominal Voltage	Output Tolerance ($\Delta V_{OUT(AC)}$)	Max Current	Max Load Step	Load Slew Rate
Communications ASIC	1.0 V	± 50 mV ($\pm 5\%$)	120 A	60 A	12 A/ μ s
Automotive CPU	0.90 V	± 22 mV ($\pm 2.5\%$)	90 A	60 A	100 A/ μ s
FPGA	0.88 V	± 17 mV ($\pm 2\%$)	200 A	100 A	200 A/ μ s
Server processor (current gen)	1.8 V	± 22 mV**	228 A	200 A	780 A/ μ s
Server processor (next gen)	1.8 V	± 22 mV**	400 A	300 A	670 A/ μ s

** Does not include DC load line (covered later)

Figure 1 – Modern processor spec examples.

It is important to understand a few key voltage rail specifications that commonly appear in processor documentation before starting a high-current, high-slew transient design. $V_{OUT(NOM)}$ is the nominal DC output voltage of the rail. Even with dynamic voltage settings most processors still call out a typical voltage a designer can expect the output to be regulated to a good portion of the time. $\Delta V_{OUT(DC)}$ is the plus-minus tolerance for regulation errors and steady-state ripple. Regulation errors can come from the switching converter itself, from component variations, such as feedback resistors, or from temperature drift. Finally, $\Delta V_{OUT(AC)}$ is the plus-minus tolerance for the transient response and usually includes

$\Delta V_{OUT(DC)}$ inside of it as drawn in Figure 2. This transient window can either be an absolute window around the set point or it can change depending on the operating conditions of the processor.

B. Standard Point of Load Design Does Not Work

In many introductory application notes to the buck regulator topology, sizing the output capacitance is usually limited to a simple equation like (1). This equation is based on the peak-to-peak inductor ripple current, switching frequency, capacitor ESR, and allowable steady state-ripple (Figure 3).

$$\Delta V_{OUT(DC)} = \frac{I_{PP}}{8 \cdot f_{SW} \cdot C_{OUT}} + I_{PP} \cdot ESR \quad (1)$$

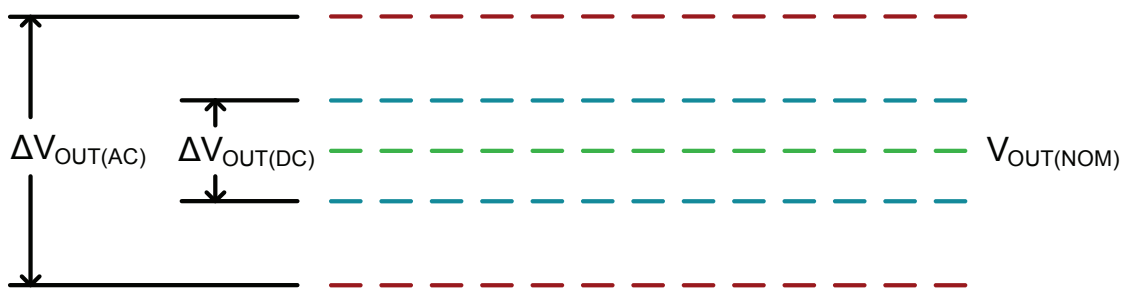


Figure 2 – Key processor specifications.



Figure 3 – Steady state ripple.

While Equation (1) may work for point of load rails that do not see large current steps, when designing for modern processors the transient response is instead the dominating factor in a design. Using only this equation to determine output capacitance, C_{OUT} , will severely underestimate the amount of capacitance needed to keep V_{OUT} within regulation tolerances. A regulator designed under these conditions will likely fall outside the $\Delta V_{OUT(AC)}$ window during transients.

II. DISSECTING THE TRANSIENT RESPONSE

Understanding transient response in both the time and frequency domain is crucial to selecting an optimal output capacitor mix and getting the maximum performance out of a power converter. To gain insight into real world performance the parasitic resistance (ESR) and inductance (ESL) of C_{OUT} must be taken into account, as shown in Figure 4.

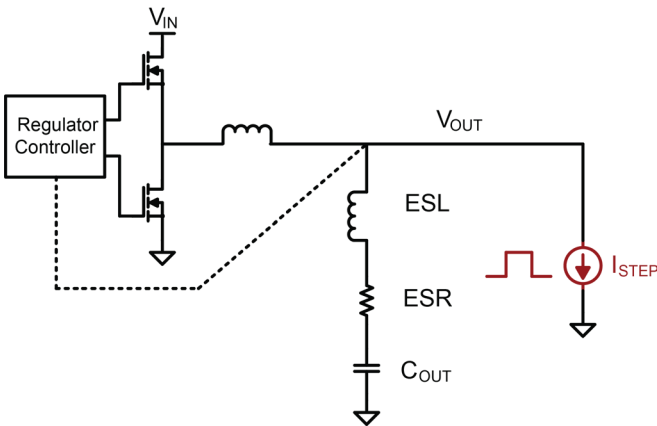


Figure 4 – Output capacitance with parasitics.

Figure 5 depicts an exaggerated version of the four main elements that compose a regulator's transient response to an aggressive load step where the slew rate of I_{STEP} is much greater than the slew rate of the converter inductor current.

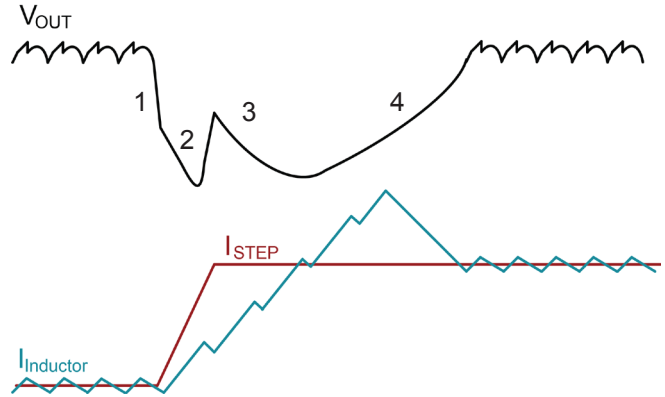


Figure 5 – Transient response in the time domain.

- Region 1 of the voltage dip is related to the ESL of C_{OUT} and the load slew rate. A faster slew rate yields a larger ESL spike.
- Region 2 is the voltage drop proportional to the step size multiplied by the ESR. During this time, inductor current begins to slew upwards in response to the step.
- V_{OUT} continues to dip in Region 3 as C_{OUT} is further discharged while trying to hold the voltage at $V_{OUT(NOM)}$. Adding additional capacitance to the output will dictate this portion of the response.
- At the inflection point between Region 3 and 4 the inductor current matches the value of the load current. As the current overshoots the new load value, charge on C_{OUT} is replenished and V_{OUT} rises back to $V_{OUT(NOM)}$.

Depending on the exact parameters of the load, regulator bandwidth and C_{OUT} mix, observing transient response on the bench might show these elements blending together. Upon load release, the same basic response occurs again only with V_{OUT} swinging above the nominal value rather than below. Should either edge's slew rate be equal to or less than the inductor's slew rate then no real transient event occurs and V_{OUT} is essentially undisturbed.

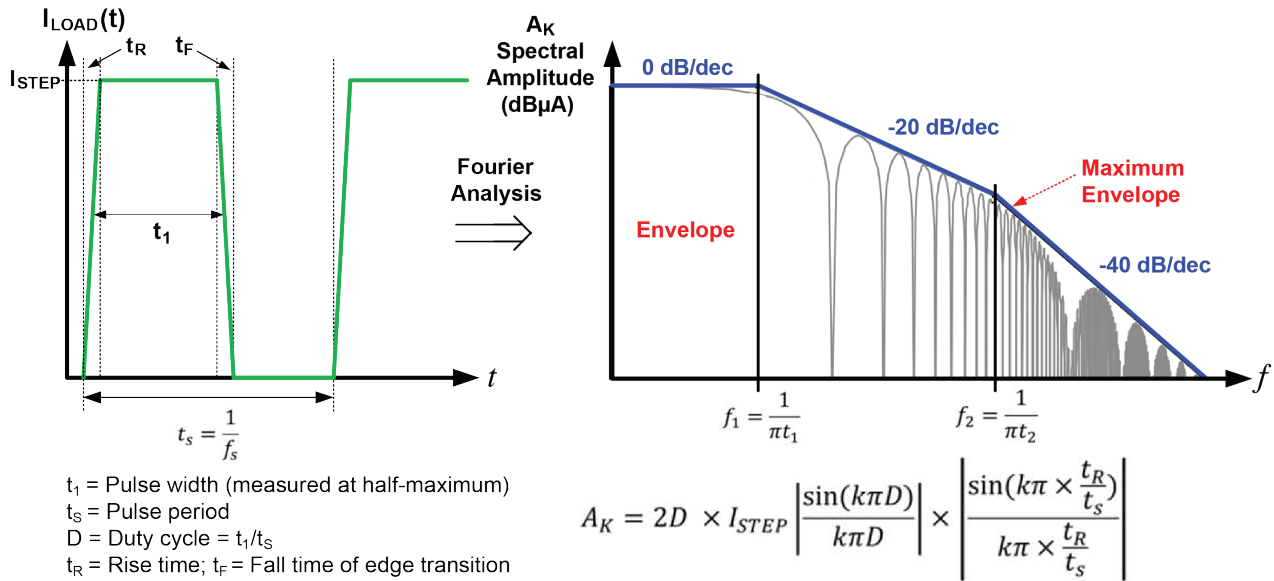


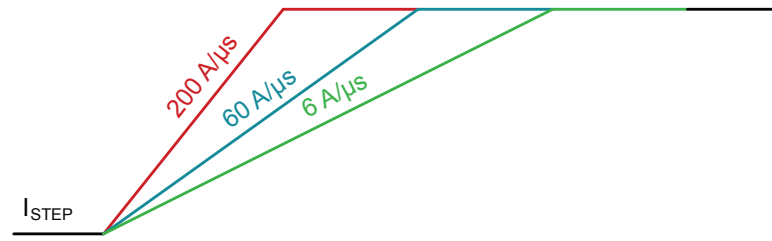
Figure 6 – Transient response in the frequency domain.

Figure 6 focuses on the load transient waveform itself in the frequency domain giving insight into the harmonic content generated by a processor as it demands more current from its supply. Assuming symmetric rise and fall times, the trapezoidal shape of the load step in time yields a double-sinc function in the frequency domain. Two corner frequencies can be seen in this function, the first dependent on pulse width and the second dependent on the rise/fall time. This high frequency content is what makes the parasitics of C_{OUT} affect overall regulator performance and differentiates high-current, high-slew rate rails from simple and relatively static auxiliary voltage rails.

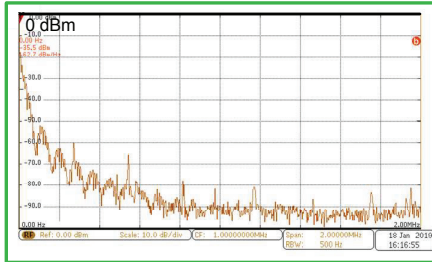
As a rule of thumb, frequencies above the -40 dB/decade breakpoint, f_2 , can be ignored as high frequency content usually drops off quickly enough to not pose an issue to the supply. However, it is a good idea to check for any processor specific requirements or high-speed bus return paths at the system level that might push the frequency of interest out higher than f_2 .

Figure 7 contextualizes the plots and equations of Figure 6 with measurements showing the relationship between load slew rate and the amplitude of high-frequency content. The slew rate was changed from 6 A/μs, to 60 A/μs, and again to 200 A/μs while the step size and on-time were fixed. The f_1 frequency from Figure 6 was kept low in order to clearly show the effects of slew rate. This was accomplished using a low duty cycle for the load transient. In a real application, the high frequency content would be even more pronounced.

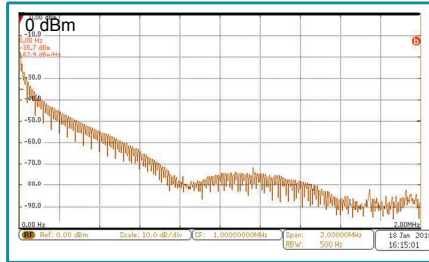
A clear relationship can be seen between load slew rate and the amplitude of the high frequency content. At the measurement center frequency, the difference between 6 A/μs and 200 A/μs is approximately 20 dB which could make the difference between the success and failure of a design that otherwise looks good on paper and in simplified simulations with ideal components.



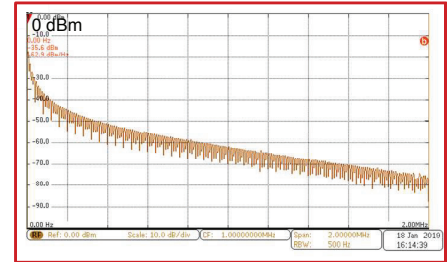
- 200 A/μs – ESR and ESL effects must be taken into account
- 60 A/μs – ESR and ESL effects might come into play
- 6 A/μs – ESR and ESL effects unlikely to affect transient response



6 A/μs – No High Frequency Content



60 A/μs – Moderate High Frequency Content



200 A/μs – Significant High Frequency Content

Figure 7 – High frequency content versus load slew rate.

III. DESIGN CASE STUDY – FPGA CORE RAIL

To illustrate the importance of working in the time and frequency domain, the output capacitance is selected for an FPGA core rail application. A TPS53681 evaluation board is used and specifications for the design are shown in Figure 8. Transient performance is evaluated using two methods for picking C_{OUT} – one charge-based and the other impedance based.

Parameter	Specifications
Input supply	12 V
Nominal output voltage	0.88 V
Max output current	200 A
Max load step	100 A at 200 A/μs
DC + AC tolerance	±2% (±17 mV)
Switching frequency	600 kHz
# of phases	6
Controller	TPS53681
Power stages	CSD95490Q5MC

Figure 8 – Case study design specifications for FPGA core rail.

IV. CHARGE-BASED DESIGN

Calculating C_{OUT} using a charge-based method is a relatively straightforward, primarily algebraic approach. From Figure 9, during a load step, the inductance, L or L_{EQ} , depending on the total phase number, takes some amount of time, $t_{UNDERSHOOT}$, to slew to the high current level. In that time, an amount of charge equal to $Q_{UNDERSHOOT}$ is pulled from the output capacitors while V_{OUT} dips below $V_{OUT(NOM)}$. Upon load release, excess charge in the inductor, $Q_{OVERSHOOT}$, is dumped into the output capacitors during time, $t_{OVERSHOOT}$, causing V_{OUT} to swing above its setpoint. After calculating $Q_{OVERSHOOT}$ and $Q_{UNDERSHOOT}$, finding the output capacitance is simply a matter of dividing the calculated charge by the allowable swing on V_{OUT} . Equations (2) through (7) show the formulas and calculations for the case study design.

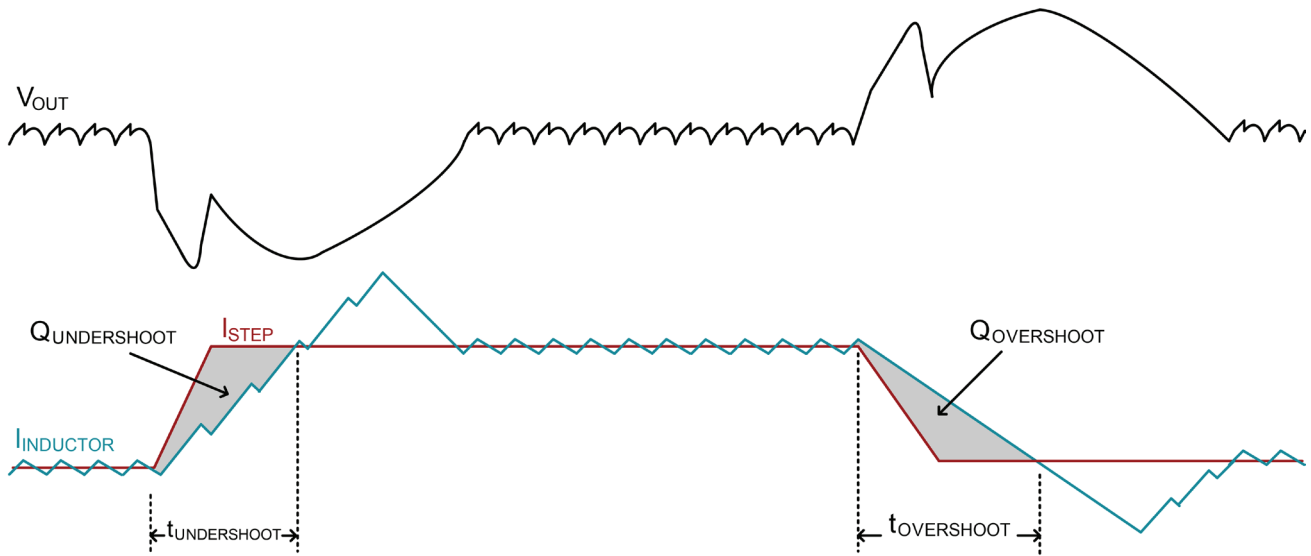


Figure 9 – Charge-based design overview.

$$t_{\text{UNDERSHOOT}} = \frac{L_{\text{EQ}} \cdot I_{\text{STEP}}}{V_{\text{IN}} - V_{\text{OUT}}} = \frac{150 \text{ nH} \cdot 100 \text{ A}}{12 - 0.88 \text{ V}} = 0.225 \mu\text{s} \quad (2)$$

$$t_{\text{OVERSHOOT}} = \frac{L_{\text{EQ}} \cdot I_{\text{STEP}}}{V_{\text{OUT}}} = \frac{150 \text{ nH} \cdot 100 \text{ A}}{0.88 \text{ V}} = 2.85 \mu\text{s} \quad (3)$$

$$Q_{\text{UNDERSHOOT}} = \frac{1}{2} \cdot t_{\text{UNDERSHOOT}} \cdot I_{\text{STEP}} = \frac{1}{2} \cdot 0.225 \mu\text{s} \cdot 100 \text{ A} = 11.2 \mu\text{C} \quad (4)$$

$$Q_{\text{OVERSHOOT}} = \frac{1}{2} \cdot t_{\text{OVERSHOOT}} \cdot I_{\text{STEP}} = \frac{1}{2} \cdot 2.85 \mu\text{s} \cdot 100 \text{ A} = 142 \mu\text{C} \quad (5)$$

$$C_{\text{UNDERSHOOT}} = \frac{Q_{\text{UNDERSHOOT}}}{\Delta V_{\text{OUT(AC)}}} = 640 \mu\text{F} \quad (6)$$

$$C_{\text{OVERSHOOT}} = \frac{Q_{\text{OVERSHOOT}}}{\Delta V_{\text{OUT(AC)}}} = 8,100 \mu\text{F} \quad (7)$$

Most of the time overshoot turns out to be the dominant factor in determining the amount of capacitance needed for a design. This is because the amount of energy stored in an inductor is proportional to I^2 . At high currents the energy stored is much larger than at low currents and more energy is absorbed by C_{OUT} during load release than is removed during a step, causing higher overshoot than undershoot.

From Equation (7), a minimum of 8,100 μF is needed to keep V_{OUT} in regulation during transients. The initial output capacitance for the design will total 8,200 μF using 11 x 470 μF , 3 m Ω bulk caps and 30 x 100 μF , 0805, X5R, 6.3 V ceramic capacitors.

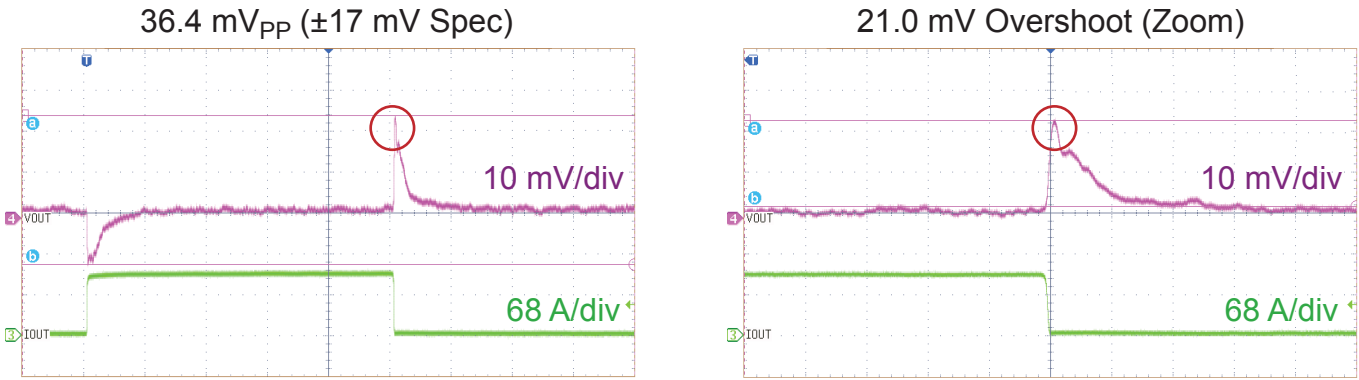


Figure 10 – Charge-based design transient response – overall response (left), overshoot zoom (right).

A. Charge-Based Approach Performance

Evaluating the transient response with this configuration of output capacitance yields the results in Figure 10. With a design spec of ± 17.6 mV_{PP} this configuration is outside of the limits during the overshoot, exceeding the target by 3.4 mV. Looking closely at the zoomed in waveform of the overshoot shows that the initial spike corresponding to the ESR and ESL of C_{OUT} is outside the upper limit of $\Delta V_{OUT(AC)}$. Using the charge-based method for selecting C_{OUT} only keeps the voltage swing related to the amount of capacitance (Region 3, Figure 5) within allowable tolerances but cannot account for ESR and ESL effects when high frequency content from the load cannot be ignored.

B. Charge-Based Shortcomings

The charge-based method for calculating the output capacitance is a starting point, but it does not include important variables that can significantly affect performance. One issue is that this method does not take into account any performance aspects of the controller, such as its bandwidth. Secondly, and more importantly, there are no terms for either ESR or ESL in the equations. There is an assumption made that the load slew rate is not fast enough for them to matter. A better method for calculating C_{OUT} is needed that takes into account the frequency domain performance of the voltage regulator and chosen capacitors.

V. TARGET IMPEDANCE DESIGN

A. Output Impedance Overview

A generalized converter output impedance curve is shown in Figure 11 looking back from the processor towards the output capacitors and voltage regulator. At low frequencies, the overall impedance of the power delivery network (PDN) is dominated by the performance of the voltage regulator. The converter will attenuate the open loop impedance by the overall loop gain at frequencies inside its bandwidth. Should the slew rate of a load transient only generate frequency content inside the loop bandwidth of the converter, the attenuated impedance of the system will show up on a scope as minimal V_{OUT} swings and the charge-based design method may be sufficient. Outside of the regulator bandwidth, transient performance is entirely dependent on the PCB layout, component placement and capacitor selection.

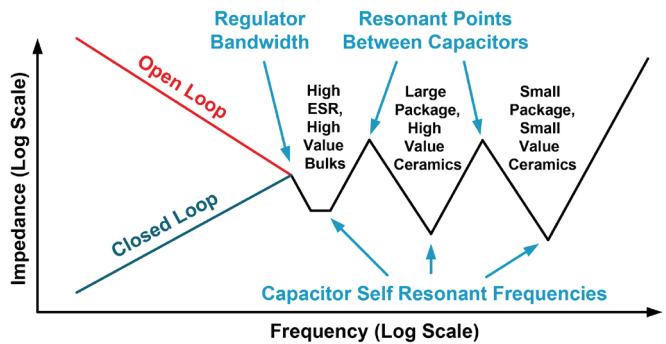


Figure 11 – Generalized converter output impedance.

As load current harmonics move outside converter bandwidth, the capacitors that make up C_{OUT} begin to dictate performance. At some frequency each capacitor type used will hit its self-resonant frequency and cease to function as a capacitor. Beyond this point ESL dominates and the impedance of the capacitor starts to rise. When properly selected, using a mix of bulk capacitors, high value ceramics and small value, small package ceramics can give good performance across a wide frequency range. Generally, the goal is to design a flat impedance profile over frequency for predictable PDN performance. Large resonant peaks and dips should be avoided where possible.

B. Target Impedance and Output Impedance Modeling

When the charge-based method for choosing C_{OUT} is ineffective, as it is for the case study, it is necessary to look at the output impedance and use frequency domain analysis. Setting a target impedance based on the performance requirements in a processor power specification early in the design stage is crucial for evaluating the impedance of a PDN. A target impedance sets a level across all frequencies that a converter’s output impedance should not exceed in order to keep V_{OUT} in regulation. At some frequency, however, impedance will always rise above the target value. Transient and processor specifications determine where the crossing point is for a given design.

In order to know if a design hits the target impedance, a model of the system’s output impedance is needed. Modeling efforts can quickly get complicated, as Figure 12 shows. PCB effects, IC packages and package caps can all be included at the cost of complexity. For high-performance systems, like the server processors detailed in Figure 1, including these terms can be a necessity. Since the current design is only using a standard evaluation board rather than a full motherboard, only the effects of the bulk and ceramic decoupling capacitors are included.

Figure 13 shows a high-level circuit diagram that can be used to quickly and easily mathematically model output impedance in a spreadsheet using Equation (8). $R_{LoadLine}$ is the

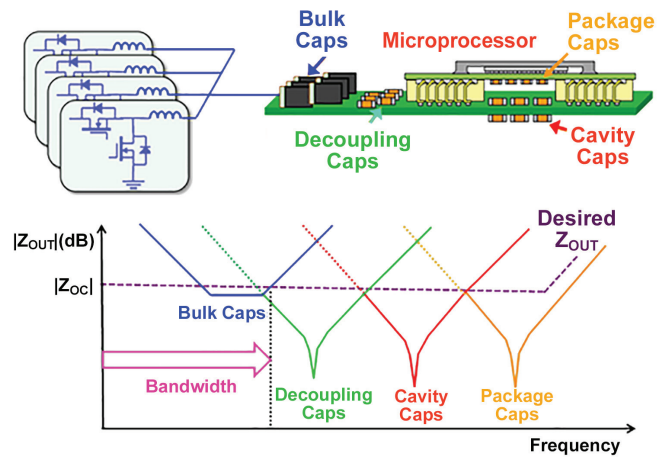


Figure 12 – Target impedance level across frequency and PCB.

output impedance of the regulator itself, including the influence of bandwidth. For simplicity, this term assumes a well-compensated control loop with single pole response. In the current design, $R_{LoadLine}$ is set well below 1 mΩ to mimic the effects of a high loop gain at low frequencies, providing significant attenuation. Actual load lines will be discussed in Section 15. $Z_{Regulator}$ and Z_{CPU} are the impedances of the 470 μF bulk capacitors close to the converter output and 100 μF ceramics near the load respectively. These terms include the effects of both ESR and ESL associated with each type of capacitor. R_{PCB} models the resistance of the PCB between the two capacitor types. An example impedance curve using this model is shown in Figure 14.

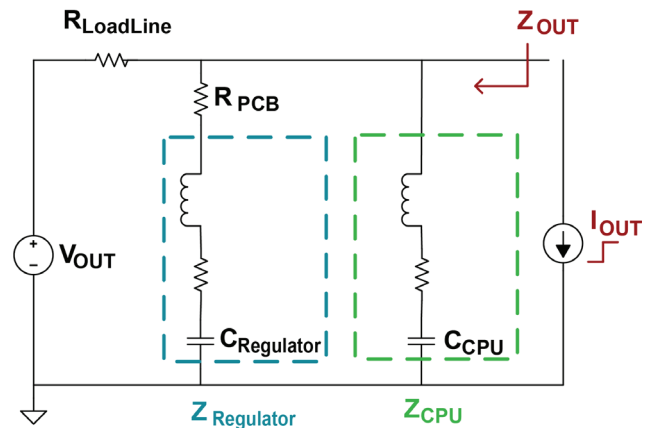


Figure 13 – Simplified output impedance model.

$$Z_{OUT} = R_{LoadLine} \left| (Z_{Regulator} + R_{PCB}) \right| Z_{CPU} \quad (8)$$

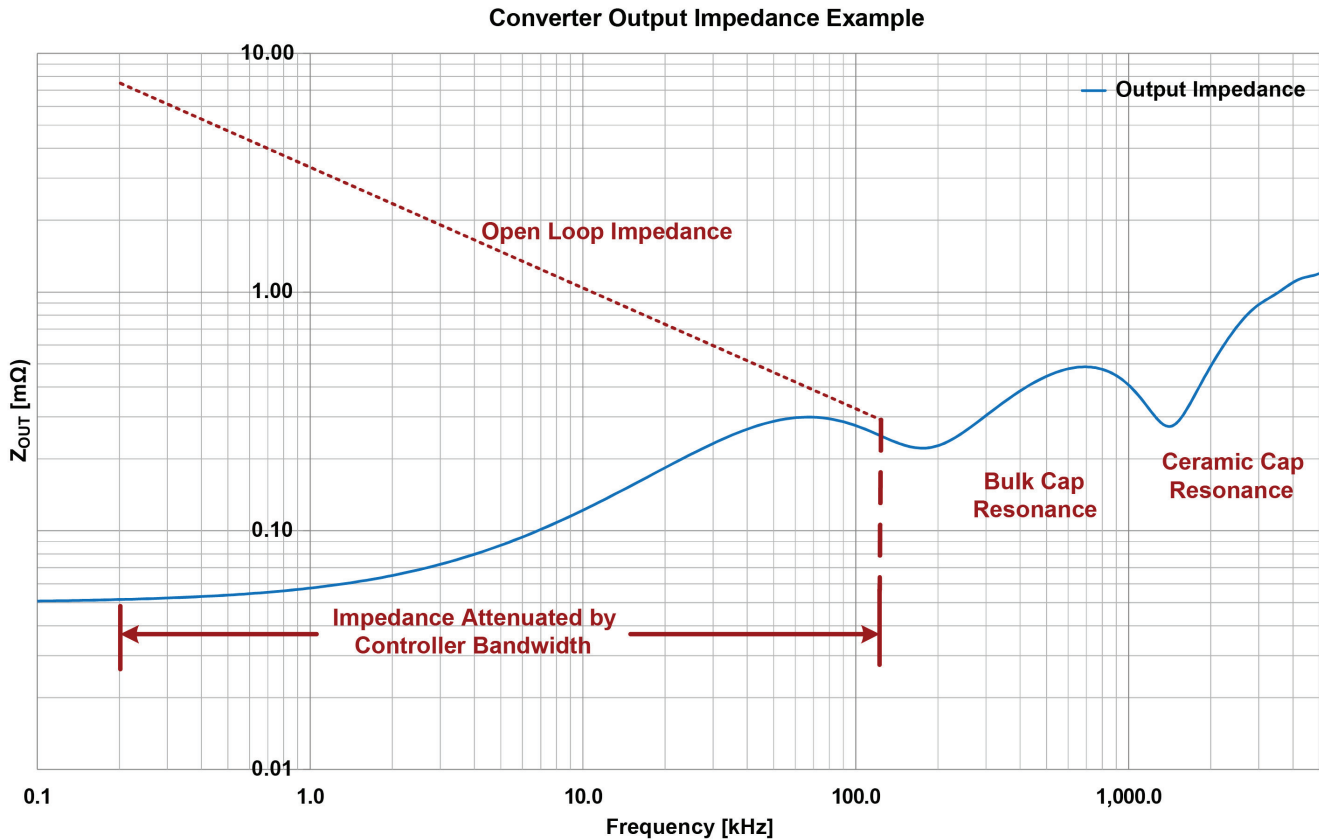


Figure 14 – Example of impedance model results.

This simple model has the benefit of being faster than full simulations for evaluating various C_{OUT} capacitor mixes. It can be used in feasibility studies or for spotting potential issues when troubleshooting in the lab. Changing the number of capacitors or other parameters updates the curve in real time rather than having to wait minutes, or more, for a full simulation to run. Real capacitor impedance data downloaded from vendor websites in CSV files can be easily incorporated into the model for Z_{PHASE} and Z_{CPU} . This gives insight at high frequencies where capacitor choice dominates performance.

The main drawback of this impedance model is also its simplicity. Only minimal PCB effects are included and incorporating all the possible

capacitors and interfaces shown in Figure 12 would quickly become cumbersome in a spreadsheet. The exact transfer function of the voltage control loop is not modeled fully either and so this model may miss performance differences between different topologies or mask potential issues if regulator stability is a concern.

A full simulation using a verified regulator model, real capacitor data and parasitic extractions of the PCB would certainly give a better picture of a PDN's impedance. However, early in the product cycle before a regulator is chosen and a board is laid out, simple models like Figure 13 are useful to get accurate C_{OUT} estimations and to key in on performance aspects that need to be addressed with more detail later in the design process.

C. Calculating Target Impedance

For the case study design, a target impedance of $0.176 \text{ m}\Omega$ can be calculated from Equation (9) and the specifications from Figure 8. Since Equation (9) is a general formula, $DC_{LL} = 0$ because this design does not call for a load line. Using Equation (10) to find the -40 dB breakpoint from Figure 6, the target frequency to meet the transient requirements for the FPGA load profile of this design is found. The output impedance should stay below the target impedance out to 636 kHz or beyond.

$$Z_{TARGET} = \frac{\Delta V_{OUT}}{I_{STEP}} + DC_{LL} = \frac{17.6 \text{ mV}}{100 \text{ A}} + 0 \text{ m}\Omega = 0.176 \text{ m}\Omega \quad (9)$$

$$f_{TARGET} = \frac{I}{\pi \cdot t_{RISE}} = \frac{I}{\pi \cdot 500 \text{ ns}} = 636 \text{ kHz} \quad (10)$$

Using the simplified output impedance model, calculated target impedance and frequency and a measured 100 kHz loop bandwidth, the output impedance of the charge-based design can be evaluated. In Figure 15 the reason why the transient response fails to meet the design targets becomes clear. Around 40 kHz , well below the 636 kHz target frequency, the output impedance rises above the $0.176 \text{ m}\Omega$ target impedance even when loop gain attenuation is taken into account. Using impedance based design techniques before soldering caps to the board would show that the large ESR and ESL overshoot spike of Figure 10 is expected despite having enough capacitance to handle the inductor energy dump upon load release. The need for more capacitance would be seen earlier in the design process, saving time and resources.

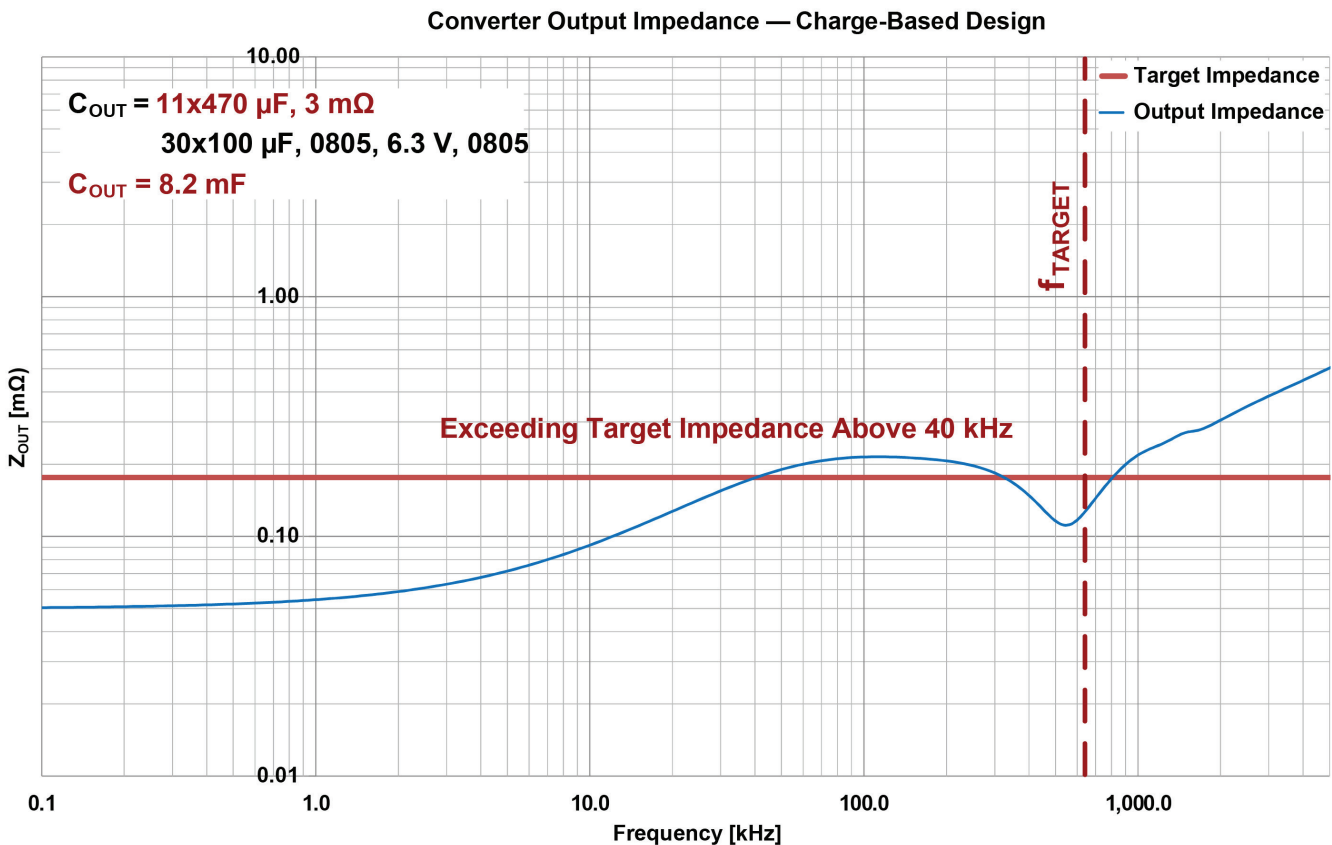


Figure 15 – Output impedance model of charge-based design.

Because the charge-based design is failing at frequencies inside the loop bandwidth, more ceramic capacitors are unlikely to affect the impedance significantly. Impedance attenuation from the loop gain is not enough to overcome the high capacitor impedance. Additional 470 μF bulks are needed instead. Increasing the number of bulk capacitors until the impedance curve drops below the target level gives the results in Figure 16. An extra six capacitors, or 2.8 mF, are needed to

reduce the impedance enough to meet specifications. When these components were soldered to the evaluation board, the transient waveforms in Figure 17 were captured. Designing to the target impedance reduced the overshoot spike to 16.4 mV from 21.0 mV and the output voltage is now within the $\Delta V_{\text{OUT(AC)}}$ window. Additionally, output impedance is now below the target level out to 1 MHz, almost twice the target frequency.

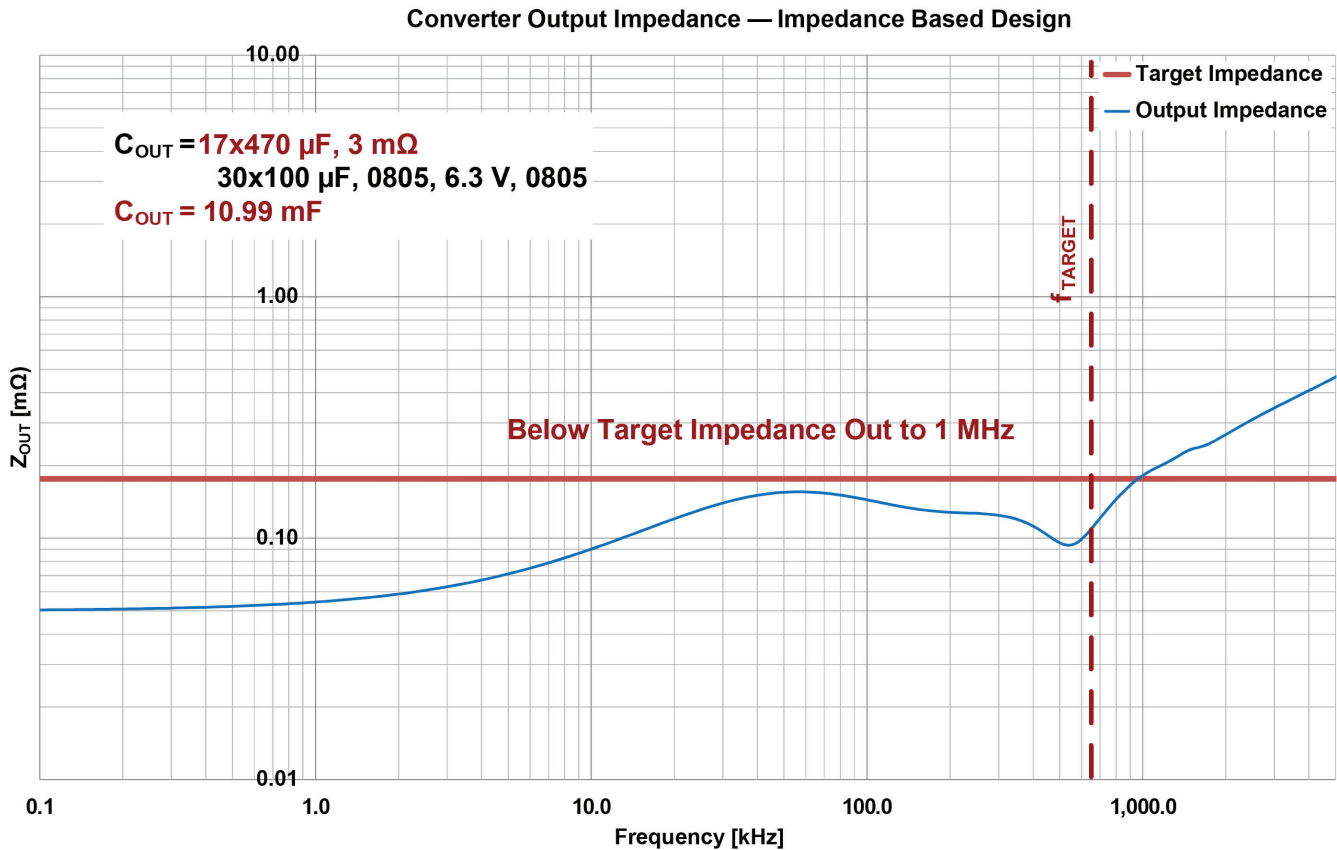


Figure 16 – Output impedance model of target impedance design.

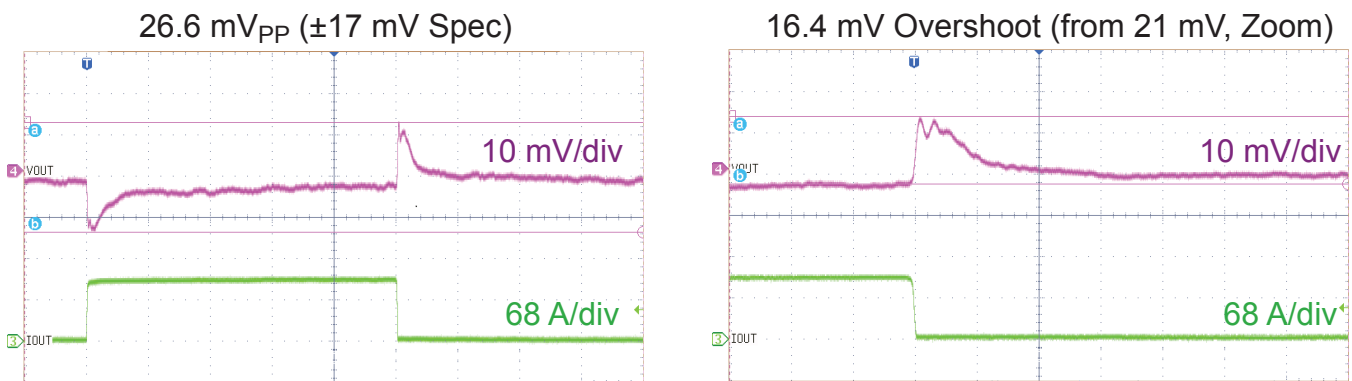


Figure 17 – Target impedance based design transient response – overall response (left), overshoot zoom (right).

VI. INFLUENCE OF CONTROL SCHEME

The importance of using a high bandwidth regulator when designing for high performance transients cannot be overstated. A fast, high bandwidth converter will react quickly to load transients and better attenuate the open loop output impedance, giving predictable performance until output capacitance and PCB effects dominate. Both benefits make it easier to design to tight regulation tolerances and can reduce both the number of output capacitors and the amount of overall capacitance needed. Alternatively, thanks to better impedance attenuation, high bandwidth can save money by allowing the use of low performance, cheaper capacitors with high ESR and ESL.

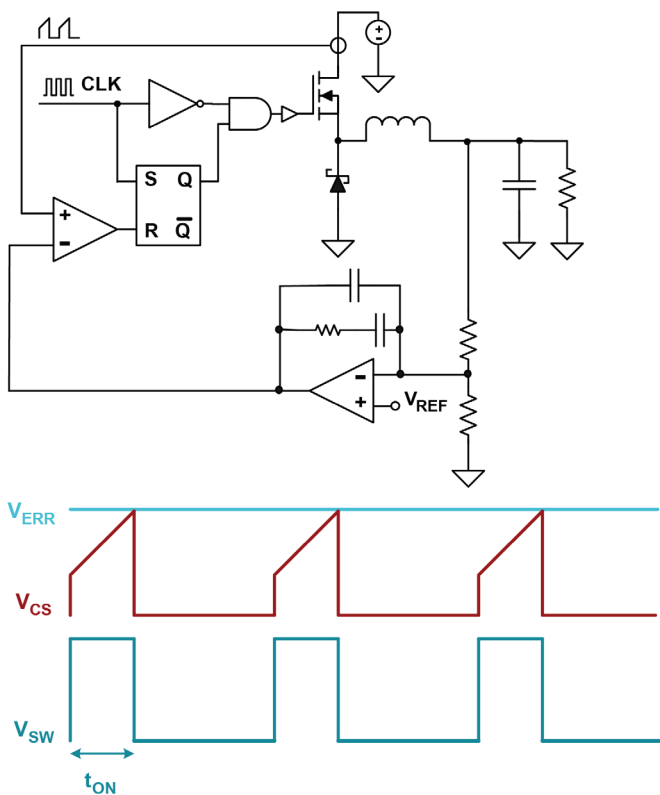


Figure 18 – Peak current mode control scheme block diagram.

Standard peak current mode control, shown in Figure 18, is an older fixed frequency control method that has inherent limits as to how high the bandwidth of a supply can be set. The inner current loop places an upper bound on the outer voltage regulation loop which reduces the speed of the system. Application notes generally suggest placing the crossover frequency of the voltage loop at approximately one tenth of the regulator switching frequency which is slow compared to modern control schemes.

TI's D-CAP+™ control mode in Figure 19 is a modern constant on-time architecture that dynamically adjusts the switching frequency during load transients while keeping it steady during static conditions. One of the benefits of this control scheme is a much higher loop bandwidth compared to peak current mode for the same design requirements. A voltage loop crossover of one quarter of the switching frequency is possible giving a faster transient response with fewer capacitors.

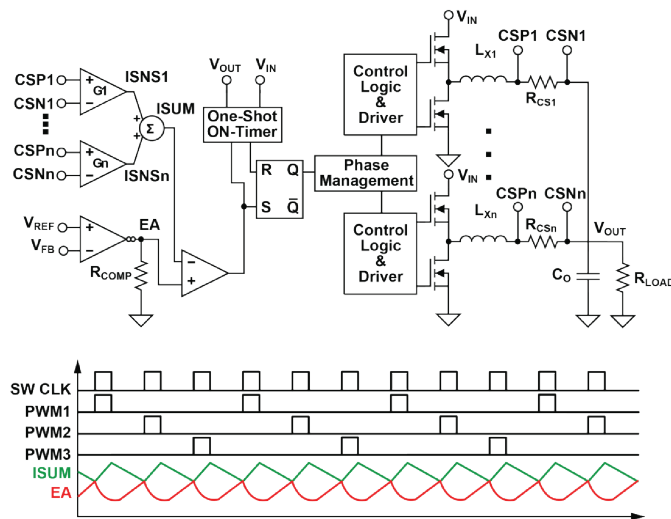


Figure 19 – D-CAP+ control mode block diagram.

The $R_{LoadLine}$ term from the simple impedance model was adjusted to study the influence of system bandwidth using the case study design specifications. Figure 20 gives the output impedance curves for both current mode and D-CAP+. A bandwidth of 60 kHz was used for evaluating current mode control, one tenth the 600 kHz switching frequency. For D-CAP+, the measured 100 kHz loop bandwidth of the design was kept. All other variables between the two curves, including C_{OUT} , were identical.

The 40 kHz difference in bandwidths has a large effect on the number of bulk capacitors needed to keep the output impedance below the 0.176 m Ω target level. Using current mode control requires an extra 8 x 470 μ F capacitors to meet the design requirements compared to D-CAP+, bringing the total number of capacitors to 25 x 470 μ F bulks and 30 x 100 μ F ceramics. At an approximate 1k price of \$0.75 each, bulk capacitors are not cheap. The right regulator control scheme can have a big impact on a design's bill of materials cost.

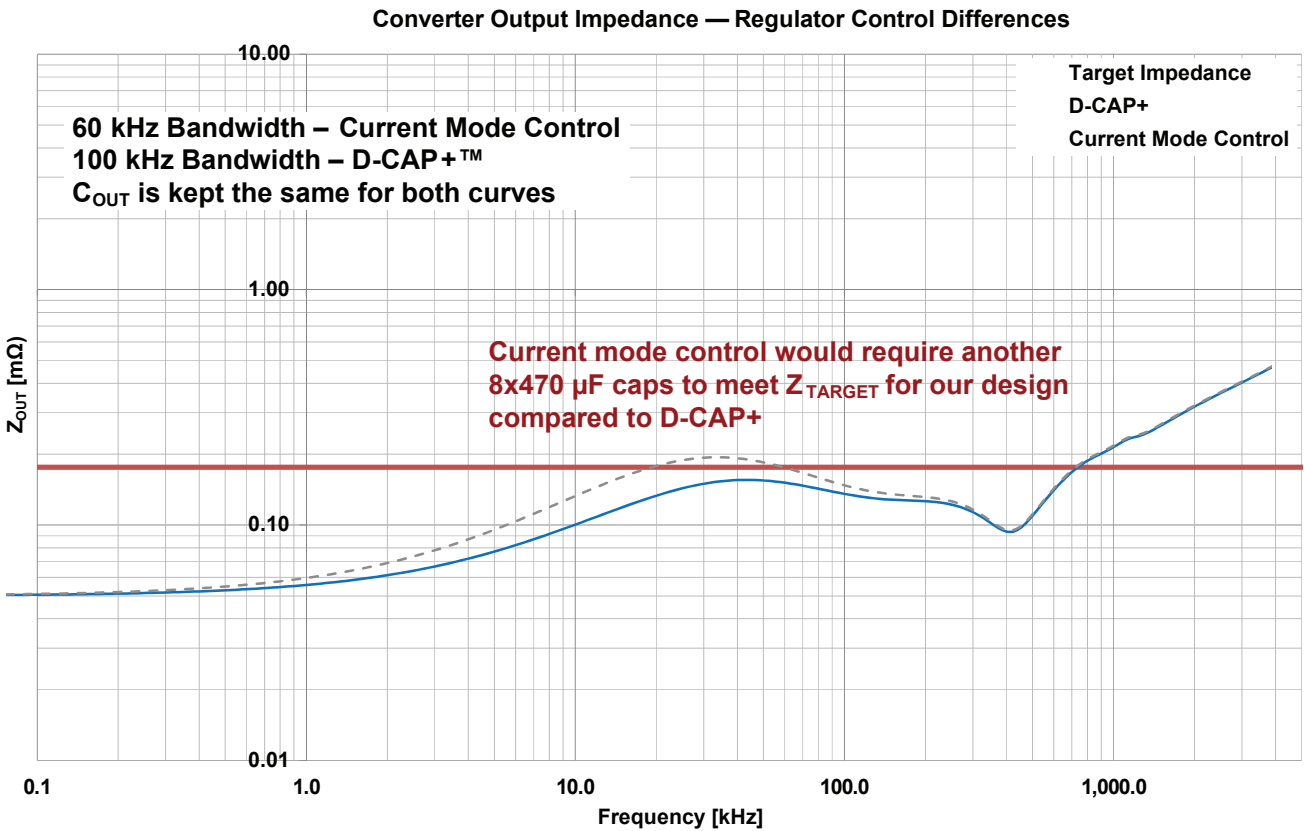


Figure 20 – Output impedance models of peak current mode versus D-CAP+.

VII. ADDING A DC LOAD LINE

Outside of a few specific vendors, DC load lines are not typically specified in the requirements for system voltage regulators. Adding a load line to a converter can go a long way to easing the difficulty of meeting a processor's power specifications by offering several performance benefits. Although not all CPUs can support a load line, it never hurts to ask the vendor if one is not explicitly called out.

A. What is a Load Line?

In the frequency domain, a DC load line looks like a fixed output impedance at frequencies inside the controller bandwidth, as shown in Figure 21. Rather than being attenuated, output impedance instead remains flat until frequencies near the converter bandwidth. Regulators with a load line can be modeled as an ideal voltage source with a series resistor on the output.

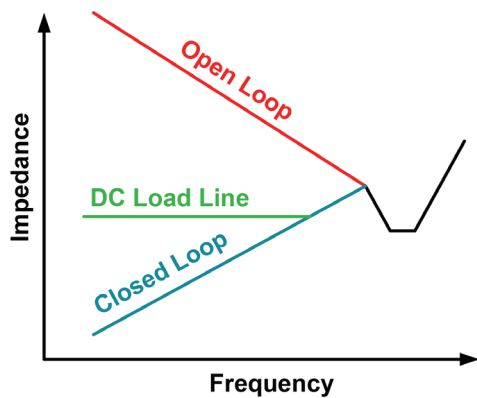


Figure 21 – DC load line in the frequency domain.

Figure 22 translates the frequency domain performance of load lines into the time domain. As load current increases, the flat output impedance corresponds to a controlled drop in V_{OUT} . The controller acts as a fixed resistor and will drop a voltage equal to the DC load line value multiplied by the load step. Because the regulator is purposefully acting as a fixed resistor, the drop, or rise, in V_{OUT} with the load would occur even with infinite bandwidth.

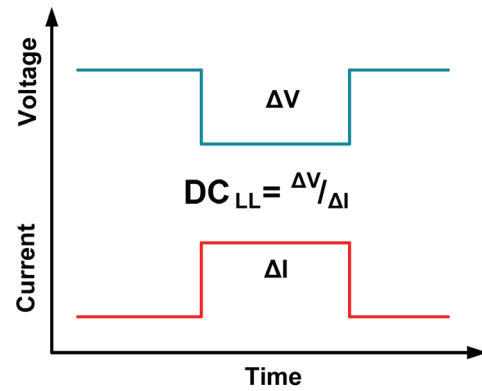


Figure 22 – DC load lines in the time domain.

Figure 23 shows the response of a regulator with a load line to a transient with slow and fast edges. A slow edge on the load step results in a slow and controlled drop in V_{OUT} proportional to the load line value and step size. When the load releases with a fast edge, the voltage regulator quickly snaps V_{OUT} up to the same voltage as before the transient occurred. For a typical transient with fast rising and falling edges, a square response with minimal over and undershoot is ideal.

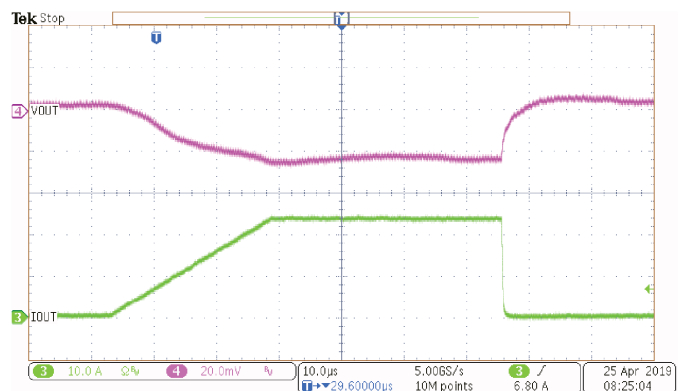


Figure 23 – Load line transient with slow and fast edges.

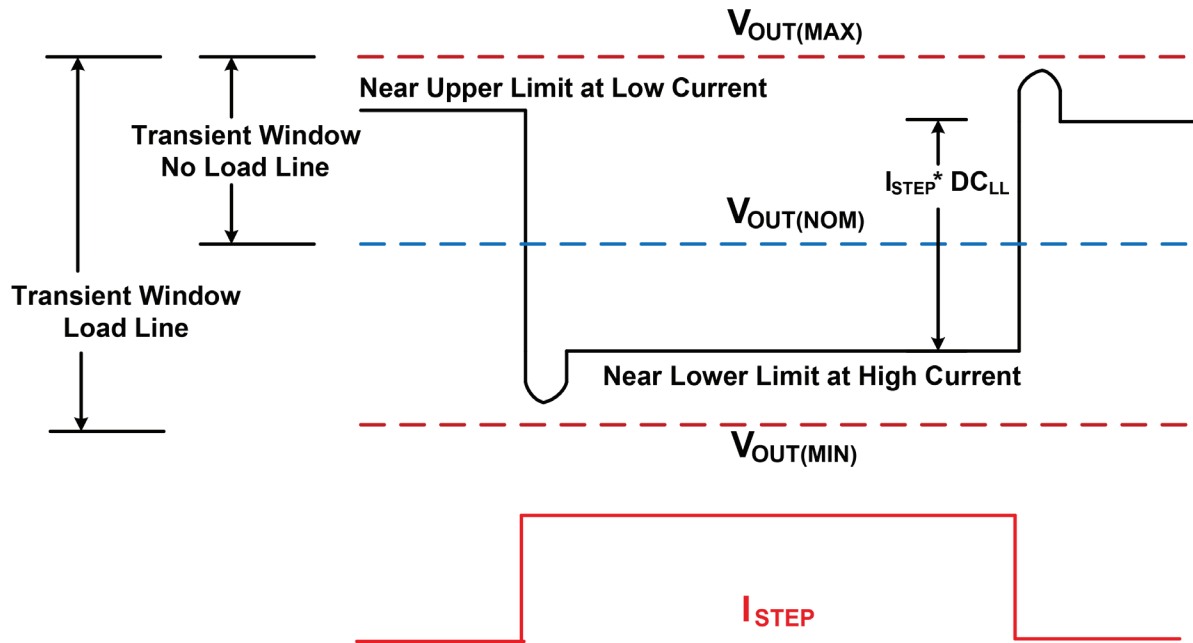


Figure 24 – Increased output swing with load lines.

B. Benefits of Load Lines

The first major benefit of adding a load line to a design is being able to make full use of the transient tolerance window in order to reduce output capacitance. Without a load line, V_{OUT} can only swing half of the tolerance window in response to either a load step or release as shown in Figure 24. With the addition of a load line, V_{OUT} can sit higher than its nominal value at low currents and lower than nominal at high currents. With this arrangement, when a step or release occurs the output voltage can now swing more than half the window, easing the design requirements on the controller.

A DC load line effectively increases the target impedance from the perspective of the voltage regulator while the processor still sees V_{OUT} staying within its tolerance band. The increased target impedance, and thus increased allowable over and undershoot, translates directly into fewer output capacitances needed to meet design targets.

The second major benefit of the load lines is an overall power savings equal to $I^2 \cdot DC_{LL}$. This power is not being burned by the regulator as heat, it is simply not drawn from the converter input supply. Significant power savings at the high currents of modern processors can ease system level thermal design constraints. For example, a voltage rail with a 0.5 mΩ load line drawing 200 A will save 20 W of CPU power draw.

Converter Output Impedance Example

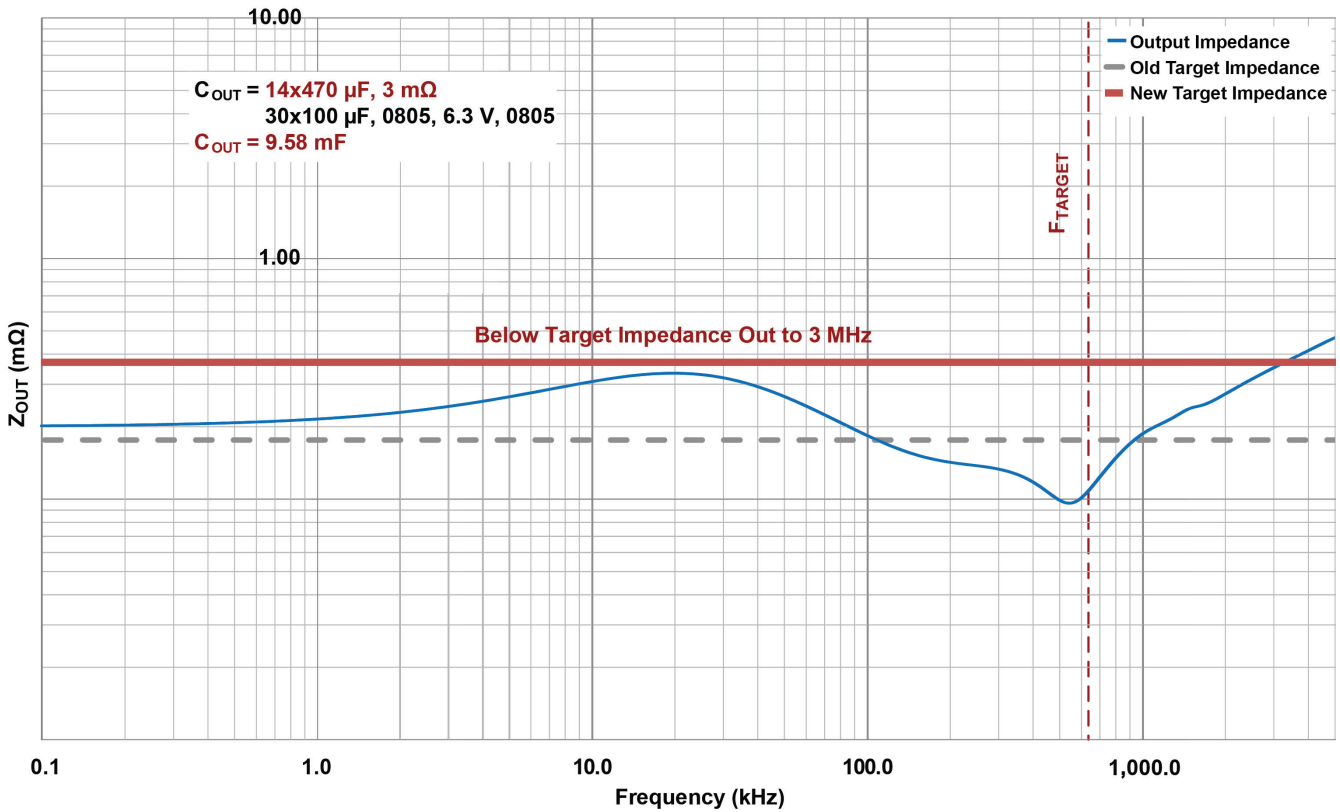


Figure 25 – Case study design impedance with 0.2 mΩ load line added.

C. Output Impedance Using Load Lines

As an experiment, the case study design’s output impedance was modelled with an additional 0.2 mΩ load line to determine the potential output capacitance savings. Using Equation (9), a new target impedance of 0.376 mΩ is found and the resulting impedance curve is shown in Figure 25.

With the addition of the load line to the design, 1.5 mF of capacitance can be saved, equal to three 470 μF bulk capacitors. With the lower capacitance, the output impedance remains below the new target impedance out to 3 MHz, almost five times the target frequency of the design.

$$New Z_{TARGET} = \frac{\Delta V_{OUT}}{I_{STEP}} + DC_{LL} = \frac{17.6 \text{ mV}}{100 \text{ A}} + 0.2 \text{ m}\Omega = 0.376 \text{ m}\Omega \tag{11}$$

VIII. SUMMARY

A comparison of the design techniques is shown in Figure 26. As stated previously, the standard ripple method underestimates C_{OUT} severely, more than a factor of ten for the case study design. A charge-based analysis can give a starting point for a design but will not give enough insight into performance for demanding transients. Working in the frequency domain to set a target impedance and estimate load frequency content can give a much greater degree of confidence in a design as they better predict real world performance.

A mix of both time and frequency domain analysis techniques are required to meet the demanding requirement of modern CPUs, FPGAs and ASICs. Capacitor impedance, regulator bandwidth, output impedance and the frequency content generated by the load are all important factors that can make or break the performance of a voltage regulator. If possible, a load line can save power and lower the overall capacitor count by increasing the effective target impedance while still keeping V_{OUT} within regulation. With proper analysis, even the tightest tolerance windows for power hungry processors can be designed to with confidence.

Design Method	Total C_{OUT}	C_{OUT} , Bulk	C_{OUT} , MLCC	Meets Design Specs
Standard ripple method	330 μ F	1 x 220 μ F, 6 m Ω	5 x 22 μ F 0805, X5R, 6.3 V	No
Charge-based	8,200 μ F	11 x 470 μ F, 3 m Ω	30 x 100 μ F, 0805, X5R, 6.3 V	No
Target Z w/ no load line	11,000 μ F	17 x 470 μ F, 3 m Ω	30 x 100 μ F, 0805, X5R, 6.3 V	Yes
Target Z w/ 0.2 m Ω load line	9,600 μ F	14 x 470 μ F, 3 m Ω	30 x 100 μ F, 0805, X5R, 6.3 V	Yes

Figure 26 – Method comparison for C_{OUT} selection.

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