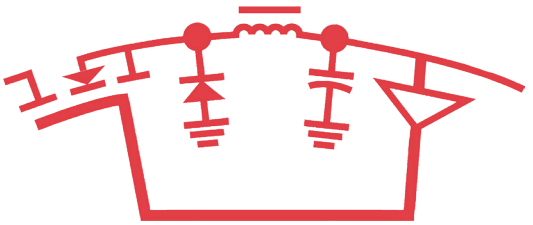

Power Supply Design Seminar

Designing a High-Power Bidirectional AC/DC Power Supply Using SiC FETs

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Designing a High-Power Bidirectional AC/DC Power Supply Using SiC FETs

Sheng-Yang Yu, Xun Gong, Gangyao Wang and Manish Bhardwaj

ABSTRACT

High-power bidirectional AC/DC power supplies are widely used as uninterruptible power supplies (UPS), energy storage systems (ESS) and onboard chargers (OBC) with vehicle-to-grid (V2G) capability. Compared to the traditional approach – using one unidirectional rectifier and one unidirectional inverter to achieve a bidirectional energy flow – a bidirectional rectifier can provide advantages such as smaller size, higher power density and higher efficiency. This paper reviews topologies, design considerations and design challenges of high-power bidirectional AC/DC power supplies. Resolving these challenges entails a deep dive into the total bidirectional AC/DC rectifier solution, including a totem-pole bridgeless PFC solution and an isolated capacitor-inductor-inductor-inductor-capacitor series resonant dual active bridge converter (CLLLC-SRes-DAB) solution using silicon carbide (SiC) MOSFETs and the gate drivers. Together, these two designs form a high-density, high-efficiency 6.6 kW bidirectional AC/DC power supply.

I. INTRODUCTION

Bidirectional energy flow using a single bidirectional power supply can save overall system cost and improve system power density when compared with using two unidirectional power supplies [1, 2]. High-power bidirectional power supplies can be found in applications including UPS, ESS and OBC with a vehicle to grid feature included in hybrid electric and electric vehicles (HEV/EV) [3]. Example system block diagrams are shown in Figure 1. As can be observed in these systems, a battery is included, requiring bidirectional energy flow capability to charge and discharge the battery. The power range of these systems is typically from 500 W to 22 kW.

Since the system power level is high, high efficiency and high-power density are required in these applications. Using the OBC system in Figure 2 as an example, the power stage of a high-power bidirectional AC/DC power supply consists of two parts – an AC/DC non-isolated rectifier/inverter and an isolated DC/DC converter. This two-stage approach optimizes overall system efficiency, power density and also provides easy ground fault protection as well as high grid interference immunity. The intermediate voltage can be variable to track the battery voltage, allowing the isolated DC/DC converter to operate

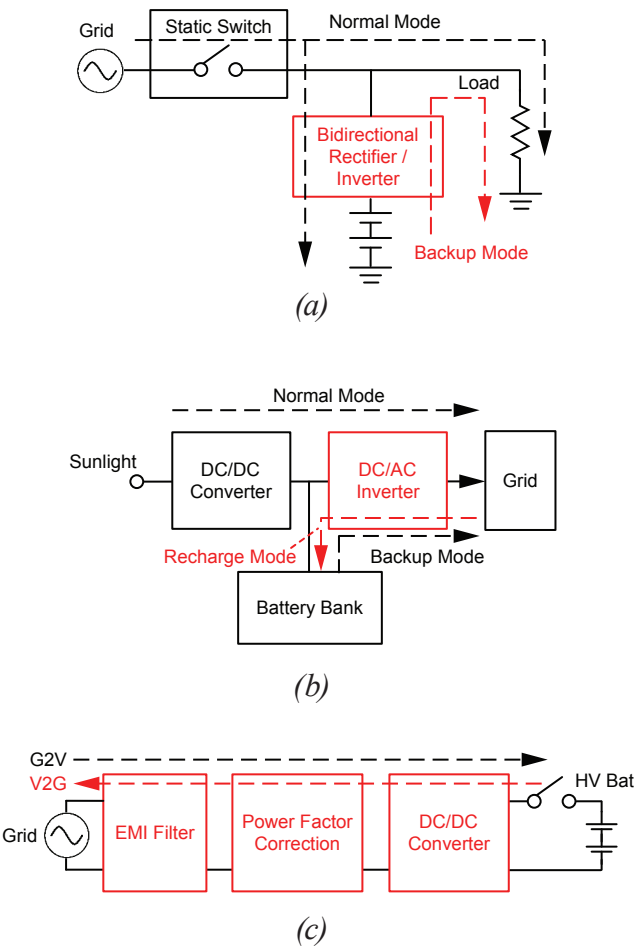

Figure 1 – Example system block diagram of: (a) uninterruptible power supply, (b) energy storage system and (c) HEV/EV onboard charger.

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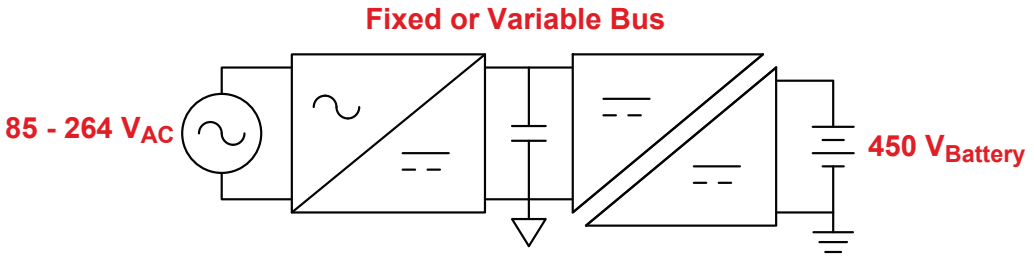


Figure 2 – An EV onboard charger system block diagram.

around the optimal efficiency point. The battery voltage level is generally high, up to 450 V_{DC} in this case, in order to decrease the conduction losses in the system for higher efficiency. Moreover, wide bandgap switching devices, such as silicon carbide (SiC) MOSFET and gallium nitride (GaN) FET, are preferred choices in OBC systems. The wide bandgap power switches have lower $R_{DS(ON)}$, lower reverse recovery charge (Q_{rr}) and lower parasitic capacitance than regular silicon MOSFETs, hence, the overall system efficiency can be further improved. The control scheme is complicated by the control and communication for bidirectional energy flow; therefore, a digital controller is implemented as the controller in a bidirectional power supply.

In this paper, we focus on the discussion of designing a two-stage high-power bidirectional AC/DC power supply using SiC MOSFETs. In Section II, various suitable topologies to be used in the rectifier/inverter stage and isolated DC/DC stage are discussed. In Section III, we focus on the detailed explanation of why wide bandgap devices, like SiC MOSFETs, are selected here as well as SiC MOSFET gate driver selection criteria. In Section IV, the controller selection criteria for this high-power density bidirectional power supply are addressed.

A totem-pole bridgeless PFC (TTPL bridgeless PFC) and a capacitor-inductor-inductor-inductor-capacitor series resonant dual active bridge converter (CLLLC-SRes-DAB) are selected as the first and the second stages of a 6.6 kW OBC reference design, respectively. Design considerations when using these topologies are addressed in Section V. Finally, experimental results are shown in Section VI. The TTPL bridgeless PFC achieves 98.9% peak efficiency while the CLLLC-SRes-DAB achieves 98% peak efficiency in this 6.6 kW design.

II. Topology Selections

This section focuses on topology selections of bidirectional AC/DC power supplies that consist of a single phase AC grid and battery. Due to the limited length of this paper, options on topology choices of bidirectional AC/DC power supplies for three-phase AC grid systems [4-6] are not discussed here. Since a two-stage approach (AC/DC rectifier/inverter + isolated DC/DC converter) is the trend in high-power bidirectional AC/DC power supplies, this section discusses topology selections for a single phase AC/DC rectifier/inverter and an isolated DC/DC converter, respectively.

A. Single Phase Rectifiers/Inverters

As the bidirectional AC/DC power supply is intended to transfer high-power, we need to ensure the power factor in the AC/DC rectifier stage is high enough to minimize the reactive power generated from power plants. Also, we need to generate a high voltage bus (intermediate voltage) to lower the conduction losses in both the AC/DC rectifier/inverter and the isolated DC/DC converter. Therefore, a boost type bidirectional AC/DC rectifier with an active power factor correction (PFC) function is needed. Three commonly used bidirectional PFC topologies – totem-pole bridgeless PFC (TTPL bridgeless PFC) and two bridgeless PFCs with bidirectional switches (AC-switch bridgeless PFC) – are shown in Figure 3.

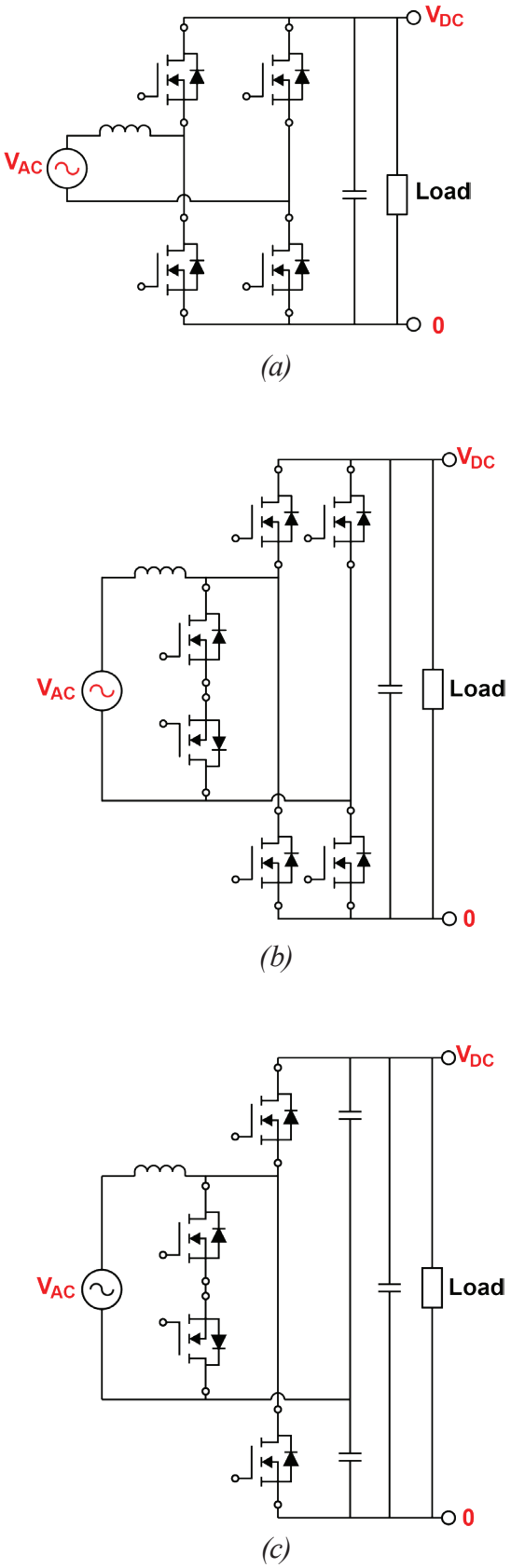


Figure 3 – Commonly used bidirectional AC/DC rectifier with active PFC: (a) totem-pole bridgeless PFC and (b) and (c) bridgeless PFC with bidirectional switches.

In their original rectifier form [7], diodes are used as part of the power switches. In order to allow bidirectional current flow, these diodes need to be replaced by power switches that allow bidirectional current flow, MOSFETs for example. The operation of these boost type AC/DC rectifier topologies can be analogous to a simple boost converter in rectifier mode or a simple buck converter in inverter mode. Taking the TTPL bridgeless PFC illustrated in Figure 3 as an example, the current flow paths are the same as a common ground boost converter in rectifier mode and a common ground buck converter in inverter mode during the AC positive half cycle. During the AC negative half cycle, the TTPL bridgeless PFC current flow paths are the same as a common source boost converter in rectifier mode and a common source buck converter in inverter mode, as shown in Figure 4.

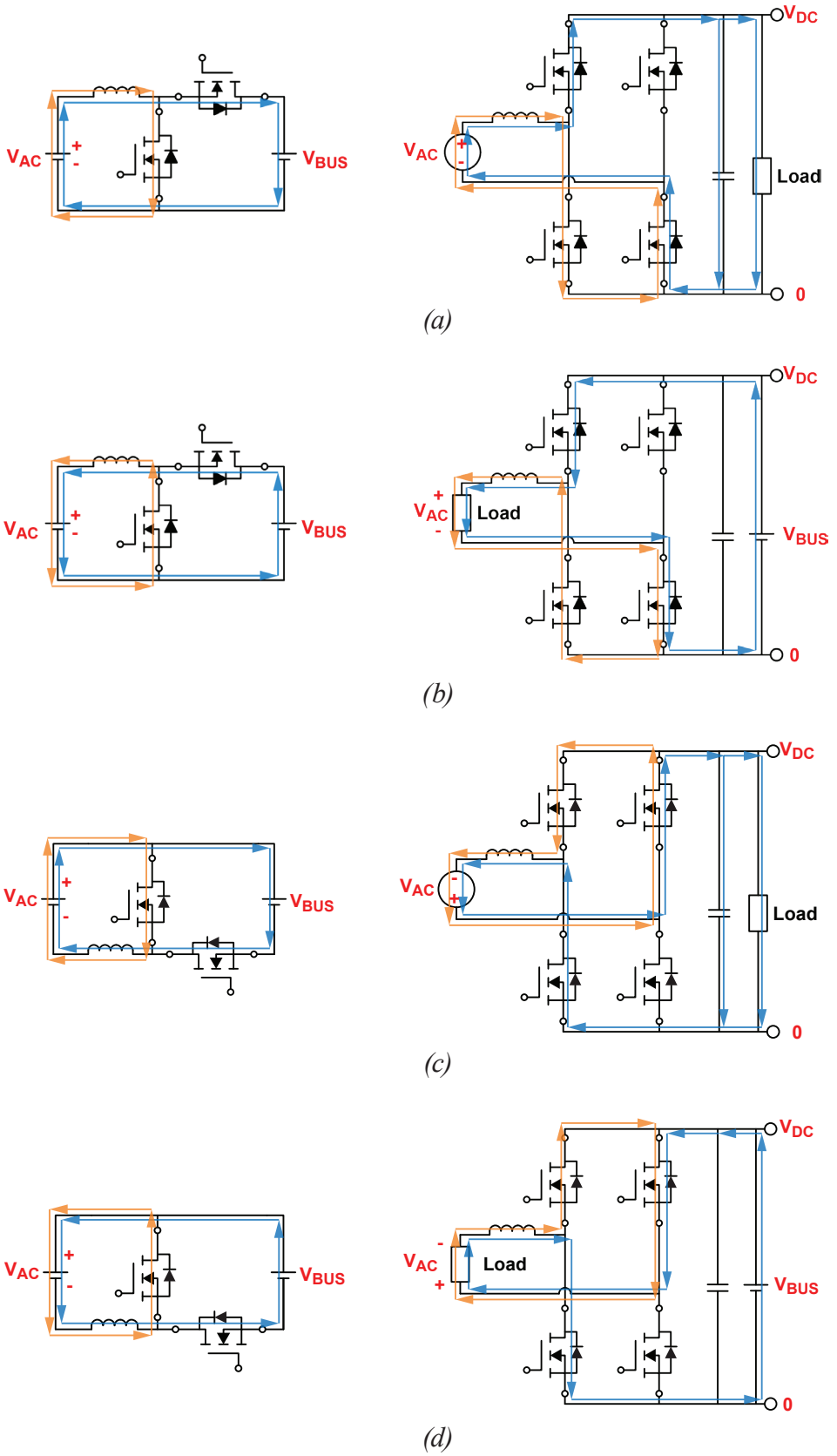
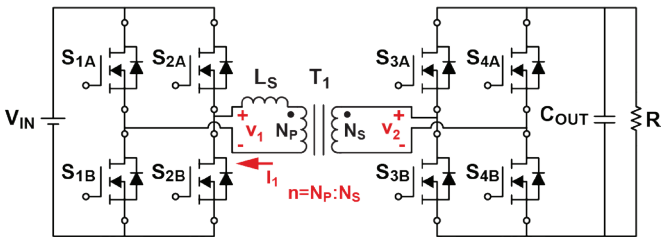


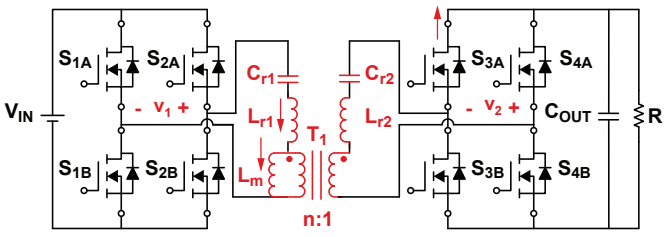
Figure 4 – Buck/boost converter and TTPL bridgeless PFC current flows in: (a) boost/rectifier mode and positive AC cycle, (b) buck/inverter mode and positive AC cycle, (c) boost/rectifier mode and negative AC cycle and (d) buck/inverter mode and negative AC cycle.

B. Bidirectional Isolated DC/DC Converters

There are many topology choices for bidirectional isolated DC/DC converters, including a dual-flyback converter, a dual-Cuk converter, a forward-flyback converter and dual active bridge (DAB) converters [8]. However, the power level of most of these converters is limited because of snubber losses and the transformer/coupled inductor size. In high-power applications, we must select the topologies without the need of a snubber circuit and coupled inductor (i.e., large energy stored in the isolation magnetic) for better converter efficiency. Among all the commonly used bidirectional isolated DC/DC converter topologies, the DAB converter is the only topology that circulates the energy in the transformer leakage or magnetizing inductances in both energy flow directions without the need of a snubber circuit. Moreover, DAB converters are capable of achieving soft-switching for lower switching losses that enable high frequency operations for high-power density. DAB converters can be divided into two categories, phase-shift DAB (PS-DAB) and resonant DAB, as illustrated in Figure 5. Key features of phase-shift and resonant DABs are described below.



(a)



(b)

Figure 5 – DAB converters: (a) phase shift DAB and (b) resonant DAB.

i. Phase-shift dual active bridge converter

The fundamental PS-DAB has a 50% duty cycle on both the primary (left-hand side) and secondary (right-hand side) bridges while a phase difference is implemented between the two bridges for energy flow control. Key waveforms of a PS-DAB are shown in Figure 6. Square waves v_1 and v_2 are generated by primary and secondary bridges and applied to two ends of the transformer.

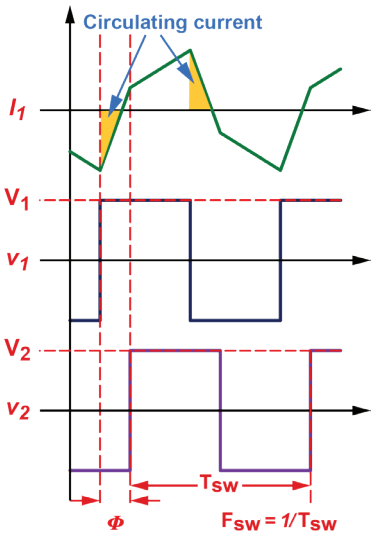


Figure 6 – PS-DAB key waveforms.

As the voltage difference is applied on the series inductor, L_S, the energy flow direction can be controlled by the phase difference (ϕ) of v_1 and v_2. The power flow equation of PS-DAB is shown in Equation (1) below [9]

$$P_{12} = \frac{V_1 V_2}{2nL_S F_{SW}} \frac{\phi}{\pi}\left(1 - \left|\frac{\phi}{\pi}\right|\right) \quad (1)$$

where V_1 and V_2 are the peak voltage of v_1 and v_2, F_{SW} is the converter switching frequency, $n=N_P:N_S$ is the transformer turns ratio and ϕ ranges from $-\pi$ to π. PS-DAB relies on the energy stored in L_S to charge/discharge the output capacitance on the input full bridge FETs to achieve a soft turn-on switching or zero voltage switching (ZVS). As the current and energy in L_S is determined by the load conditions, it is possible for a PS-DAB to lose ZVS when the load is light. Depending on the application, it might be necessary to add an external series inductor in addition to the

transformer leakage inductance to extend the ZVS range over a wider range of loads. However, large L_s implies the converter efficiency at heavy load will be reduced. Therefore, a tradeoff between ZVS range and converter efficiency must be made in a PS-DAB design.

There will be a larger amount of circulating energy in the 1ϕ controlled PS-DAB. In the highlighted regions in Figure 6, the L_S current flow direction is different from the polarity of $(v_1\text{-}v_2)$. That is, L_S energy is circulating in these highlighted regions and will result in high conduction loss. To overcome the high conduction loss disadvantage of the 1ϕ controlled PS-DAB, multiple-phase control [8] can be implemented to a PS-DAB. Not only is phase-shift implemented between the primary and secondary bridges, but it is also implemented between the half bridges of both the primary and secondary bridges. However, the multiple-phase shifted scheme increases the control complexity.

ii. Resonant dual active bridge converter

Unlike PS-DAB, a resonant DAB operates at a variable switching frequency. As illustrated in Figure 7, the input full bridge generates a square wave that feeds into the resonant tank. By varying the switching frequency, the resonant tank would respond with different voltage levels, hence different output voltages. Figures 5(b) and 7 show one type of resonant DAB, which is CLLLC-SRes-DAB. Different resonant tanks are also possible in a resonant DAB resulting in different responses. It is important to make sure the resonant DAB is operated at a point where the gain curve has negative slope because a negative slope voltage gain curve ensures inductive input impedance, a necessary condition for input switches to achieve ZVS [10, 11]. Like the CLLLC-SRes-DAB, the most commonly used resonant DABs are series resonant DABs. A series resonant DAB relies on the energy stored in the transformer magnetizing inductance, L_m, to achieve ZVS. Ideally, the minimum current flowing through L_m during the dead time is independent of load conditions. A series resonant DAB can achieve ZVS over the entire load range without trading off efficiency like the PS-DAB must.

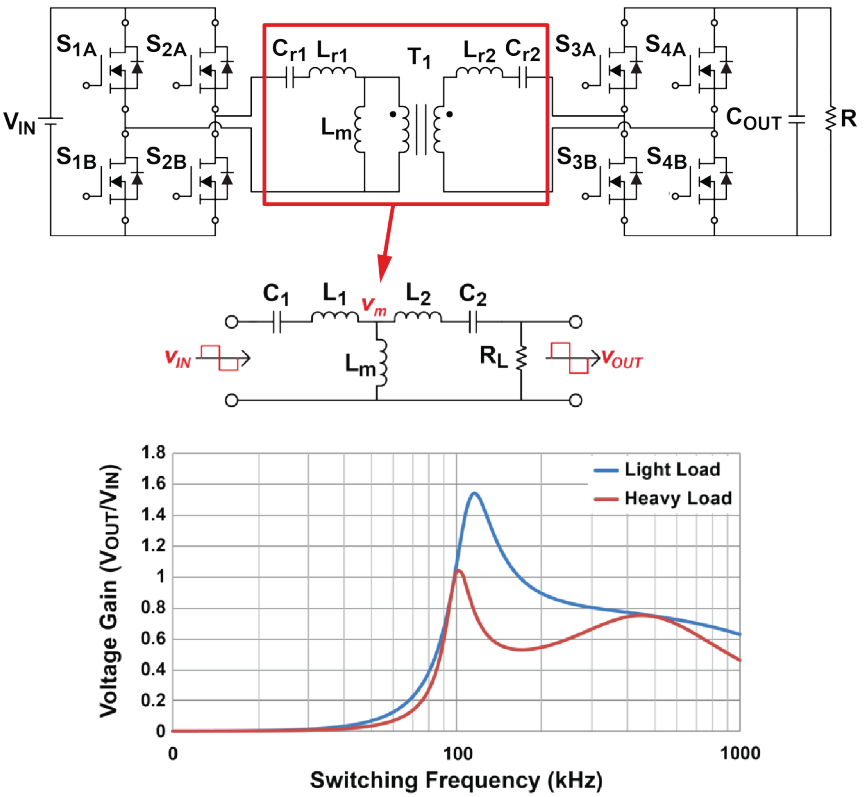


Figure 7 – Resonant DAB circuit diagram, resonant tank and voltage gain.

	Phase Shift DAB	CLLLC Resonant DAB
Turn-on loss	**Low to medium** – large L_s ⇒ wide ZVS	**Low** – small L_m ⇒ ZVS over wide F_{SW}
Turn-off loss	**High** – FET turn-off at high inductor current on two sides of bridges	**Low** – can achieve zero current switching on rectifier bridge FETs
Conduction loss	High – w/ 1Φ control Low – w/ multiple Φ control	**High** – due to small L_m
Operation range	**Wide – okay for fixed bus voltage***	**Narrow – better with variable bus***
Converter control	**Simple** – w/ 1Φ control **Complex** – w/ multiple Φ control	**Simple** – frequency variation
SR control	**No need for SR current sensing**	**Requires current sensing for SR control**
Transient response	**Fast** – response w/ Φ	**Slow** – response w/ switching frequency

* *Consider charger applications*

Table 1 – Dual active bridge comparisons.

Table 1 compares some key features of the PS-DAB and CLLLC-SRes-DAB. A series resonant DAB, including CLLLC-SRes-DAB, can easily achieve a wider ZVS range over a load than a PS-DAB for lower turn-on switching losses. Also, a series resonant DAB has lower turn-off switching losses on the output full bridge as the turn-off current stress of a series resonant DAB is generally lower than that of a PS-DAB with the same input/output specifications. Because the series resonant DAB and PS-DAB rely on different circuit components to achieve soft switching, the conduction loss on these two types of DAB can be very different at different load conditions.

With the same specification, a series resonant DAB is expected to have a much lower L_m than a PS-DAB, as L_m in a series resonant DAB is used to achieve ZVS. Hence, a series resonant DAB is expected to have a higher conduction loss from the L_m circulating current than a PS-DAB.

On the other hand, a PS-DAB needs to have a large L_S for a wide ZVS range over load. And the large L_S creates large circulating currents, increasing conduction loss. Overall, the conduction loss of these two types of DAB is expected to be higher than other hard switching PWM converters because of the circulating energy.

A series resonant DAB has optimized efficiency only when the switching frequency is close to the series resonant frequency. It is better for a series resonant DAB to operate with a narrow input/output voltage range while PS-DAB doesn't have such a limitation.

Control for both the PS-DAB and series resonant DAB can be simple, 1ϕ control for PS-DAB and variable frequency control for series resonant DAB. It is notable that synchronous rectifier (SR) control is required in a series resonant DAB to avoid output energy backflow, while it is not necessary in a PS-DAB. Because of the resonant characteristic of the series resonant DAB, SR sensing becomes a challenge in series resonant DAB design.

Besides converter losses, operation range, converter control and SR control, one important difference between these two types of DAB is the transient response. As power regulation in a PS-DAB is controlled by the simple Equation (1), theoretically, it is possible to adjust the phase angle to a desired value in one switching cycle after the transient (either input or output) is detected.

In comparison, the voltage gain of a series resonant DAB is generally a complex equation. Therefore, it is difficult for a controller (even a digital controller) to solve the voltage gain equation (if available) after a transient is detected for a desired switching frequency. That is, a series resonant DAB always responds to the transient with incremental or decremental frequency changes. Response to a transient event by a duty cycle change or phase angle (PS-DAB) is expected to be much faster than a frequency change (series resonant DAB). Hence, a series resonant DAB is expected to take more switching cycles to reach steady state than a PS-DAB during the transient.

III. Power Switch and Driver Selections

Wide band-gap FETs have lower specific $R_{DS(ON)}$ and faster switching speed than silicon MOSFETs [12, 13] which enables higher efficiency and more compact power converters. SiC wide band-gap MOSFETs are specifically suitable for high voltage applications. This section compares SiC MOSFETs with silicon MOSFETs and discusses the advantages of SiC MOSFETs as well as the driver circuit design considerations for SiC MOSFETs.

A. Silicon-Carbide vs. Silicon MOSFETs

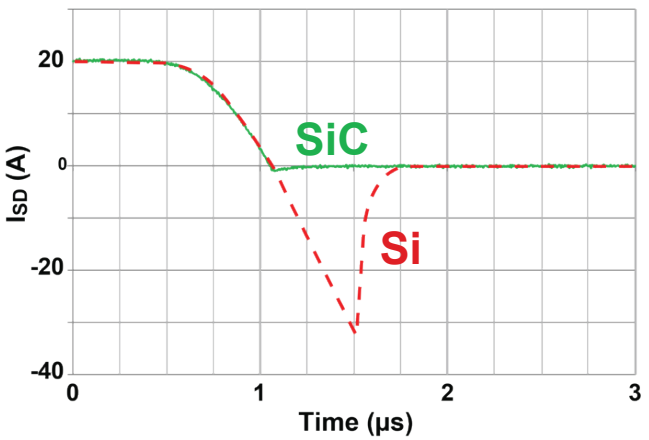


Figure 8 – SiC vs silicon MOSFET reverse recovery.

A silicon MOSFET with a 650 V voltage rating is widely used for telecom and consumer charger applications, but due to its large Q_{rr}, it has rarely been used for high-power full bridge rectifier or inverter applications. Figure 8 shows an example of a reverse recovery comparison between a silicon MOSFET and SiC MOSFET with similar $R_{DS(ON)}$.

Assuming silicon MOSFETs are applied as power switches in Figure 9, the top MOSFET body diode will generate a large reverse recovery current when turning on the bottom MOSFET, resulting in high switching losses in the bottom MOSFET. During the negative half cycle of the AC input voltage, the reverse recovery current from the bottom MOSFET will generate large

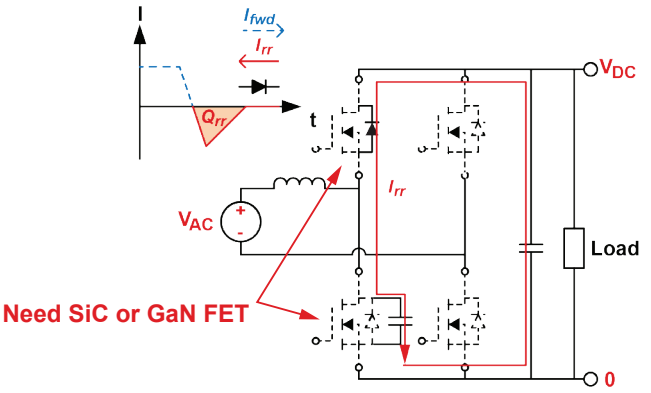


Figure 9 – Hard switching reverse recovery for AC/DC.

switching losses in the top MOSFET. In the worst case, the MOSFETs could be damaged due to the large reverse recovery current. Therefore, it is critical to select low or no Q_{rr} MOSFETs for topologies requiring current conduction through MOSFET body diodes. This is the reason why 650 V silicon MOSFETs are not used for hard switching rectifiers or inverters. SiC MOSFETs or GaN FETs, which have low Q_{rr} or even no Q_{rr}, can be used for such applications directly.

For soft switching DC/DC applications, the MOSFET has zero voltage turn-on during normal operation. Since there is no hard turn-on or reverse recovery, silicon MOSFETs can be used safely under steady state operation. However, soft switching is achieved by the resonant process between an inductor and the MOSFET output capacitance (C_{OSS}) during the dead time. More inductor energy and/or longer dead time is needed if the C_{OSS} is large. The minimum dead time is calculated as in Equation (2) below

$$t_{DT} = \frac{2\int_0^{V_{DS}} C_{OSS}(V_{DS})d(V_{DS})}{I_L} = \frac{2 \bullet Q_{OSS}}{I_L} \qquad (2)$$

where V_{DS} is the MOSFET drain to source voltage, I_L is inductor current (assumed to be a constant) and Q_{OSS} is the output capacitor charge of the MOSFET. The C_{OSS} and Q_{OSS} of a silicon MOSFET and a SiC MOSFET with similar $R_{DS(ON)}$ are compared in Figure 10. As shown in the figure, the silicon MOSFET has much higher C_{OSS}. Since C_{OSS} is nonlinear, the Q_{OSS} is used to calculate the required current and time to discharge

C_{OSS}. As shown in Figure 10, the silicon MOSFET Q_{OSS} is almost 6 times that of the SiC MOSFET Q_{OSS} at 400 V. Because of this, the dead time has to be selected much longer for the silicon MOSFET based soft switching DC/DC circuits. Less dead time is required with a soft-switching converter using SiC MOSFETs and implies the converter has less "duty cycle loss", lower circulating current, less conduction loss and allows higher switching frequency operation.

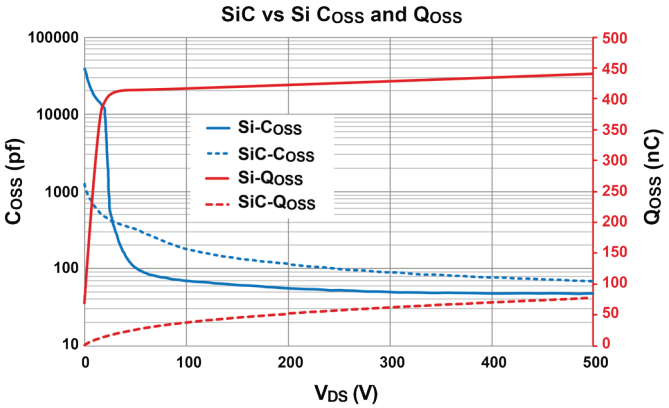


Figure 10 – SiC MOSFET vs silicon MOSFET C_{OSS} and Q_{OSS}.

Other than the low reverse recovery and small output capacitance, SiC MOSFETs also have lower specific $R_{DS(ON)}$, especially for voltage ratings higher than 650 V. Therefore, SiC MOSFETs are a better choice than silicon MOSFETs for the application of high voltage, high-power converters, rectifiers or inverters.

B. Silicon-Carbide MOSFET Gate Driver Selections

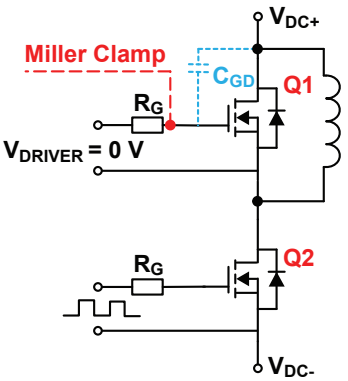


Figure 11 – SiC MOSFET half bridge leg under hard switching.

Since SiC MOSFETs can be switched much faster than silicon MOSFETs, some additional considerations are needed for the gate driver design. First of all, the high dv/dt switching can generate significant crosstalk voltage on the MOSFET gate. A half bridge leg circuit under a double pulse test is shown in Figure 11. Q_1 V_{DS} will rise and has positive dV_{DS}/dt when turning on Q_2, the dV_{DS}/dt induced current will pass through Q_1 C_{GD} and then R_G, which can pull up the SiC MOSFET gate voltage. The induced voltage can be calculated using Equation (3) if the C_{GS} stored charge change is ignored.

$$V_{GS} = R_G \bullet C_{GD} \bullet \frac{dV_{DS}}{dt} \tag{3}$$

Figure 12 gives example waveforms of dv/dt induced cross talk. The Q_1 V_{GS} voltage (circled in red) has about a 6 V overshoot during the Q_1 turn-on transient. On the other hand, a SiC MOSFET typically has low gate threshold voltage, which can be even lower than 1 V at 150°C. When the cross talk generated gate voltage is higher than the gate threshold voltage, shoot through, or at least partial shoot through, can happen for the bridge leg. In order to avoid such shoot through situations, negative gate turn-off voltage is needed to keep the MOSFET in the fully OFF state. Another way to limit this induced V_{GS} overshoot voltage is using a miller clamp circuit, which provides a separate miller clamp path (the path with red dash in Figure 11, as an example) to pull the gate directly to zero voltage or negative voltage.

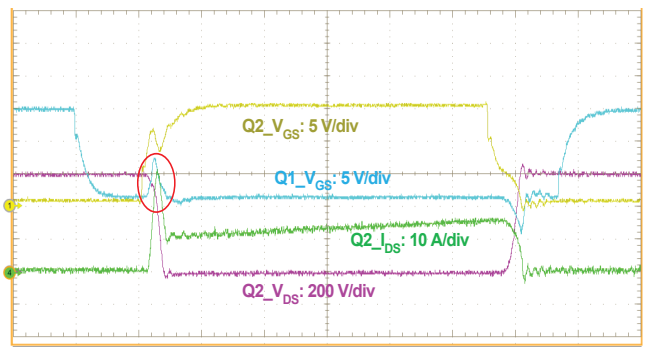


Figure 12 – SiC MOSFET hard-switching gate voltage cross talk.

Common mode transient immunity (CMTI) is another key parameter for SiC MOSFET driver selection. In a half bridge leg (Figure 13), the switching node high dv/dt transient will stress the isolation barrier of the top MOSFET gate driver. If the gate driver doesn't have robust CMTI, parasitic noise current induced by dv/dt could cause a malfunction of the driver including missing pulses, excessive propagation delay, high or low error or output latch.

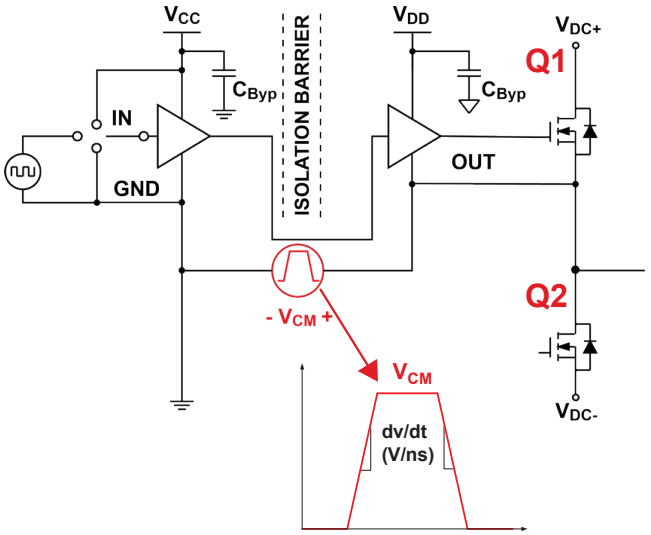


Figure 13 – High common mode voltage dv/dt stress on top gate driver isolation barrier.

Figure 14 is an example waveform which shows a driver malfunction with common mode voltage transient stress. When the driver input logic signal (yellow curve) goes high, the driver output voltage (blue curve) fails to follow the input logic signal.

Isolation is a safety requirement for the driver, which is very important for the safe operation of the power converter system when driving power switches referenced to a "hot" ground from a controller referenced to a "cold" or safety ground. There are three main types of isolation technologies: optical, magnetic and capacitive, which utilizes epoxy, polyimide or silicon-dioxide (SiO_2) as the insulation material. SiO_2 offers the highest dielectric strength in the industry, unlike polyimide and other polymer based insulators. The reliability of a SiO_2-insulated capacitor does not degrade with exposure to moisture, which gives capacitive isolation the highest lifetime in the industry, achieving more than 40 years with 1.5 kV_{RMS} isolation voltage. Optical isolation has LED degradation (current transfer ratio degradation) associated with temperature and age. Magnetic isolation has lower working voltages while capacitive isolation offers the highest working voltage.

One advantage for optical isolation is its lower cost than the other two, but it has a long propagation delay and wide variation as well as high quiescent current which are not desirable for high frequency converter drivers. It is also notable that power increases linearly with the data-rate for magnetic isolation while it is not the case for capacitive isolation. The comparison of the three types of isolation technologies is summarized in Table 2.

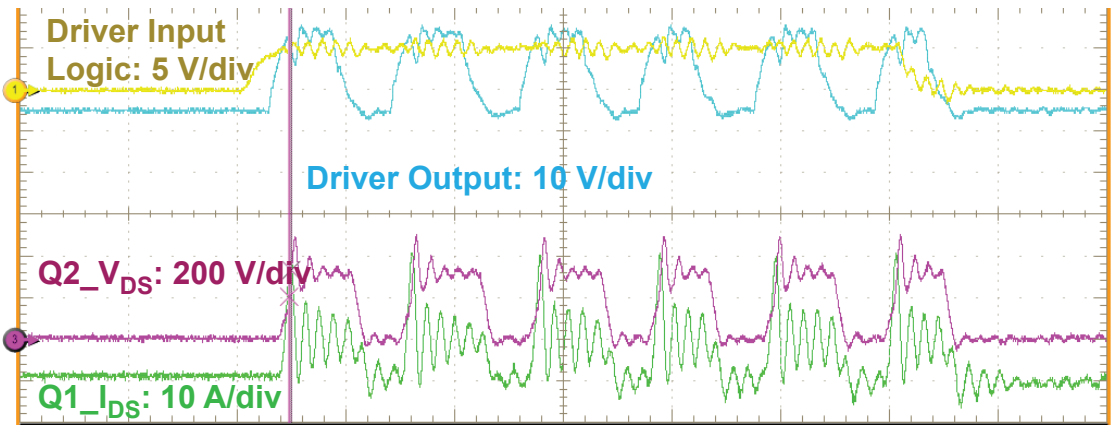


Figure 14 – Example waveform of CMTI failure.

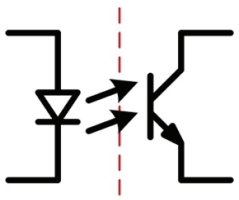
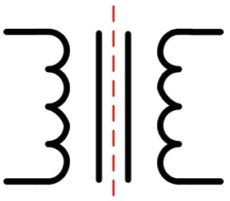
	Optical	Magnetic	Capacitive
			
Insulator material (dielectric strength)	**Epoxies (~20 V_{RMS}/µm)**	**Polyimide (~300 V_{RMS}/µm)**	**SiO_2 (~500 V_{RMS}/µm)**
Reliability	**Low**	**Medium**	**High**
Robustness	**Low**	**Low**	**High**
Other characteristics	**Low cost Long propagation delay Wide variation High quiescent current**	**Power increases linearly with data-rate High EMI**	**Power doesn't scale with data-rate Low EMI**

Table 2 – Comparison of isolation technologies.

IV. Digital Power Design Considerations

In bidirectional power flow applications, the variable being controlled and the control structure need to change for different operation use cases. Take the controls for bidirectional OBC in Figure 15 as an example. The AC/DC stage controls the bus voltage and the DC/DC stage controls the output voltage or current in charging mode. Whereas in the discharging mode, the DC/DC stage controls the bus voltage and the AC/DC stage feeds power into the AC load by controlling the AC current (grid tie) or AC voltage (islanding). Since mode changing might require external communications, a digital controller is the optimal choice for such an application, as making these decisions is easily implemented as part of the firmware.

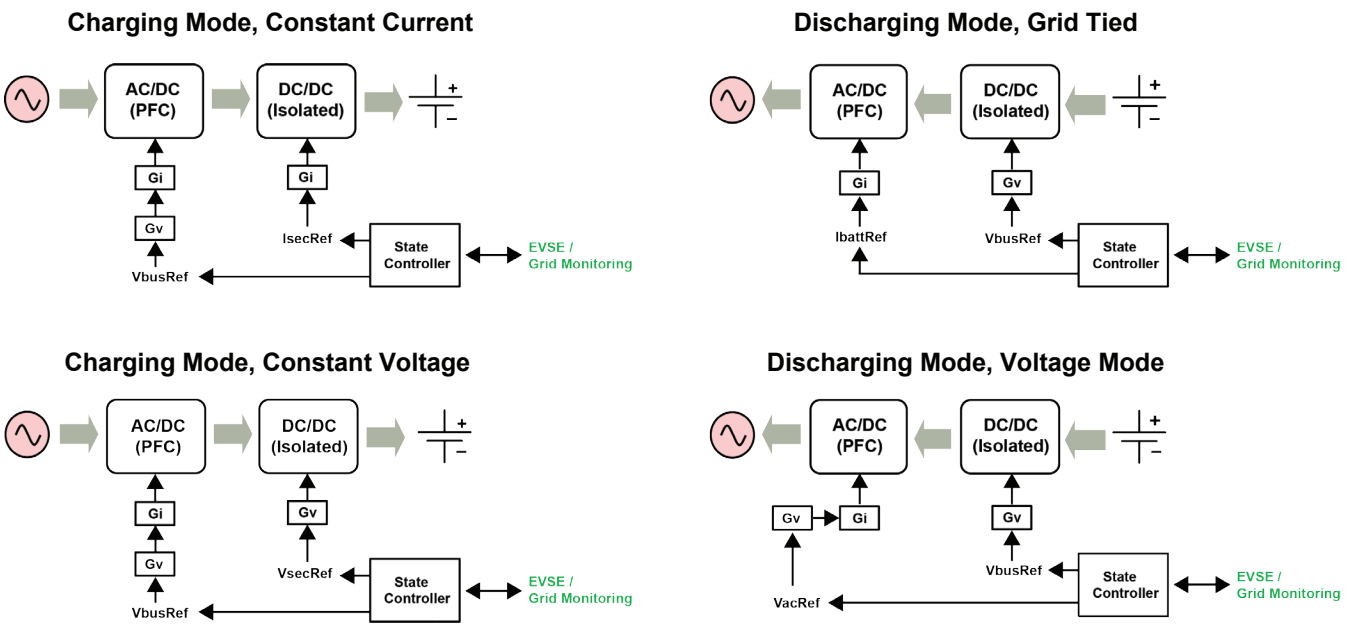


Figure 15 – Control block diagrams of an onboard charger under different modes of operation.

The selection of the digital controller must be done with several factors taken into consideration, such as the pulse width modulator (PWM) capability, integrated analog to digital converter (ADC) and CPU performance in control applications. The PWM is a critical component of the power supply. With the advent of higher switching frequencies, more precision is needed to avoid limit cycles from the control. This is achieved using precision extension features as the controller frequency itself might not be increased due to power consumption concerns. With these precision extenders, it is important to note that not only is high resolution duty cycle needed but high resolution dead time and phase-shift are also necessary. Furthermore, the flexibility of the PWM peripheral, such as configuring up-count, down-count mode and ability to add blanking windows to avoid noise, must be considered to avoid additional logic elements outside of the controller chip.

Integrated analog functions, such as the ADC in the digital controller, play an important role in the closed loop performance. As the voltages increase, the sensing circuitry needs to be designed to accommodate the sense range and any overshoot voltage. For example, select a bus voltage with a 600 V range. The digital controller's integrated ADC will then convert it into bits; the number of bits the ADC converts this data into is referred to as the resolution of the ADC. With a 12 bit ADC, due to quantization, the step is 0.14 V, which will present as error in the system. This error is then further increased by the fact that most ADCs will have additional errors due to non-linearities. The effective number of bits (ENOB) is used to present the value of these additional errors. While selecting the controller, the user must evaluate the ENOB for the ADC integrated with the digital controller. Typically, 11 ENOB is necessary to meet system performance in these applications.

For implementing protection integrated comparator sub-systems, which include comparators and digital to analog converters (DACs) for reference generation on the microcontroller itself, the design must reduce the needed external components, save space and eliminate extra pins needed to interface with the controller, as shown in Figure 16. Additionally, programmable amplifiers are available in the microcontroller to integrate most of the active signal chain from the non-isolated current sensing and protection subsystem. In bidirectional converters, since power can flow in both directions, dual comparators are needed which can be configured to trip in the event of power flow in the reverse direction of what is intended. Since multiple trip sources exist in systems, such as overcurrent for the tank and overvoltage for the battery, a cross bar structure (X-bar), is employed to bring these trips together in a structured manner to the PWM for appropriate action.

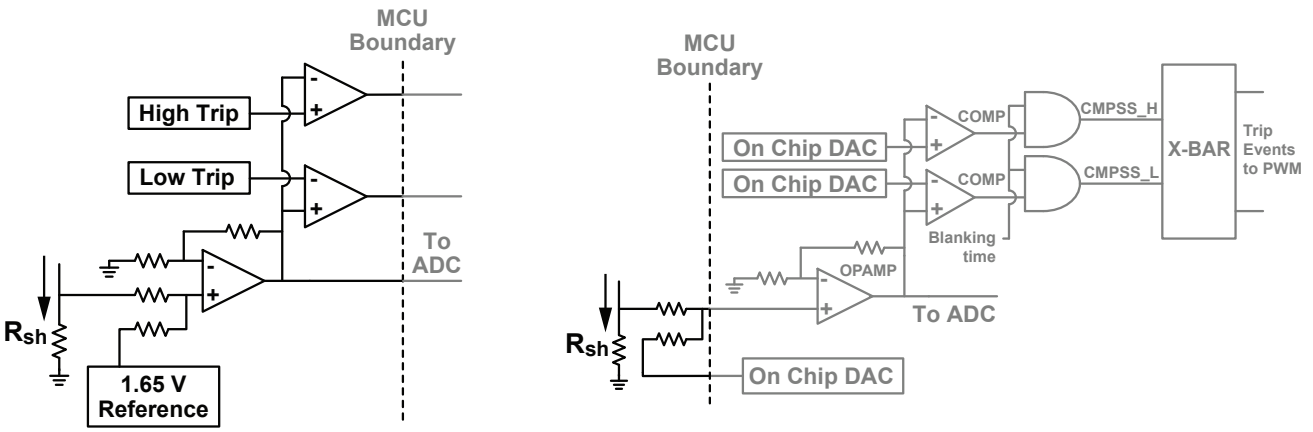


Figure 16 – Protection circuitry for high low trips in bidirectional converter using external components vs. integrated analog on digital controllers.

Additionally, as most chargers include an AC/DC rectifier stage and isolated DC/DC converter stage, the control method of each stage will need to be decided. With the advent of high performance isolation sensing products and the higher computational power available on the digital controller, combining control on a single controller can offer reduction of the total system cost and size. This choice needs to consider the number of PWMs, ADC channels and computational power required for control of each stage.

V. Design Example – Bidirectional Onboard Charger

Target Specifications	
Input	85 V_{AC} to 265 V_{AC}, 50/60 Hz, less than 3% iTHD
Output	250 V_{DC} to 450 V_{DC}, 6.6 kW_{max} at 230 V_{AC} input
Regulation	Less than 5% ripple for the battery current and voltage
Peak Efficiency	>96.5% (>98.5% at PFC stage and >98% at DC/DC stage)
Power Density	>60 W/in^3

Table 3 – Target specifications of a high-power bidirectional AC/DC rectifier.

An OBC specification, shown in Table 3, is used as the target specification for the high-power bidirectional AC/DC power supply design example. A single phase AC voltage is applied to charge a 400 V_{DC} battery with a battery voltage range from 250 V_{DC} to 450 V_{DC}. The target charging profile is shown in Figure 17. When the battery voltage is low, it is charged with a 20 A constant current. Once the battery voltage reaches 330 V_{DC}, it is charged with a 6.6 kW constant power. When the battery voltage reaches 420 V_{DC}, the charger enters constant voltage regulation. This design is aimed at achieving high converter efficiency (>96.5%) and high-power density (>60 W/in^3) with low thermal dissipation and light weight.

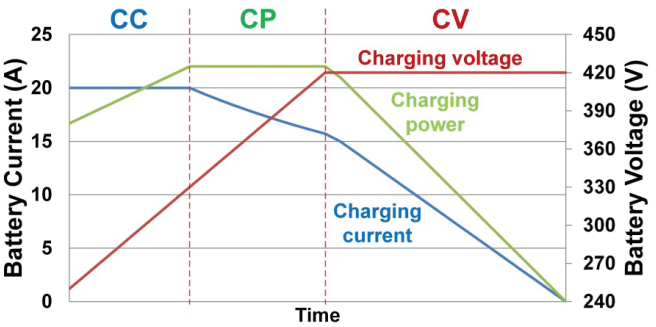


Figure 17 – Target charging profile for the 6.6 kW onboard charger design.

As shown in Figure 18, an interleaved TTPL bridgeless PFC and CLLLC-SRes-DAB are selected for the AC/DC rectifier stage and the isolated DC/DC stage, respectively. SiC MOSFETs are selected for the power switches on both stages to boost converter efficiency and a digital controller is selected to handle the complicated bidirectional control and communication needs. A capacitive based isolated driver is selected for its high reliability and high robustness in this high-power density design. In order to optimize the isolated DC/DC stage efficiency, the PFC output voltage adaptively follows the battery voltage in this design. As a design example of TTPL bridgeless PFC has been previously addressed in [14], this section will focus more on the isolated DC/DC stage side.

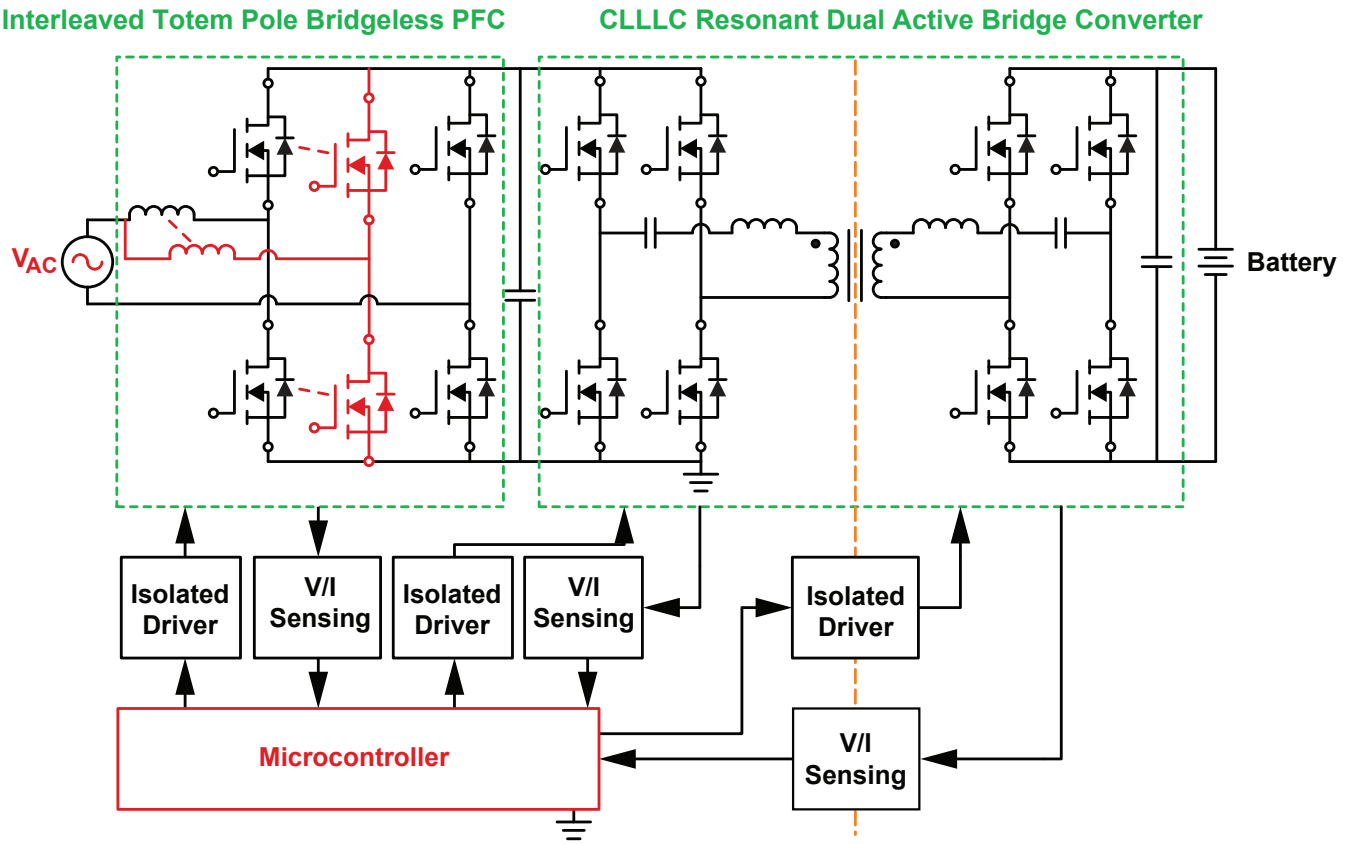


Figure 18 – Power topology and control architecture selections for the 6.6 kW onboard charger design.

A. Interleaved Totem-Pole Bridgeless PFC

Using an interleaved boost PFC can reduce the current ripple on both ends of the converter and the component stress on each power stage device. A power loss comparison is shown in Table 4 for a totem-pole bridgeless PFC with a different number of phases.

V_{DC} (V)	Phases	Freq (kHz)	P_{con} (W) /device	P_{SW} (W) /device	P_d(W) Total
400	2	150	9.2	4.6	55.4
	3	100	4.2	2.5	40.2
	4	75	2.4	1.8	33.6
500	2	150	9.2	7.5	66.8
	3	100	4.2	4.05	49.5
	4	75	2.4	3.0	43.2
600	2	150	9.2	10.5	78
	3	100	4.2	5.8	60
	4	75	2.4	4.2	52.8

Table 4 – TTPL bridgeless PFC loss comparison with different number of phases.

The switching frequency changes with the different number of phases to keep the same 300 kHz inductor current ripple frequency. It is notable that when the phase number increases, the power dissipation decreases. However, the bill of material (BOM) cost also increases along with the number of phases. Therefore, three-phase interleaved TTPL bridgeless PFC is selected in this design to have a balance between the efficiency and BOM cost. Although variable bus voltage can help with efficiency optimization on the isolated DC/DC stage, it is notable that when the bus voltage is higher, the power dissipation on the PFC is higher. In this PFC design, the target bus voltage is ranging from 380 V_{DC} to 600 V_{DC}. More design details of this three-phase interleaved TTPL bridgeless PFC can be found in [15, 16].

B. CLLLC Series Resonant Dual Active Bridge Converter

In order to achieve both high-power density and efficiency targets, the CLLLC-SRes-DAB, as shown in Figure 5(b), has to operate at a high switching frequency. Since a series resonant converter has its efficiency optimized around the series resonant frequency, we can set the two series resonant frequencies, F_{r1} and F_{r2}, equal and allow the converter to operate at the series resonant frequency. Notice that

$$F_{r1} = \frac{1}{2\pi\sqrt{L_{r1}C_{r1}}} \qquad F_{r2} = \frac{1}{2\pi\sqrt{L_{r2}C_{r2}}} \tag{4}$$

When $F_{sw} = F_{r1} = F_{r2}$, the series resonance impedance is zero and the input voltage to output voltage relationship becomes the transformer turns ratio, n. We can then select n with a given input and output voltage range by assuming $F_{sw} = F_{r1} = F_{r2}$. n = 1.33 is selected to cover the major battery voltage ranges with a given 380 V_{DC} to 600 V_{DC} bus voltage while relying on frequency variation or burst operation to support an output voltage less than 285 V_{DC}, as shown in Figure 19.

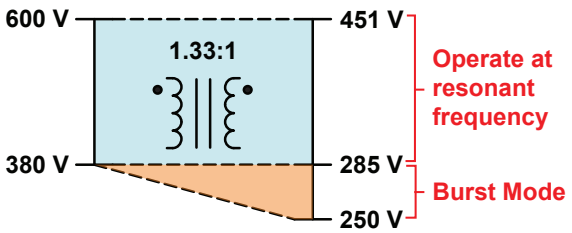


Figure 19 – Transformer turns ratio selection for the 6.6 kW CLLLC-SRes-DAB design.

The next resonant tank parameter to be determined is L_m. The energy stored in L_m during the dead time period is used to charge/discharge the MOSFETs' C_{OSS} to achieve ZVS. Assuming an ideal transformer – no winding capacitance – and ideal switches on the output full bridge, the CLLLC-SRes-DAB dead time circuit model can be illustrated in Figure 20.

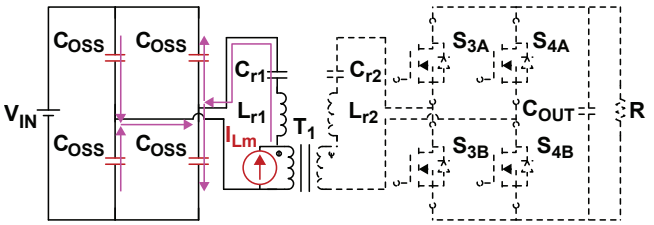


Figure 20 – CLLLC-SRes-DAB dead time circuit model without considering transformer parasitic capacitance and rectifier switches' C_{OSS}.

The magnetizing inductor current during dead time, I_{Lm}, can be assumed as a constant. In order to achieve ZVS on the input full bridge, we must first make sure that the energy stored in L_m is larger than the energy stored in all the C_{OSS}. Hence, the following inequality must be met.

$$\frac{1}{2}L_m I_{Lm}^2 \geq \frac{1}{2}(4C_{OSS})V_{IN}^2 \tag{5}$$

I_{Lm} is the peak magnetizing inductor current and can be calculated using the following equation.

$$I_{Lm} = \frac{nV_{OUT}}{4L_m F_{SW}} \tag{6}$$

Substituting Equation (6) into (5), we can find the maximum allowed L_m for ZVS to be

$$L_{m_{max}} \leq \frac{n^2 V_{OUT}^2}{64 C_{OSS} V_{IN}^2 F_{SW}^2}. \tag{7}$$

However, by using the L_m derived from Equation (7) we won't be able to achieve ZVS with a real transformer because of transformer intra-winding capacitance (C_{TX}) and the C_{OSS} on the output full bridge switches, $C_{OSS(OUT)}$. With the presence of C_{TX} and $C_{OSS(OUT)}$, the L_m current during the dead-time transient can no longer be assumed as a constant. The current on L_m not only flows to the C_{OSS} of the input full bridge, but also needs to flow to C_{TX} in order to change the winding voltage polarity, as shown in Figure 21.

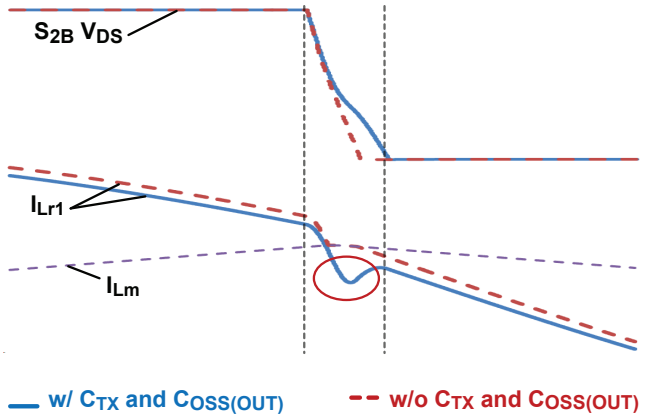


Figure 21 – Switching node voltage and magnetizing current around dead time transient w/ and w/o C_{TX} and $C_{OSS(OUT)}$.

We need to minimize C_{TX} or we will have to use a much smaller L_m value than what is derived from Equation (7) to achieve ZVS. Notice that using a smaller L_m value will result in a higher circulating current and lower converter efficiency. Hence, it is very important to properly design a transformer with C_{TX} minimized in a series resonant DAB. It is suggested to include C_{TX} and C_{OSS} on switches at both ends in a simulation model and verify if ZVS is achieved in the simulation. A rule of thumb for L_m selection is to start with $L_m = 0.5L_{m(max)}$ calculated in Equation (7).

Once L_m is determined, the next step is to determine the inductance ratio of L_m/L_r, as the inductance ratio affects the gain variation range within a given frequency range. L_r is the series inductance where $L_r = L_{r1}$ determines the resonant tank at the primary side and $L_r = L_{r2}$ determines the resonant tank at the secondary side. Defining $L_n = L_m/L_r$ and setting $F_{r1} = F_{r2} = 500$ kHz, the voltage gain variation with different L_n values is illustrated in Figure 22.

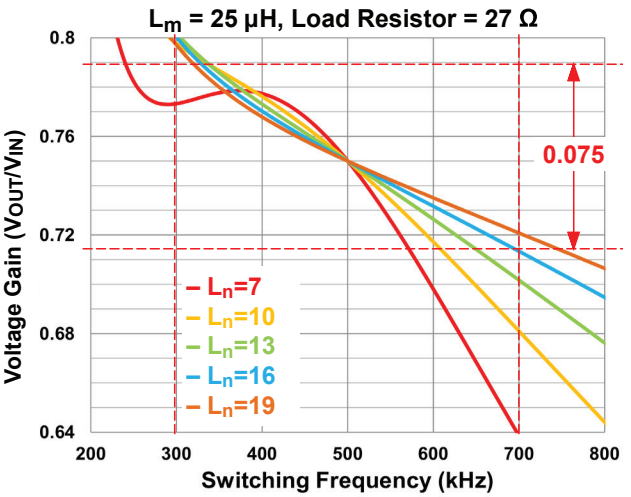


Figure 22 – CLLLC-SRes-DAB voltage gain curves with $F_{r1} = F_{r2} = 500$ kHz.

As can be observed in Figure 22, a smaller L_n results in a larger gain variation within a given switching frequency range, which implies that using a smaller L_n can support wider input or output voltage variations. In order to get smaller L_n, we have to use a smaller L_m and larger L_r. However, a smaller L_m means higher circulating current and a larger L_r implies higher conduction losses and higher fringing flux related losses (if using a ferrite core material). That is, it is better to design an inductor with less turns to minimize losses due to fringing flux than an inductor with more turns. Therefore, a tradeoff between converter efficiency and gain variation range must be made. In this OBC design, we are targeting to achieve less than 5% ripple on the battery current and voltage. To achieve the regulation goal, we can design the L_n using the worst case – to regulate 420 V_{DC} at 6.6 kW output power with a 5% ripple on the PFC output voltage. A 0.075 voltage gain variance is needed to cover the worst case. With $F_{r1} = F_{r2}$ set to 500 kHz to achieve high-power density and given a 300 kHz to 700 kHz switching frequency range, we need $L_n<16$, as can be observed in Figure 22.

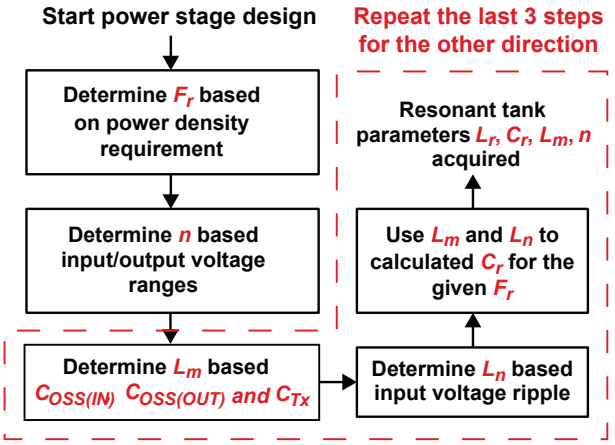


Figure 23 – CLLLC-SRes-DAB design flow chart.

With F_{r1}, F_{r2}, n, L_m and L_n selected, C_{r1} and C_{r2} can be calculated. A CLLLC-SRes-DAB design flow chart is shown in Figure 23. It is notable that we go through the five steps in the flow chart for power flow in one direction and we will need to repeat the last 3 steps in the flow chart for power flow in the other direction. Simulation or calculation results for L_m in the charging direction might be different from the result in the discharging direction. The smaller of the two L_m results must be applied to guarantee ZVS on all switches in both energy flow directions.

As mentioned in Section II, SR sensing and control is a challenge in a series resonant DAB. Figure 24 shows the CLLLC-SRes-DAB key waveforms. The input full bridge MOSFETs have a fixed 50% duty cycle (assuming a negligible dead time) while the duty cycle of the rectifier current is determined by F_{sw}, F_{r1} and load conditions. When $F_{sw} < F_{r1}$, the rectifier current goes to zero before an input switch turns off.

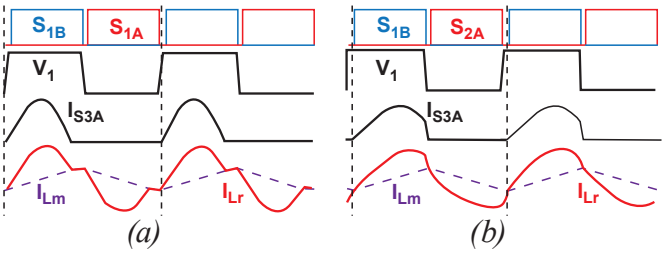


Figure 24 – CLLLC-SRes-DAB modes of operation at a heavy load in charging direction: (a) $F_{sw} < F_{r1}$ and (b) $F_{sw} > F_{r1}$.

Therefore, when a MOSFET is functioning as a rectifier, it must be turned off with less than 50% duty cycle to avoid any rectifier current backflow. Otherwise, the converter efficiency will be reduced by excessive circulating current. The rectifier current conduction time is actually $0.5/F_{r1}$ at a heavy load. So it is possible to limit the SR conduction time to slightly less than $0.5/F_{r1}$ at a heavy load and disable the SR at a lighter load [17]. This open-loop SR control method won't be able to optimize the converter efficiency, however. Other SR sensing and control methods, like MOSFET V_{DS} sensing [18], current transformers and Hall sensors, all have frequency limitations (generally <400 kHz bandwidth or operational frequency) and hence are not suitable for high frequency SRCs. In addition, the MOSFET V_{DS} sensing method requires accurate V_{DS} voltage sensing; therefore, its sensing voltage level is limited. Current transformer size is analogous to its sensing current and could be a power-density killer in high-frequency SRCs.

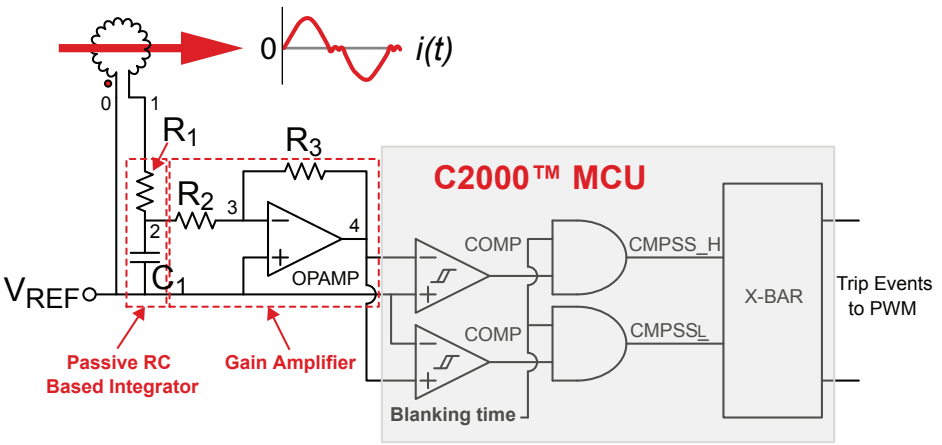


Figure 25 – Rogowski coil based SR sensing and control circuit.

A better SR sensing method is required for this high frequency, high-power density and high voltage CLLLC-SRes-DAB design. A Rogowski coil [19] based SR sensing and control method is proposed in this paper for the CLLLC-SRes-DAB design, as shown in Figure 25. An air core coil, specifically a Rogowski coil, is placed on the transformer winding for current sensing. When a time-varying current flows through the coil, the current-generated magnetic field induces voltage on the coil windings. The induced voltage will have a 90º phase difference when compared to the original time-varying current. Adding an integrator after the Rogowski coil can generate a voltage that is in phase or even leading the original time-varying current. Thus, it is possible to set the zero voltage crossing of the integrator output to be a little bit earlier than the time-varying current zero current crossing to accommodate possible propagation and control delay, and then compare the integrated and amplified voltage signal with the given comparator thresholds. Defining the time-varying current in Figure 25 to be i(t) and assuming that the Rogowski coil is placed vertically on the transformer winding, the Rogowski coil winding output voltage is

$$v_{10}(t) = \frac{-AN\mu_0}{l}\frac{di(t)}{dt} \tag{8}$$

where A is the cross-section area of each turn on the Rogowski coil (assuming that the turns on the Rogowski coil all have the same cross-sectional area), N is the number of turns on the Rogowski coil, l is the circumference of the Rogowski coil and $\mu_0=4\pi\cdot10^{-7}$ H/m is the permeability constant.

Also assuming an ideal operational amplifier is used in the proposed sensing circuit, the voltage relationship between the Rogowski coil output $v_{10}(t)$ and the passive integrator output $v_{20}(t)$ can be found to be

$$\frac{dv_{20}(t)}{dt} + \left(\frac{1}{R_1C_1} + \frac{1}{R_2C_1}\right)v_{20}(t) = \frac{v_{10}(t)}{R_1C_1} \tag{9}$$

It's possible to solve the differential equation in Equation (9) in the form of

$$v_{20}(t) = \frac{1}{I}\int 1\frac{v_{10}(t)}{R_1C_1}\,dt + \frac{a_0}{I} \tag{10}$$

where a_0 is a constant and $I = e^{\left(\frac{1}{R_1C_1}+\frac{1}{R_2C_1}\right)t+const}$.

To better understand how to adjust the phase difference with the passive integrator and amplifier, assume that the time-varying current is purely sinusoidal. This will make both the Rogowski coil output voltage and the integrator output purely sinusoidal. In other words, solving Equations (8) and (9) to get the solution of i(t) with the assumption of $v_{20}(t) = a_1 \sin(\omega t)$, Equation (9) can be rewritten as

$$i(t) = \frac{a_1 l}{AN\mu_0}\sin\left(\omega t + \phi + \frac{\pi}{2}\right) \tag{11}$$

where $\phi = \tan^{-1}\left(\frac{a_1\omega}{a_2}\right) = \tan^{-1}\left[\frac{\omega}{\left(\frac{1}{R_1C_1}+\frac{1}{R_2C_1}\right)}\right]$.

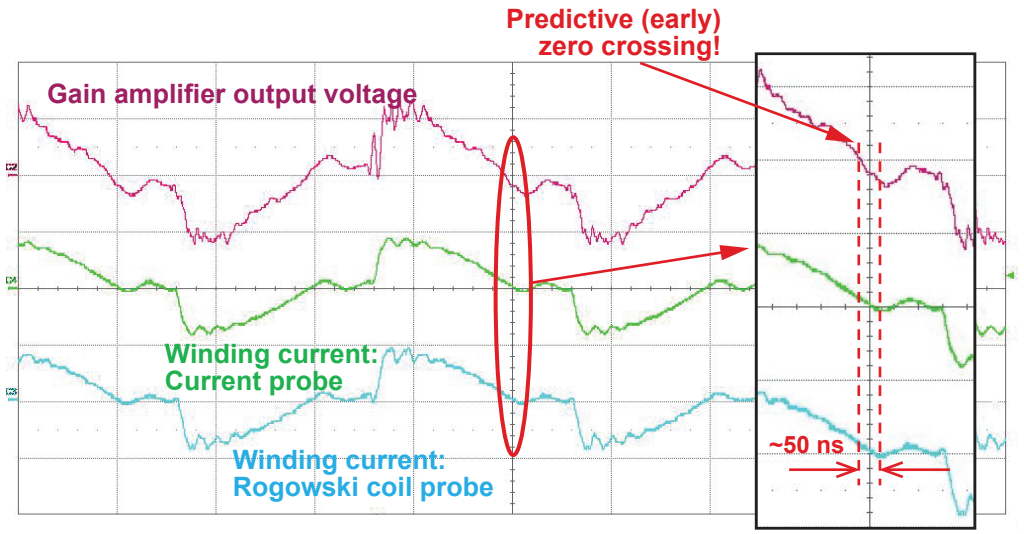


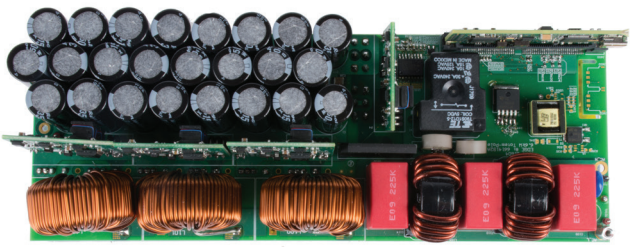
Figure 26 – SR sensing and current waveforms.

Changing the connection polarity of the Rogowski coil, the time-varying current becomes

$$i(t) = \frac{a_1 l}{AN\mu_0} sin\left(\omega t + \phi - \frac{\pi}{2}\right). \quad (12)$$

When making $|\phi| = \frac{\pi}{2}$ by varying the values of R_1, R_2, C_1 and the switching frequency $F_{sw}(\omega=2\pi F_{sw})$ with the right connection polarity between the Rogowski coil output and integrator input, the integrator output, v_{20} (t), can be in phase with the SR current i(t). Moreover, in practical applications, the integrator waveform can be set to lead the SR current. Taking into account the response time and propagation delay on the controller and driver, the SR turn-off timing can still be at the zero current crossing point. Figure 26 shows the proposed SR sensor gain amplifier output waveforms versus i(t) waveform on this CLLLC-SRes-DAB design. As can be observed in Figure 26, the zero voltage crossing is programmed to be turned off earlier than the actual sensing current to accommodate propagation and control delays.

VI. PERFORMANCE VERIFICATIONS



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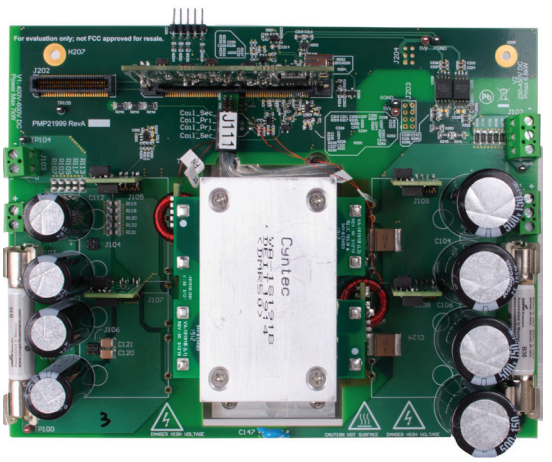
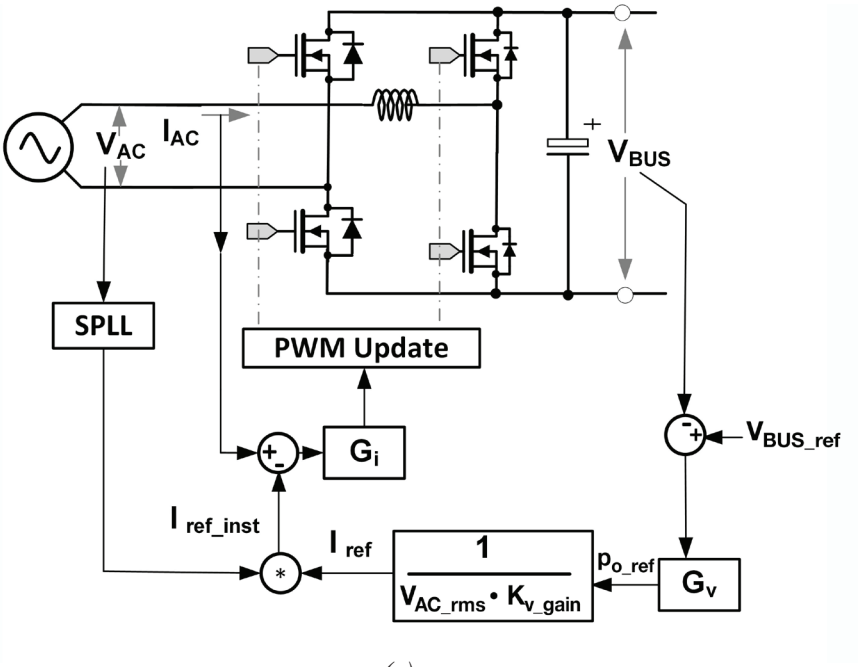


(b)

Figure 27 – 6.6 kW onboard charger reference designs: (a) TTPL bridgeless PFC and (b) CLLLC-SRes-DAB.



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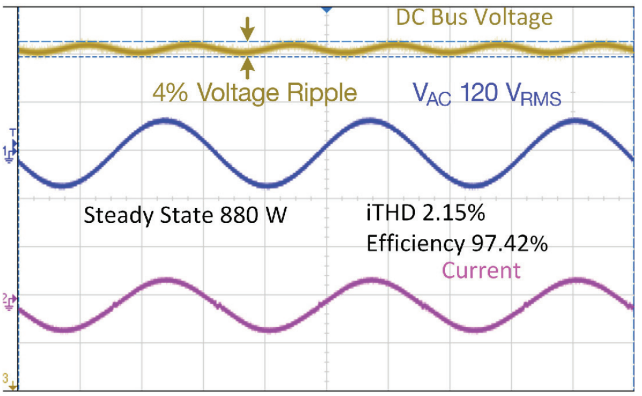

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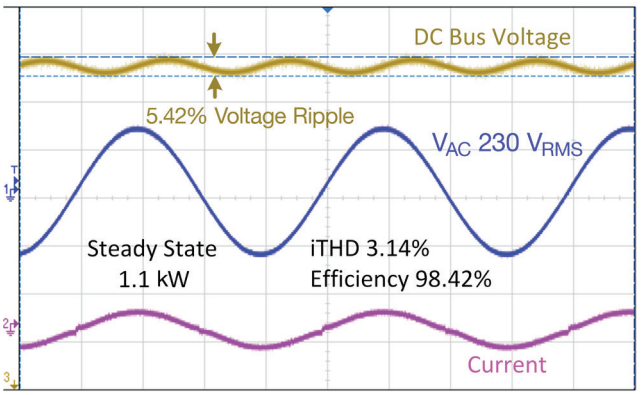
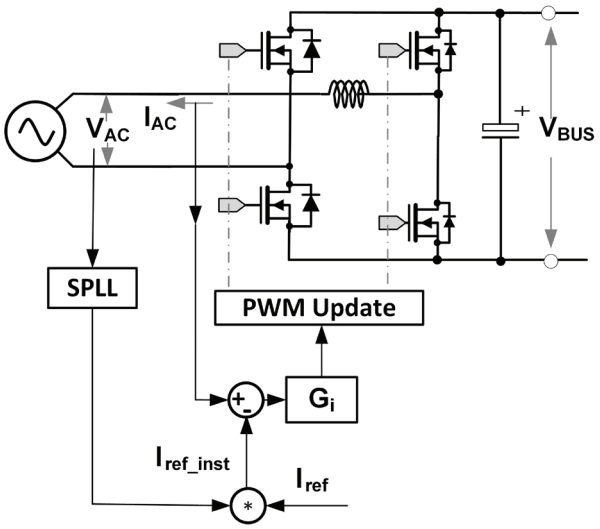


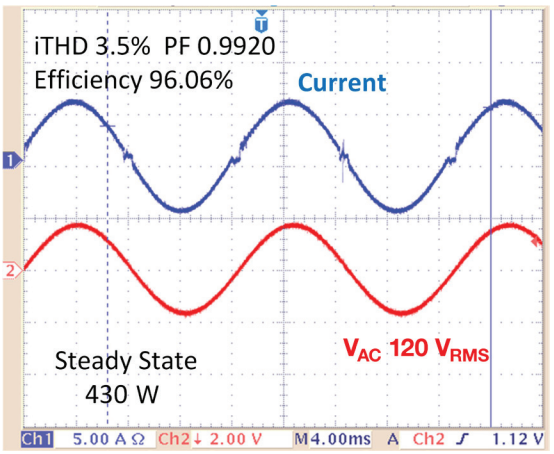
(c)

Figure 28 – TTPL bridgeless PFC design in rectifier mode: (a) control block diagram, (b) low line waveforms and (c) high line waveforms.

Two prototypes, a 6.6 kW interleaved TTPL bridgeless PFC [16] and a 6.6 kW CLLLC-SRes-DAB, were built for performance evaluation, as shown in Figure 27. These prototypes each have their own microcontroller for the ease of evaluating each stage. The interleaved TTPL bridgeless PFC stage achieves 92 W/in^3 power density and the CLLLC-SRes-DAB achieves 76 W/in^3 power density. Based on the design process mentioned in Section V, the following resonant tank parameters are selected for the CLLLC-SRes-DAB: n=1.33, L_m=25 µH, L_{r1}=1.9 µH, C_{r1}=53 nF, L_{r2}=1.45 µH and C_{r2}=70 nF. Control block diagrams and waveforms of the TTPL bridgeless PFC under rectifier mode and grid tied inverter mode are shown in Figures 28 and 29, respectively. In rectifier mode, the PFC output voltage feedback and AC input current feedforward are used in the control loop to perform the PFC function and output regulation. The input current follows the input voltage perfectly, with low current total harmonic distortion (iTHD) at both the low line and high line.



(a)



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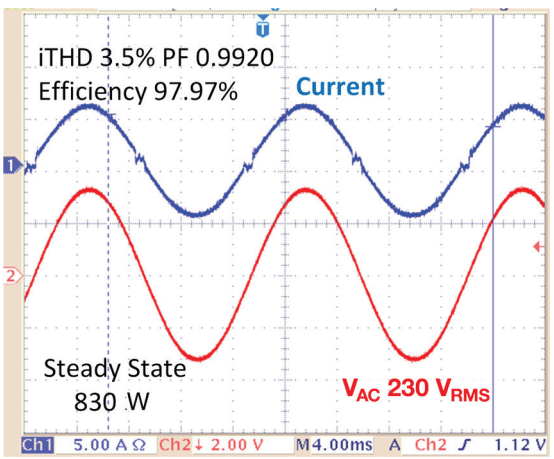


(c)

Figure 29 – TTPL bridgeless PFC design in grid tied inverter mode: (a) control block diagram, (b) low line waveforms and (c) high line waveforms.

In grid tied inverter mode, only the AC current is used for regulation control as the grid can be considered a voltage source. Close to unity power factor (PF) and low iTHD are also observed even with light load. The phase shedding transition of this TTPL bridgeless PFC design is shown in Figure 30. Only one-phase is switching for lower power dissipation at a lighter load while three phases are switching to handle the high current stress at a heavier load. It is notable that the high frequency ripple on the total input current is actually smaller when three phases are actively switching due to ripple current cancellation. Efficiencies of the TTPL bridgeless PFC with and without phase shedding are shown in Figure 31. With phase shedding control implemented, the light load efficiency is greatly improved and reaches 98.9% peak efficiency.

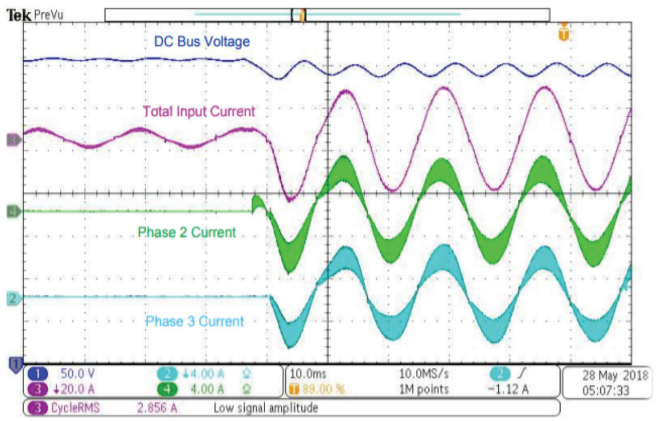


Figure 30 – TTPL bridgeless PFC phase shedding transition.

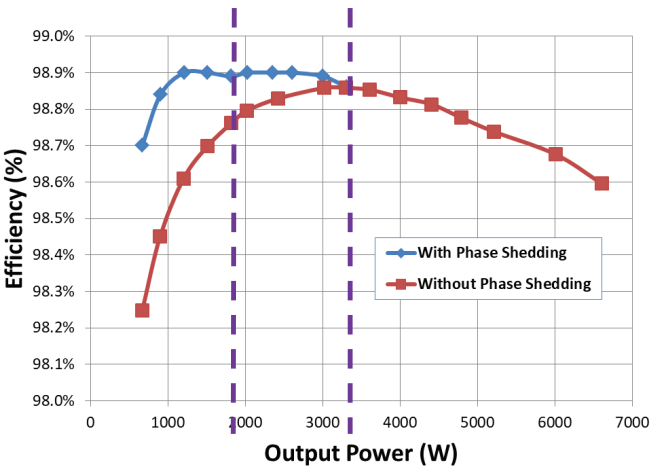
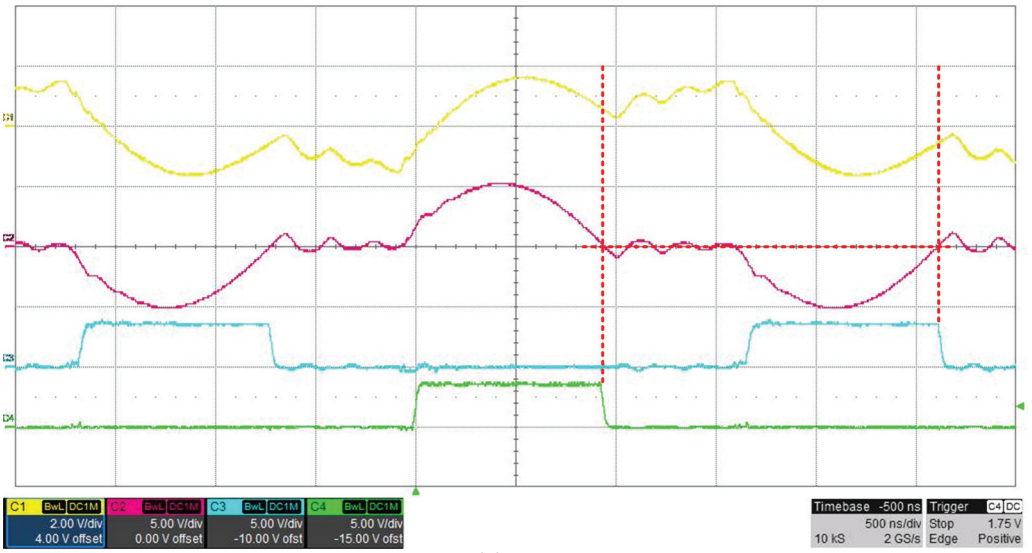
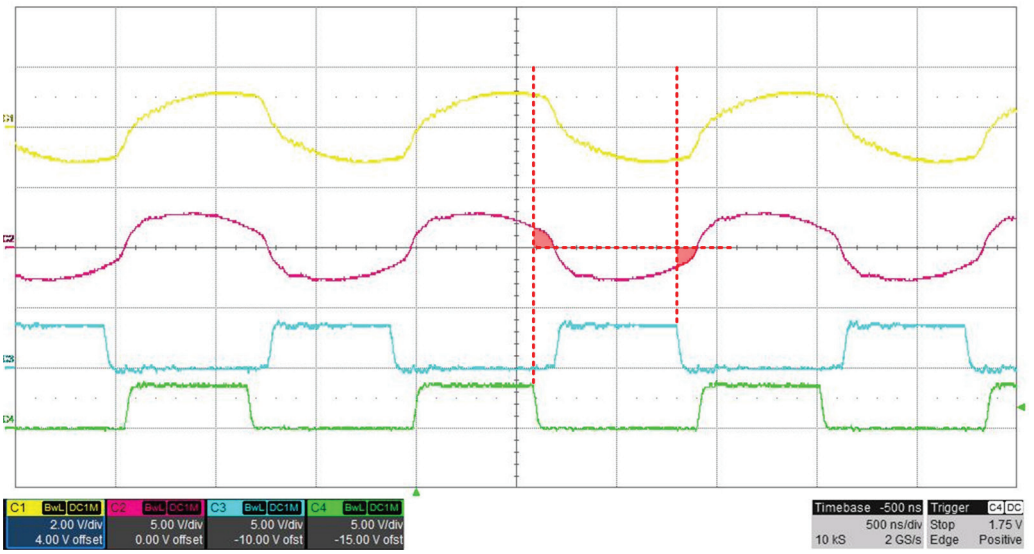


Figure 31 – TTPL bridgeless PFC efficiencies with and without phase shedding.



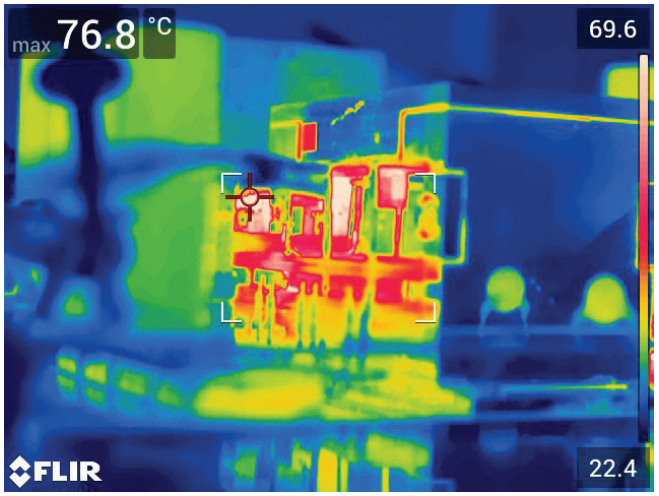
(a)

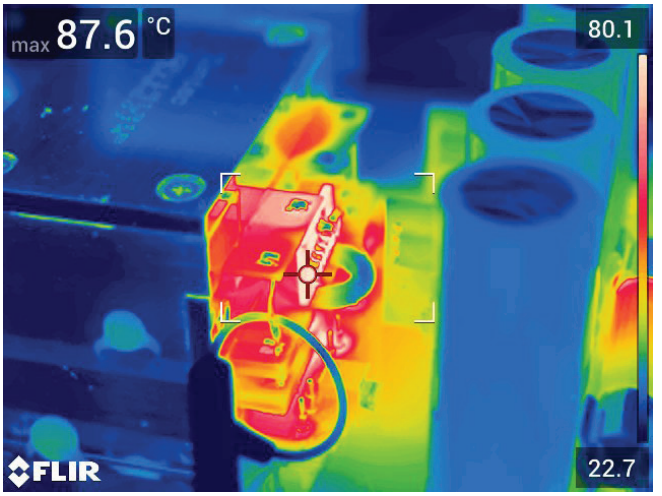


(b)

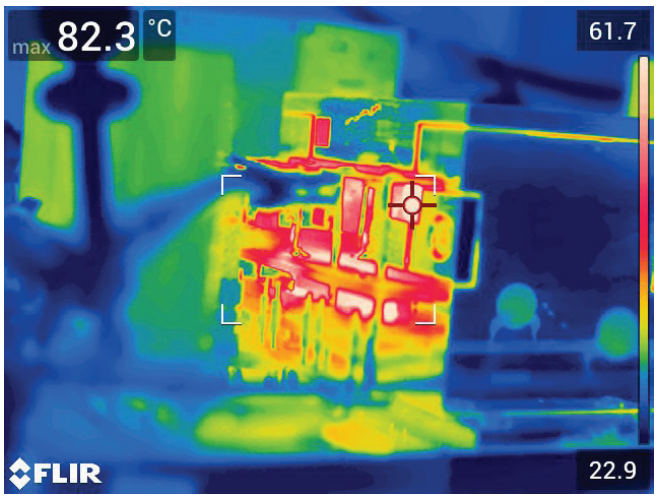
Figure 32 – Winding currents (CH1: I_{Lr1} – 100 mV/A and CH2: I_{Lr2} – 200 mV/A) and SR driving signals (CH3: S_{3B} and CH4: S_{3A}) at (a) 300 kHz and (b) 700 kHz.

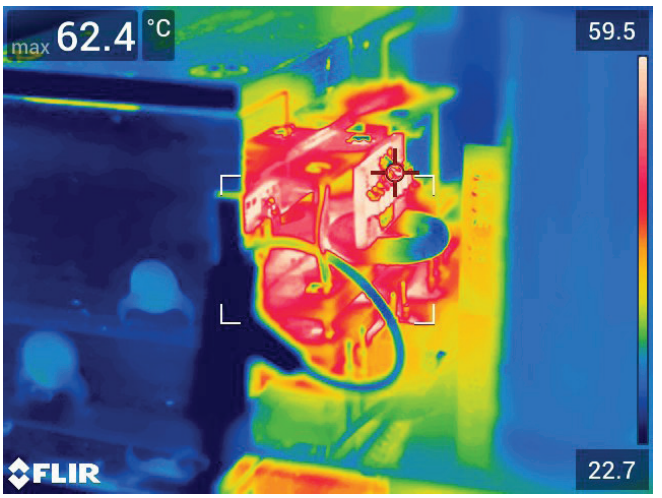
Figure 32 shows the transformer winding currents and SR driving voltages of the CLLLC-SRes-DAB design. The SR driving signals are turned off at the zero current crossing when F_{sw} is lower than F_{r1} – zero current switching (ZCS). It is notable that even when the SR is turned off, the parasitic capacitance will still resonate with the transformer winding capacitance and resonant tank elements, resulting in ringing [20]. When F_{sw} is higher than F_{r1}, the SR driver duty cycles are limited to 50% minus the dead time and lost ZCS.





(a)





(b)

Figure 33 – Thermal images at P_{OUT} = 6.6 kW and F_{SW} = 517 kHz with (a) V_{IN} = 383 V and V_{OUT} = 280 V and (b) V_{IN} = 565 V and V_{OUT} = 420 V.

Key thermal images at 6.6 kW output are shown in Figure 33. At lower output voltage, the hot spot is on the output resonant capacitor board due to the output current being higher. At higher output voltage, the transformer core presents the highest temperature as the voltage-second of the core is higher. Efficiency measurement results are shown in Figure 34; 98% peak efficiency is achieved at a lower battery voltage. It can be observed from Figure 34(a), that light load efficiency is lower when output voltage is higher.

This is due to the increased transformer core loss. Efficiency at a heavy load is higher when the output voltage is lower as the conduction loss is high. Converter efficiency in the charging direction is similar to the efficiency in the discharging direction as the voltage level at the two ends is similar.

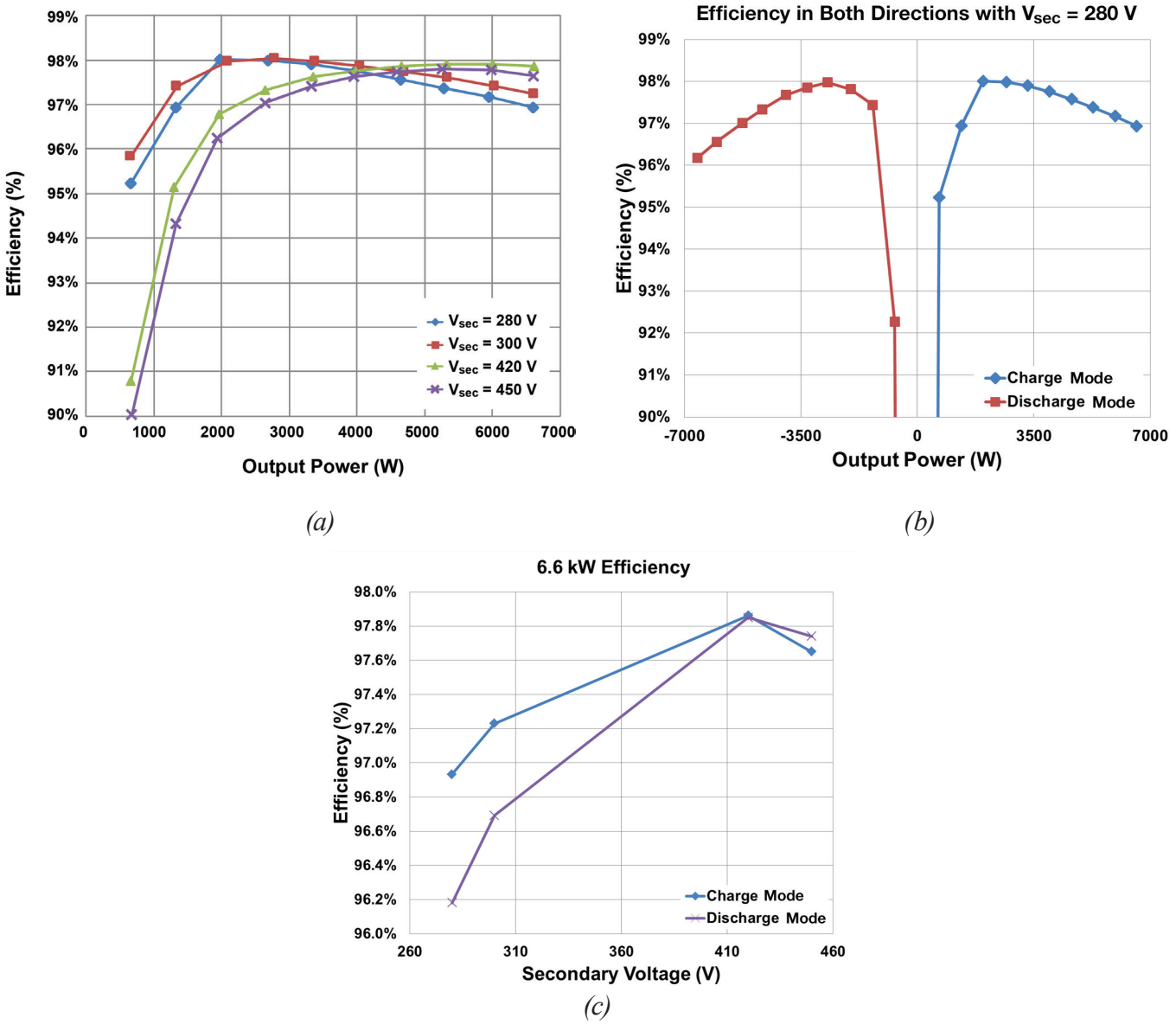


Figure 34 – Converter efficiencies in (a) charging mode, (b) charging and discharging modes and (c) charging and discharging modes at 6.6 kW output power.

VII. SUMMARY

This paper provides the analysis and design of high-power bidirectional AC/DC rectifier applications and topologies. A two-stage approach is generally applied in a bidirectional AC/DC rectifier in order to provide high converter efficiency, high-power density and high immunity to ground fault protections. A 6.6 kW OBC design with a TTPL bridgeless PFC as the AC/DC rectifier/inverter stage and a CLLLC-SRes-DAB as the isolated DC/DC stage are introduced. Design considerations, including the power switch, driver and controller selections, are addressed. Key considerations of using the SiC MOSFET and gate driver design are also introduced. In addition, a Rogowski coil based SR sensing method for high voltage and high frequency synchronous rectification is proposed. As a result, a 98.9% peak efficiency is achieved on the TTPL bridgeless PFC stage and a 98% peak efficiency is achieved on the CLLLC-SRes-DAB stage on the 6.6 kW OBC reference design.

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