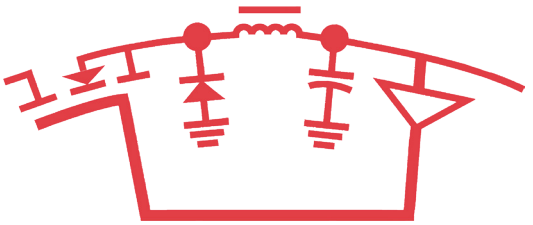

Power Supply Design Seminar

Practical EMI Considerations for Low-Power AC/DC Supplies

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Practical EMI Considerations for Low-Power AC/DC Supplies

Bernard Keogh and Joe Leisten

ABSTRACT

Electromagnetic interference (EMI) is an essential part of every power supply design, but too often gets relegated to the end of the design flow, at which point its resolution can be time-consuming, costly and inefficient. This topic will help dispel fears about EMI, and show how to find and fix the issues.

Most EMI issues are caused by component parasitics that are not even represented in design schematics, such as transformer input/output capacitance, stray capacitance and inductances on the board assembly. EMI filter components have a parasitic capacitance and inductance that limit their useful frequency range, and can even make EMI worse.

To highlight the debugging techniques, we will show practical examples throughout, using a high-density 65 W USB Power Delivery active clamp flyback adapter [1]. These examples will illustrate how a few basic changes result in an almost 50 dB improvement at the fundamental switching frequency without a major sacrifice in efficiency, size or cost.

I. INTRODUCTION

For many power supply designers, the topic of EMI consists of a list of troublesome standards with which their products must comply. Table 1 (from [2]) provides a list of some common EMI standards associated with major product categories. This paper aims to shine some light onto the broader subject. We will look at why EMI is important for all of us, what causes EMI and how it is measured. We cover practical measures to minimize EMI output from a power supply, including shielding, cancellation and filtering.

II. THE CAUSES AND SOURCES OF EMI

A. Component Parasitics

Practical inductors can be modeled by the circuit shown in Figure 1. Parasitic capacitance between turns, between layers or between the windings and core is represented by an equivalent parallel capacitance, C_{PAR}. Winding resistance, magnified by skin and proximity effects, is represented by an equivalent series resistance (ESR). At low frequency this circuit performs like an inductor; at high frequency it will change to being capacitive.

Component parasitics cannot be neglected when considering EMI filters since many components will change in nature due to parasitics over some part of the EMI frequency spectrum [3].

Product Sector	CISPR Standard	EN Standard	FCC Standard
Automotive	CISPR 25	EN55025	–
Multimedia	CISPR 32	EN55032	Part 15
Industrial, scientific and medical (ISM)	CISPR 11	EN55011	Part 18
Household appliances, electric tools and similar apparatus	CISPR 14-1	EN55014-1	–
Lighting equipment	CISPR 15	EN55015	Part 15/18

Table 1 – Summary of product standards for conducted emissions.

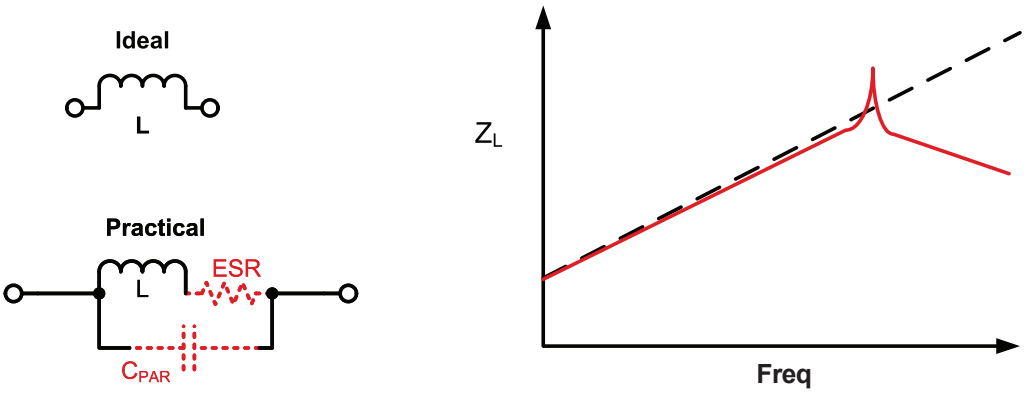


Figure 1 – Ideal vs practical inductor.

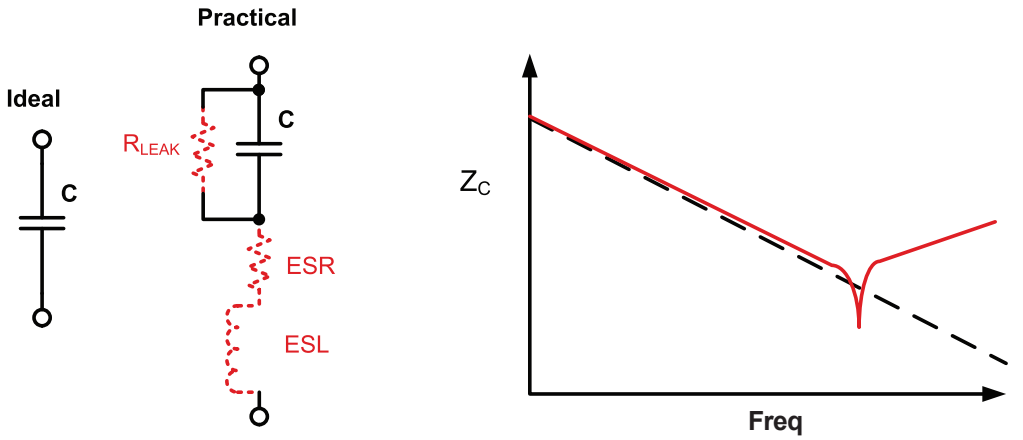


Figure 2 – Ideal vs practical capacitor.

Practical capacitors can be modeled by the circuit shown in Figure 2. Aluminum electrolytic capacitors in particular can have high series resistance or ESR. Compact electrolytic capacitors, often found at the input of 5 to 10 W mobile phone chargers, have impedance values in the range 1 to 10 Ω measured at 150 kHz, room temperature. In the differential filter design, these components should be considered as resistors or inductors and not capacitors.

III. Differential-Mode vs Common-Mode EMI

A. Conducted EMI Test Setup

An important source of common-mode conducted emissions is capacitive coupling. This transfers high frequency signals from the equipment under test (EUT), and its associated input/output cables, to EARTH-ground.

A repeatable measurement across different sites requires that the parasitic capacitance between EARTH-ground and EUT plus associated cables is always the same. This is achieved by using the conducted EMI test setup shown in Figure 3.

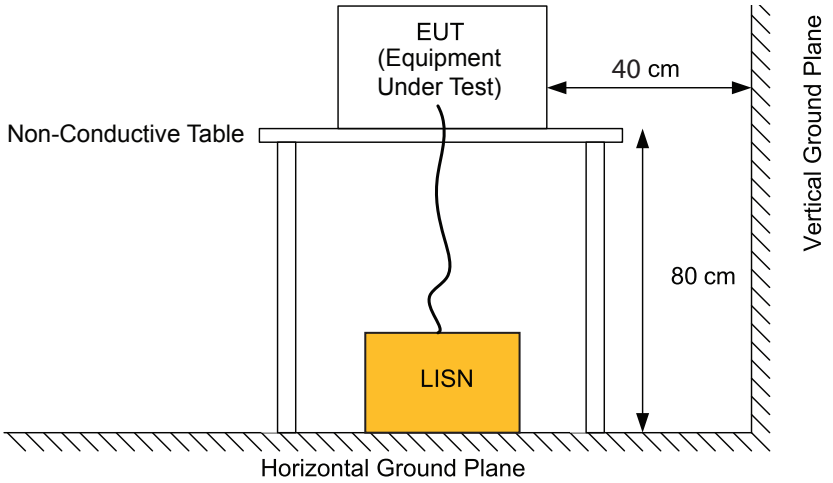


Figure 3 – Conducted EMI test setup.

B. LISN and Its Function

A line impedance stabilization network (LISN) is used to separate the high frequency EMI current signal from the line frequency current feeding the EUT. The LISN is a network of passive components, as shown in Figure 4. It is designed to perform the following functions:

- The LISN provides consistent source impedance with which to feed the EUT. It ensures conducted emissions measurements are repeatable and not dependent on the line impedance at the laboratory.
- The LISN separates the high frequency EMI current signal from the 50/60 Hz line current waveform. The high frequency EMI current signal is converted to a voltage at the two RF outputs of the LISN. From here it can be transferred to an EMI receiver to be measured.
- It filters out high frequency signals coming from the line feed. This ensures measurements made at different sites are repeatable and not influenced by differences in high frequency content of the laboratory supply.

A detector is used to convert the time varying output of the bandpass-filtered LISN output into a fixed level for measurement. The three types of commonly used detectors are illustrated in Figure 5. The peak detector simply captures the highest signal amplitude observed during the measurement time-window. The peak detector, often used for indicative results, is not included in the standards of Table 1. Both the quasi-peak and average detectors give outputs that reflect the power of the signal to interfere with radio communications. These detectors are included in the standards listed in Table 1.

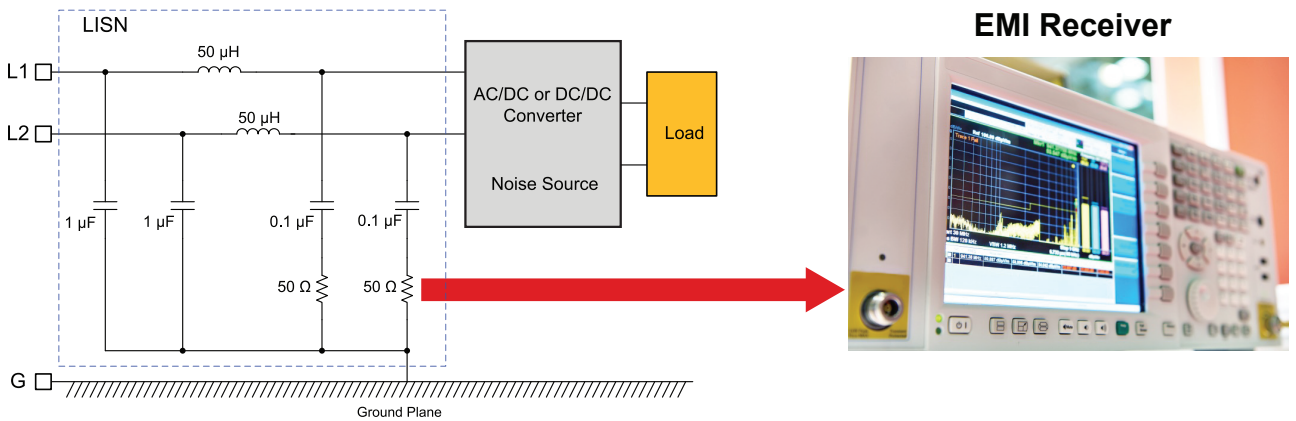


Figure 4 – Line impedance stabilization network (LISN) for conducted EMI.

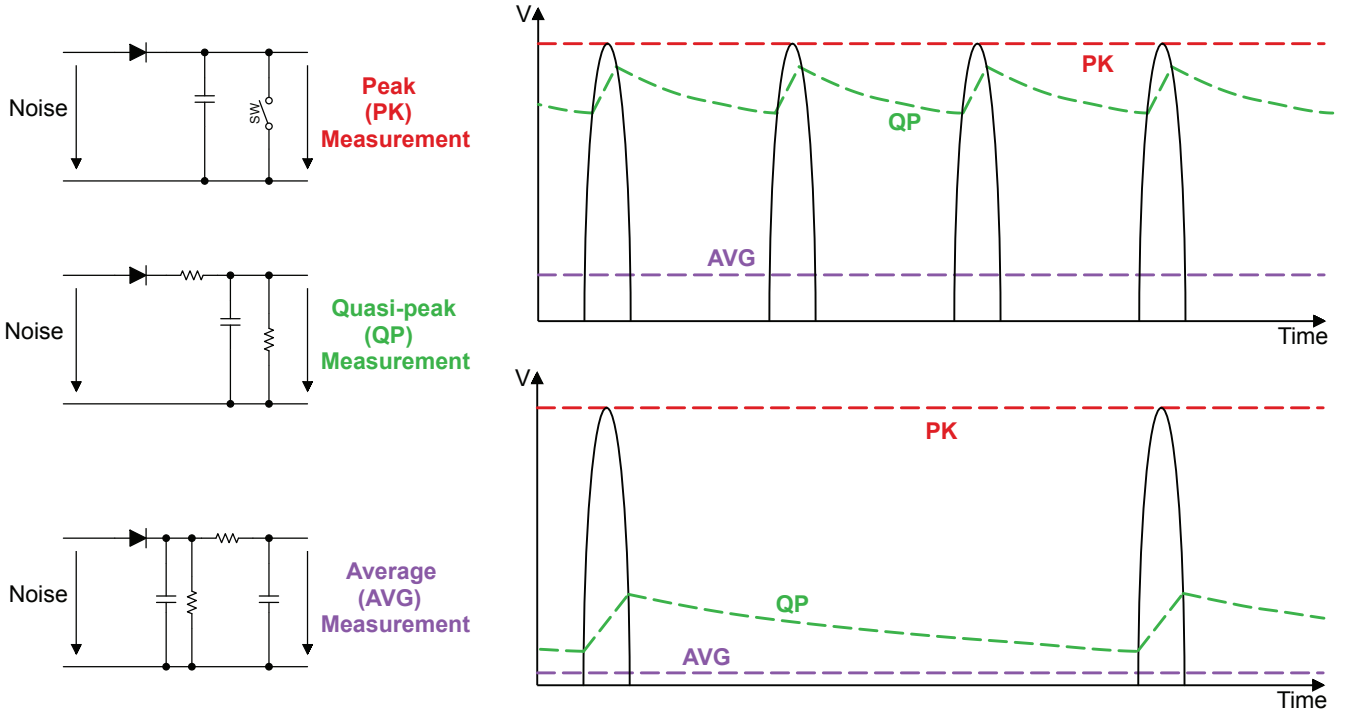


Figure 5 – EMI receiver detector types and their characteristics.

C. EMI Filter and Its Function

Figure 6 illustrates the EMI measurement schematic. A switched mode power supply, including EMI filter network, is powered from the line via a LISN. The EMI filter components shown in blue are present to attenuate the differential-mode current signal. The EMI filter components shown in red (solid-line) will attenuate the common-mode current signal. Components shown in dashed-red are actually parasitic elements that cause the CM EMI to propagate.

D. Current Paths Through the LISN – DM vs CM

Operation of the line frequency rectifier at the input of the power supply can be divided into two intervals. During its conducting interval, one pair of diodes is forward biased. In this interval, current flows from the line charging the storage capacitor, C_{BULK}, and feeding the switched mode converter. In its non-conducting interval, all input rectifier diodes are reverse-biased and no current flows from the line. During this non-conducting interval, input current for the switched mode converter is provided by discharging the storage capacitor, C_{BULK}. The

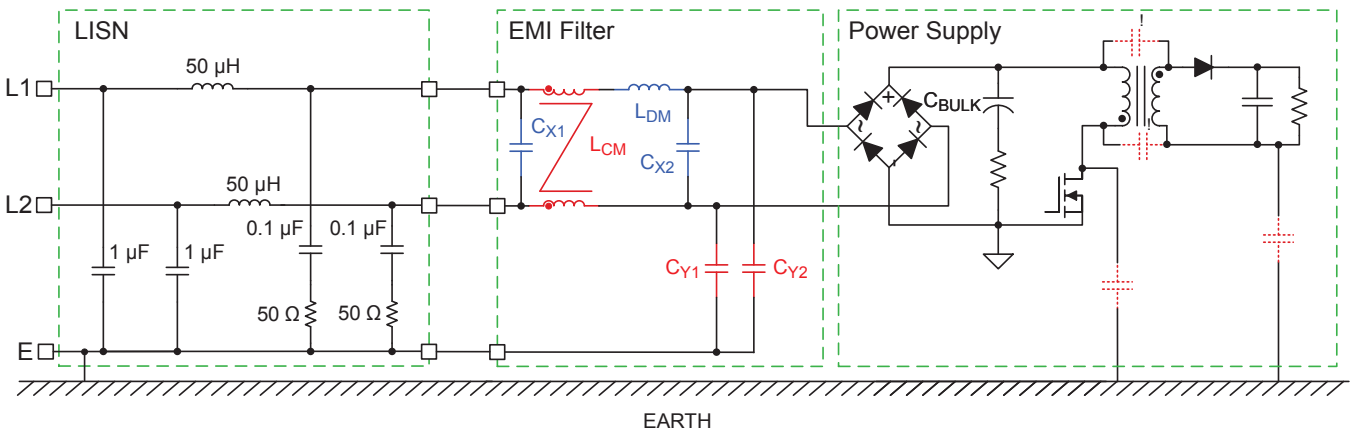


Figure 6 – LISN interface to EMI filter and power supply.

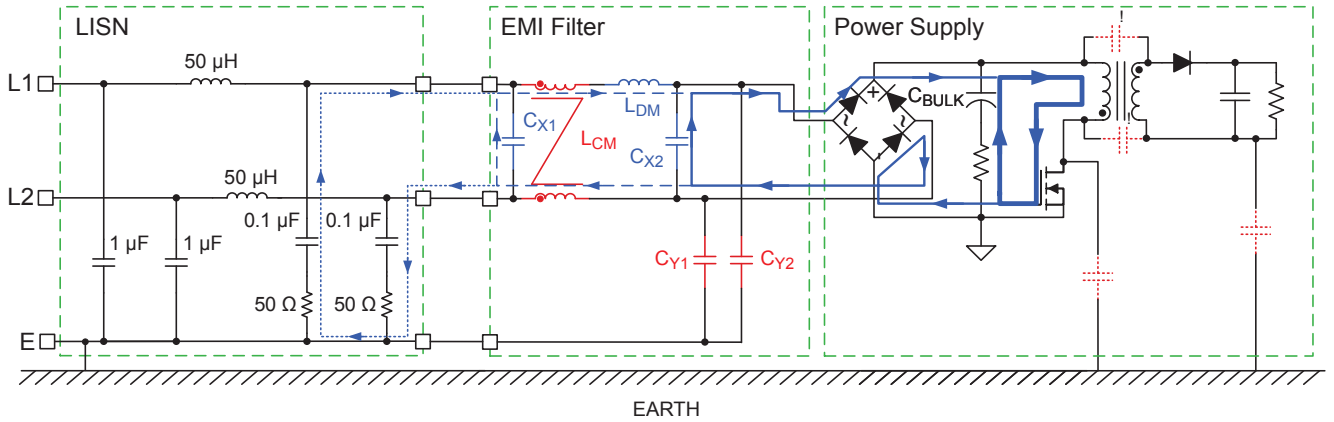


Figure 7 – LISN DM current path.

input rectifier draws input current pulses at twice the line frequency. These twice line frequency current pulses can normally be neglected when calculating differential-mode EMI due to their low frequency and low harmonic content. Differential-mode EMI will be estimated assuming constant line current during the conducting interval of the input rectifier.

A differential-mode current signal is generated by the switched-mode power supply, which draws a pulsed current signal from its input. It is the harmonics contained in this switching frequency, pulsed current waveform that make up the differential-mode current signal. The differential-mode current is illustrated by arrowed blue lines in Figure 7. This differential current signal is attenuated by the differential filter components, also shown in blue, on its way to the LISN. The differential current is sensed by both RF outputs of the LISN (across the 50 Ω resistors). The phase at one RF output is inverted compared with the other.

Common-mode current results when current leaks to EARTH via parasitic capacitance paths. The path taken by the common-mode current is illustrated by the arrowed red lines in Figure 8. The common-mode current returns from EARTH via the LISN to the line feed (L and N). It is converted to a voltage signal across the two 50 Ω resistors and passed to the receiver for measurement. The EMI filter components, shown in solid red, attenuate the common-mode current signal.

The LISN output is a combination of both common-mode and differential-mode signals. The measured EMI spectrum may be dominated by differential-mode or common-mode signals; it is not possible to tell which just by looking at the result. A large (10 times bigger than C_{X1}) X-capacitor placed between the L and N wires in the cable connecting the EUT to the LISN will greatly attenuate the differential-mode signal flowing in the LISN, but will have no effect on common-mode. This provides a quick way to determine if our measured EMI signal is dominated by common-mode or differential-mode signals. If the measured EMI signal with the added X-capacitor is similar to the original, then it is dominated by common-mode. If the measured EMI signal with the added X-capacitor is significantly lower than the original, then it is dominated by differential-mode. There is little point in improving the differential filter if our problem EMI signal is dominated by common-mode current and vice versa. Knowing the type of EMI that dominates a problem region of the spectrum is helpful in targeting our efforts to resolve EMI issues.

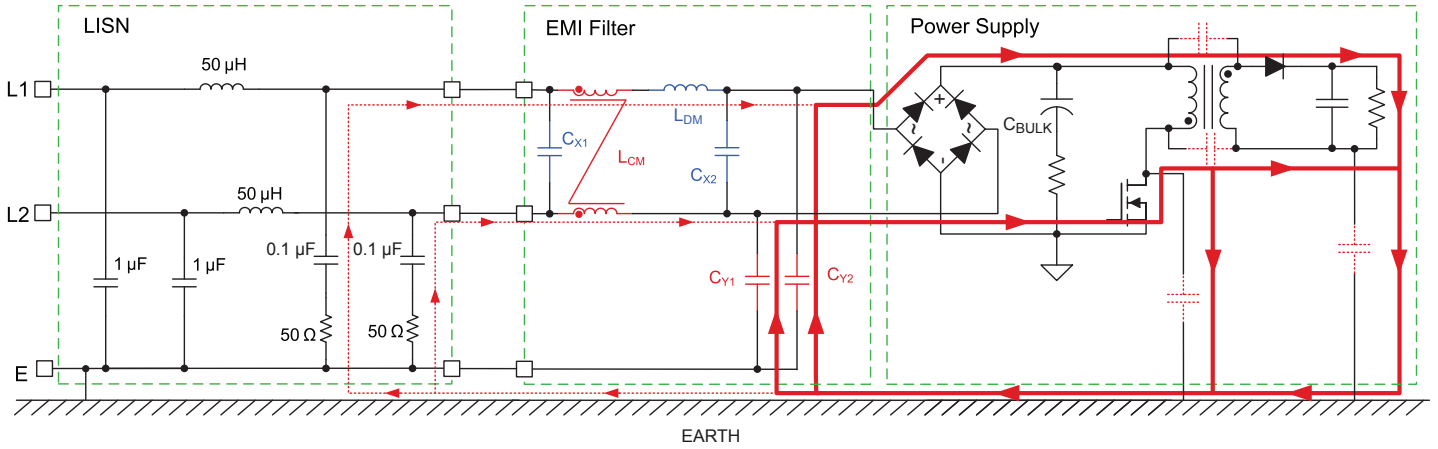


Figure 8 – LISN CM current path.

IV. Differential-Mode EMI and Mitigation Options

A. How Does DM EMI Cause Issues

It is important that differential-mode currents are attenuated before they reach the wall socket since the AC supply distribution system represents a large antenna, as illustrated in Figure 9.

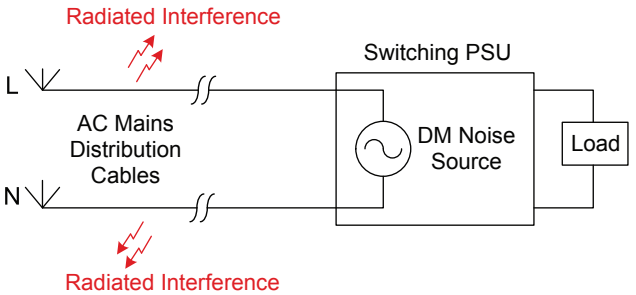


Figure 9 – DM noise interference.

B. Sources of DM EMI Noise

Differential-mode EMI consists of a high frequency AC current flowing between the line (L and N) voltage terminals. Switched mode power converters typically draw a pulsed current waveform from their input terminals (Figure 10).

A differential filter (Figure 7) is used to reduce the amplitude of the pulsed current waveform reaching the line voltage terminal so that its magnitude is reduced below the required limit before reaching the LISN.

C. DM Filter Design Methodology

Let us assume that the switched mode converter draws the current waveform shown in Figure 11 from its DC input. Fourier series expansion can decompose this waveform into its sinusoidal component (harmonic) frequencies. Figure 13

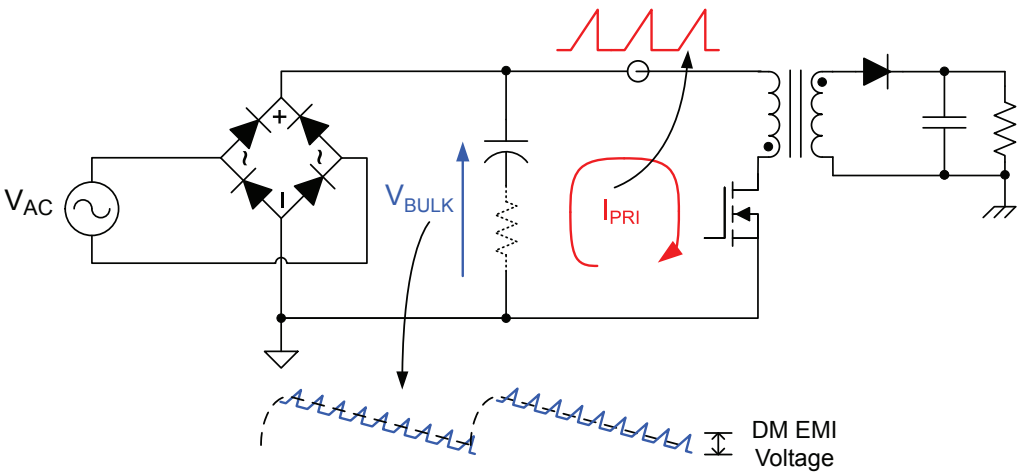


Figure 10 – DM noise.

shows how the trapezoidal waveform of Figure 11 can be represented in the frequency domain. It depicts the amplitude of the fundamental switching frequency and a series of harmonics of the switching frequency. The corner frequency of the differential filter must be chosen to provide sufficient attenuation to reduce all the harmonics in the EMI band below the level of the required limit line. Normally the lowest harmonic that comes within the conducted EMI spectrum is the only one that needs to be considered when setting the corner frequency of the differential filter.

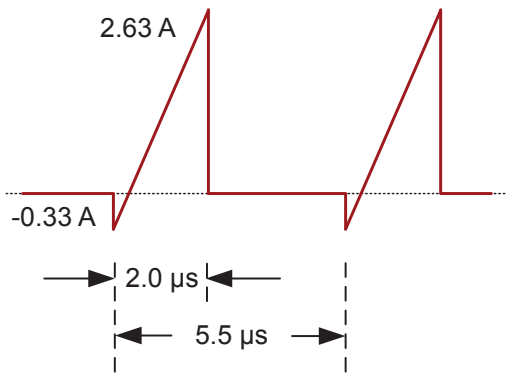


Figure 11 – Switch current waveform, 65 W active clamp-flyback at 115 V.

The first step is to express the switching frequency input current waveform in mathematical form. Figure 11 shows the switch current waveform that flows in a 65 W flyback adapter circuit when delivering full load from a 115 V line supply. The switch current waveform, for this condition, can be represented mathematically by Equation (1).

$$
\begin{aligned}
I_D(\theta) &= 0 && : -\pi \le \theta < \theta_0 \\
&= I_{PK1} \bullet \frac{\theta - \theta_0}{\theta_{Fall}} && : \theta_0 \le \theta < \theta_1 \\
&= \left(I_{PK2} - I_{PK1}\right) \bullet \frac{\theta - \theta_1}{\theta_{Rise}} + I_{PK1} && : \theta_1 \le \theta < \theta_2 \\
&= I_{PK2} \bullet \left[1 - \frac{\theta - \theta_2}{\theta_{Fall}}\right] && : \theta_2 \le \theta < \theta_3 \\
&= 0 && : \theta_3 \le \theta < \pi
\end{aligned}
\qquad (1)
$$

The variables used in Equation (1) are defined in Equation (2).

$$
\begin{aligned}
f_{sw} &= \frac{1}{t_{Per}} \\
\omega &= 2 \bullet \pi \bullet f_{sw} \\
\theta_{Fall} &= \omega \bullet t_{Fall} \\
\theta_{Rise} &= \omega \bullet t_{Rise} \\
\theta_0 &= -\frac{\theta_{Rise} + 2 \bullet \theta_{Fall}}{2} \\
\theta_1 &= \theta_0 + \theta_{Fall} \\
\theta_2 &= \theta_1 + \theta_{Rise} \\
\theta_3 &= -\theta_0 \\
t_{Per} &= 5.5\ \mu s \\
t_{Rise} &= 2.0\ \mu s \\
t_{Fall} &= 20\ ns
\end{aligned}
\qquad (2)
$$

For convenience we have chosen to normalize time by the angular switching period, represented by θ, as defined in Equation (3).

$$\theta = \omega \bullet t \qquad (3)$$

The switch current expression, Equation (1), generates the waveform shown in Figure 12.

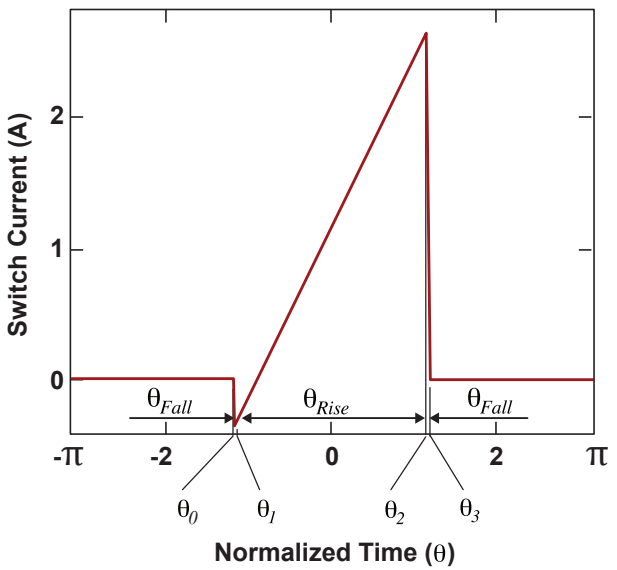


Figure 12 – Mathematical representation of switch current, $I_D(\theta)$.

The second step is to break up the switch current waveform into its sinusoidal constituent parts by Fourier series expansion. The RMS amplitude of the n^{th} harmonic of the switching frequency is calculated using Equation (4). The resulting EMI spectrum can be obtained by multiplying the current harmonics by the 50 Ω sense resistor of the LISN to generate the unfiltered differential EMI plot shown in Figure 13.

$$I_{DM}(n) = \frac{1}{\sqrt{2}} \bullet \left| \frac{1}{\pi} \bullet \int_{-\pi}^{\pi} I_D(\theta) \bullet e^{-j \bullet n \bullet \theta} d\theta \right| \quad (4)$$

When designing the differential-mode filter, it is normally necessary only to consider the lowest harmonic component that comes within the conducted emissions frequency band (150 kHz to 30 MHz). In this case our switching frequency (181 kHz) is in the band, so the filter must be designed to ensure the fundamental comes below the quasi-peak limit line.

$$I_{DM}(1) = 554\ mA \quad (5)$$

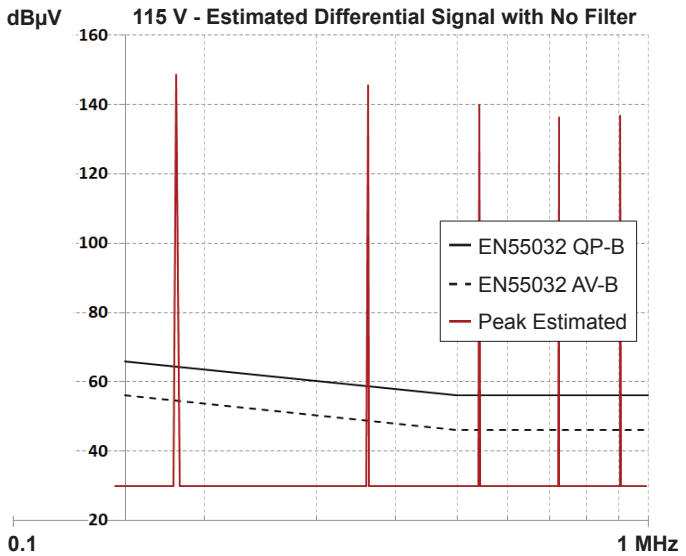


Figure 13 – Calculated differential-mode EMI spectrum without filter, $I_{DM}(n)$.

The differential filter must provide attenuation (Attn) expressed by Equation (6), at the switching frequency, in order to satisfy the quasi-peak limit. The quasi-peak limit is approximately 64 dBµV at 181 kHz.

$$Attn = 20 \bullet log\left(\frac{I_{DM}(1) \bullet 50\ \Omega}{1\ \mu V}\right) - 64\ dB\mu V \approx 84\ dB \quad (6)$$

Assuming a CLC filter with a roll off of 60 dB/decade, the corner frequency (f_C) for the differential filter can be calculated using Equation (7).

$$f_C = \frac{f_{sw}}{10^{\frac{Attn}{60}}} \approx 7\ kHz \quad (7)$$

However, a practical power supply design includes several components that attenuate the differential-mode signal, even though that is not their primary purpose. For example, the bulk energy storage capacitors will also attenuate the differential signal. The common-mode choke leakage inductance will also attenuate the differential current, although that is not its primary purpose. Figure 14 presents the complete differential-mode schematic of the 65 W flyback adapter [1]. In this schematic, only the components shown in red (C_X and L_{DM}) are explicitly added for the sole purpose of attenuating the differential signal.

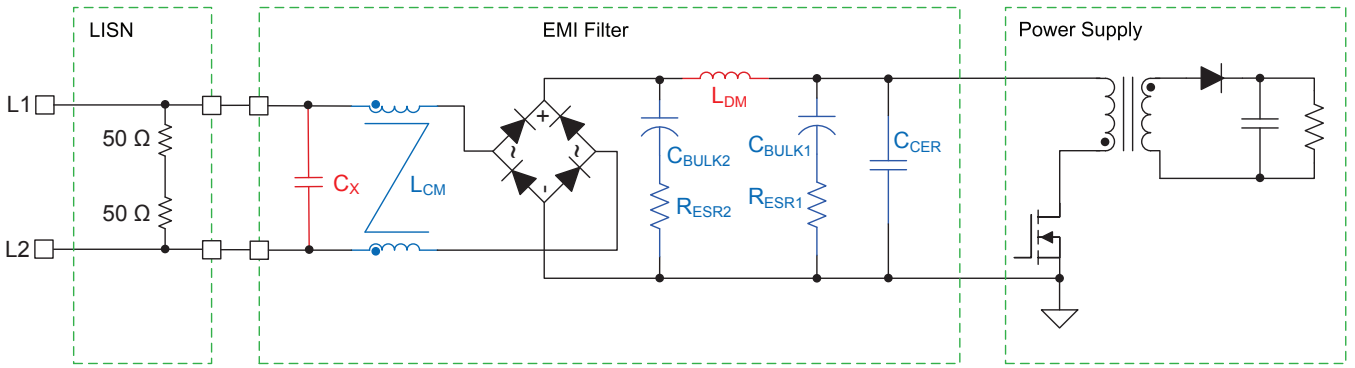


Figure 14 – 65 W flyback adapter input schematic.

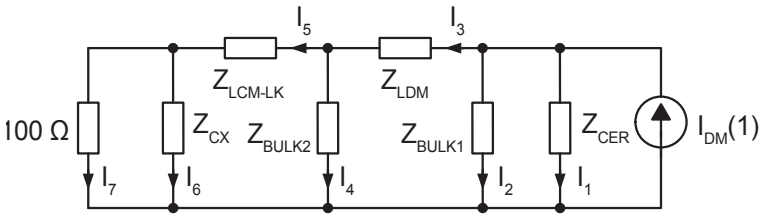


Figure 15 – Differential filter equivalent circuit.

Figure 15 presents the differential equivalent of the circuit shown in Figure 14. Z_{CER} represents the capacitive impedance of the 0.2 µF ceramic filter capacitor (C_{CER}) at the switching frequency. Its value is calculated in Equation (8). Z_{BULK1} and Z_{BULK2} represent the effective impedance of the 56 µF bulk capacitors located in positions C_{BULK1} and C_{BULK2}, given by Equation (9). The ESR of these components dominates at the switching frequency – high-temperature (~100°C) ESR is 0.31 Ω. A 22 µH inductor is located in position L_{DM}. Its series resistance can be neglected, hence the effective impedance (Z_{LDM}) at switching frequency is given by Equation (10). Leakage inductance of the common-mode inductor, L_{CM}, is 0.1 µH. Hence, the effective differential mode impedance of this component, Z_{LCM-LK}, is given by Equation (11). Finally, the effective impedance (Z_{CX}) of the 0.1 µF X-capacitor at switching frequency is given by Equation (12).

The switching frequency differential-mode currents flowing through the input circuit components can be determined by application of Kirchhoff's voltage law. The results for this example are presented in Equation (13).

$$Z_{CER} = \frac{1}{j \cdot \omega \cdot 0.2\mu F} \approx 4.4 \angle -90\ \Omega \tag{8}$$

$$Z_{BULK\,1,2} = \frac{1}{j \cdot \omega \cdot 56\mu F} + R_{ESR} \approx 0.31 \angle 0\ \Omega \tag{9}$$

$$Z_{LDM} = j \cdot \omega \cdot 22\mu H \approx 25 \angle 90\ \Omega \tag{10}$$

$$Z_{LCM-LK} = j \cdot \omega \cdot 0.1\ \mu H \approx 0.11 \angle 90\ \Omega \tag{11}$$

$$Z_{CX} = \frac{1}{j \cdot \omega \cdot 0.1\ \mu F} \approx 8.8 \angle -90\ \Omega \tag{12}$$

$$\begin{aligned} I_1 &= 38.3 \angle -86.7°\ mA \\ I_2 &= 543 \angle -3.32°\ mA \\ I_3 &= 6.74 \angle -92.6°\ mA \\ I_4 &= 6.72 \angle -94.7°\ mA \\ I_5 &= 241 \angle -9.75°\ \mu A \\ I_6 &= 240 \angle -4.72°\ \mu A \\ I_7 &= 21 \angle -94.7°\ \mu A \end{aligned} \tag{13}$$

The filtered differential-mode signal at switching frequency for 115 V full power operation can be calculated as shown in Equation (14). The quasi-peak limit line at this frequency is 64 dBµV, giving a small predicted margin of ~4 dBµV.

$$V_{DM@181\ kHz} = 20 \bullet log\left(\frac{|I_7| \bullet 50\ \Omega}{1\ \mu V}\right) \approx 60\ dB\mu V \quad (14)$$

Comparing this theoretical result to the measured result in Figure 51, the measured result is ~8 dB better. This is predominantly due to the natural frequency dithering effect from operating in transition mode with low-frequency 100/120 Hz ripple on the bulk capacitors, which forces the instantaneous switching frequency to vary over a certain range during each AC line half-cycle. This is evident from the flat-topped spreading of the fundamental switching frequency in Figure 51 over ~170 to 200 kHz, versus the narrow fixed-frequency fundamental at 181 kHz in Figure 13. Published analyses [4] have shown typically ~5 dB benefit from frequency dithering, which accounts for most of the difference in this example between measured and calculated results.

D. DM Filter Choke Practicalities

Once the corner frequency and required attenuation are known, there are a few important practical considerations when implementing the differential filter:

- Inductive elements in the differential filter must be rated to carry the RMS line current drawn by the converter from the wall socket. They must also not saturate when carrying the peak line current. As illustrated in Figure 16, the peak line current can be many times higher than its RMS value when not employing a power factor correction circuit.
- High voltage aluminum electrolytic capacitors are frequently used at the input of switched mode converters to provide line frequency energy storage. Even at the start of the conducted emissions frequency band, 150 kHz, the impedance of these capacitors is likely to be dominated by their equivalent series resistance (ESR).
- Careful attention must be paid to layout to ensure that the high attenuation offered by the differential filter cannot be bypassed. See Section V.E.iii "Stray coupling to CM filter choke" for examples of how sub-optimum PCB layout allows the EMI filter components to be bypassed.

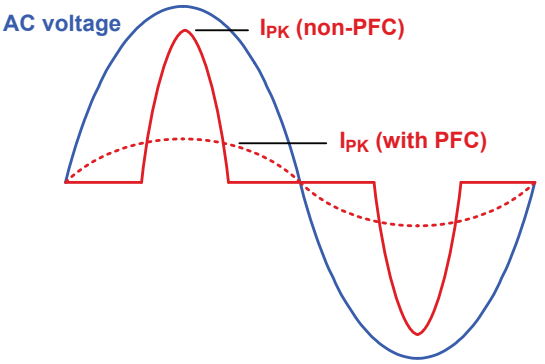


Figure 16 – AC line current with PFC and non-PFC front-ends.

V. Common-Mode EMI and Mitigation Options

A. How Does CM EMI Cause Issues

Common-mode EMI takes the form of high frequency current flowing between the line (L and N) terminals and EARTH. Common-mode EMI signals generated by a power supply will be transmitted by a combination of the line feed cables and the power supply output cables. To avoid interference with nearby radio communications the common-mode noise source signal amplitude shown in Figure 17 must be attenuated to limit the radiated interference.

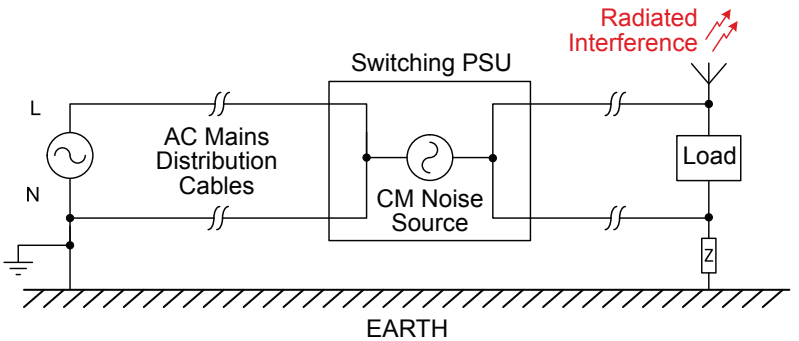


Figure 17 – CM noise interference.

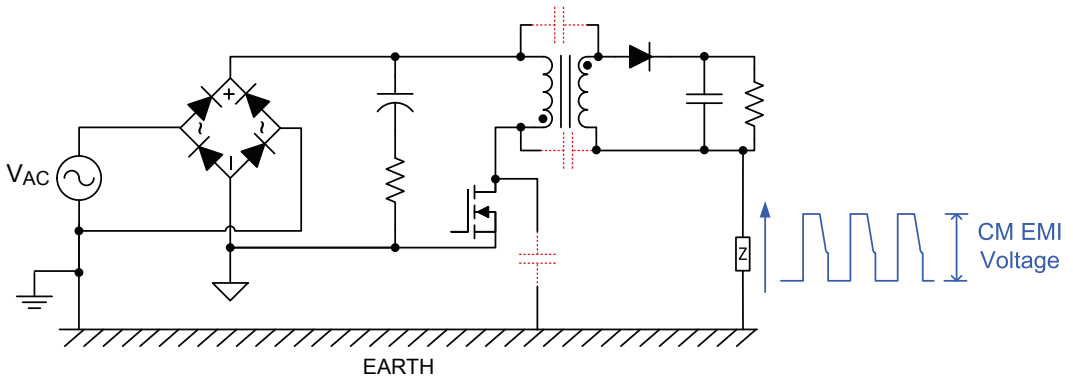


Figure 18 – CM noise sources.

B. Sources of CM EMI Noise

As illustrated in Figure 18, common-mode currents can flow directly from primary to EARTH via the parasitic capacitance associated with each switched node. They also flow from primary to secondary via parasitic capacitance between the windings.

C. Measuring CM EMI in the Time Domain

Typically, assessment of the CM-only emissions in the frequency domain requires use of specialized splitters to separate CM and DM. However, the CM performance of any AC/DC power supply can be assessed very simply in the time domain, as shown in Figure 19, without any need for these special splitters. The AC/DC power supply is powered through the LISN per normal conducted EMI setup, using a floating resistive load at the output. A simple "pick-up coil" is wound around both the positive and negative leads that run from the power supply output to the resistive load. Photographs of a typical setup are shown in Figure 20. The zoomed photograph shows the simple pickup coil that is used – this is basically a number of turns of wire that are wound tightly around both the load positive and negative leads. The pick-up coil is intended to have equal capacitive coupling to both the positive and negative load leads, so that only the CM signal at the output is sensed.

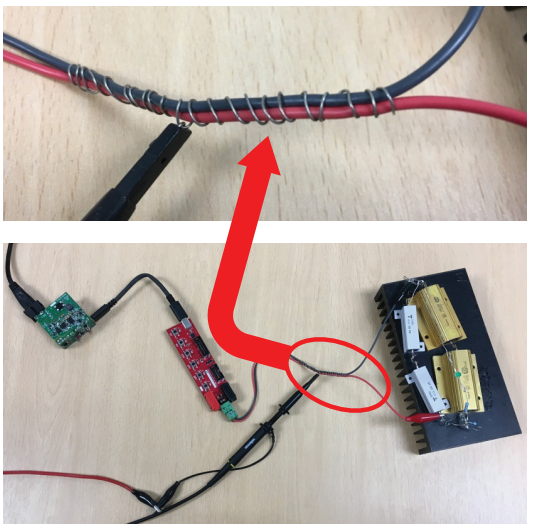


Figure 20 – Time-domain CM noise measurement – setup example, with zoom of pick-up coil.

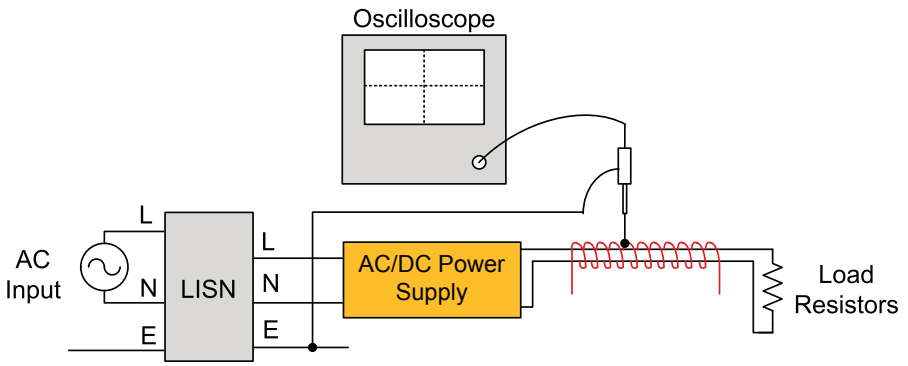


Figure 19 – Time-domain CM noise measurement.

The scope is used to measure the CM signal at the pick-up coil relative to the LISN EARTH. The expected time-domain CM waveform should be a lower-amplitude version of the primary switching node of the AC/DC power supply. The lower the amplitude of the CM waveform at the output, the better the expected CM EMI performance. The observed CM signal gives a relative indication of CM performance rather than an absolute result. But if the same pick-up coil and setup is consistently used, it can give a very useful indication of relative CM performance between different AC/DC power supplies, and between different transformers and other changes within a given power supply.

Figure 21 shows an example of a relatively high CM signal at the output. This was taken on the initial active clamp flyback (ACF) power supply [1] that was showing 100 dBµV EMI levels at the fundamental switching frequency (see Figure 49). The upper waveform shows the result over an entire AC line cycle (2 ms/div.), and the lower waveform is zoomed to show the switching waveform. Clearly, the CM signal looks a square-wave running in transition-mode, at approximately 180 kHz – this is the fundamental switching frequency of the ACF design at low-line 115 V_{RMS}.

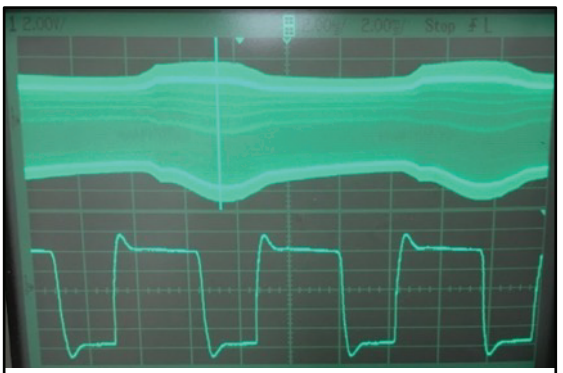


Figure 21 – Time-domain CM noise result – example of "bad" CM noise.

Figure 22 shows the same measurement, taken in the same setup, using the same pick-up coil – but testing an improved version of the ACF PCB design, and with an improved transformer design (for lower CM). The difference in the performance is dramatically clear – the CM signal amplitude has been reduced from approximately 10 V_{PP} to approximately 40 mV_{PP}.

This debug method is very fast and easy to set up and use, and requires no special equipment. It can be used to rapidly assess the impact of various changes, before taking the time to run more time-consuming EMI scans. It can also be used to observe in real-time the impact of various changes. And it offers a very simple way to separate out and observe only the CM signal – which is often more dominant and more difficult to solve than DM.

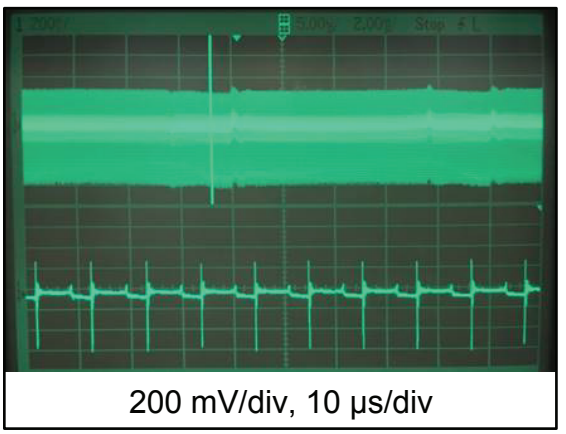


Figure 22 – Time-domain CM noise result – example of "good" CM noise.

D. Mitigation of CM EMI

There are three main ways to tackle CM noise: shield the CM noise generators, arrange the power circuit to be balanced for low CM or simply add filtering to limit the CM noise.

i. CM shielding

Shielding of CM noise generators can be accomplished in several ways. In Figure 23, there is no internal transformer shield, so the parasitic capacitance between primary and secondary windings (which depends on the detailed internal transformer layer structure) will have a relatively large CM voltage imposed across it, and will thus allow a relatively large CM current to flow to the secondary and from there to EARTH.

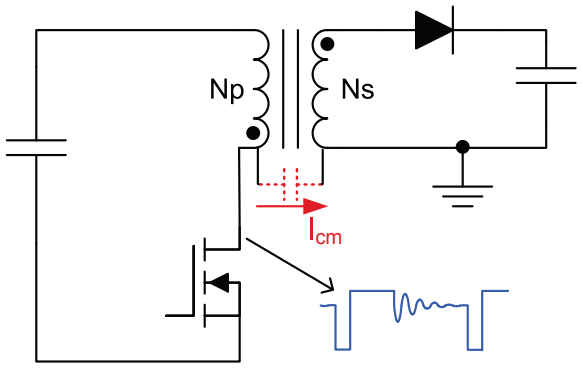


Figure 23 – Transformer with no internal shielding.

In Figure 24, the transformer structure is modified to insert a shield in between the primary and secondary. In this case, any CM current flow from the primary to the shield will be returned directly to the local primary ground, keeping it away from EARTH. The parasitic capacitance from the shield-to-secondary will still cause CM current to flow to the secondary; but, since the CM voltage across this capacitance will be much lower, the resulting CM current will also be much lower.

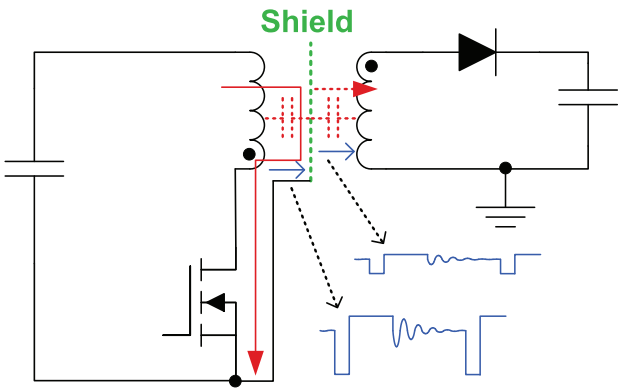


Figure 24 – Transformer with internal shielding.

Figure 25 shows a shield added around the outside of a transformer – this shield has two main functions: to connect the ferrite core to local primary ground and to "flux-band" any stray magnetic field from the transformer windings. If not addressed, both of these effects can cause significant EMI coupling to nearby circuit nodes. Adding a locally-grounded flux-band to the transformer can improve EMI by 10 to 20 dB, depending on the specific PCB layout and proximity of the power stage components and EMI filter to each other.

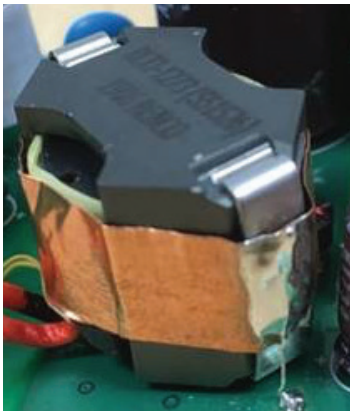


Figure 25 – Transformer external shielding example.

Although the transformer parasitic primary-secondary capacitance is the dominant cause of CM EMI in most cases, there can also be significant CM EMI from the power circuit switching nodes, especially when there are high-amplitude switching voltages. Even if the switching node trace area is minimized (to minimize parasitic coupling capacitance to EARTH and other circuit nodes), CM coupling can still be an issue. In such cases, it can be useful to shield the noisy switching nodes – an example is shown in Figure 26. A copper shield, tied to local primary ground, is fitted over the noisy switching nodes to divert much of the CM noise to local ground and away from EARTH. (Note that the copper shield is covered with insulating tape).

Figure 26 – Circuit shielding example.

In some cases, especially in high-density designs where the power stage and EMI filter are very close together, an EMI shield can be added beside or around the EMI filter, as shown in Figure 27; this limits EMI noise from the power stage coupling to the AC input terminals, bypassing the EMI filter.

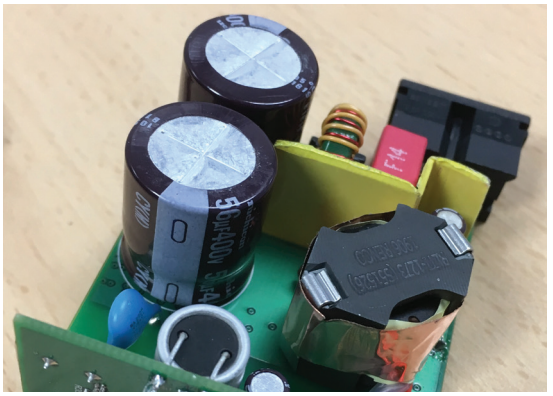


Figure 27 – EMI filter shielding example.

ii. CM cancellation and balance

CM balance or cancellation is another way to deal with CM noise [5]. This involves rearranging the transformer internal layers, or possibly adding extra internal layers and auxiliary windings, in order to ensure that the secondary CM injection is balanced – i.e., any CM current injected into the secondary is balanced with a similar-amplitude but opposite-phase cancelling current, resulting in close to zero net CM current flowing to the secondary. Or, alternatively, the transformer layer structure is arranged so that any parasitic capacitance to the secondary has the same average voltage at both sides of the capacitor, so that zero net CM current flows in the capacitance to the secondary. This is shown in more detail in Section VI.

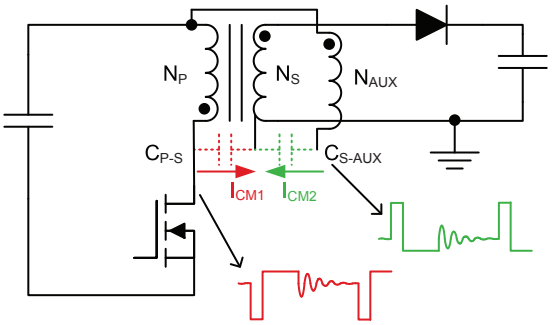


Figure 28 – Example AUX winding for CM balance/cancellation.

iii. CM filtering

Finally, the flow of CM current to LISN EARTH can be filtered with a suitable CM filter as shown in Figure 8. The objective of the CM filter is to limit or minimize the amount of CM current that flows through the LISN 50 Ω measurement resistors.

The Y-capacitors, C_{Y1} and C_{Y2}, present a low-impedance to bypass the CM current local to the power stage and keep it away from the LISN. The CM choke, L_{CM}, presents a high-impedance to the CM current in order to minimize the amount of CM current flowing through the LISN 50 Ω resistors.

E. CM Filter Choke Practicalities

i. Winding structure

The CM filter choke can be implemented in several ways. Some commonly-used structures are shown in Figure 29. Split-wound chokes are popular because the loose coupling between the two windings results in a large parasitic "air-core" leakage inductance in series with the CM choke. This "free" leakage inductance gives extra DM filtering and, in some cases, can allow the explicit DM filter choke to be eliminated.

Split-Wound* **Bifilar-Wound*** **Multi-Section**

**CM choke 3-D images reproduced with permission of Wurth Elektronic*

Figure 29 – Different CM filter choke winding structures.

However, at high frequency, the split-wound CM choke does not perform well and the poor coupling of the two windings can cause high-frequency EMI issues or make the choke susceptible to high-frequency EMI noise pickup.

The bifilar-wound structure in Figure 29 is wound with both windings side-by-side, all the way around the core. This results in better coupling between the windings with better performance at high frequency and lower noise susceptibility. However, the reduced stray inductance results in less "free" DM filtering and an explicit DM filter choke will often be required – but this is usually a better option given the better high frequency CM choke performance.

The multi-section bobbin-wound CM choke in Figure 29 can also be used for better high-frequency performance – the various sections of the winding are physically kept apart to minimize parasitic capacitance, which is a limiting factor on the high frequency choke performance.

ii. Parasitic capacitance

Figure 30 shows an equivalent circuit of a CM choke, highlighting the parasitic input-output capacitance. This parasitic capacitance is highly dependent on the winding structure of the choke. At high frequency, the parasitic capacitance will bypass the CM choke inductance, making the choke less effective and allowing high frequency CM noise to pass through unattenuated.

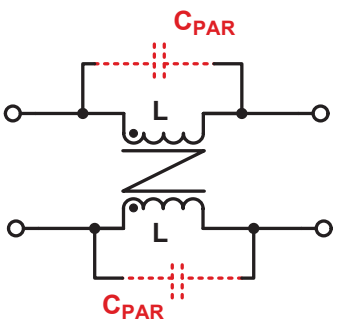


Figure 30 – CM filter choke equivalent circuit.

Figure 31 shows an example of a CM choke wound with a two-layer winding on each side. Two layers are required in order to accommodate the numbers of turns necessary (25 T) to achieve the target inductance of ~5 mH and to ensure that the series DC resistance (DCR) is not excessive. In this example, the winding progresses from the bottom (start) to the top of the toroid in a layer and then progresses back down from top to bottom in a second winding layer sitting on top of the first layer. This structure is replicated on both sides of the toroid, for each side of the split CM choke. This two-layer winding results in relatively high parasitic input-output capacitance, especially since the start/finish of the windings sit directly on top of each other.

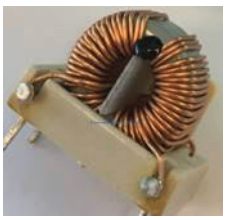


Figure 31 – Example split-wound, 2-layer CM filter choke.

The resulting conducted EMI scan for a power supply using this choke is shown in Figure 32 – clearly, the high value of CM inductance together with the high stray inductance (from the high number of turns) results in a lot of filtering, with good pass margin over most of the frequency range. However, at approximately 20 MHz, the emissions increase significantly, resulting in insufficient pass margin. This increase is a result of the parasitic input-output capacitance, which allows CM noise at ~20 MHz to pass through to the LISN.

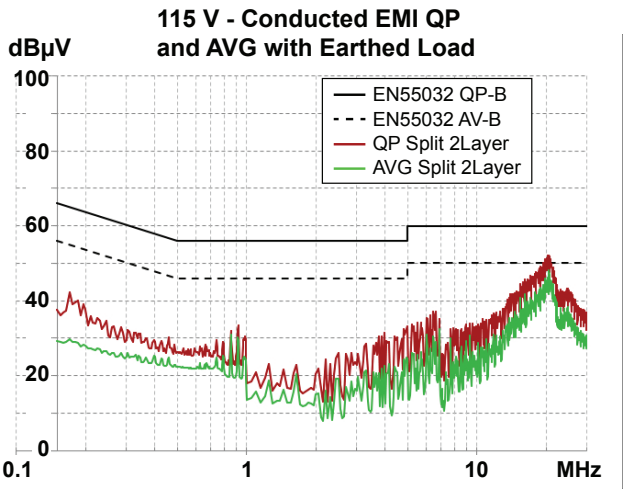


Figure 32 – EMI result using split-wound, 2-layer CM filter choke from Figure 31.

The two-layer split-wound CM choke was replaced with a different choke of similar physical size, shown in Figure 33 – this is a bifilar-wound choke, with a single-layer winding. The single-layer winding has approximately half the number of turns as the original choke, resulting in significantly lower CM inductance, ~1.1 mH (less than a quarter of the original choke). The bifilar-wound structure also has much less "free" DM inductance. Despite the lower inductance of this choke, the resulting conducted EMI scan in Figure 34 shows excellent pass margin over the entire frequency range. In effect, the previous excessive pass margin at low frequency (with the two-layer split-wound choke) has been reduced, in favor of better pass margin at the more difficult 10 to 30 MHz range; in effect, the new choke offers a better optimized result across the frequency range. This is an example of how more filtering (in terms of more filter inductance, more turns and more winding layers) can actually make the EMI result worse. An added bonus of the new bifilar-wound choke is that it has less turns, therefore lower DCR, and improves the power stage efficiency, especially at low-line input voltage.

Figure 33 – Example bifilar-wound, 1-layer CM filter choke.

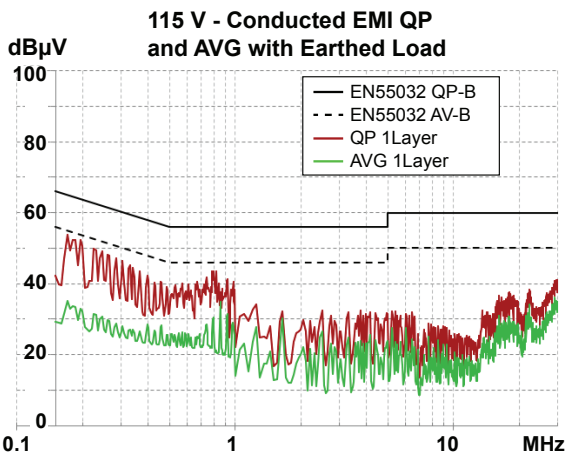


Figure 34 – EMI result using split-wound, 2-layer CM filter choke from Figure 33.

Given the improved performance of the single-layer choke in Figure 33, the original choke was modified, to convert it into a single-layer split-wound choke, as shown in Figure 35. Effectively, almost half the turns were removed, converting the original 25-T two-layer winding into a 14-T single-layer winding. The reduced turns lowered both CM and DM leakage inductance. When tested in the power supply, the measured conducted EMI result was almost identical to that shown in Figure 34 for the bifilar-wound version. This result confirmed the importance of minimizing the parasitic input-output capacitance of all filter chokes.

Figure 35 – Modified 1-layer split-wound CM filter choke.

iii. Stray coupling to CM filter choke

Figure 36 shows a picture of the 65 W active clamp flyback USB-PD adapter design [1]. This initial prototype used a two-board "sandwich" construction, with the lower board used for all the primary-referenced circuitry and the upper board for the secondary. Initial EMI scans (see Figure 49) showed very high emissions, caused by several issues with the initial design.

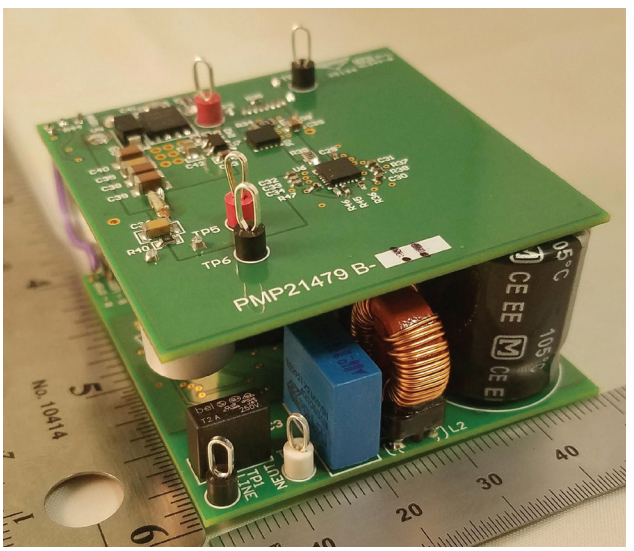
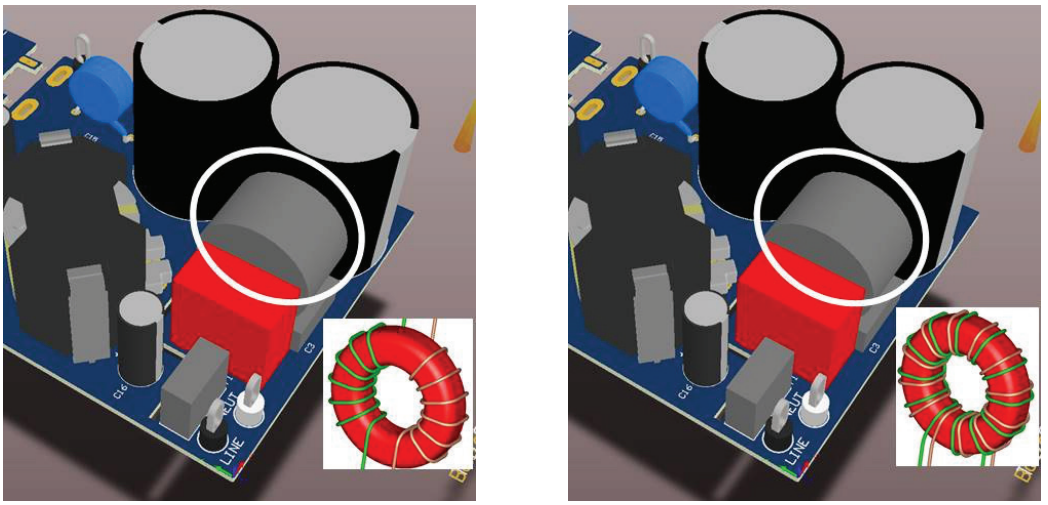


Figure 36 – Example 65 W adapter design.



**CM choke 3-D images reproduced with permission of Wurth Elektronic*

Figure 37 – Close proximity of noisy transformer to CM filter choke.

One of the issues identified with this initial design was the type, orientation and proximity of the CM choke to the noisy primary side of the transformer. Figure 37 shows a 3-D image of the design, with the secondary board removed for clarity. The CM choke is located quite close to the transformer, especially the noisy switch-node connection to the primary winding of the transformer. The initial design used a split-wound CM choke and as can be readily seen in Figure 37, one side of the CM choke sits much closer the transformer primary compared to the other. This arrangement results in asymmetric noise coupling to one side of the CM choke (the nearer winding) compared to the other. This is observed in the conducted EMI scans as a significant difference in the emissions measured on the live versus neutral lines, at the fundamental switching frequency in particular. When the split-wound CM choke was replaced with a bifilar-wound type of similar size and inductance, the conducted emissions at the fundamental switching frequency were reduced by approximately 12 dB, as shown in Figure 38. This reduction was seen on one line only – the bifilar-wound choke is arranged with both windings side-by-side, so that each was equally exposed to any noise from the transformer, avoiding the large asymmetry observed with the split-wound choke.

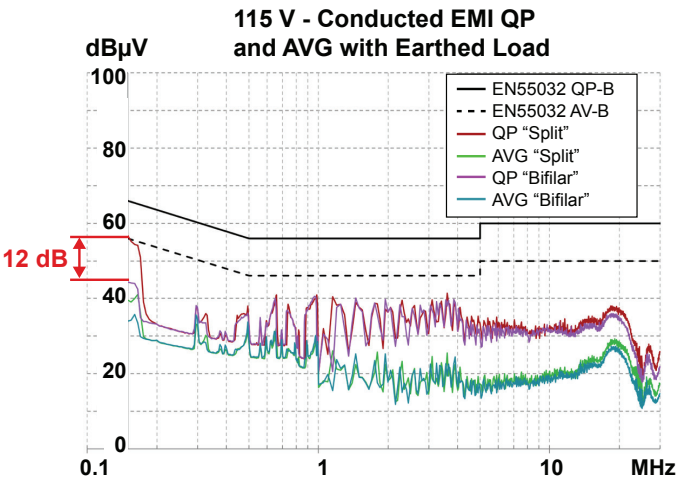


Figure 38 – Measured EMI improvement by split-wound vs bifilar-wound CM filter choke.

The final design also employed a shield in between the transformer and EMI filter as shown in Figure 27 and a flux-band around the transformer as shown in Figure 25, to limit the noise coupling to the EMI filter.

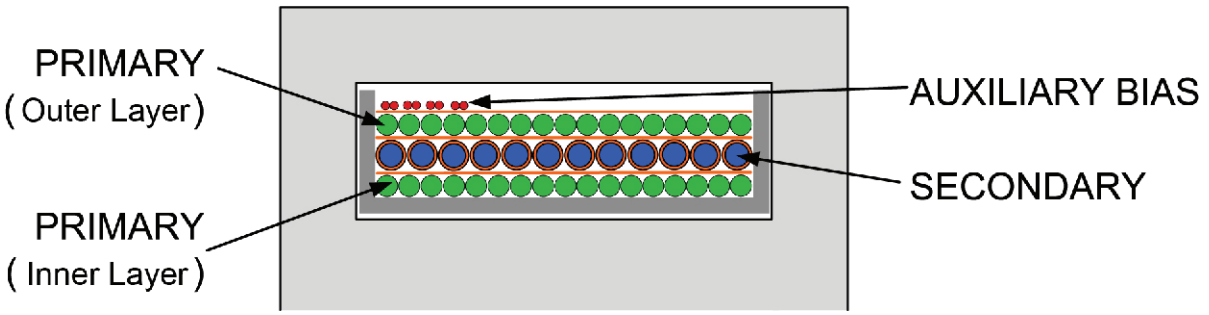


Figure 39 – Initial internal structure – no shielding.

VI. Transformer EMI Shielding and Cancellation Techniques

A. CM Balance – Design Example

i. Initial transformer construction – no shields

The initial design of the PMP21479 [1] reference design used the internal transformer structure shown in Figure 39. This is an interleaved construction, using a split primary on the inner and outer layers, with a secondary layer sandwiched in-between the primaries. The auxiliary bias windings are placed on a separate layer, outside the outer primary.

Figure 40 shows how the transformer windings are connected to the active clamp flyback power circuit. The inner half-primary is connected to the ACF switching node at one end and then center-tap connected to the outer half-primary; the other end of the outer half-primary finishes at the DC bulk capacitor, V_{BULK}+. The secondary winding connects at one end to the DC output capacitor, V_{OUT}+, and the other end to the cathode of the rectifying diode. The actual design uses a synchronous rectifier (SR), but a diode is shown here for simplicity. Note that the secondary rectifier is placed at the low-side, in the transformer return leg – this is done to simplify the SR gate drive, but it does have an impact on the CM EMI performance. Finally, the auxiliary bias winding connects to the primary ground at one end and to a rectifying diode at the other to generate an auxiliary bias rail to power the primary control circuit.

Figure 41 shows the switching waveforms that would be observed at each end of the main windings. The end of the primary that connects to the main switch-node will see the full primary voltage peak-to-peak swing; the primary center-tap will see half of that voltage amplitude (assuming the primary is symmetrically split). Thus, the inner half-primary will have an average voltage approximately 75% of the primary switch-node peak-to-peak voltage swing.

The outer half-primary will thus vary between approximately zero (at the DC bulk cap end) and half the primary switch-node peak-to-peak voltage swing, for an average of approximately 25% of the primary switch-node peak-to-peak voltage swing.

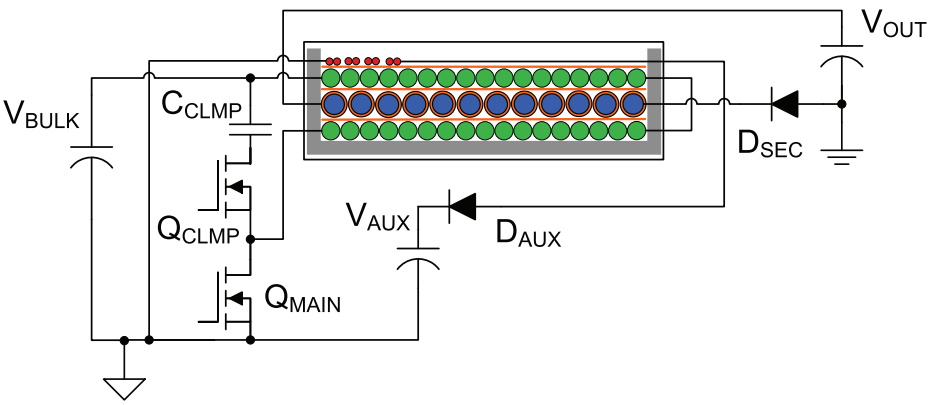


Figure 40 – Initial transformer showing power circuit connections.

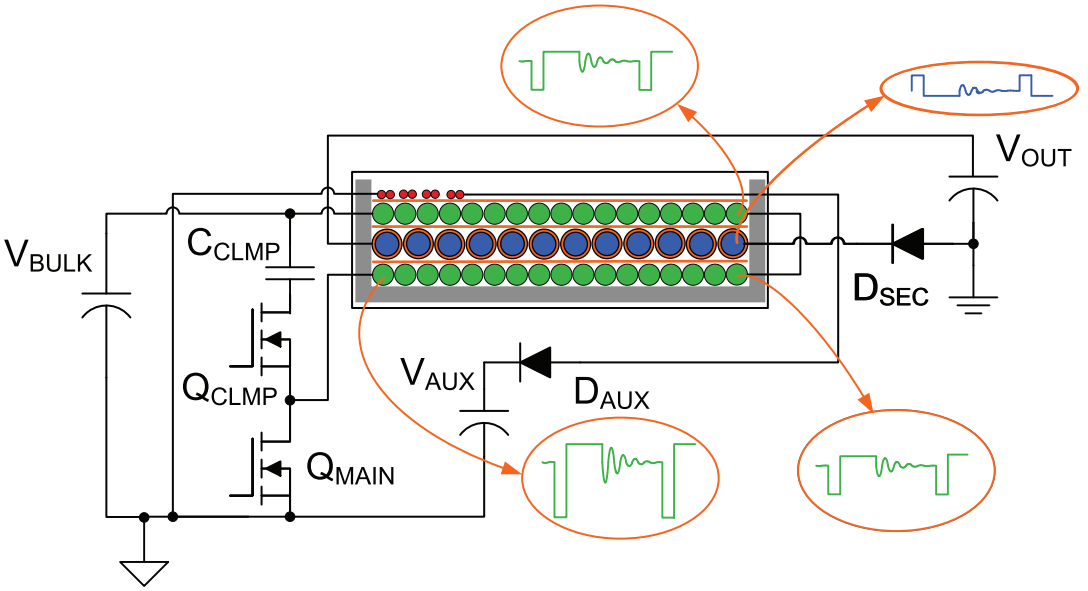


Figure 41 – Initial transformer showing waveforms.

The secondary will see a similar shape as the primary switch-node waveform, scaled down by the primary-to-secondary turns ratio, N_{PS}. However, since the secondary rectifier is placed at the low-side of the secondary winding, the secondary voltage swing will be the inverse polarity compared to the primary.

The parasitic capacitance between each adjacent primary-secondary winding layer pair can be modeled as a lumped capacitor between each layer-pair. The voltage at each terminal of this lumped capacitor will then be equal to the average of the voltage across each winding layer. Thus, the parasitic capacitance between the inner primary and secondary will see a very significant net voltage that will be larger than 75% of the primary V_{PK-PK}, depending on the turns ratio. The inverted secondary polarity (to allow use of a low-side rectifier) increases the net voltage across the parasitic capacitance, slightly worsening CM EMI, whereas a more conventional high-side rectifier deployment would benefit from some degree of inherent CM EMI cancellation (depending on the turns ratio and layer structure).

Similarly, the parasitic capacitance between the outer primary and secondary will see a lesser, but still significant, net voltage that will be larger than 25% of the primary V_{PK-PK}, again depending on the turns ratio.

Overall, considering both the primary-to-secondary interfaces, the average CM injection voltage will be in excess of the full primary switch-node peak-to-peak voltage. This is the initial transformer that was tested, showing the not-unexpected high level of CM noise observed in both the time-domain (Figure 21) and frequency domain (Figure 49).

ii. Improved transformer construction – with cancellation/shield

Many possible shielding and cancellation approaches can be taken to improve the CM performance of the original transformer by using foil shields, actively-driven shields, auxiliary CM cancellation windings or combinations of these. They all have their advantages and disadvantages, so there is often a trade-off to be made between CM-effectiveness, cost and efficiency impact of possible solutions.

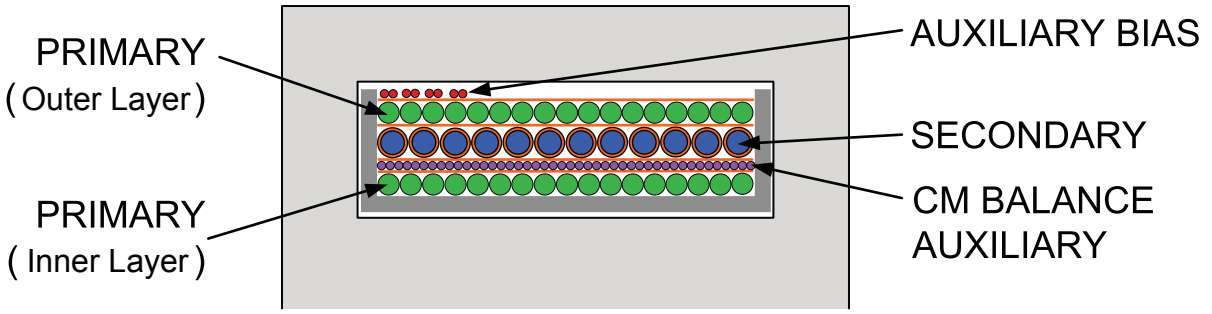


Figure 42 – Improved interleaved transformer internal structure with shielding/cancellation layer.

An example improved internal transformer structure is shown in Figure 42 – this is very similar to the original structure, with an extra auxiliary winding layer (shown in purple) inserted in between the inner primary and the secondary for CM balance. The auxiliary CM balance layer performs two key functions:

- Shielding of the inner half-primary to secondary interface.
- Generating cancelling CM voltage to null the CM injection from the outer half-primary.

The shielding function of the auxiliary CM balance layer is very important – that layer must be implemented with an appropriate number of wire strands and diameter in order to completely fill the full layer width, with no gaps in the winding. That requirement does mean iteration of the wire size/stranding in conjunction with the number of turns in order to make the layer as full as possible. However, once the layer is completely full, it acts as a shield, blocking any CM EMI noise from the inner half-primary, and keeps that noise local to the primary circuit. That simplifies the second function of the auxiliary CM cancellation layer – the remaining CM noise to be cancelled is just the noise that couples from the outer (the less noisy) half-primary to the secondary.

Figure 44 shows the waveforms at each end of the main windings. As outlined above, the inner half-primary is now shielded by the CM cancellation layer, so it should contribute no CM noise to the secondary. The outer half-primary to secondary interface will still contribute the same level of CM current as the original transformer. However, the

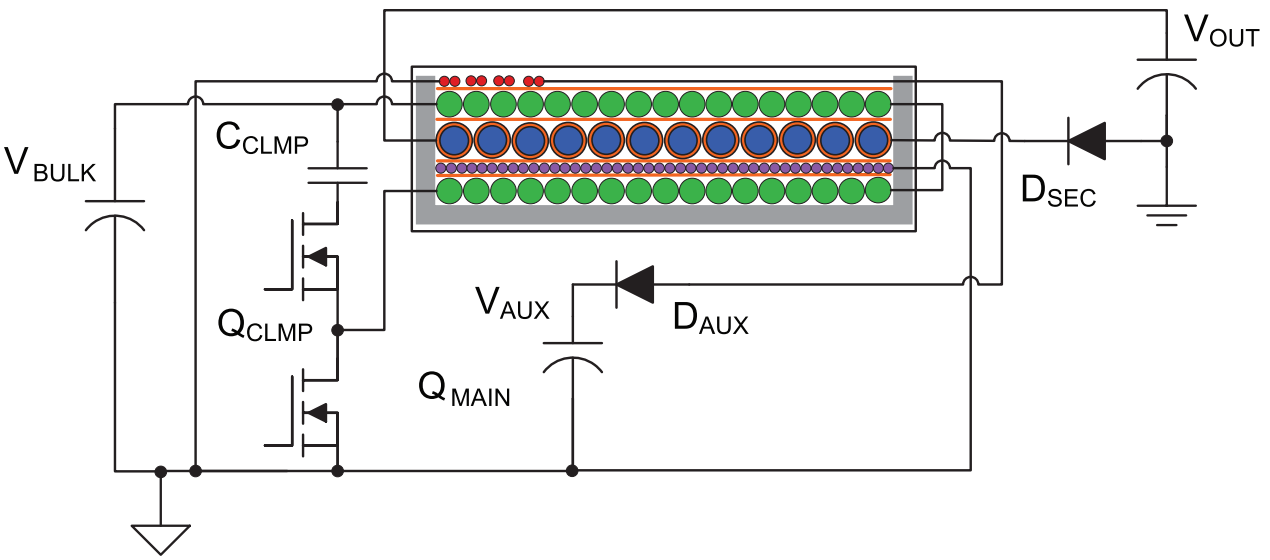


Figure 43 – Improved transformer showing power circuit connections.

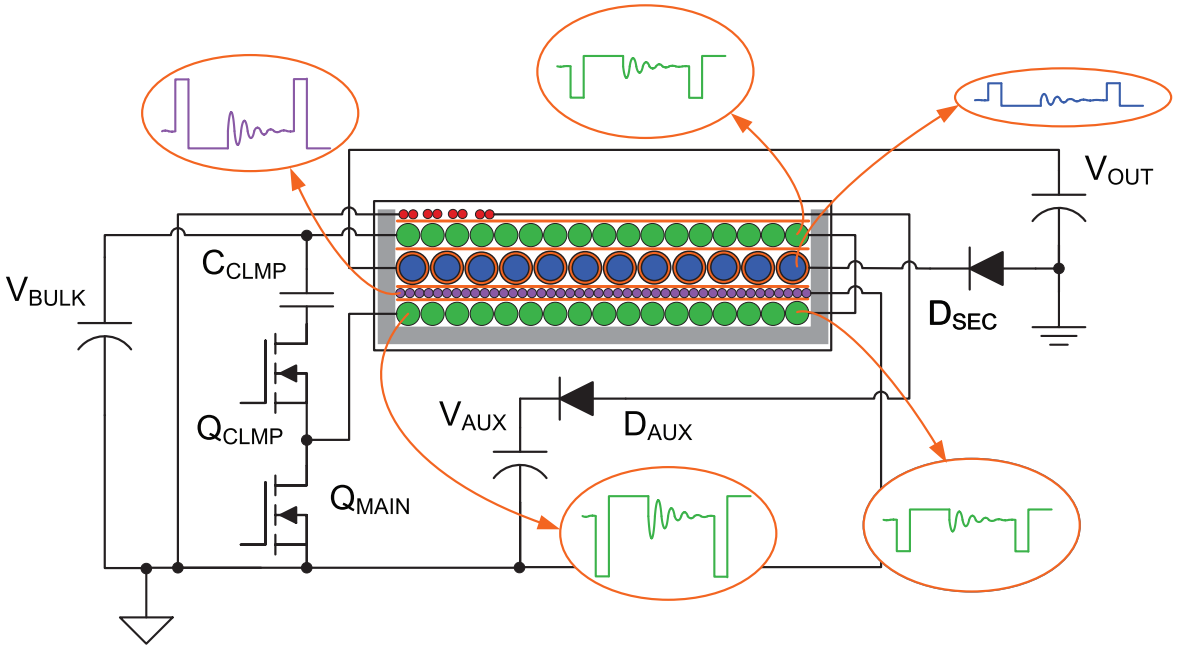


Figure 44 – Improved transformer showing waveforms.

new CM cancellation layer is arranged with the same polarity as the secondary, and with more turns, so that whatever net average voltage appears across the capacitance between the outer half-primary to secondary, a similar amplitude but opposite phase average voltage will appear across the capacitance between the cancellation layer and secondary. Assuming both the parasitic capacitances to the secondary layer are similar (same layer widths and same tape/insulation spacing between layers), the CM current that gets injected into the secondary from the outer half-primary will be nulled or cancelled by an equal amplitude, but opposite phase CM current flowing out of the secondary and into the cancellation layer. The net effect is close to zero CM current flowing into the secondary layer.

The initial or minimum number of turns required in the cancellation layer can be determined from the number of turns in the secondary and outer half-primary layers. In the example of Figure 44, the outer half-primary has 12 T and the secondary has 5 T. Due to the secondary polarity inversion (for the low-side rectifier), there is a net 17 T of CM difference between the layers. The CM cancellation layer needs to achieve at least 17 T net of cancellation, so it needs a minimum of 22 T [17 T – (– 5 T)]. In practice, due to other CM coupling paths and imperfections in the shielding effectiveness of the CM cancellation layer, the CM cancellation layer will require more turns than this minimum – it is difficult to predict since it depends on every individual design and PCB layout. For example, in this case of the PMP21479 [1], it was determined empirically through trial and error that 32 T were required in the cancellation layer.

There are some points to note about the addition of the CM cancellation layer. Firstly, it does increase the leakage inductance by increasing the primary-secondary separation. In this example, the leakage inductance increased by approximately 10%, from ~1.7 µH to ~1.85 µH. This increase is not that significant, especially since the ACF topology does not dissipate the leakage energy but instead recycles it to the output.

Secondly, since the CM cancellation layer sits in between the primary-secondary, in a high-field region, it can have large induced eddy current loss. It's important to use the smallest possible wire diameter in the cancellation layer, with several parallel strands to fill the layer width – this reduces the magnitude of the induced eddy currents, lowering the eddy current loss.

VII. Transformer Housekeeping and Best Practices

There are a number of useful tips to keep in mind, to minimize the EMI issues caused by the power stage transformer.

A. No Outer-Leg Air-Gaps

As recommended in [3], transformer outer-leg air-gaps should never be used. As shown in Figure 45, there will be a significant stray field from the outer leg air-gaps. This will cause major EMI issues due to the stray field coupling to other circuit nodes and possibly bypassing the EMI filter. It's always much better for EMI noise to keep to center-leg gaps only – this minimizes stray field coupling, since the transformer windings shield the field from the center-leg air-gap.

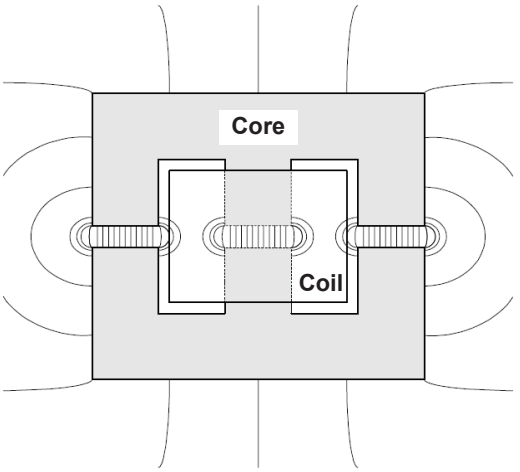


Figure 45 – Transformer stray field from outer-leg air-gaps.

B. Transformer Flux-Banding

Also as recommended in [3], adding a transformer "flux-band" (or sometimes called "flux strap" or "belly band"), like that shown in Figure 46, can significantly reduce the EMI due to stray magnetic fields. In addition, by connecting the flux-band to the local primary ground as shown, the ferrite core itself is also then grounded. There can be significant CM noise coupled to the core itself from the internal windings and, since the core has a very large surface area, it will have significant parasitic capacitance to EARTH and to other circuit nodes. If it is left floating, it can also couple to the CM EMI.

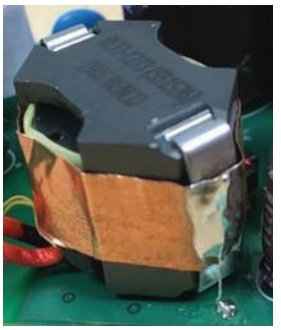


Figure 46 – Transformer grounded flux-band to reduce stray magnetic field.

Figure 47 shows the conducted EMI benefit measured on the PMP21479 [1] ACF reference design, of adding a grounded flux-band and EMI shield, versus a transformer with no flux-band or shield, and a floating ferrite core. The benefit, in the range 0.15 to 10 MHz, is very significant, with a 15 dB reduction seen at some switching harmonics.

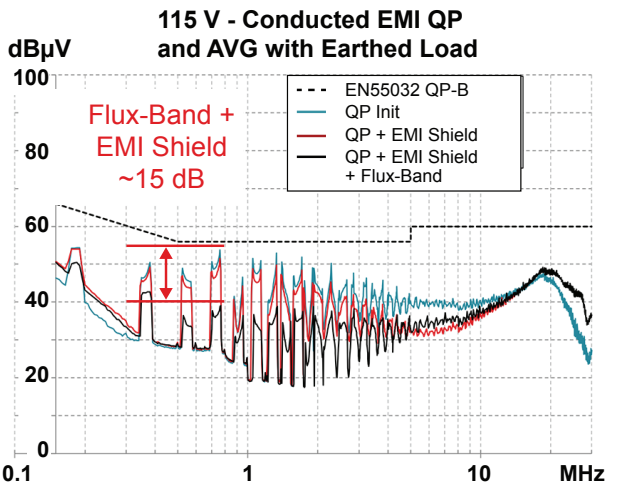


Figure 47 – Measured EMI benefit of added transformer grounded flux-band vs only EMI filter shield and vs neither shield (initial scan).

C. Other Transformer Best Practices

Interleaving the primary and secondary layers in flyback transformers is often done because the loss savings from the reduction in leakage inductance is very beneficial. However, interleaving does increase the number of primary-to-secondary layer interfaces, and thus will increase the effective primary-secondary CM capacitance. This will usually increase the level of CM noise, requiring more CM filtering, or extra CM balance mitigation

may be required. However, the internal layer structure and winding layer arrangements should always be examined for ways to minimize the effective CM voltage between layers to improve the inherent CM performance of the structure. Many internal layer structures are possible that will deliver equivalent electrical performance in terms of magnetizing inductance, turns ratio and even leakage inductance, but they may deliver very different CM performance. It's always recommended to examine the internal layer structure and work with the transformer vendor/ manufacturer to understand the internal structure and consider its CM performance.

VIII. Design Example – 65 W Active Clamp Flyback USB PD Adapter

A 65 W active clamp flyback USB-C Power Delivery (PD) reference design, PMP21479 [1], was used to illustrate the effectiveness of transformer CM cancellation, the impact of EMI filter parasitics and PCB layout effects. The initial prototype design is shown in Figure 48. The corresponding time-domain CM performance is shown in Figure 21 and the frequency-domain conducted EMI in Figure 49. As can be seen, both results indicate poor EMI performance, with the fundamental switching frequency component almost 100 dBµV, more than 30 dB over the limit. An improvement of ~40 dB is required to get below the limit with good pass margin.

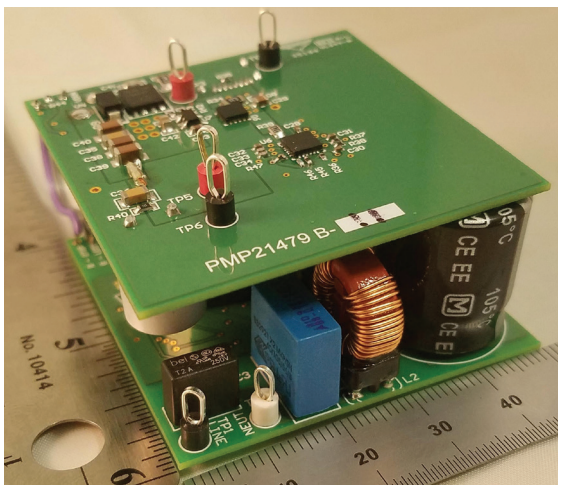


Figure 48 – Initial 65 W adapter design using two-board "sandwich" construction.

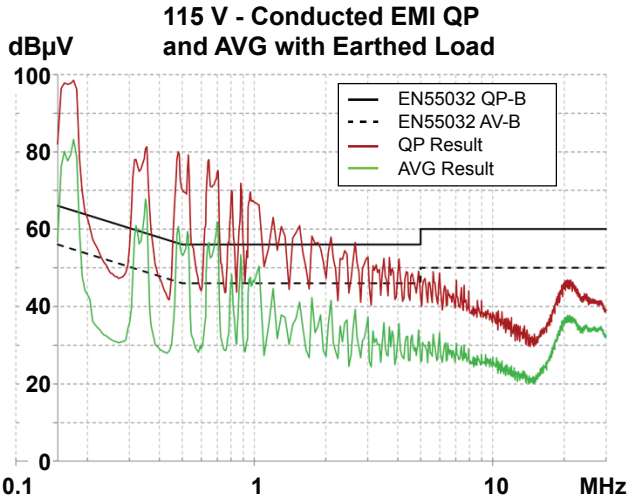


Figure 49 – Initial EMI result for two-board "sandwich" construction.

Five main areas of the design were addressed and improved:

- Transformer internal CM cancellation layer added (as described in Section VI.A.ii)
- Addition of a grounded flux-band around the transformer (per Figure 46)
- Change the CM filter choke to a bifilar-wound type (per Figure 37)
- Add copper shield over the noisy primary switch-node, folded through the PCB slot to also shield the EMI filter from the power stage (per Figure 26 and Figure 27)
- Two-board sandwich in Figure 48 changed to revised structure shown in Figure 50 – to move the output cap and secondary-side components away from the AC input pins, and minimize EMI filter bypass.

Overall, these changes resulted in 48 dB improvement at the fundamental switching frequency at low line, giving the required pass result with very good margin.

The final conducted EMI results at low-line (115 V_{RMS}) and high-line (230 V_{RMS}) are shown in Figure 51 and Figure 52, respectively.

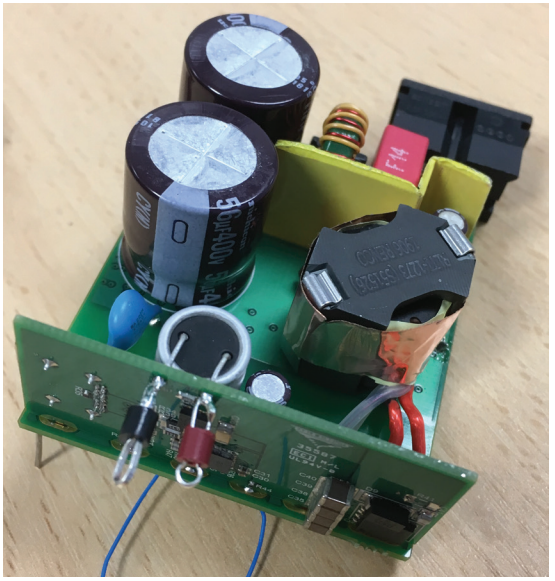


Figure 50 – Final PMP21479 65-W adapter design.

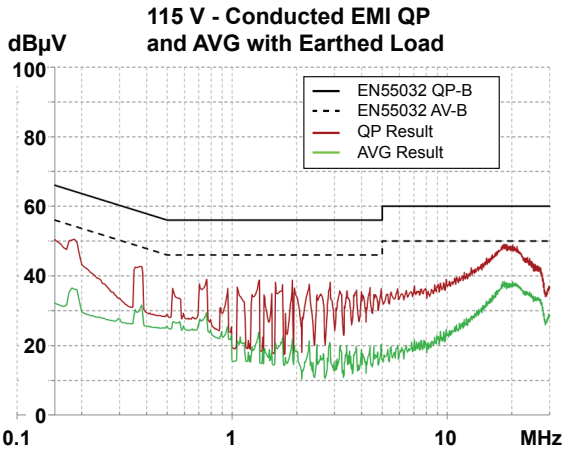


Figure 51 – Final EMI result for improved construction – 115 V.

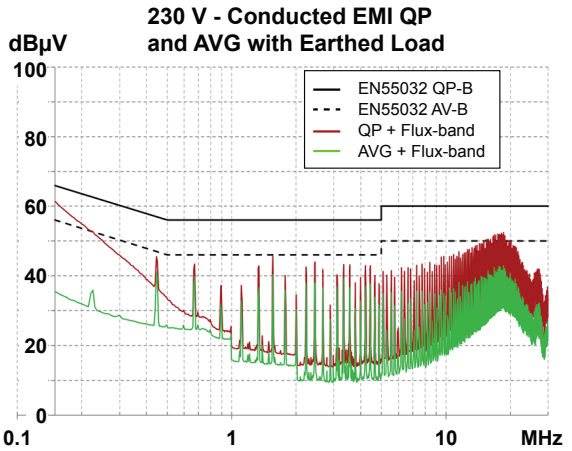


Figure 52 – Final EMI result for improved construction – 230 V.

IX. Summary

As this paper has shown, EMI has to be considered as part of any power supply design from the start. It cannot always be easily solved at the end of the design process, after everything else is already addressed. Typically, an "EMI last" approach would lead to a more costly and bulky EMI solution (if a solution is possible), with high risk that other previously passing requirements could fail after all EMI fixes are in place – especially efficiency performance.

In the 65 W design example, it was shown how some design choices, such as the location and proximity of the EMI filter to the transformer and the initial 2-board sandwich construction, caused much of the EMI issues to begin with. This paper also showed how simple steps to shield the EMI filter and flux-band and shield the transformer led to significant improvement, with incremental cost increase and little or no impact on efficiency performance.

Finally, the transformer is the most important component for an isolated AC/DC power supply, in terms of the CM EMI performance in particular. The 65 W example showed how a small change to the structure, to add a shielding/cancellation layer, dramatically improved the CM performance. Taken together, the total design changes on the 65 W example improved EMI by almost 50 dB at some frequencies, resulting in a design that passes with good margin, with little impact on efficiency or cost.

ACKNOWLEDGEMENTS

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