Power Factor Correction (PFC) Circuit Basics

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Power Factor Correction (PFC) Circuit Basics

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Objectives & agenda

• **Introduction**
  – What is power factor correction (PFC)?
  – Why is it needed?
  – How is it measured?

• **Overview**
  – Critical conduction mode (CrCM)
    • Compensation
    • Feed-forward
    • Sources of distortion
  – Continuous conduction mode (CCM)
  – Interleaved
  – Bridgeless
Regional power quality requirements
What is power factor and why should I care?

- Laptop ~ 60 W
- USA > 3.2 TW

\[ \text{PF} = 0.40 \]
\[ \text{PF} = 0.99 \]
How is the “PF” measured & regulated?

\[ THD = \sqrt{\sum_{n=2}^{\infty} \frac{i_n^2}{I_1}} \]

\[ PF = \frac{\cos(\varphi)}{\sqrt{1 + THD}} \]
How is it done?

- Boost
- Flyback
- Sepic
- Buck
- Passive solutions

**Benefits**
- Achieve unity PF
- Regulated output
- Energy hold up
- Universal input

**Solutions include**

- Power Factor: 0.69
- Power Factor: 1.00

**Diagram**

- PFC
- DC/DC
The boost converter

\[ \frac{V_{OUT}}{V_{IN}} = \frac{1}{1 - D} \]
The CrCM PFC

- Constant ON-time
  - \( I_{L(AVG)} = \frac{V_{IN}}{2L} t_{ON} \)
- Operates on the boundary between DCM and CCM
- Huge switching frequency variation
- Zero current switching for boost diode, no reverse recovery
The CrCM PFC

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DCM & valley switching
DCM & valley switching
Valley switching impact on $f_s$
Distortion

Valley = 0
$\text{PF} = 0.9945$, $\text{THD} = 23.4\%$

$\text{VIN} \text{ (RMS)} = 240 \text{ V}$, $\text{P_OUT} = 265 \text{ W}$

Valley = 1
$\text{PF} = 0.9990$, $\text{THD} = 15.6\%$

$\text{VIN} \text{ (RMS)} = 240 \text{ V}$, $\text{P_OUT} = 265 \text{ W}$

Valley = 2
$\text{PF} = 0.9992$, $\text{THD} = 17.6\%$

$\text{VIN} \text{ (RMS)} = 240 \text{ V}$, $\text{P_OUT} = 265 \text{ W}$
Compensation

- Feed-forward power delivery independent of line voltage
  - One compensation parameter set works for very wide input voltage range

- Trade-off
  - Good PF requires a slow control loop (<10 Hz typical)
  - Good transient response requires fast control loop
  - Non-linear error amplifier gain helps address transient response performance
Putting it all together – CrCM
CrCM wrap up – Low solution $, <300 W

- Simple implementation

- Valley switched
  - Low $C_{OSS}$ loss at MOSFET turn-on

- No reverse recovery
  - Able to use lower cost ultra-fast diode

- Inductor current ripple is large (200%)
  - Larger RMS currents
  - Larger core loss in inductor

- Good PF, mediocre THD
  - THD can be improved using more complex approaches
CCM PFC operation

- Converter operates at a fixed switching frequency, duty-cycle now a function of instantaneous line voltage
- Much smaller current ripple than CrCM but no longer valley switched
- Non-ZCS switching for boost diode, good $Q_{RR}$ performance needed
- Capable of delivering a lot more power
CCM PFC operation

- Converter operates at a fixed switching frequency, duty-cycle now a function of instantaneous line voltage
- Much smaller current ripple than CrCM but no longer valley switched
- Non-ZCS switching for boost diode, good $Q_{RR}$ performance needed
- Capable of delivering a lot more power
The CCM PFC
CCM wrap up – Better PF/THD, >300 W

• Fixed frequency with limited inductor current ripple
  – Smaller RMS currents
  – Smaller conduction losses than CrCM
  – Lower cost core material

• Hard switching for both boost MOSFET and boost diode
  – Higher switching losses than CrCM
  – Good $Q_{RR}$ performance is essential
  – SiC diode often used

• More complex control scheme
  – Slow voltage loop, fast current loop
  – Most modern CCM PFC controllers will simplify complexity for the end user
Interleaved PFC

- Two converters operated 180° out of phase
- Works with CrCM or CCM types
- Ripple cancellation at 50% duty-cycle

![Diagram of Interleaved PFC](image)

Note: Time base in zoomed plots is relative to 2.5 ms.
Interleaved PFC

- Two converters operated 180° out of phase
- Works with CrCM or CCM types
- Ripple cancellation at 50% duty-cycle
When to consider interleaving

• Power loss distributed between two power stages
  – Improved thermal management
  – More component choices

• Power density
  – Reduced z-height at the expense of x/y space

• Lower input and output current ripple
  – EMI filter may be physically smaller
I want bridgeless, can I do this?
Bridgeless PFC

Semi-Bridgeless
- Advantages
  - Simple control
  - Ground referenced gate drive
- Disadvantages
  - 2 power stages
  - 6 semiconductors
  - Poor core utilization

AC Switch
- Advantages
  - Lowest ON-state conduction
  - Balanced EMI
- Disadvantages
  - Isolated drive
  - Current sense
  - 6 semiconductors

Totem Pole
- Advantages
  - Minimum components
  - Good efficiency
- Disadvantages
  - Complex
  - High side drive
  - Current sense
  - Common mode
  - Reverse recovery
Selecting the right PFC topology: Output power

- How does output power influence decision?
- Peak inductor current comparison at 500 W
  - Single phase CCM: 8.84 A
  - Single phase CrCM: 17.49 A
Selecting the right PFC topology: Interleaved CrCM vs single phase CCM

<table>
<thead>
<tr>
<th>Design Characteristics</th>
<th>Interleaved CrCM</th>
<th>Single Phase CCM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Component stress</td>
<td>Conduction loss split between two power stages, valley switched</td>
<td>Single power stage, hard switched</td>
</tr>
<tr>
<td>Power density</td>
<td>Lower</td>
<td>Higher</td>
</tr>
<tr>
<td>Height</td>
<td>Smaller overall component height</td>
<td>Single inductor, larger heatsinks</td>
</tr>
<tr>
<td>Thermal management</td>
<td>Power dissipation spread over greater X/Y space</td>
<td>More challenging</td>
</tr>
<tr>
<td>Complexity</td>
<td>High power stage component count</td>
<td>Single power stage</td>
</tr>
<tr>
<td>Cost</td>
<td>Higher</td>
<td>Lower</td>
</tr>
</tbody>
</table>
Selecting the right PFC topology: EMI comparison

- **Critical conduction mode**
  - Inductor current ripple is 200%, requires physically larger EMI filter
  - Variable frequency – noise less concentrated in one frequency

- **Continuous conduction mode**
  - Physically smaller filter but fixed frequency

- **Interleaved**
  - Ripple current cancellation allows for physically smaller EMI filter

- **Bridgeless**
  - Common mode challenging for some variations
Topology selection exercise

Design specification
- Laptop adaptor
- USB-C, 100 W output
- 100 VAC to 240 VAC input
- Smallest form factor critical

TIDA-01623
- Single phase CrCM PFC + active clamp flyback
- Form factor: 70 mm × 42 mm × 16.5 mm
- 93.4% efficiency end-to-end at full load
Topology selection exercise

Design specification
- Class-D audio amplifier
- 90 $V_{AC}$ to 265 $V_{AC}$ input
- 200 W continuous, 750 W peak
- Small solution size preferable (length, width and height)

TIDA-00776
- Single phase CCM PFC + 2-switch forward
- Form factor: 88 mm x 173 mm x 35 mm
- http://www.ti.com/tool/PMP30183
Topology selection exercise

Design specification
- OLED TV
- 85 \( V_{AC} \) to 265 \( V_{AC} \) input
- Peak output power: 480 W
- AC/DC supply embedded within panel: thin profile needed

TIDA-01495
- Interleaved CrCM PFC + half-bridge LLC
- <17 mm height
Summary

• Overall
  – Huge benefit to infrastructure
  – Regional regulatory requirements

• Control method impacts power stage behavior
  – Conduction losses
  – Switching losses
  – Switching frequency profile

• PFC solution considerations
  – Output power capability
  – Size
  – Complexity vs performance
BACKUP
Interleaved PFC

Current Ripple Cancellation

Normalized Ripple Current

Duty Cycle
Benefits of active PFC

- **Output of PFC is a regulated voltage**
  - Easier design of isolated DC/DC stage

- **PFC can easily handle wide input voltage range**
  - One design able to support different line voltages around the world (115 V for US, 230 V for EU, 100 V for Japan, etc.)

- **PFC output capacitance provides holdup time when AC is disconnected**
  - Allows for a controlled shutdown sequence
Valley switching

0\textsuperscript{th} Valley

1\textsuperscript{st} Valley

2\textsuperscript{nd} Valley

\[ t_{ON} \quad t_{OFF} \quad t_{ON} \quad t_{OFF} \]

\[ t_{ON} \quad t_{OFF} \quad t_{ON} \quad t_{OFF} \]

\[ t_{ON} \quad t_{OFF} \quad t_{ON} \quad t_{OFF} \]
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