Power Supply Design Seminar

Power Factor Correction (PFC) Circuit Basics

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Power Seminar topics and online power training modules are available at: ti.com/psds

Texas Instruments

Power Factor Correction (PFC) Circuit Basics

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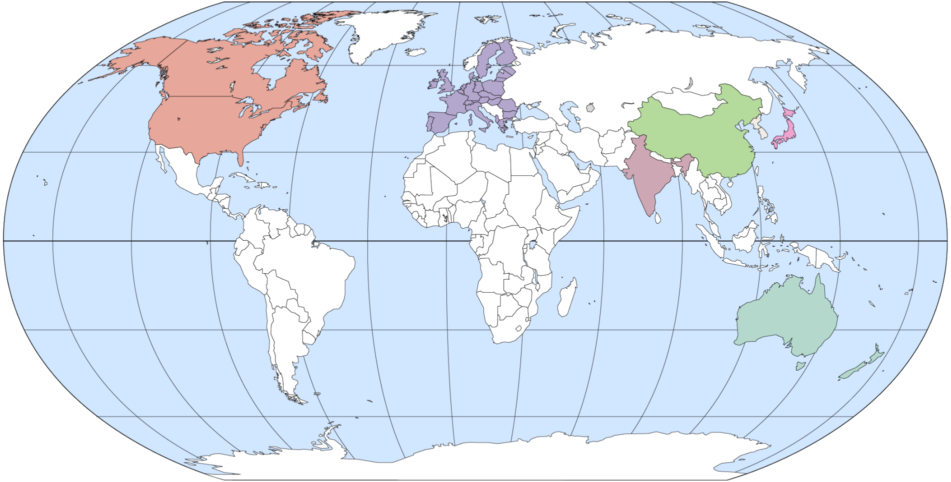
Objectives & agenda

- **Introduction**
  - What is power factor correction (PFC)?
  - Why is it needed?
  - How is it measured?
- **Overview**
  - Critical conduction mode (CrCM)
    - Compensation
    - Feed-forward
    - Sources of distortion
  - Continuous conduction mode (CCM)
  - Interleaved
  - Bridgeless

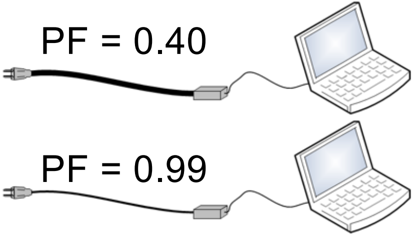
Regional power quality requirements

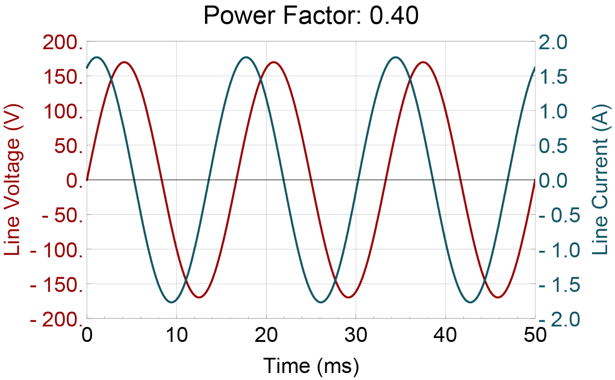


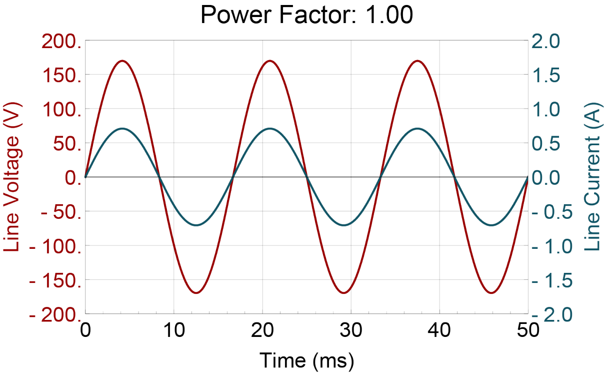
European Union, EN61000-3-2
US/Canada, IEC61000-3-2, Energy Star
China, GB/T 14549-93
Japan, JIS 61000-3-2
Australia/New Zealand, AS/NZS 61000.3.2
India, IS 14700-3-2
Korea, K6100-3-2

What is power factor and why should I care?

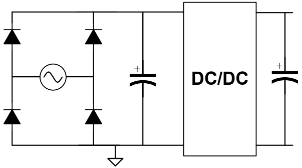
- Laptop ~ 60 W
- USA > 3.2 TW

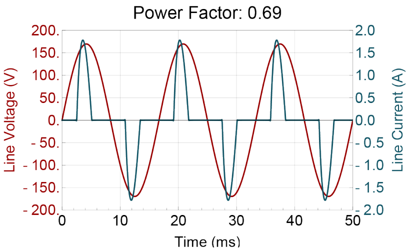


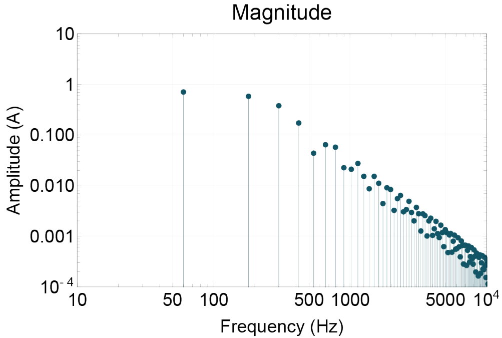


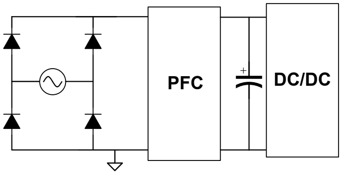


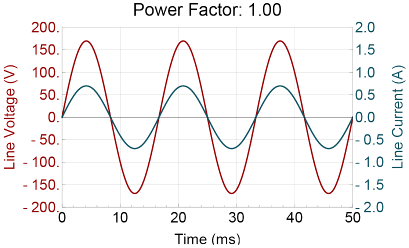
How is the “PF” measured & regulated?

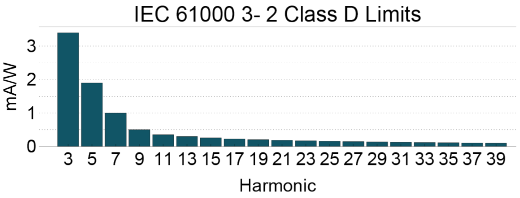






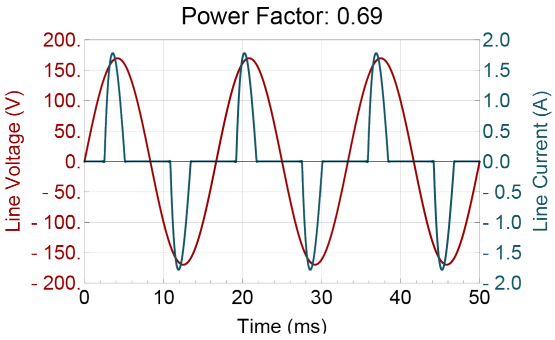






$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1} \qquad PF = \frac{\cos(\varphi)}{\sqrt{1 + THD}}$$

How is it done?



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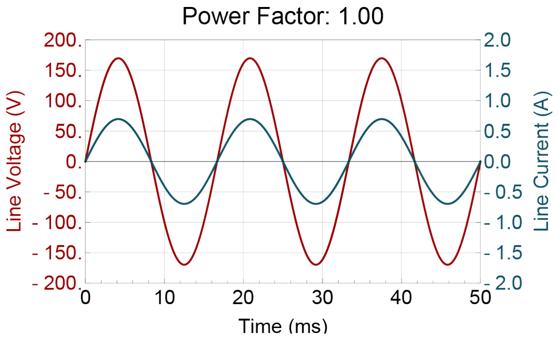
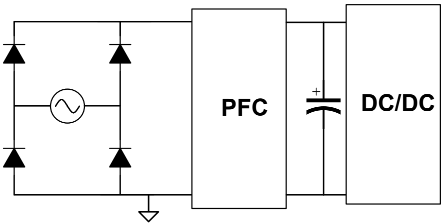




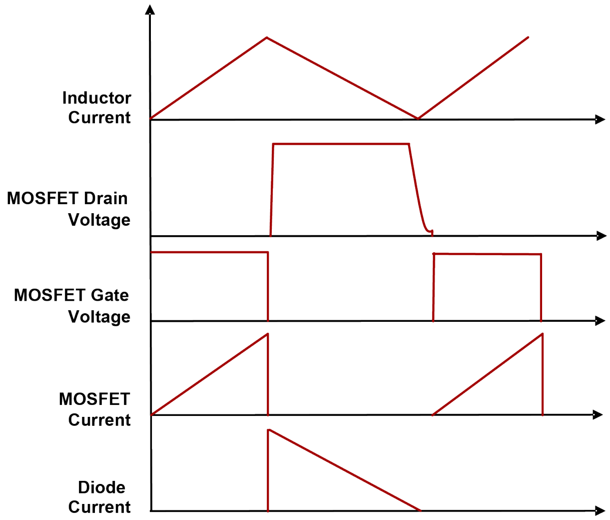
Solutions include

- Boost
- Flyback
- Sepic
- Buck
- Passive solutions

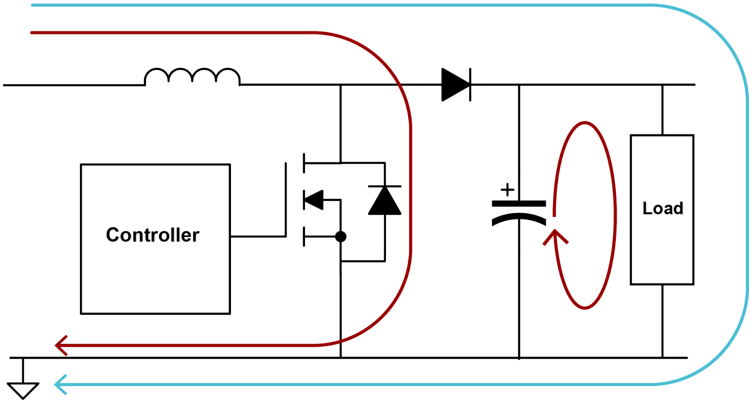
Benefits

- Achieve unity PF
- Regulated output
- Energy hold up
- Universal input

The boost converter

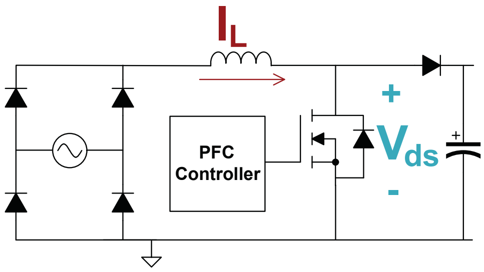


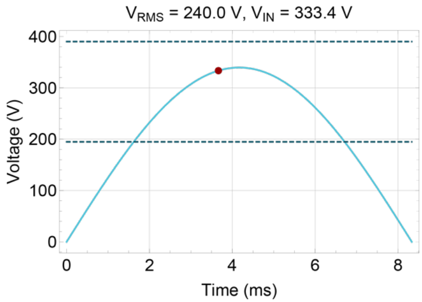
$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1-D}$$

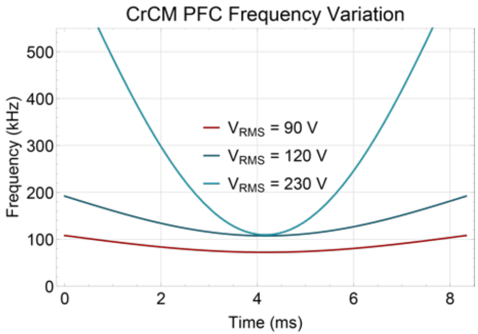


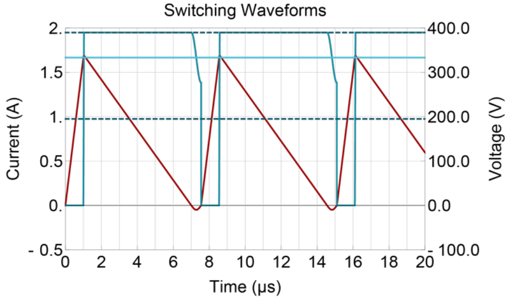
The CrCM PFC

- Constant ON-time
  - $I_{L(AVG)} = \frac{V_{IN}}{2L} t_{ON}$
- Operates on the boundary between DCM and CCM
- Huge switching frequency variation
- Zero current switching for boost diode, no reverse recovery









Note: Time base in zoomed plots is relative to: 3.7 ms.

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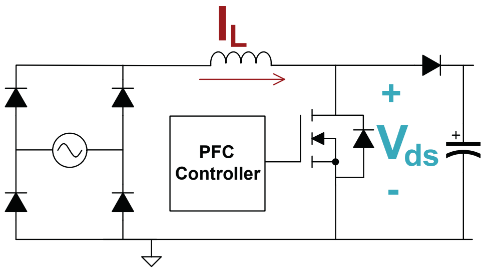
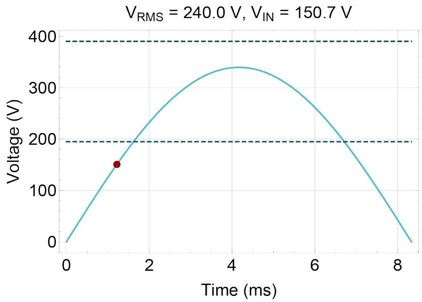
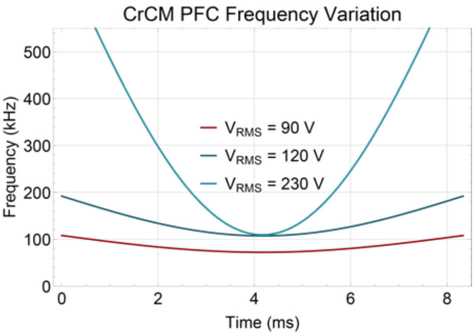
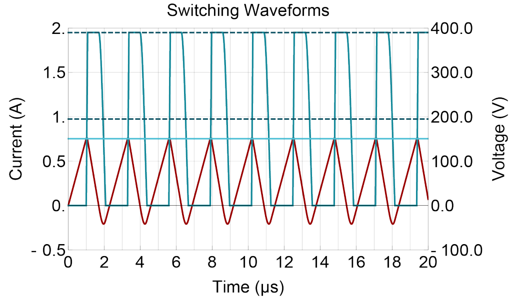


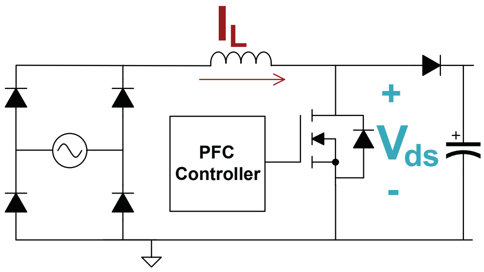


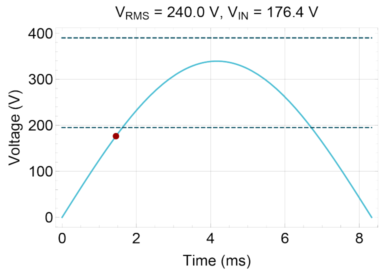


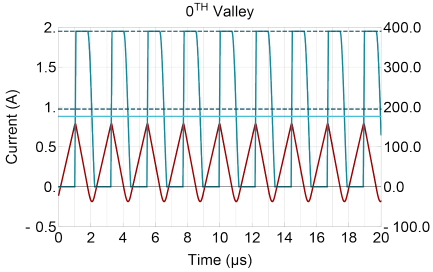


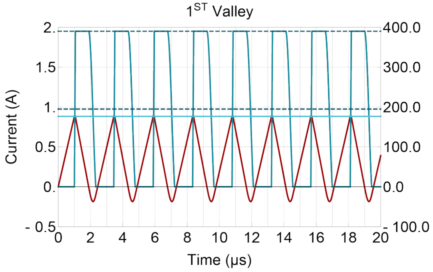
Note: Time base in zoomed plots is relative to: 1.2 ms.

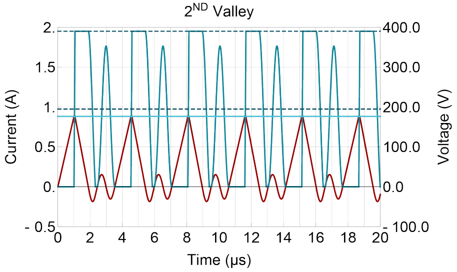
DCM & valley switching



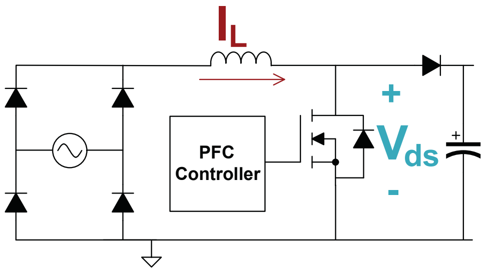


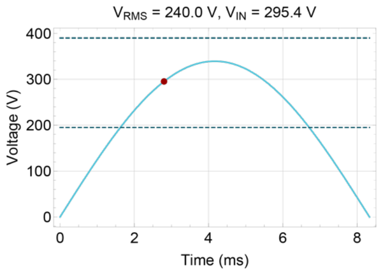


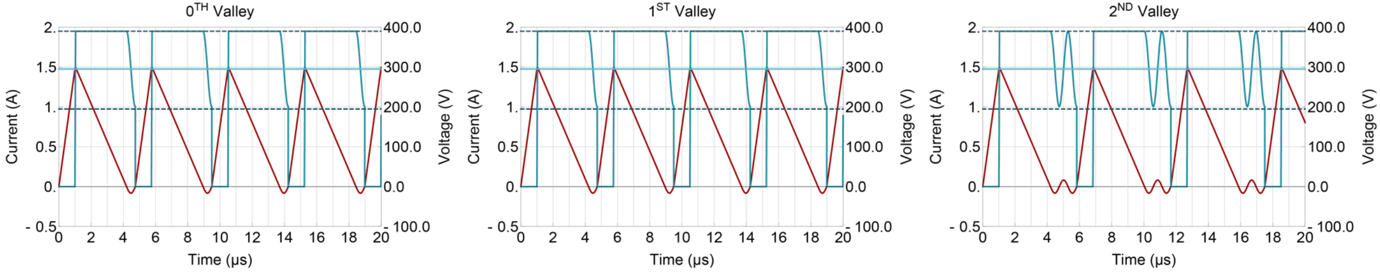




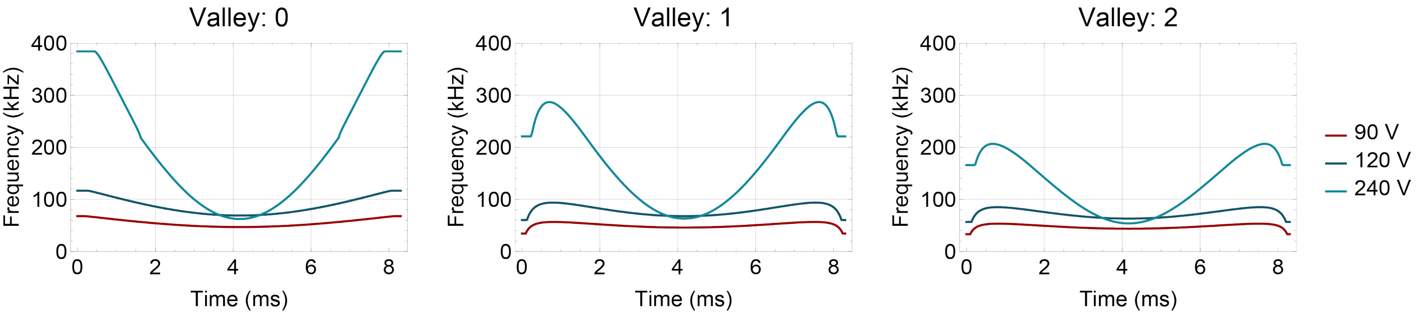
DCM & valley switching



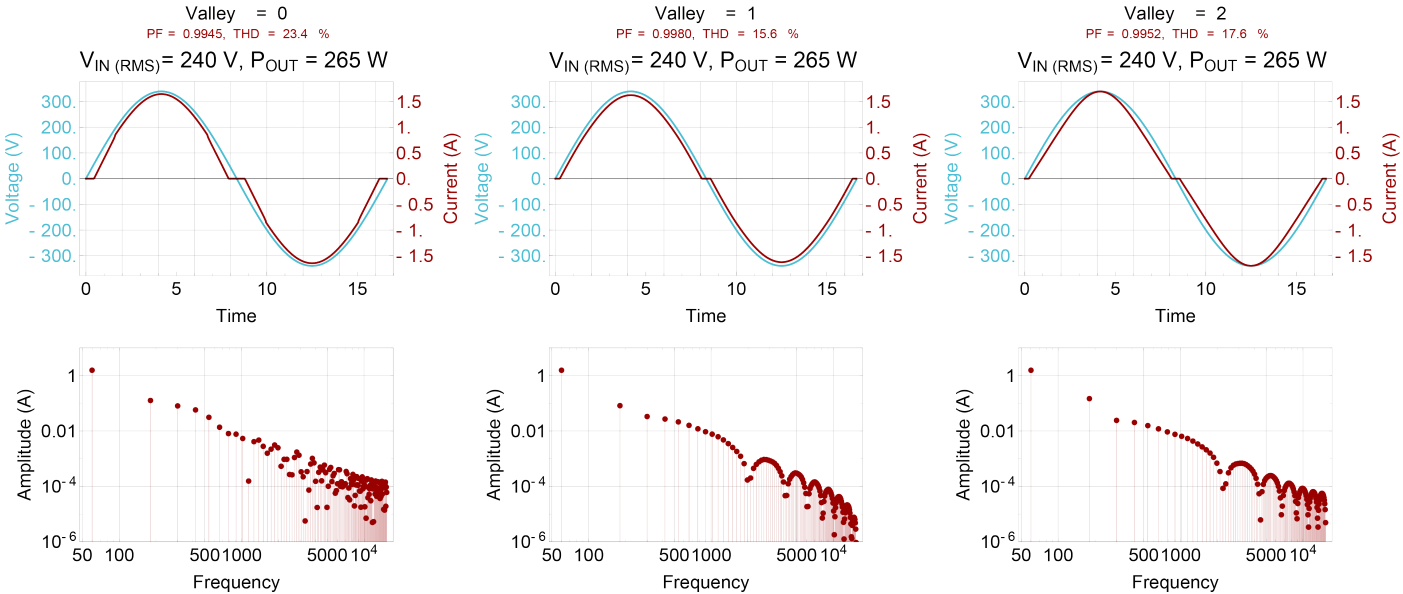




Valley switching impact on f_s

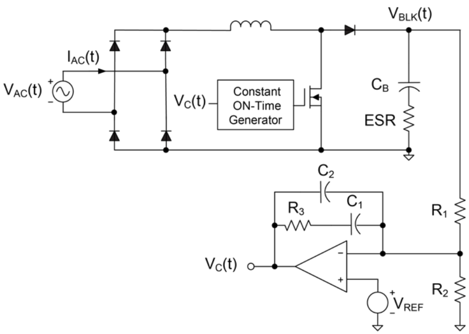


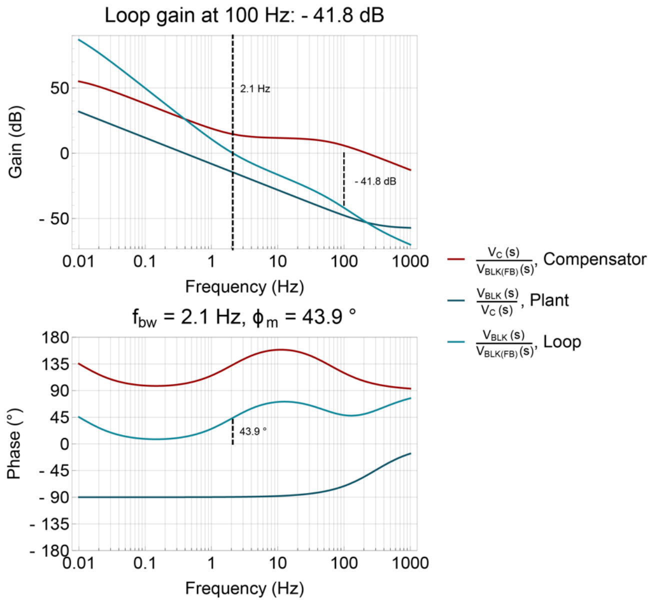
Distortion



Valley = 0
PF = 0.9945, THD = 23.4 %
$V_{IN\ (RMS)}$ = 240 V, P_{OUT} = 265 W
Valley = 1
PF = 0.9980, THD = 15.6 %
$V_{IN\ (RMS)}$ = 240 V, P_{OUT} = 265 W
Valley = 2
PF = 0.9952, THD = 17.6 %
$V_{IN\ (RMS)}$ = 240 V, P_{OUT} = 265 W
Voltage (V)
Current (A)
Time
Amplitude (A)
Frequency

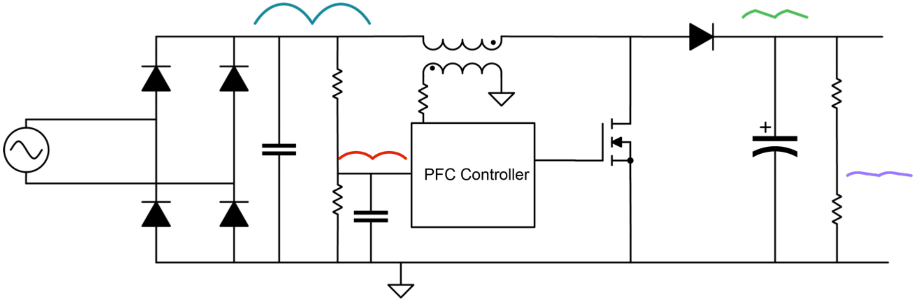
Compensation

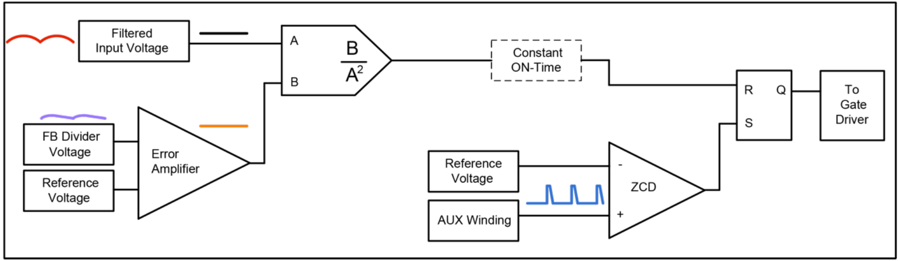




- Feed-forward power delivery independent of line voltage
  - One compensation parameter set works for very wide input voltage range
- Trade-off
  - Good PF requires a slow control loop (<10 Hz typical)
  - Good transient response requires fast control loop
  - Non-linear error amplifier gain helps address transient response performance

Putting it all together – CrCM

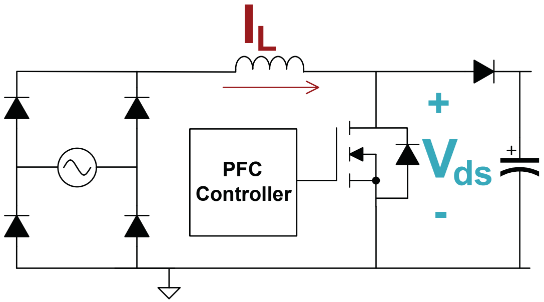


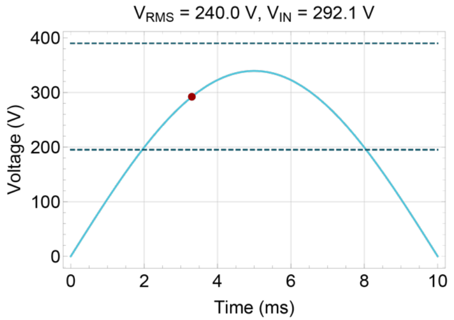


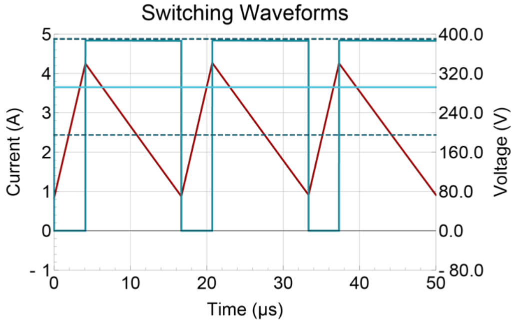
CrCM wrap up – Low solution $, <300 W

- **Simple implementation**
- **Valley switched**
  - Low C_{OSS} loss at MOSFET turn-on
- **No reverse recovery**
  - Able to use lower cost ultra-fast diode
- **Inductor current ripple is large (200%)**
  - Larger RMS currents
  - Larger core loss in inductor
- **Good PF, mediocre THD**
  - THD can be improved using more complex approaches

CCM PFC operation



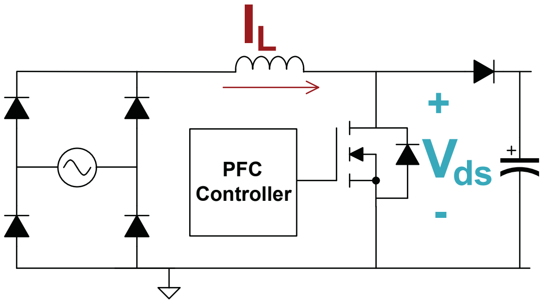


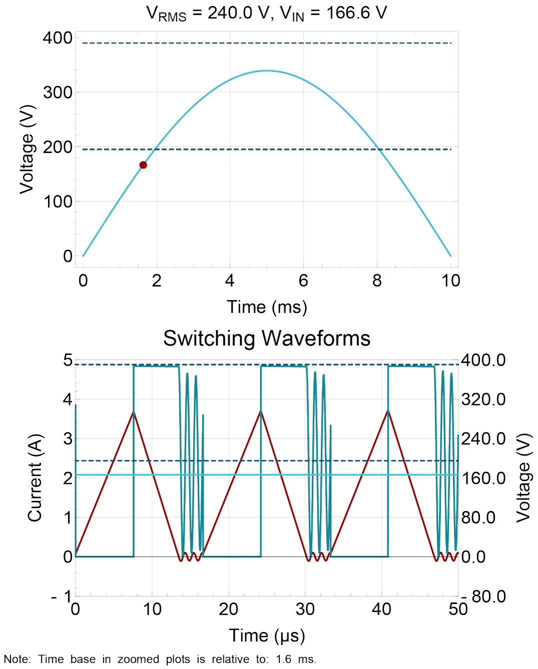


Note: Time base in zoomed plots is relative to: 3.3 ms.

- Converter operates at a fixed switching frequency, duty-cycle now a function of instantaneous line voltage
- Much smaller current ripple than CrCM but no longer valley switched
- Non-ZCS switching for boost diode, good Q_{RR} performance needed
- Capable of delivering a lot more power

CCM PFC operation





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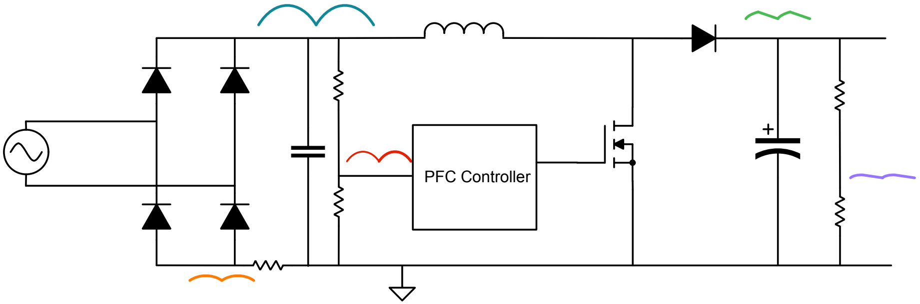
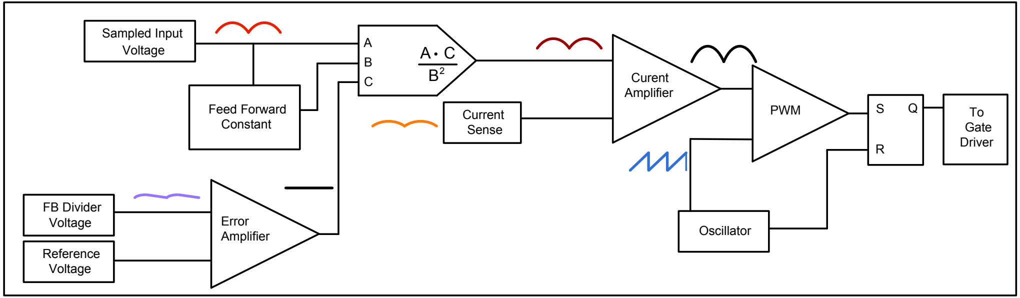
The CCM PFC

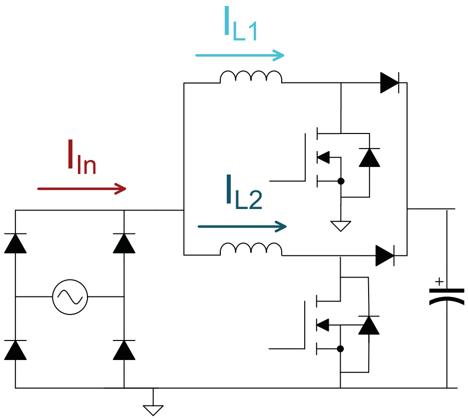

PFC Controller


Sampled Input Voltage
Feed Forward Constant
A
B
C
A • C
B2
Curent Amplifier
Current Sense
PWM
S
Q
R
To Gate Driver
Oscillator
FB Divider Voltage
Reference Voltage
Error Amplifier

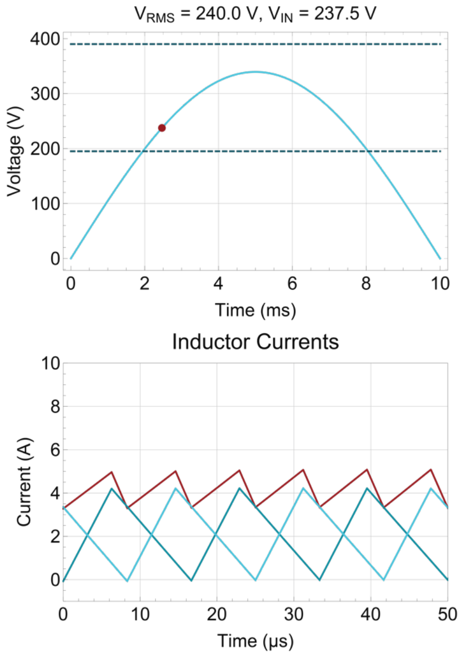
CCM wrap up – Better PF/THD, >300 W

- **Fixed frequency with limited inductor current ripple**
  - Smaller RMS currents
  - Smaller conduction losses than CrCM
  - Lower cost core material
- **Hard switching for both boost MOSFET and boost diode**
  - Higher switching losses than CrCM
  - Good Q_{RR} performance is essential
  - SiC diode often used
- **More complex control scheme**
  - Slow voltage loop, fast current loop
  - Most modern CCM PFC controllers will simplify complexity for the end user

Interleaved PFC

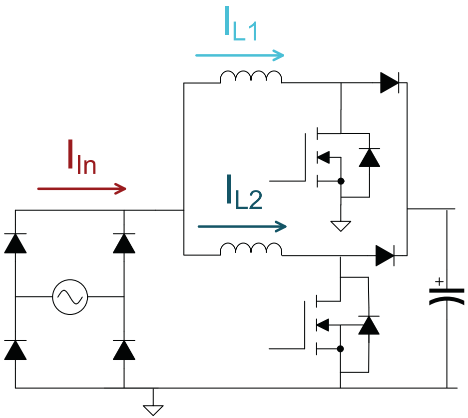


- Two converters operated 180° out of phase
- Works with CrCM or CCM types
- Ripple cancellation at 50% duty-cycle



Note: Time base in zoomed plots is relative to: 2.5 ms.

Interleaved PFC



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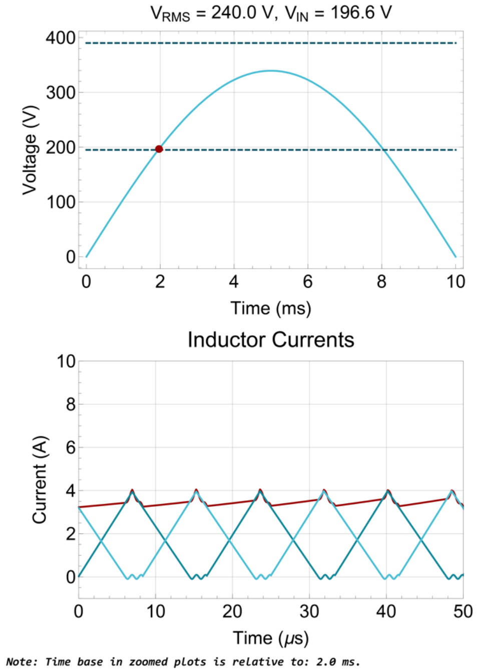
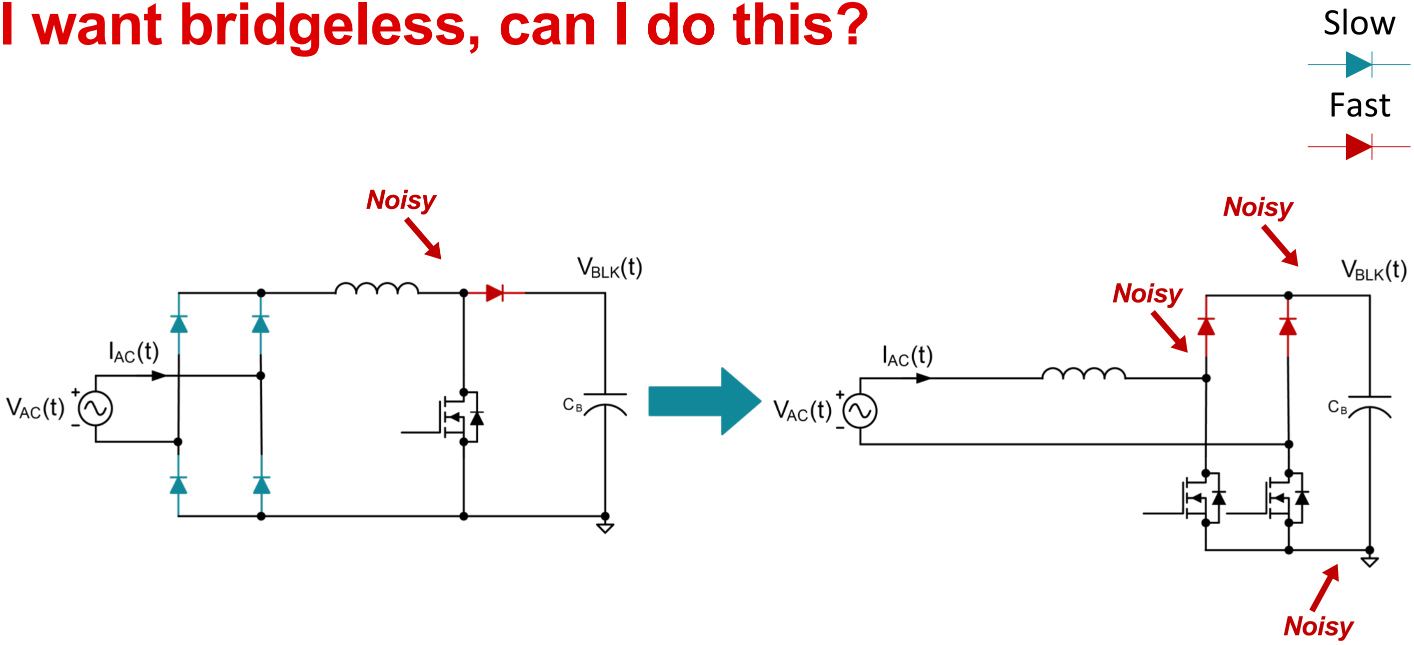


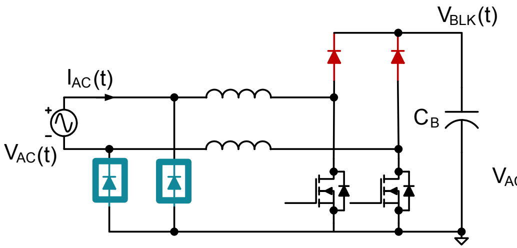
When to consider interleaving

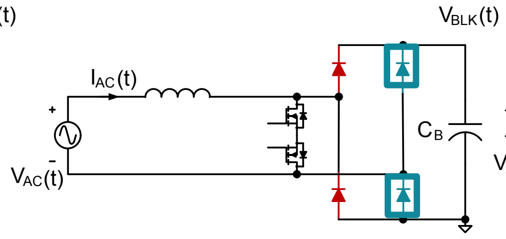
- **Power loss distributed between two power stages**
  - Improved thermal management
  - More component choices
- **Power density**
  - Reduced z-height at the expense of x/y space
- **Lower input and output current ripple**
  - EMI filter may be physically smaller

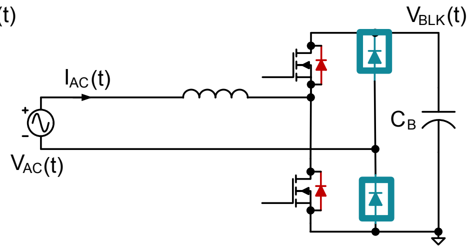
I want bridgeless, can I do this?



Bridgeless PFC







Semi-Bridgeless

- Advantages
  - Simple control
  - Ground referenced gate drive
- Disadvantages
  - 2 power stages
  - 6 semiconductors
  - Poor core utilization

AC Switch

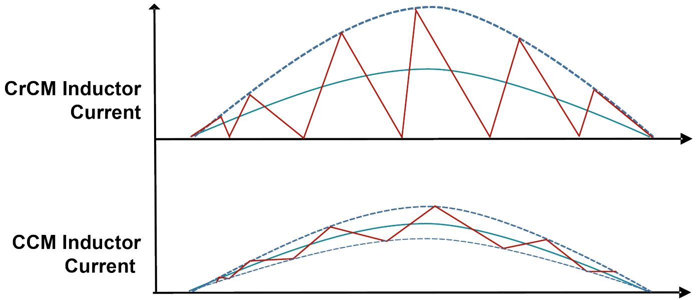
- Advantages
  - Lowest ON-state conduction
  - Balanced EMI
- Disadvantages
  - Isolated drive
  - Current sense
  - 6 semiconductors

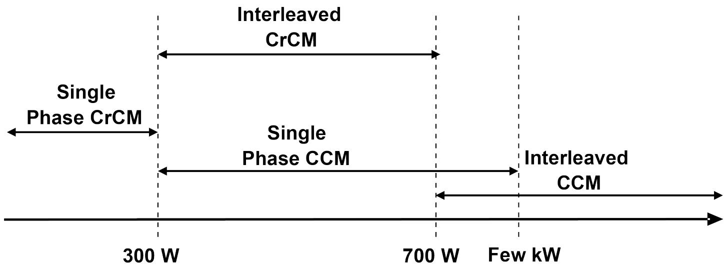
Totem Pole

- Advantages
  - Minimum components
  - Good efficiency
- Disadvantages
  - Complex
  - High side drive
  - Current sense
  - Common mode
  - Reverse recovery

Selecting the right PFC topology: Output power

- **How does output power influence decision?**
- **Peak inductor current comparison at 500 W**
  - Single phase CCM: 8.84 A
  - Single phase CrCM: 17.49 A

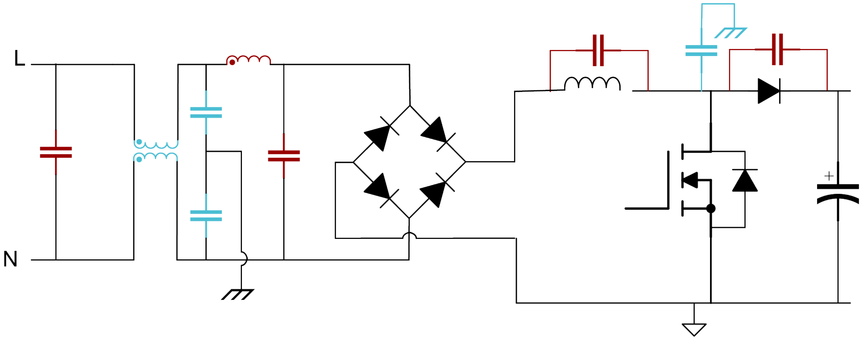




Selecting the right PFC topology: Interleaved CrCM vs single phase CCM

Design Characteristics	Interleaved CrCM	Single Phase CCM
Component stress	Conduction loss split between two power stages, valley switched	Single power stage, hard switched
Power density	Lower	Higher
Height	Smaller overall component height	Single inductor, larger heatsinks
Thermal management	Power dissipation spread over greater X/Y space	More challenging
Complexity	High power stage component count	Single power stage
Cost	Higher	Lower

Selecting the right PFC topology: EMI comparison

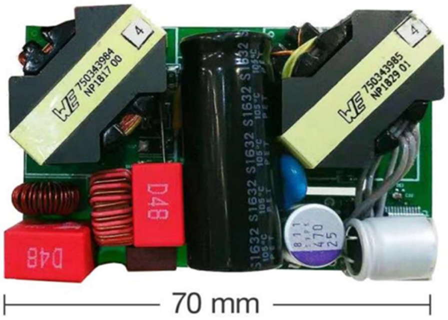


- **Critical conduction mode**
  - Inductor current ripple is 200%, requires physically larger EMI filter
  - Variable frequency – noise less concentrated in one frequency
- **Continuous conduction mode**
  - Physically smaller filter but fixed frequency
- **Interleaved**
  - Ripple current cancellation allows for physically smaller EMI filter
- **Bridgeless**
  - Common mode challenging for some variations

Topology selection exercise

Design specification

- Laptop adaptor
- USB-C, 100 W output
- 100 V_{AC} to 240 V_{AC} input
- Smallest form factor critical



TIDA-01623

- Single phase CrCM PFC + active clamp flyback
- Form factor: 70 mm × 42 mm × 16.5 mm
- 93.4% efficiency end-to-end at full load
- http://www.ti.com/tool/TIDA-01623

Topology selection exercise

Design specification

- Class-D audio amplifier
- 90 V_{AC} to 265 V_{AC} input
- 200 W continuous, 750 W peak
- Small solution size preferable (length, width and height)

TIDA-00776

- Single phase CCM PFC + 2-switch forward
- Form factor: 88 mm x 173 mm x 35 mm
- http://www.ti.com/tool/PMP30183

Topology selection exercise

Design specification

- OLED TV
- 85 V_{AC} to 265 V_{AC} input
- Peak output power: 480 W
- AC/DC supply embedded within panel: thin profile needed

TIDA-01495

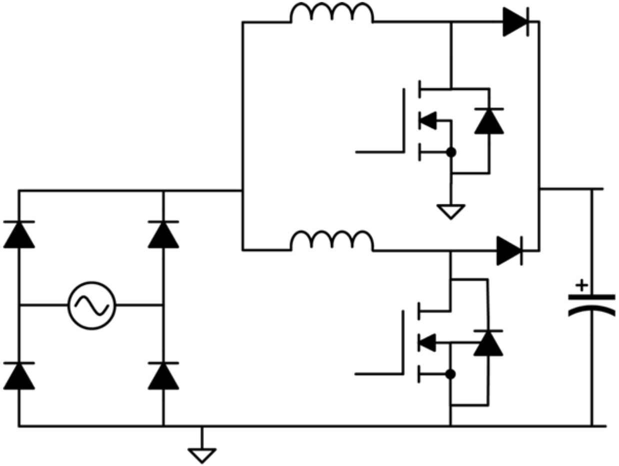
- Interleaved CrCM PFC + half-bridge LLC
- <17 mm height
- http://www.ti.com/tool/TIDA-01495

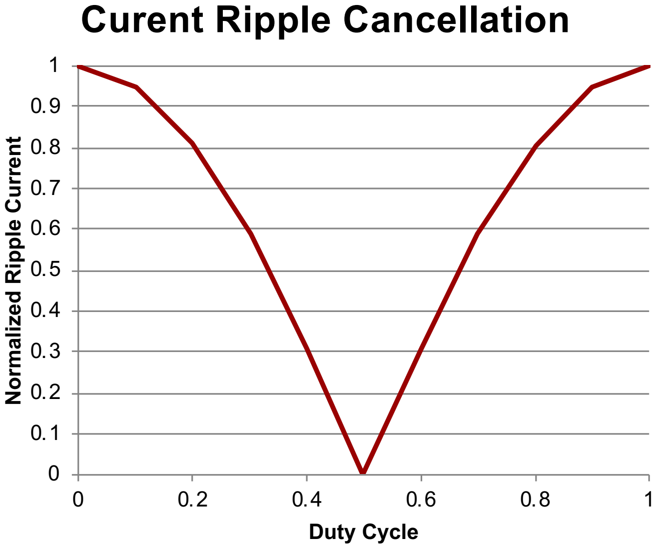
Summary

- **Overall**
  - Huge benefit to infrastructure
  - Regional regulatory requirements
- **Control method impacts power stage behavior**
  - Conduction losses
  - Switching losses
  - Switching frequency profile
- **PFC solution considerations**
  - Output power capability
  - Size
  - Complexity vs performance

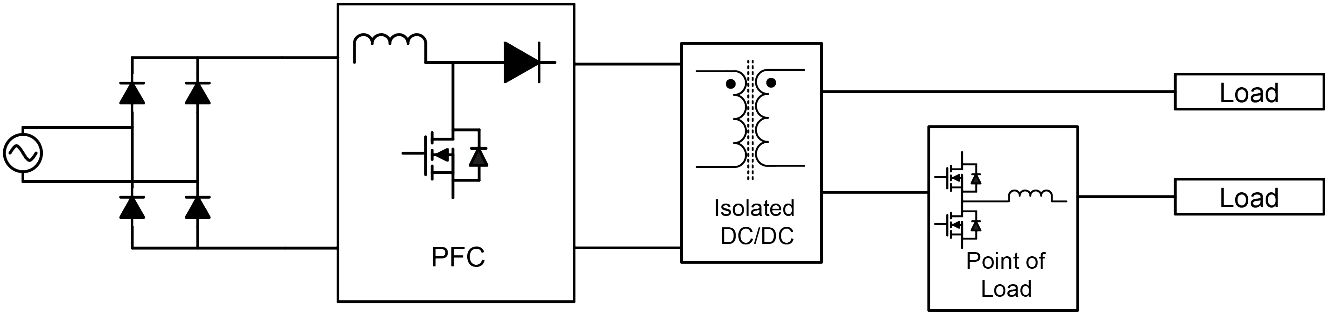
BACKUP

Interleaved PFC





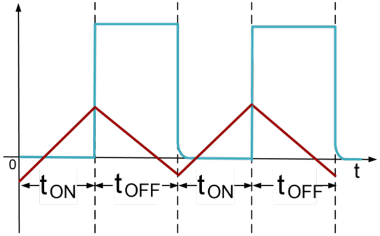
Benefits of active PFC



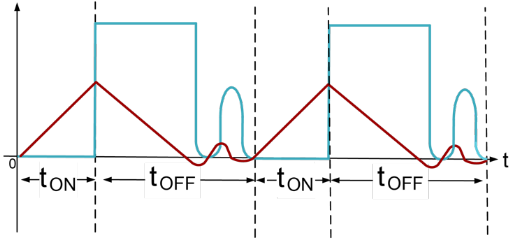
- **Output of PFC is a regulated voltage**
  - Easier design of isolated DC/DC stage
- **PFC can easily handle wide input voltage range**
  - One design able to support different line voltages around the world (115 V for US, 230 V for EU, 100 V for Japan, etc.)
- **PFC output capacitance provides holdup time when AC is disconnected**
  - Allows for a controlled shutdown sequence

Valley switching

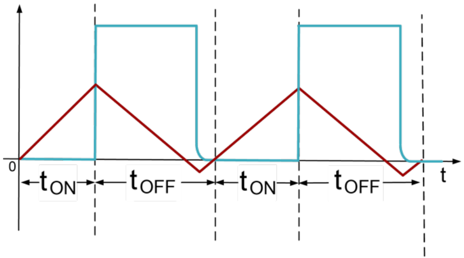
0^{th} Valley

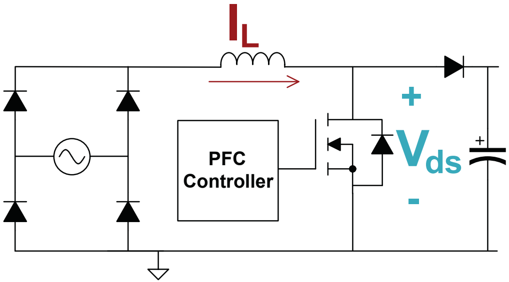


2^{nd} Valley



1^{st} Valley





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