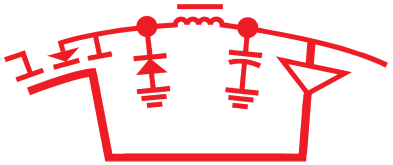

Power Supply Design Seminar

Common Mistakes in Flyback Power Supplies and How to Fix Them

Reproduced from
2020 Texas Instruments Power Supply Design Seminar SEM2400
TI Literature Number: **SLUP398**

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Texas Instruments

Common Mistakes in Flyback Power Supplies and How to Fix Them

Brian King

Michael O'Loughlin

Agenda

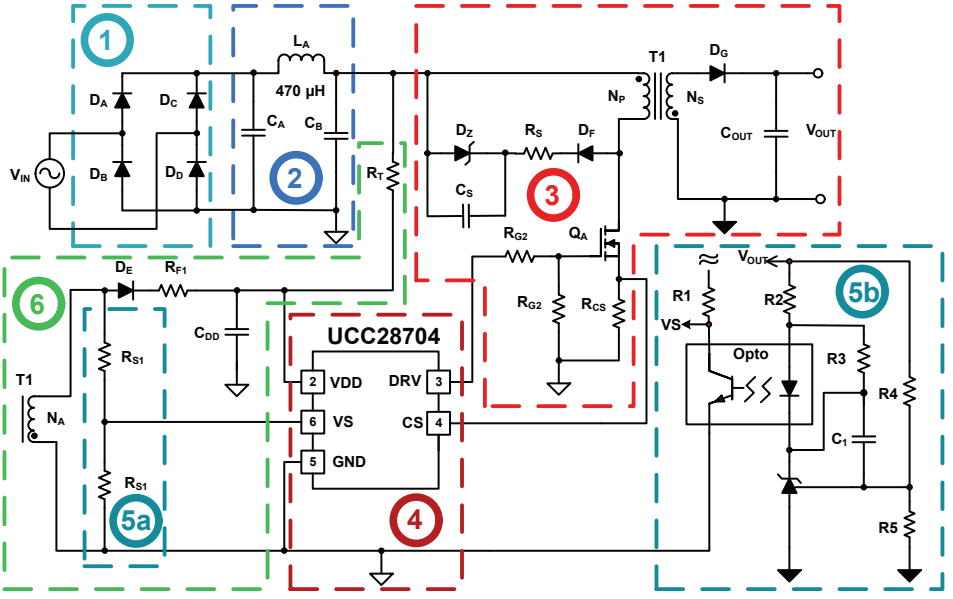
- Introduction to low power AC/DC flyback converters
- 10 common design/performance issues
  - Examine scenario and symptoms
  - Group debug discussion
  - Problem resolution
  - Troubleshooting, tips and guidance
  - References provided for deeper study
- Summary

“Experience is simply the name we give our mistakes.” – Oscar Wilde

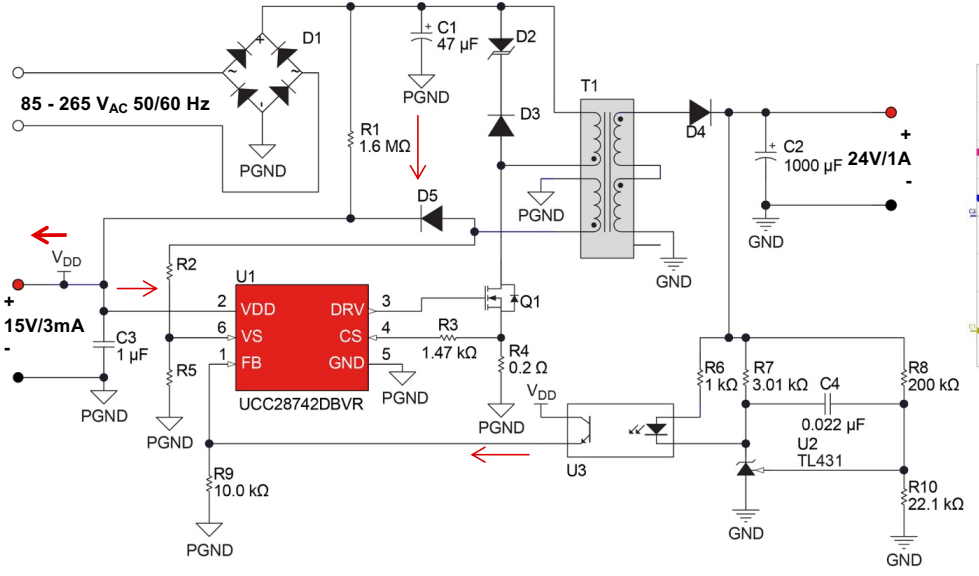
Introduction

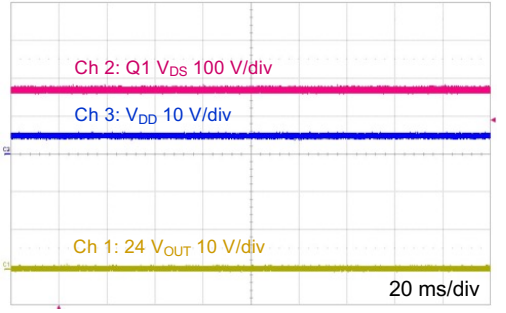
AC to DC Flyback Converter

1. Bridge rectifier
2. EMI filter
3. Flyback power stage
4. PWM controller
5. Feedback
   a) Primary-side regulation
   b) Secondary-side regulation
6. AUX supply with startup



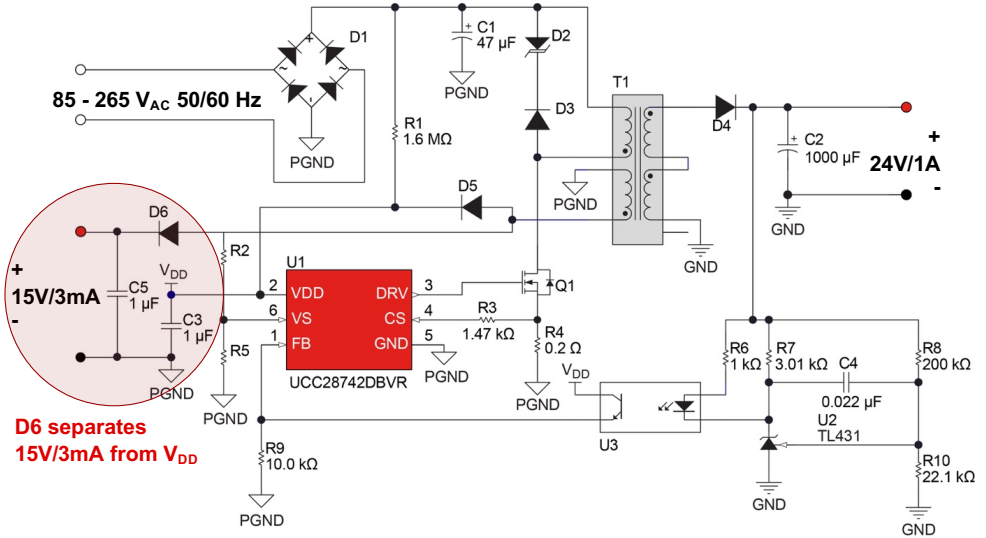
1A) Why does the power supply not start?



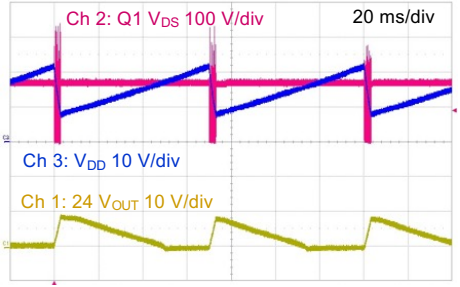


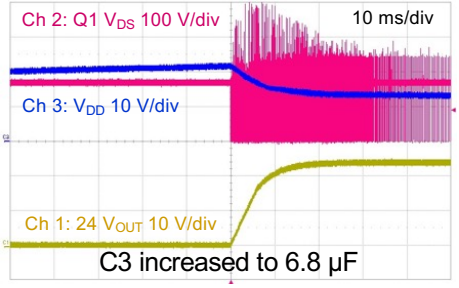
15 V / 3 mA loading prevents V_{DD} from reaching UVLO turn-on threshold

1B) Why does the power supply not start?



Not enough capacitance to prevent V_{DD} from dropping to UVLO turn-off threshold

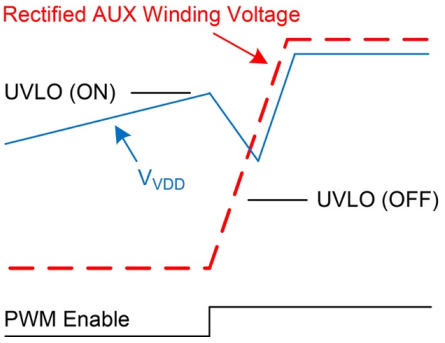




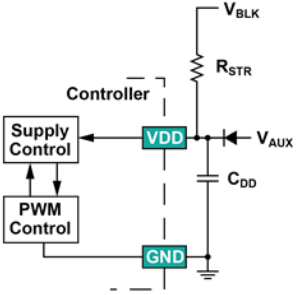
C3 increased to 6.8 µF

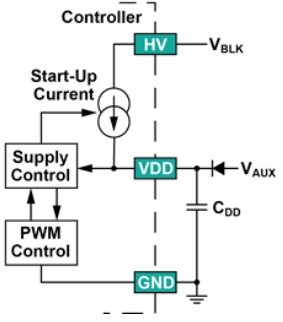
Startup tips and tricks

- Properly size C_{DD}
- Types of startup circuits:
  - Resistive
  - Active
- Controllers that minimize C_{DD}
  - Wide UVLO hysteresis
  - Low operating current
- Watch out for:
  - Properly set number of AUX turns
  - Extra loading on V_{DD}
  - Capacitance vs. DC bias of ceramic caps
  - Long startup times
    - Charging excessive output capacitance

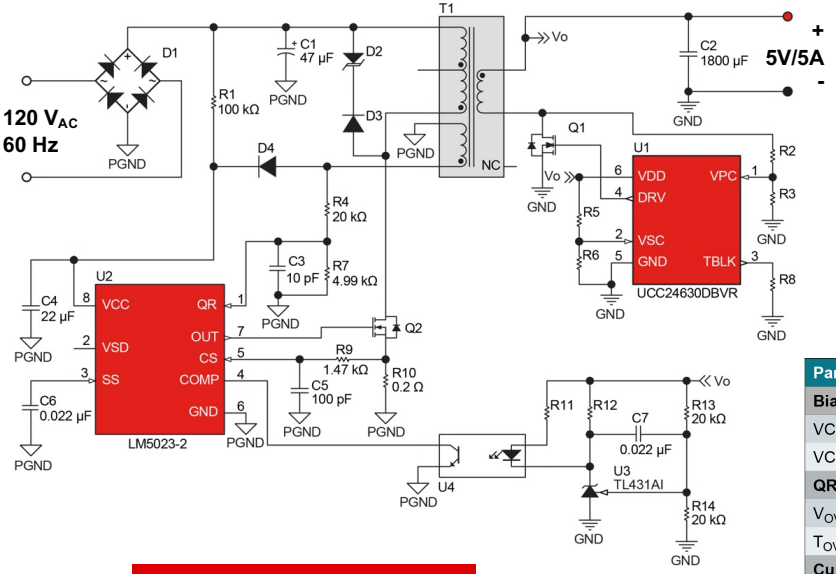


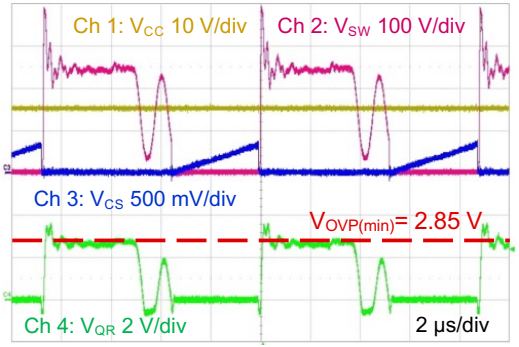
$$C_{DD} = I_{bias} \times \frac{t_{startup}}{UVLO_{ON} - UVLO_{OFF}}$$





2A) Why is your power supply shutting down?

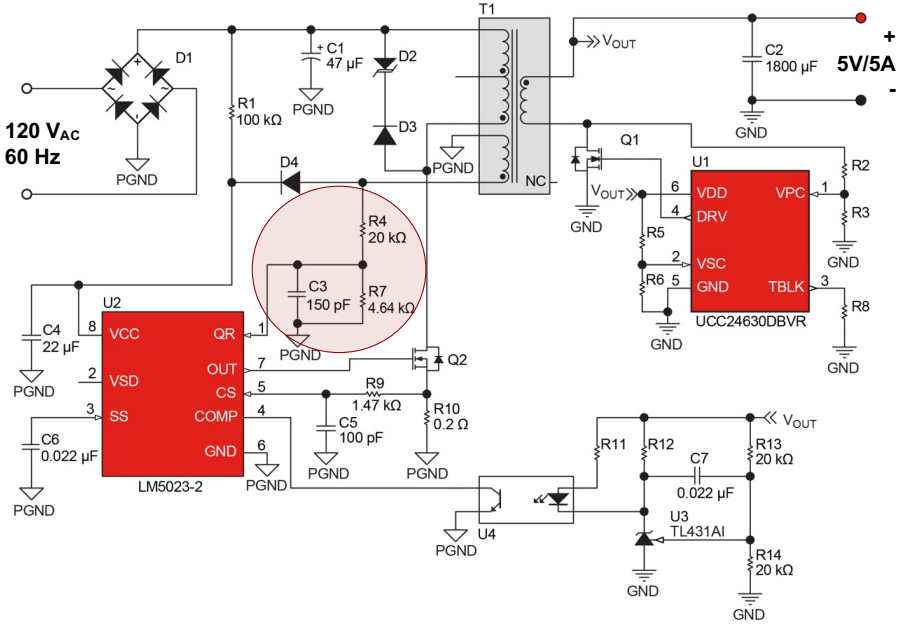


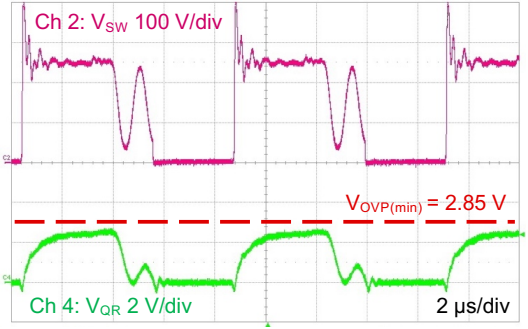


Triggering OVP

Parameter		MIN	TYP	MAX	Unit
Bias Supply Input					
VCC_{ON}	Controller enable threshold	12	12.8	13.5	V
VCC_{OFF}	Minimum operating voltage	7	7.5	8	V
QR Detect					
V_{OVP}	Overvoltage comparator threshold	2.85	3	3.17	V
T_{OVP}	Sample delay for OVP	870	1050	1270	ns
Current Limit					
V_{CS}	Cycle-by-cycle sense voltage limit threshold	450	500	550	mV
T_{LEB}	Leading edge blanking time		130		ns

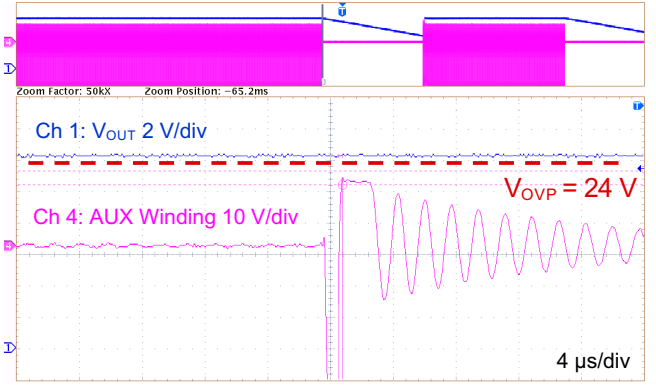
Adjusted and filtered AUX voltage sense



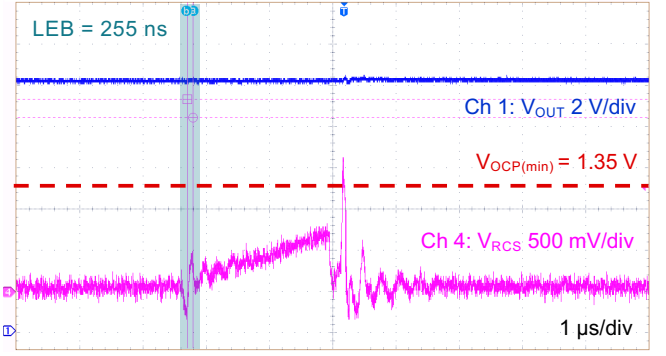


2B) Why is your power supply shutting down?

- 12 V output was regulating and just shut down
- OVP trip point set at 24 V on AUX winding



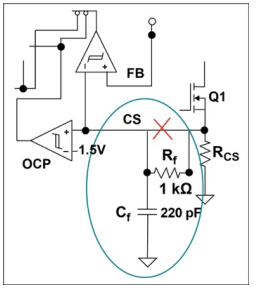
OCP triggered by trailing-edge spike, caused by dv/dt on switch node capacitor



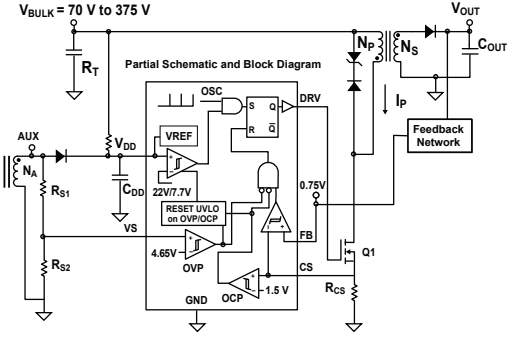
Parameter		MIN	TYP	MAX	Unit
CS Input					
$V_{CST(max)}$	MAX CS threshold voltage	720	750	784	mV
T_{CSLEB}	Leading edge blanking time	170	255	340	ns
Protection					
V_{OCP}	Over-current threshold	1.35	1.51	1.6	V
$T_{J(stop)}$	Thermal shut-down temperature		150		°C

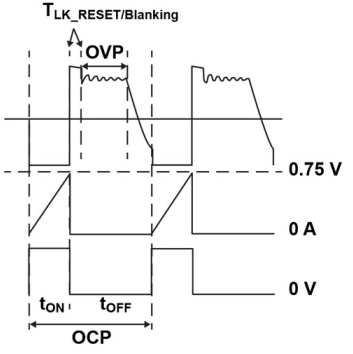
Peak current mode control, OCP and OVP review

- Use an RC to filter spikes on the current sense pin
- Know your controller – study the data sheet!
- For the example shown below:
  - Peak current is controlled by FB voltage (0.75 V_{peak})
  - OVP sensed on AUX winding, after T_{LK_RESET} during t_{dmag}
  - OCP sensed on CS pin, > 1.5 V, all the time
- Common protection mechanisms:
  - Cycle-by-cycle OCP
  - Shutdown OCP
  - OTP
  - V_{DD}
  - UVLO
  - Line UV
  - OPP

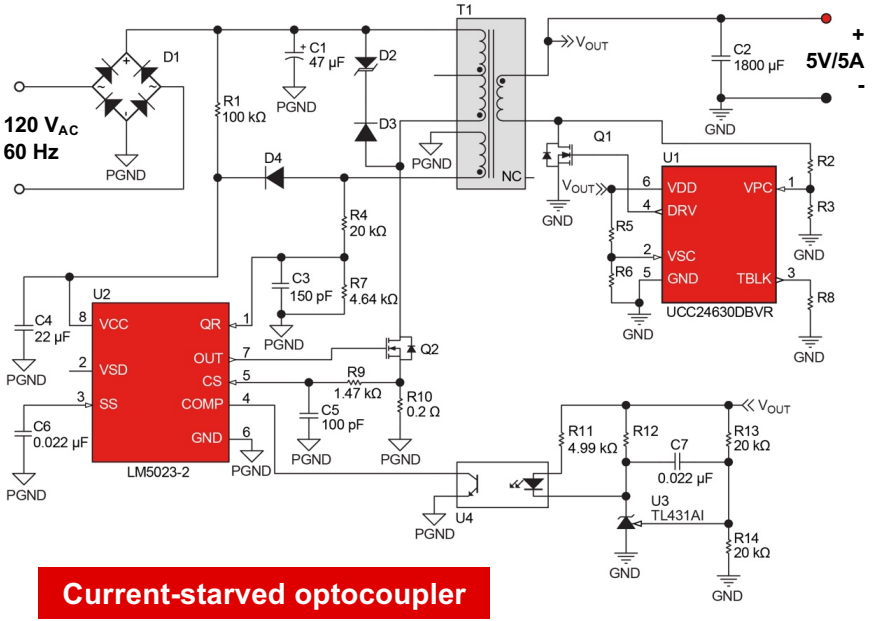


$$f_p \geq 10 \times f_{sw} = \frac{1}{2\pi R_f C_f}$$



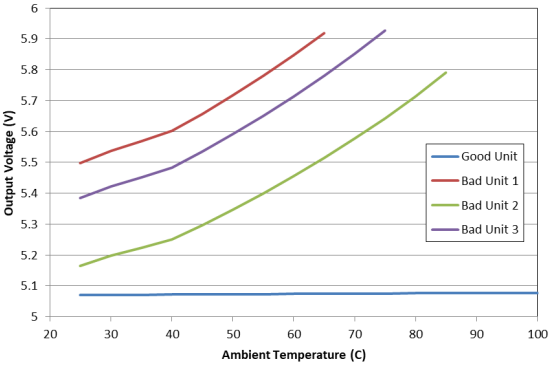


3) Why are some units losing regulation?



Current-starved optocoupler

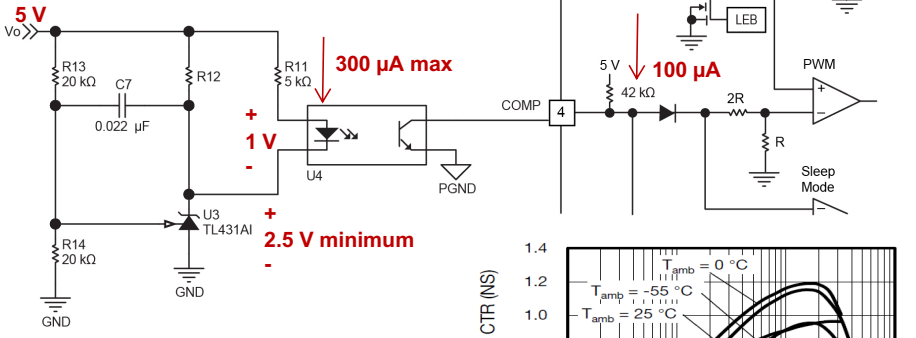
- OVP issue resolved on QR pin
- Now 2% return rate from field
- Returned units shut down under heavy load for extended time



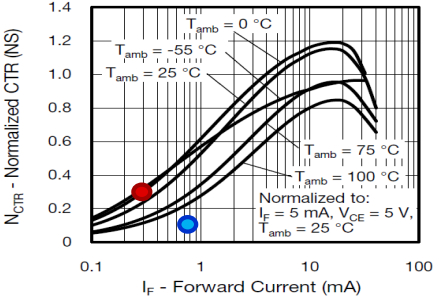
Properly biasing optocoupler feedback

$$CTR_{min} = \frac{100\ \mu A}{300\ \mu A} = 0.33\ for\ R11{=}5\ k\Omega$$

$$= \frac{100\ \mu A}{750\ \mu A} = 0.13\ for\ R11{=}2\ k\Omega$$



P/N suffix	CTR min	CTR max
A	80%	160%
B	130%	260%
C	200%	400%
D	300%	600%
None	80%	600%



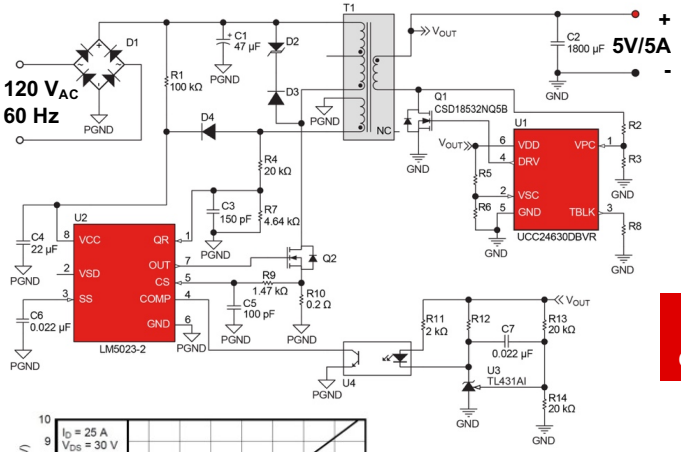
Design Procedure

1. Find max collector current needed
2. Find max forward current available
3. Calculate min CTR needed

Tips and Tricks

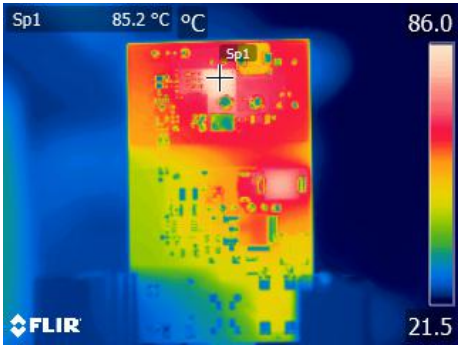
- Reduce R11 or choose higher CTR to improve situation
- Consider CTR initial tolerance + forward current + temperature + life
- Study the internal block diagram from data sheet!
- Watch out for loop gain increase
- TLV431 provides extra 1.25 V across R11

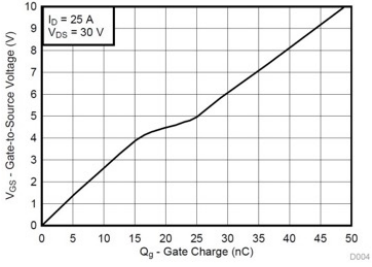
4) Why is the SR getting hot?



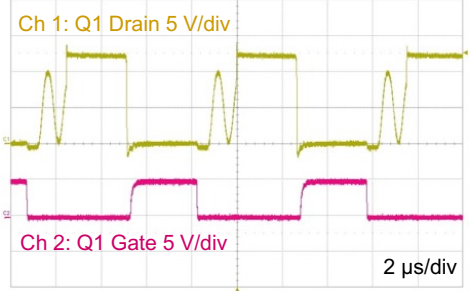
~10 A_{RMS} in Q1

Q1 not fully enhanced at 5 V

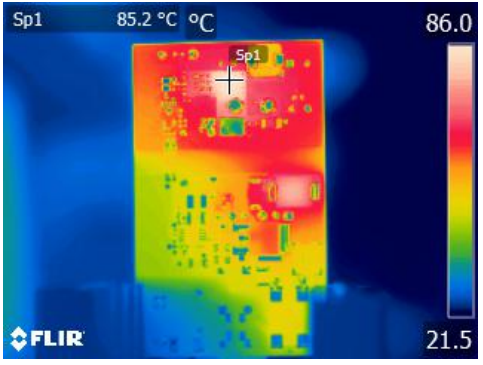




T_A=25°C		Typical Value		Unit
V_{DS}	Drain-to-source voltage	60		V
Q_g	Gate charge total (10 V)	49		nC
Q_{gd}	Gate charge gate-to-drain	7.9		nC
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 6 V	3.5	mΩ
		V_{GS} = 10 V	2.7	
$V_{GS(th)}$	Threshold voltage	2.8		V

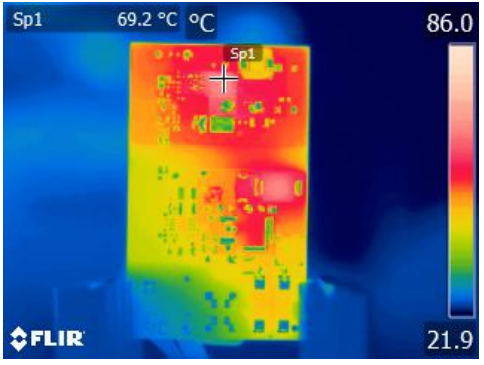


A more appropriate synchronous rectifier



CSD18532NQ5B

T_A=25°C		Typical Value		Unit
V_{DS}	Drain-to-source voltage	60		V
Q_g	Gate charge total (10 V)	49		nC
Q_{gd}	Gate charge gate-to-drain	7.9		nC
$R_{DS(ON)}$	Drain-to-source on-resistance	V_{GS} = 6 V	3.5	mΩ
		V_{GS} = 10 V	2.7	
$V_{GS(th)}$	Threshold voltage	2.8		V

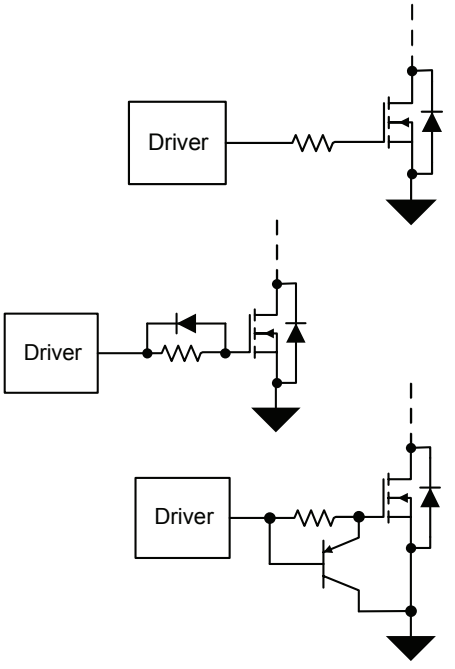


CSD17559Q5

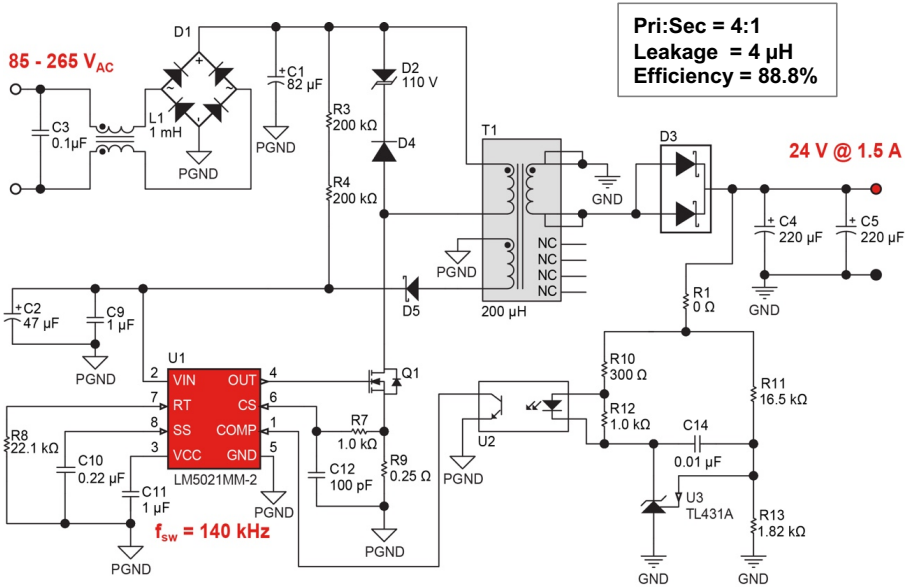
T_A=25°C		Typical Value		Unit
V_{DS}	Drain-to-source voltage	30		V
Q_g	Gate charge total (4.5 V)	39		nC
Q_{gd}	Gate charge gate-to-drain	9.3		nC
$R_{DS(ON)}$	Drain-to-source on-resistance	V_{GS} = 4.5 V	1.15	mΩ
		V_{GS} = 10 V	0.95	
$V_{GS(th)}$	Threshold voltage	1.4		V

Gate drive tips

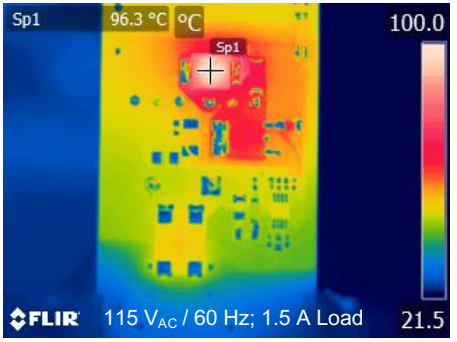
- *Pay attention to turn-on threshold of FET*
- *Size V_{CC} capacitor to hold 10 • Q_g*
- *Use a gate driver resistor to:*
  - Limit drive current, older PWMs not I limited
  - Damp gate ringing
  - Soften dv/dt slew rate for EMI
  - Reduce turn-on current spike
    - Discharging C_{SW}
    - Reverse recovery of output diode
    - Shoot-through of synchronous rectifiers
- *Fast turn-off with slow turn-on*
  - Minimize turn-off switching loss
  - Less susceptible to bounce back from D-G charge

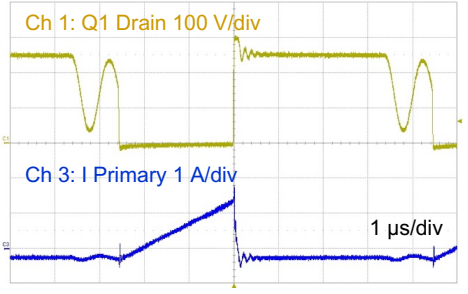


5) Why is the clamp getting so hot?

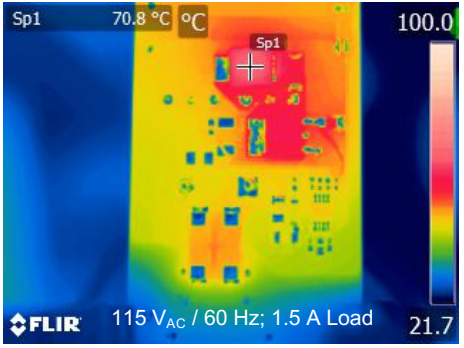


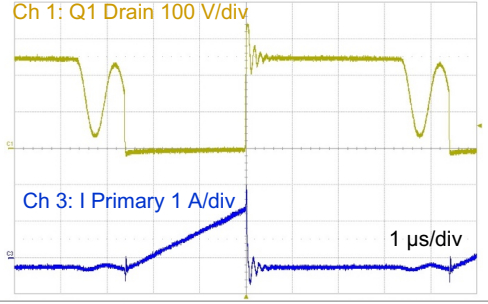
Clamping voltage too low





Reset leakage faster to reduce clamp loss





TVS = SMCJ150A
Efficiency = 89.7%

Clamping Tips

Minimize leakage reset time*
- Some magnetizing energy is lost in clamp
- Clamp voltage as high as possible
- Minimize leakage inductance

TVS clamp
- Predictable and repeatable
- Good efficiency at very light loads

Resistor-capacitor clamp
- Cheap
- Resistor package sized for power loss
- Burns more power at very light loads

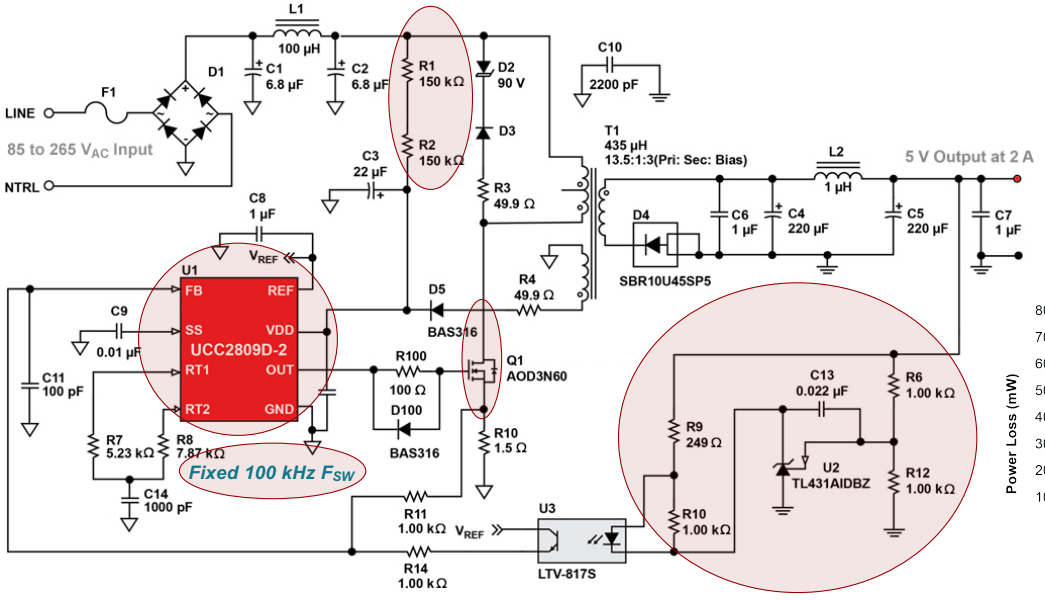
Active clamp
- Best efficiency – recycles leakage energy
- Lower noise
- Requires specialized controller

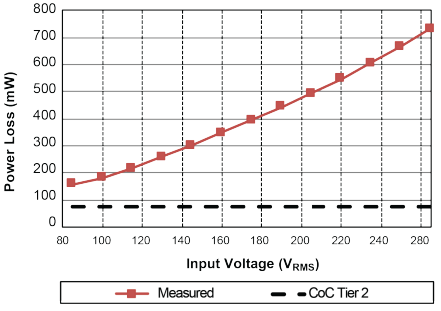
See reference [3]

6) How can we reduce standby power loss?

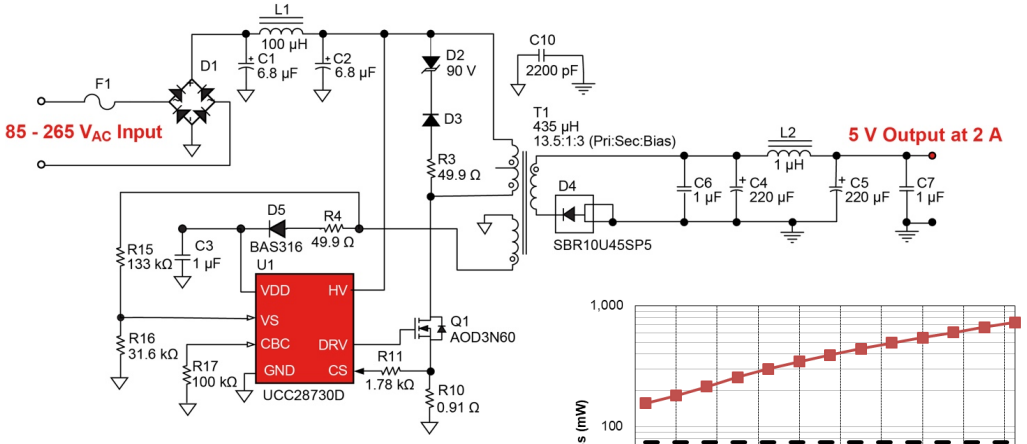
EU Code of Conduct Tier 2

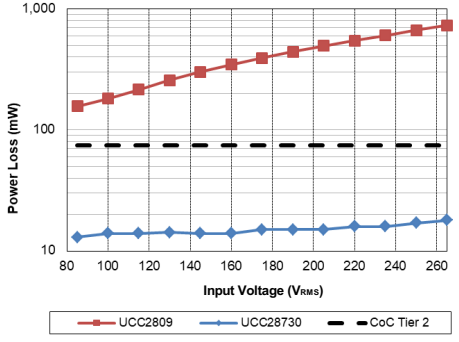
75 mW maximum





A better answer for low standby power





Low Standby Checklist

Controller features

- Low startup power
  - Low startup current
  - Active startup circuit (depletion mode FET)
- Light load modes
  - Low F_{SW}
  - Burst mode
- PSR

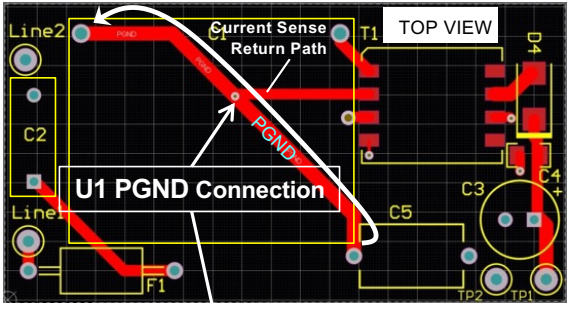
FET features

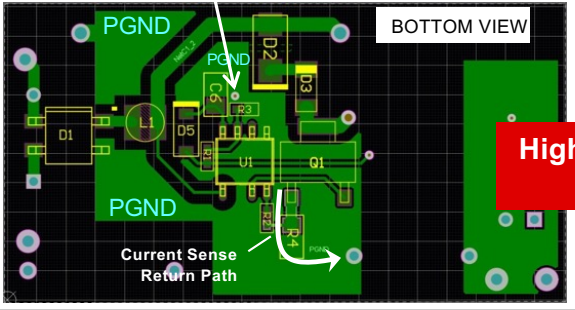
- Low C_{OSS}
- Low gate charge

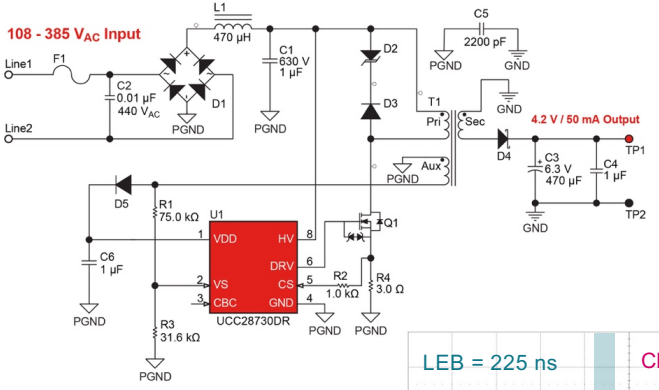
Rectifier features

- Low junction capacitance

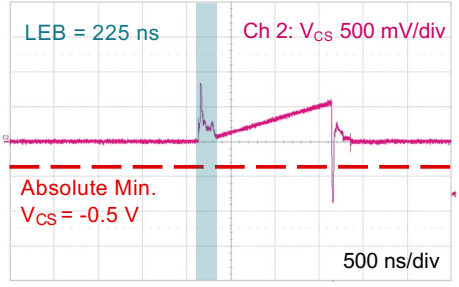
7) What's causing the negative spike on CS?



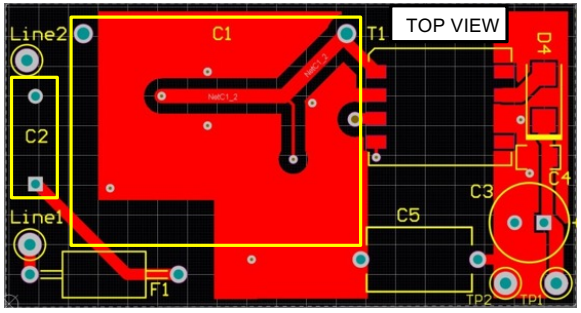


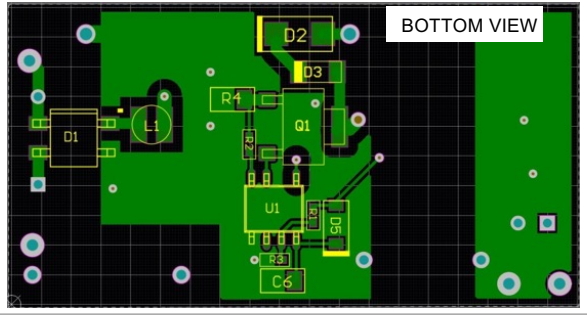


High inductance in current sense return path



An improved layout





Layout Tips

Parasitic inductance

- Minimize area of switching current loops
- Use ground planes where possible
- Place capacitors directly between V_{CC} pins and ground

Parasitic capacitance

- Minimize cross-sectional area of switch node
- Cross traces orthogonally
- Ground heat sinks

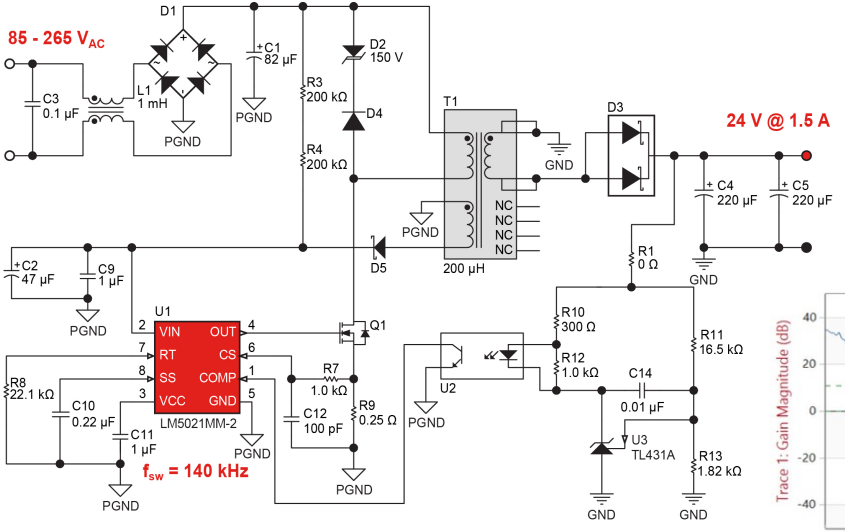
Parasitic resistance

- Place power components near each other
- Know the high current paths
- Estimate etch resistance – count the squares
- Use wide, short etch for high current paths

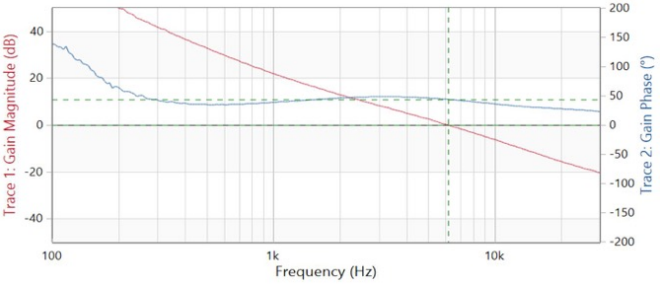
Noise mitigation

- Avoid high currents through signal ground
- Minimize traces between resistor dividers
- Don’t place ICs or traces under magnetics

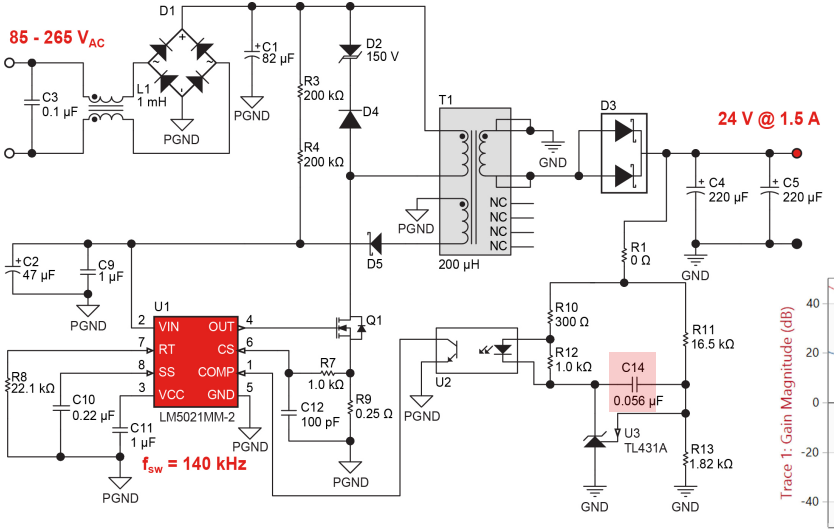
8) How can we increase the phase margin?

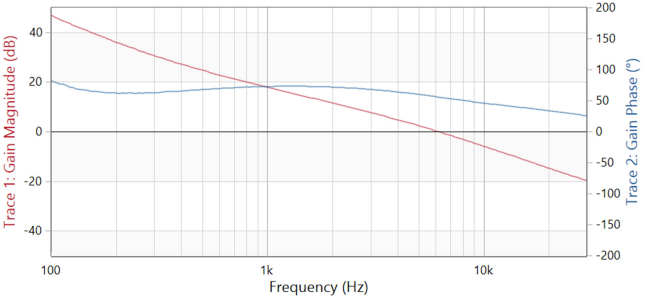


6.2 kHz bandwidth
44º phase margin



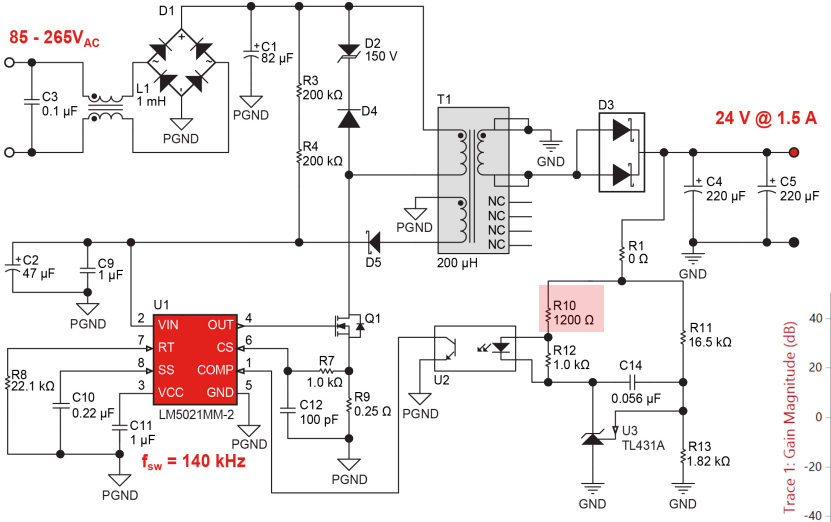
TL431 integrating capacitor effects

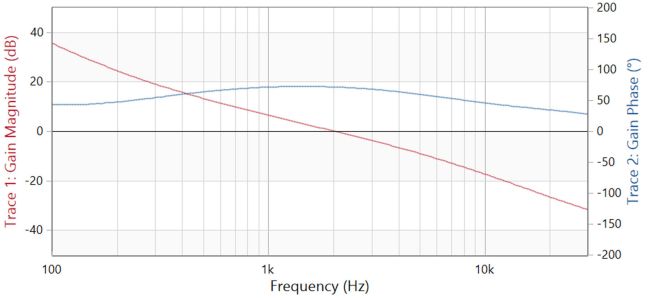




C14 = 0.056 µF F_{CO} = 6.2 kHz Φ_M = 56°

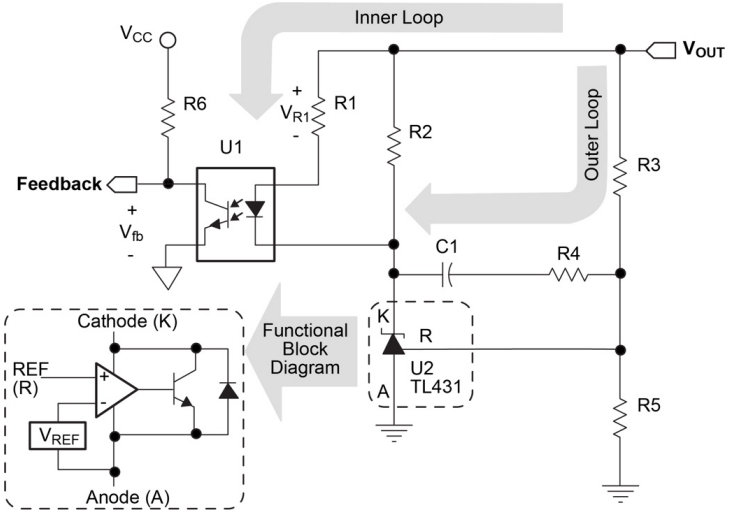
Optocoupler pull-up resistor effects

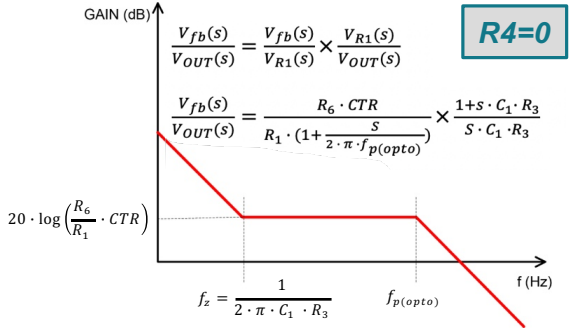


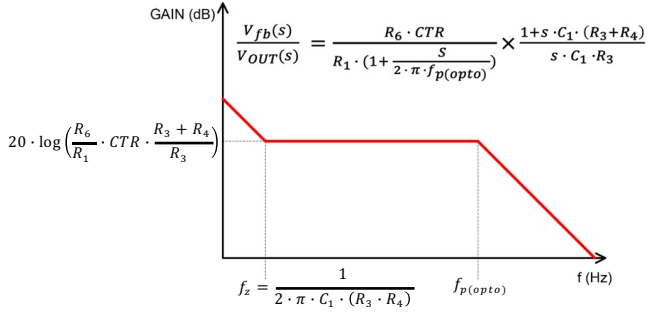


R10 = 1200 Ω F_{CO} = 2.0 kHz Φ_M = 72°

Compensating isolated supplies with a TL431

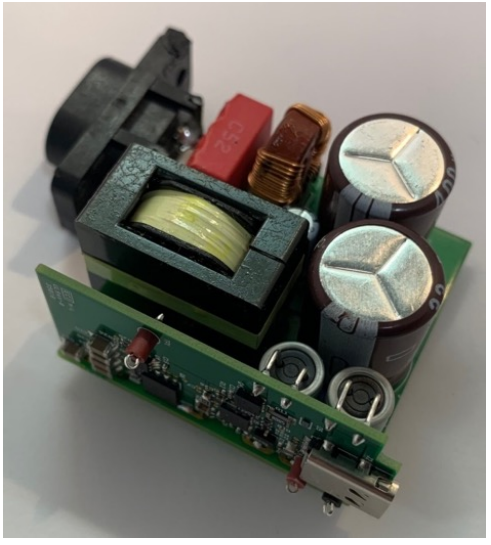


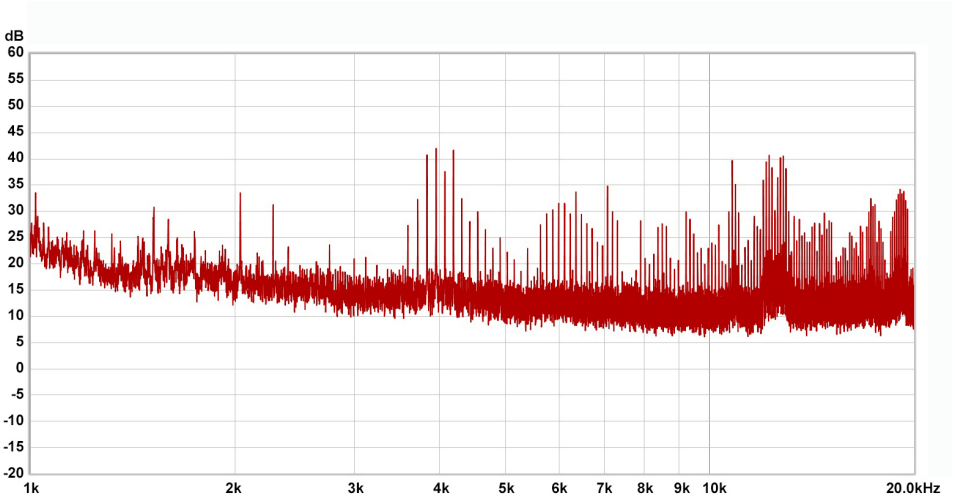




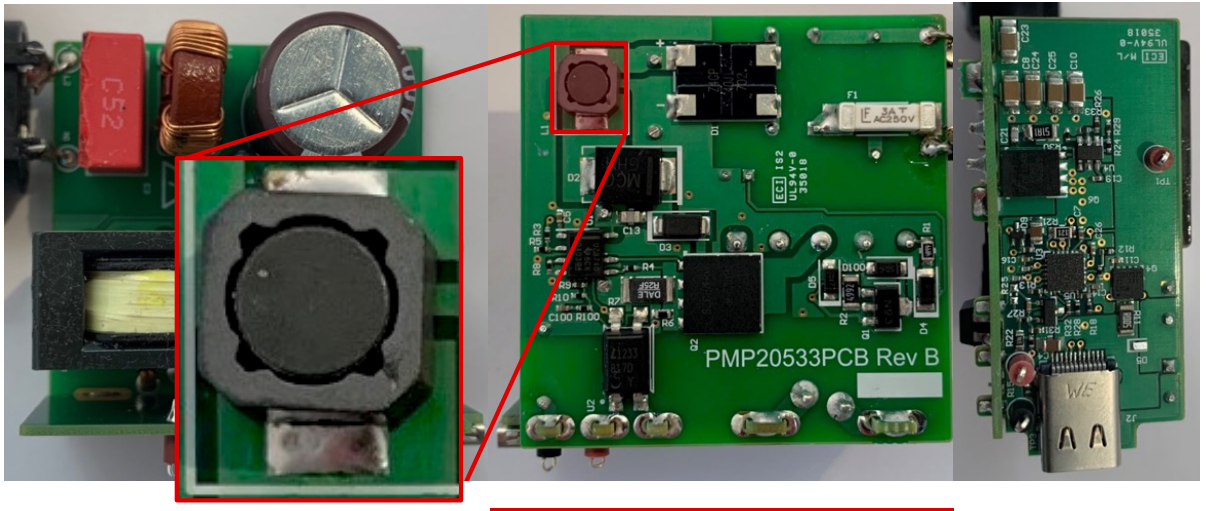
- Scaling R6/R1 is the only way to attenuate gain!
- Eliminating inner loop also an option

9) Where is that buzzing sound coming from?



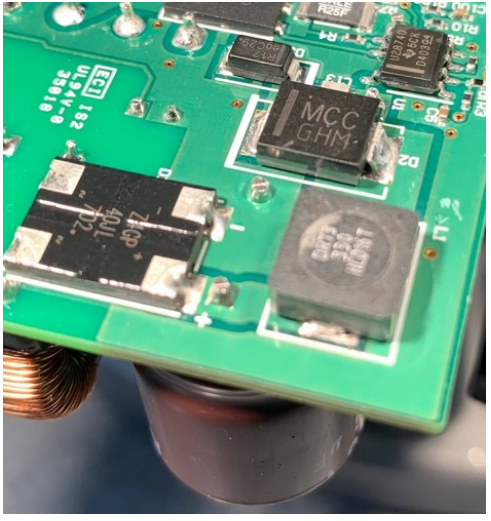


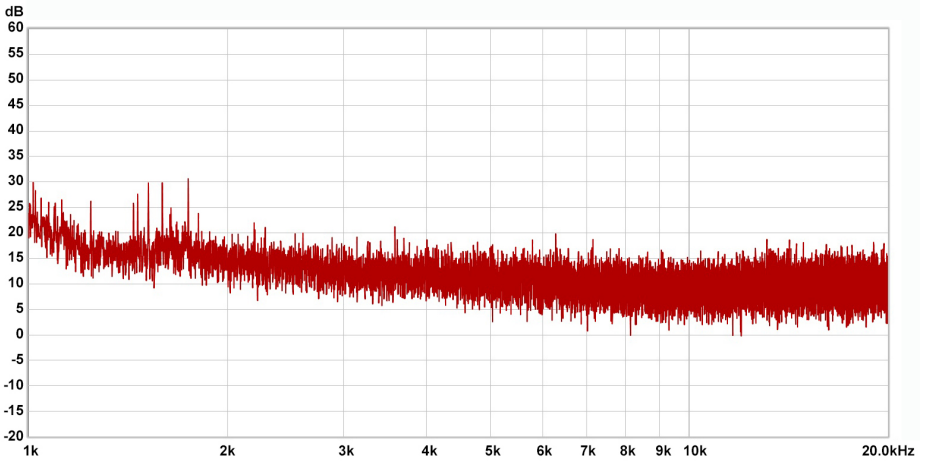
9) Where is that buzzing sound coming from?



Drum core inductor acts like a speaker

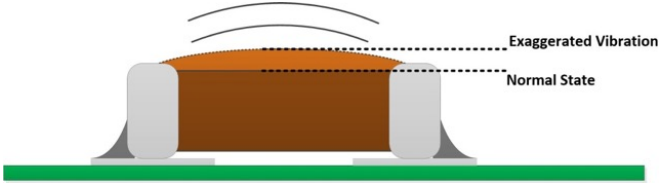
A quiet inductor



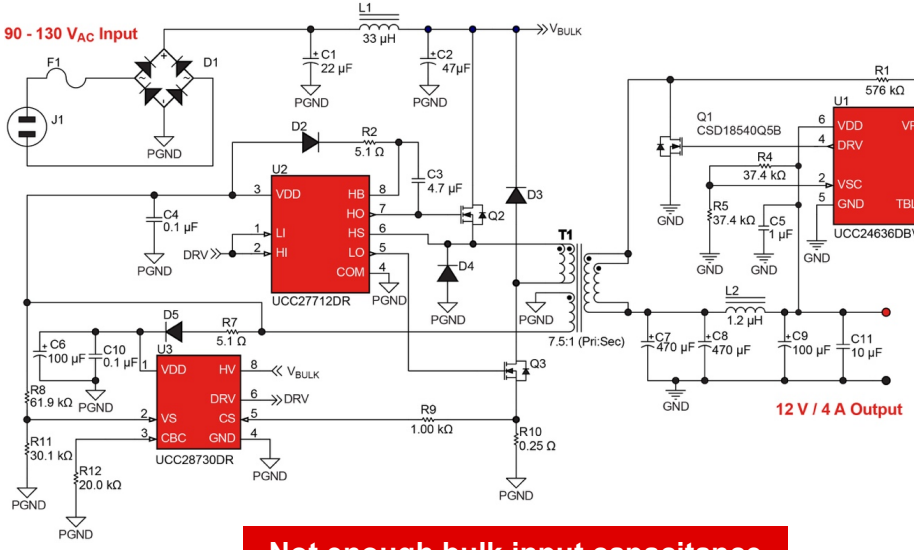


Avoiding audible noise transducers

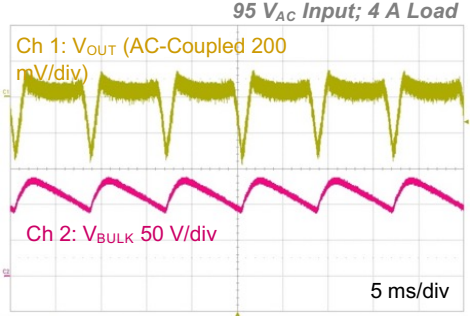
- **Secure through-hole components with high energy**
- **Transformers**
  - Core halves glued
  - Assembly varnished
- **Inductors**
  - Avoid constructions with loose parts
- **Ceramic capacitors**
  - Place at edge of PCB
  - Mount symmetrically on opposite sides of PCB
  - Add slit in PCB under MLCC



10) Why is there excessive low frequency ripple?

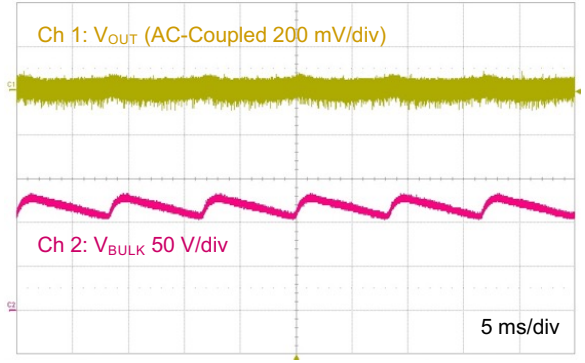


Not enough bulk input capacitance and limited max duty-cycle

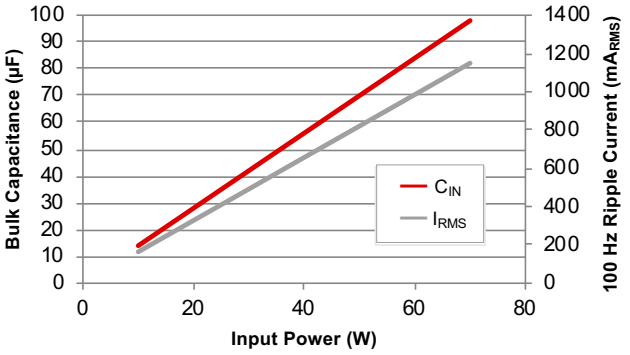


Bulk input capacitor considerations

90 V_{AC} Input; 4 A Load – 2 x 68 µF



Bulk Cap Needed to Maintain 80 V Valley at 90 V_{AC} / 50 Hz



- 1.5 µF/W is a good rule of thumb for 90 V_{AC} minimum input
- Watch RMS current; consider both 100 Hz & 100 kHz content
- Bulk cap is usually the least reliable component in power supply – determines product life
- Arrhenius' law: capacitor life doubles for every 10ºC decrease in temperature
- ESR increases significantly at low temperatures

Summary: Low power AC/DC troubleshooting

- **Startup issues** – start by monitoring V_{DD}, V_{OUT} and V_{SW}
- **Shutdown issues** – understand all possible shutdown mechanisms of the controller (read the data sheet!)
- **Regulation issues** – check operation of TL431 & optocoupler
- **Efficiency/thermal issues** – use thermal camera to identify problem spots; understand core/copper loss in transformer
- **Standby power issues** – use a controller with light load mode and active startup
- **Layout issues** – understand how parasitic inductance and capacitance are manifested and how to mitigate
- **Stability issues** – understand the frequency response of TL431 circuit
- **Audible noise issues** – know what components act as transducers
- **Bulk capacitor issues** – check operation and life at min input, max load

References and further reading

- *"**Control Challenges for Low Power AC/DC Converters**," Brian King, Rich Valley, TI Power Supply Design Seminar 2014 SEM2100, slup325.* http://www.ti.com/lit/slup325
- *"**Power Tips #81: Make sure your optocoupler is properly biased**," Brian King, EDN Network, October 2017.* https://www.edn.com/electronics-blogs/power-tips-/4459005/Make-sure-your-optocoupler-is-properly-biased
- *"**Flyback transformer design considerations for efficiency and EMI**," Isaac Cohen, Bernard Keogh, TI Power Supply Design Seminar 2016 SEM2200, slup338.* http://www.ti.com/lit/slup338
- *"**The Magnetics Design Handbook For Switching Power Supplies**," Lloyd H. Dixon, slup132 (slup123/4/5/6/7/8).* http://www.ti.com/lit/slup132
- *"**Designing Magnetic Components for Optimum Performance in Low Cost AC/DC Converter Applications**," Seamus O'Driscoll, Peter Meaney, John Flannery, George Young, TI Power Supply Design Seminar 2010 SEM1900, slup265.* http://www.ti.com/lit/slup265
- *"**Constructing Your Power Supply – Layout Considerations**," Robert Kollman, TI Power Supply Design Seminar 2004 SEM1600, slup230.* http://www.ti.com/lit/slup230
- *"**Power Tips: Compensating Isolated Power Supplies**," Brian King, EE Times, February 2015.* https://www.eetimes.com/author.asp?section_id=36&doc_id=1325778#

Further references listed in full paper

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