Optimizing GaN-Based High-Voltage, High-Power Designs

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Silicon carbide (SiC) and gallium nitride (GaN) wide-bandgap devices make it possible to switch at higher frequencies, with better performance than silicon devices. These devices also enable smaller solution sizes because the switching components generate smaller losses overall.

Introduction

The first generations of onboard chargers (OBCs) leveraged insulated gate bipolar transistors (IGBTs) and were huge and bulky. **Figure 1** illustrates the improvement in solution size with better technologies and thermal concepts.

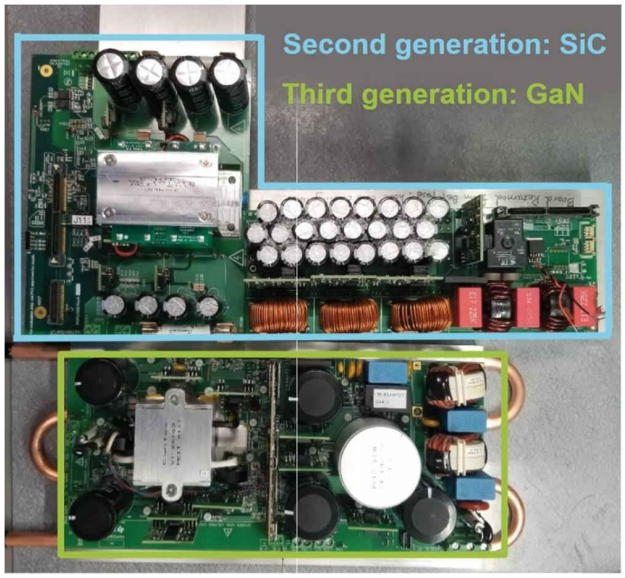


Figure 1. *Second-generation SiC-based OBC reference designs [1] (light-blue frame, convection-cooled) and a third-generation GaN-based OBC reference design (green frame, liquid-cooled).*

GaN's ultra-fast switching slew rates and liquid-cooled thermal interface yield a 22% reduction in size (area: 38,171 mm^2) [2] compared to the convection-cooled SiC-based DC/DC and power factor correction (PFC) reference designs on the left [3] and right [4] inside the light-blue frame in **Figure 1**, respectively. Texas Instruments (TI) had designed these latter two reference designs (area: 27,886 mm^2 + 20,915 mm^2) three years earlier than the reference design in the green frame. This topic explains the design process behind the GaN-based reference design in the green frame.

Comparing Different Technologies

Table 1 compares the parameters of silicon/IGBT, SiC and GaN devices. The reason why the vast majority of designs use silicon is because silicon still has a cost advantage over wide-bandgap devices. This gap will likely become smaller in the near future.

Parameter	Silicon/IGBT	SiC	TI GaN
$R_{DS(on)}$	High	Medium	Low
V_{DS}	Up to several kilovolts	650 V/900 V/ 1,200 V/1,700 V	600 V/650 V
Maximum operating f_{sw}	Low	Medium	High
Q_{rr}	High	Low	Zero
$T_{j,max}$	150°C/175°C	175°C/200°C	150°C
Thermal Conductivity	1.5 W/(cm × K)	5 W/(cm × K)	1.3 W/(cm × K)
Cost	Low	High	Medium

Table 1. *Comparing silicon/IGBT, SiC and GaN parameters.*

Wide-bandgap devices come into play when the design calls for the transfer of high power in a specified form factor and silicon-based solutions reach their thermal limits, either generating too many losses or requiring too many semiconductor components in parallel to keep the losses at bay, which can lead to a more expensive overall solution.

GaN high-electron mobility transistors enable designers to reach higher power density levels than any other technology on the market. Their parasitic elements are smaller compared to silicon and SiC devices, allowing switching at higher frequencies with acceptable losses. Direct drive of TI GaN FETs results in a zero reverse-recovery charge characteristic, which is beneficial for hard-switched continuous conduction mode (CCM) topologies such as the CCM totem-pole PFC converter [5]. CCM totem-pole PFC converters with silicon switches have never been viable given the immense losses caused by the large reverse-recovery

charge of silicon metal-oxide semiconductor field-effect transistors (MOSFETs).

Writing this paper called for a performance comparison between SiC MOSFETs and GaN. To accurately compare TI GaN devices with ultra-fast slew rates (>150 V/ns), you would need to consider SiC MOSFETs in a low-inductance package with fast-switching-speed capability. In the commercial market, however, SiC FETs with similar $R_{DS(on)}$ and voltage ratings are not readily available in a low-inductance package with a Kelvin source connection. So instead, SiC FETs with a larger $R_{DS(on)}$ were tested and used the switching figure-of-merit (FOM) concept for both hard- and soft-switching comparisons, as shown in **Figure 2** and **Figure 3**.

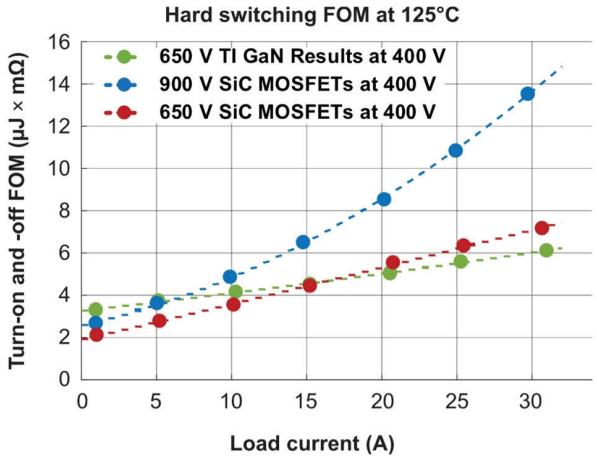


Figure 2. *Hard-switching FOM comparison of SiC and TI GaN.*

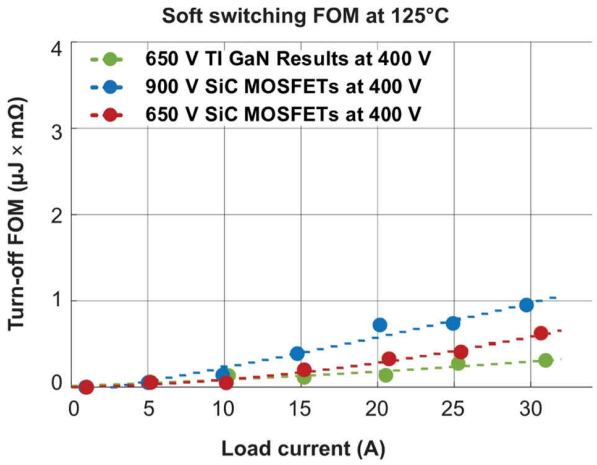


Figure 3. *Soft-switching FOM comparison of SiC and TI GaN.*

From the FOM graphs, you can see that under soft switching, TI GaN has an immense advantage over SiC MOSFETs, with significantly lower turnoff losses as a result of the direct-drive approach. In hard-switching conditions, the total switching loss includes both turnon and turnoff energy losses. The overall switching losses are proportional to the product of the switching frequency and energy required to turn the respective FET on and off. **Equation 1** expresses this relationship:

$$P_{SW} = \left(E_{on} + E_{off}\right) \times f_{sw} \quad (1)$$

The hard-switching FOM shows that TI GaN generates fewer losses at load currents greater than 15 A and is a better fit for high-current applications.

Advantages of Integrating the Driver With GaN FETs

Two types of parasitic inductance between the driver and the FET limit the ultra-fast switching performance of GaN FETs: the common source inductance (CSI) and the gate-loop inductance. Minimizing both parasitic elements will help achieve the best possible switching performance.

A completely discrete approach will result in a large CSI because of inductance contributions from the integrated circuit (IC) packages and the driver to FET routing distance on the printed circuit board (PCB). The result will cause slower turnon of the GaN FET, with increased losses. Most GaN FET manufacturers currently only offer packages with a separate Kelvin source connection to reduce the CSI. A discrete FET solution with an external gate driver will have a larger CSI compared to the integrated driver and GaN solution from TI (see **Figure 4** through **Figure 7**).

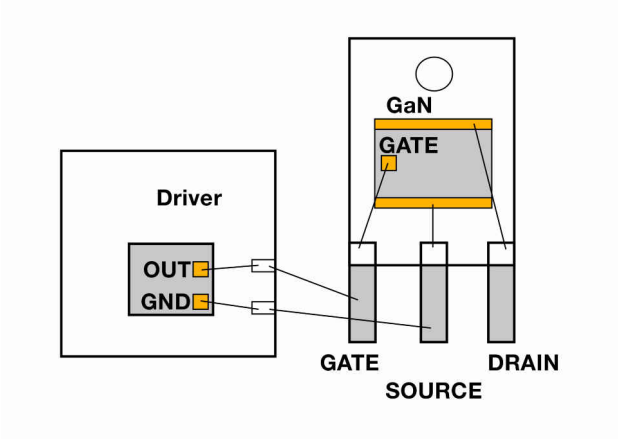


Figure 4. *Discrete GaN FET and driver.*

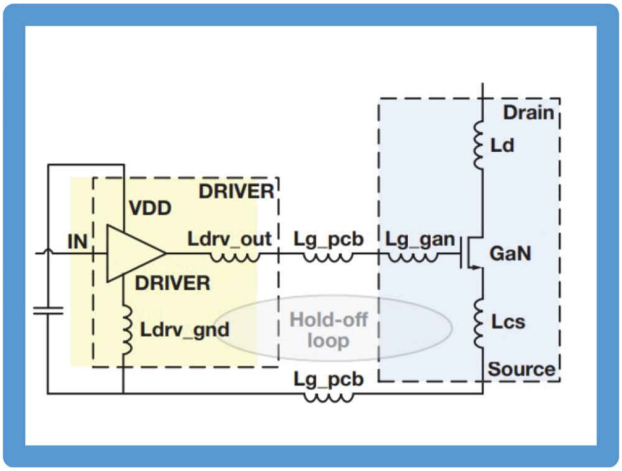


Figure 5. *Discrete GaN FET and equivalent circuit diagram.*

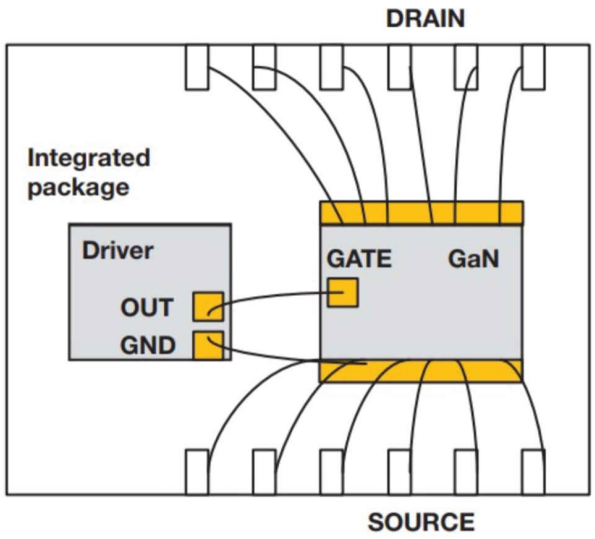


Figure 6. *TI GaN FET with integrated driver.*

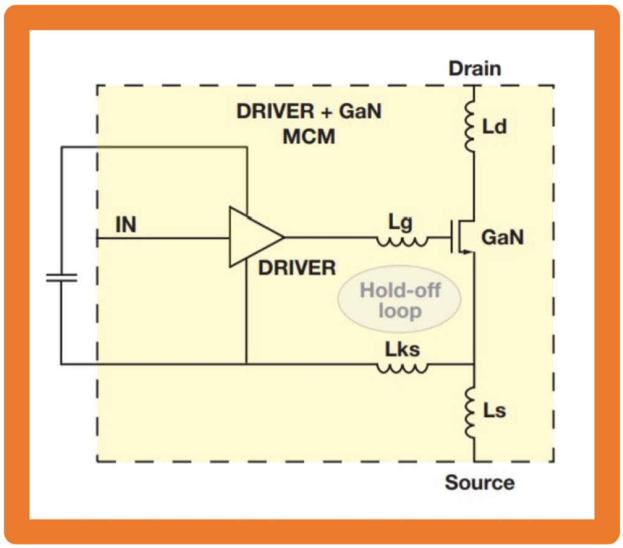


Figure 7. *TI GaN FET with equivalent circuit diagram.*

Meanwhile, integrating the driver and GaN also minimizes the gate-loop inductance, helping reduce gate-loop ringing, mitigating crosstalk, and improving gate reliability [6][7][8].

Figure 8 shows the simulated turnon switching waveforms of the high-side FET in a GaN FET half bridge for two different CSI values (0 nH and 5 nH).

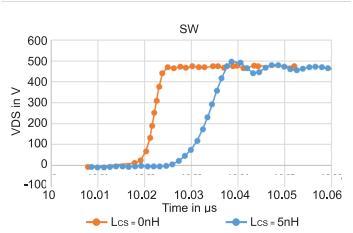


Figure 8. *Simulated switching waveform for different CSI values.*

Having the smallest possible CSI enables the GaN FET to turnon much faster, without causing any switch-node ringing. In addition, the turnon switching losses of the GaN FET are smaller with a lower CSI value, which helps improve system efficiency (see **Figure 9**).

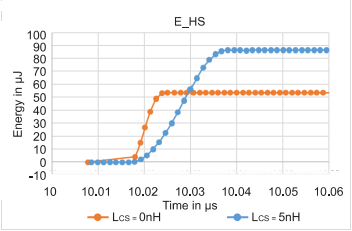


Figure 9. *Simulated turnon energy for different CSI values.*

There is a similar effect for the parasitic gate-loop inductance. **Figure 10** illustrates that the smaller the gate-loop inductance value, the smaller the energy required to turnon the GaN FET (2 nH and 10 nH).

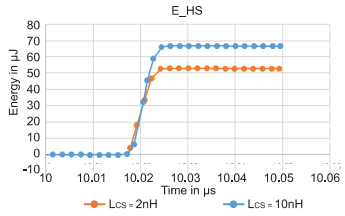


Figure 10. *Simulated turnon energy for different gate-loop inductance values.*

The GaN-Based 6.6-kW OBC Reference Design

The GaN-Based 6.6-kW Bidirectional Onboard Charger Reference Design [2] supports operation from a universal single-phase input off the AC grid and provides full output power (6.6 kW) to the load at an input voltage of 208 VAC and above. Below this input voltage level, the output power is linearly derated. The main target of this reference design is to deliver the maximum possible power to the battery, with a power density level greater than 60 W/inch3 (3.66 kW/L) and a battery voltage range between 250 V and 450 V. Additionally, this OBC design supports bidirectional operation. **Table 2** lists the power-supply specifications.

Parameter Description	Minimum	Typical	Maximum	Units
AC input voltage	90	220	264	VRMS
AC input current			32	ARMS
DC output voltage	250	400	450	V
DC output current (CC mode)			20	A
DC output power (CP mode)			6.6	kW
Power density	60			W/inch3
EMI compliance level		CISPR 32, Class B [9]		
AC line frequency	47		63	Hz
Power factor (full load)	0.99			
Cold-plate coolant temperature		65	85	°C

Table 2. *Power-supply specification for the 6.6-kW OBC reference design.*

Figure 11 is a block diagram of the 6.6-kW OBC reference design.

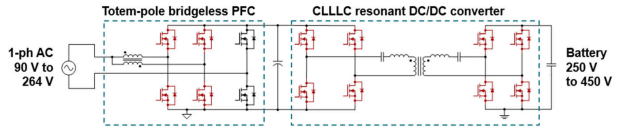


Figure 11. *Block diagram of the 6.6-kW OBC reference design.*

Both the PFC stage and the DC/DC converter leverage 30-mΩ automotive-qualified 650-V **LMG3522R030-Q1** GaN FETs for control by a single C2000™ **TMS320F28388D** real-time microcontroller (MCU). In total, the converters use 12 GaN FETs; the low-frequency FETs for the bridgeless input rectifier are regular silicon MOSFETs.

PFC Stage

To reach a power density target of more than 60 W/inch^3, it's important to design the PFC with the smallest possible number of components while still maintaining good efficiency and keeping the components within their thermal limits. With these requirements, the topology of choice is the totem-pole bridgeless PFC [10][11].

After having selected the PFC topology, the next step in the design process is to decide on a mode of operation:

CCM or critical conduction mode (CrCM). For both modes of operation, **Figure 12** illustrates the envelope of the actual current waveform and the average current waveform for a single AC half cycle.

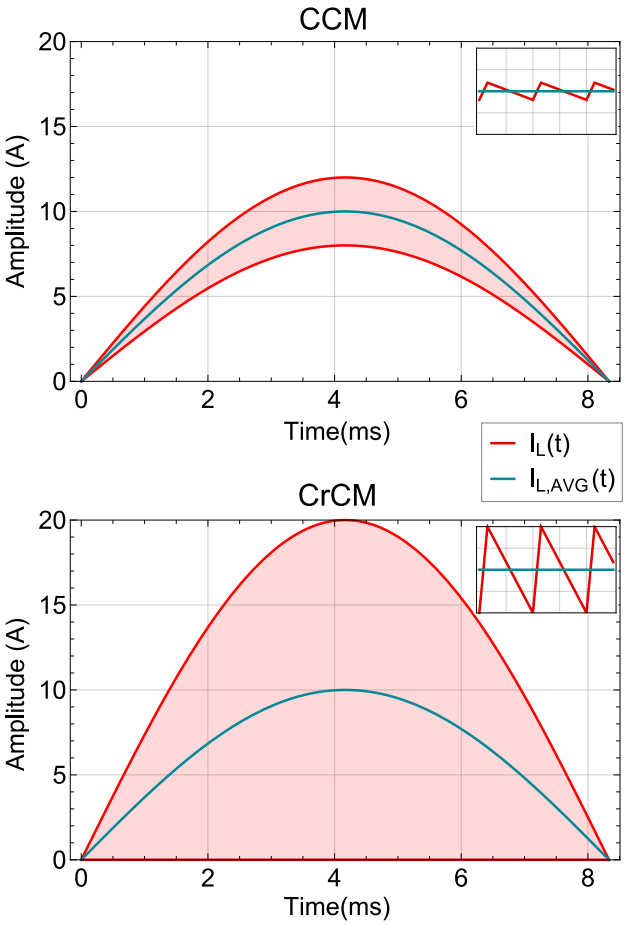


Figure 12. *CCM (top) and CrCM (bottom) PFC current waveform envelopes (red) and average currents (blue).*

The average current is identical for both modes, but by leveraging different inductance values and control schemes, the shape of the actual current waveform is completely different.

CCM operation offers a smaller inductor current ripple and thus smaller root-mean-square (RMS) current stress in the FETs. CrCM operation enables zero-voltage switching of the FETs when the input voltage is smaller than half the output voltage. For higher input voltages, it is possible to turnon the FETs with a reduced voltage, because the current always returns to 0 A before every new switching cycle.

With CCM operation, the power stage is hard switching, which means that the FETs will exhibit losses at every turnon and turnoff transition. Thus, CCM produces higher switching losses in the FETs than CrCM operation.

Large reverse-recovery charge losses would prevent the use of CCM operation with silicon FETs. In CrCM, there are no reverse-recovery losses because the current always returns to 0 A. Given the zero reverse-recovery charge characteristic of directly driven TI GaN FETs, these losses are also out of the equation for CCM operation and make it an attractive alternative.

Choosing an inductance value for CrCM operation that's several times smaller than in CCM has the potential to reduce inductor size. The peak and RMS currents in the FETs will be several times larger than in CCM, however.

For the 6.6-kW OBC reference design and its 30-mΩ TI GaN FETs, the larger RMS currents would have required the use of a three-phase CrCM PFC approach in order to keep all components within their thermal limits. In CCM, with a two-phase approach, the GaN FETs would stay within their thermal limits.

A multiphase approach distributes the losses among more components and spreads them to a wider area. In addition, these components may have slightly more disadvantageous parameters, such as higher direct current resistance (DCR) and lower I_{sat} for inductors, or higher $R_{DS(on)}$ for the FETs than in a single-phase configuration. Thus, leveraging a multiphase converter makes it easier to find more cost-effective and fitting components for a high-power design.

Figure 13 shows the relative loss reduction for one-, two- and three-phase 6.6-kW CCM PFC switching at 120 kHz. The loss reduction from one to two phases is roughly 40%. Adding a third phase makes sense if the main design target is to maximize efficiency.

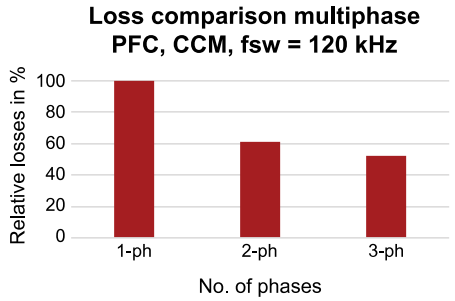


Figure 13. *Loss comparison for different numbers of phases for a CCM PFC switching at 120 kHz using 30-mΩ TI GaN FETs.*

Three factors determine the choice of operating switching frequency: the power density target, the efficiency and the electromagnetic interference (EMI) limit lines. There will have to be a trade-off between raising the switching frequency to improve the power density and reducing the switching frequency to optimize converter efficiency.

It is also important to remember the worst-case limit lines of the EMI standard against those you need to test the design to test the design. For multiphase converters, consider the effective switching frequency for the electromagnetic measurement, which is n-times the base switching frequency of each phase, where n is the number of phases. You also need to consider that the switching frequency for a PFC converter operating in CrCM is variable, which requires a more complex EMI filter design. **Figure 14** shows the limit lines for CISPR 32 Class B.

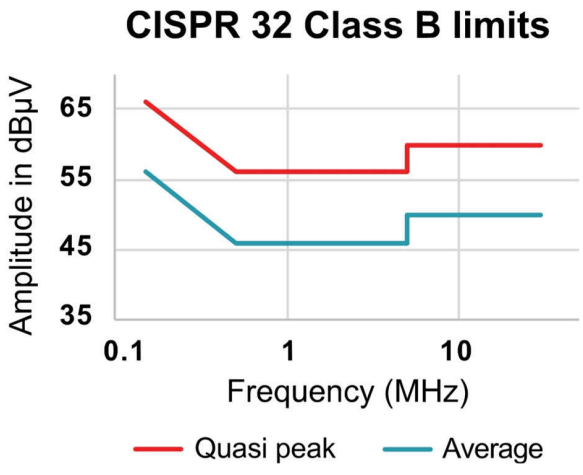


Figure 14. *CISPR 32 Class B limits.*

A switching frequency of 120 kHz was chosen for this design, as the losses per GaN device would still keep them comfortably below the recommended maximum junction temperature, while the power dissipation is in a range that enables PFC efficiency of more than 98%.

Figure 15 illustrates the TI GaN FET losses over switching frequency for two different thermal resistances. The end of each graph indicates where the device reaches its maximum acceptable junction temperature.

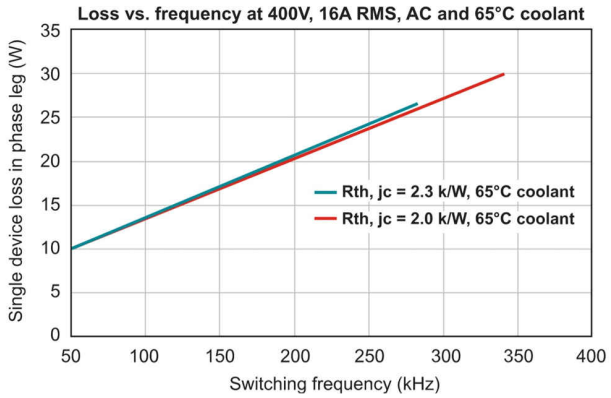


Figure 15. *Single GaN device losses vs. switching frequency for different thermal resistances to the thermal interface.*

Using a negatively coupled inductor instead of two separate PFC inductors will further improve the power density of an interleaved dual-phase totem-pole PFC converter. Negative coupling means that the orientation of the coupled winding ends is inverted (as shown in **Figure 11**), where the coupling dots are located at opposite sides.

The resulting ripple-current cancellation in this negatively coupled configuration can significantly lower the required inductance for each leg compared to a single inductor, while having a similar output ripple level. And, also introduces the option to use a slightly smaller core. For this design, the volume reduction was around 30% compared to a two-phase PFC implementation using two separate inductors.

Figure 16 shows the effect of the coupling coefficient on the RMS current per phase for different self-inductance values.

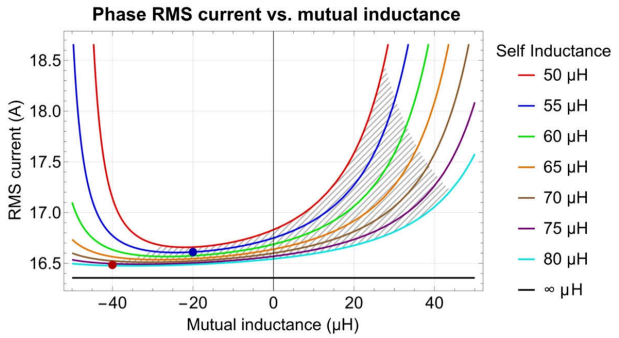


Figure 16. *Single-phase RMS current vs. mutual inductance: the grayed-out area is not manufacturable, the blue dot indicates the optimal combination, and the red dot represents the coupled inductor used in the 6.6-kW OBC reference design.*

Choosing the correct values for the self- and mutual inductance of this coupled inductor is a bit tricky, because the optimal simulated results are mechanically not manufacturable, as indicated by the grayed-out area in **Figure 16**. Only by having a "bad" coupling coefficient can you achieve the optimal ripple-current cancellation. The worse coupling also reduces the common-mode noise generated by the coupled inductor.

When using an interleaved approach, two phases with a 180-degree phase shift and negative coupling yield better ripple-current cancellation than positive coupling. The coupled inductor used in the 6.6-kW OBC reference design leverages two stacked 0079439A7 Kool Mμ® Max 60-μ cores with 77 μH of self-inductance, a coupling coefficient of 55% and a DCR of 12 mΩ per winding.

Measured efficiency data for the PFC (**Figure 17**) shows that it is possible to reach more than 98% efficiency at 30% output power and above, leveraging 650-V 30-mΩ GaN FETs in a very compact form factor.

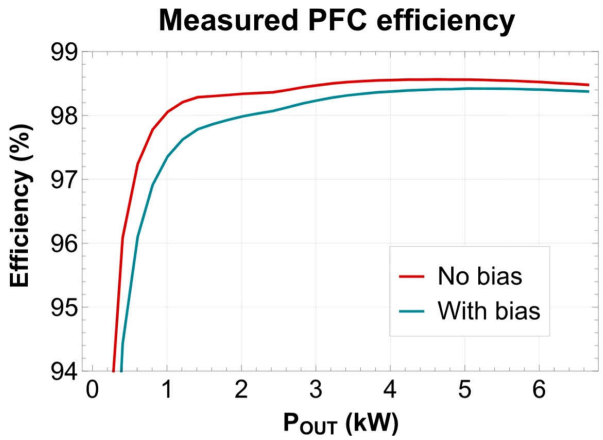


Figure 17. *Measured efficiency of the PFC converter accounting for the bias supplies (in blue) and not accounting for the bias supplies (in red).*

DC/DC Stage

The primary goals for the GaN-based OBC reference design are to minimize overall solution volume and maximize the electrical efficiency of the power conversion. To effectively optimize these parameters, the DC/DC stage must meet a few critical requirements. First and foremost, this converter is a battery charger. The wide range of output voltage values that the output needs to cover present significant challenges to many topologies; see the highlighted levels in **Table 3**. For example, a popular topology such as an inductor-inductor-capacitor (LLC) converter may have some difficulty meeting high efficiency over such a wide output range. In addition, the bidirectional nature of the converter might require a traditional LLC to have some additional tank components and facilitate the necessary gain.

Description	Minimum	Typical	Maximum	Units
DC output voltage	250	400	450	V
DC output current			20	A
DC output power			6.6	kW

Table 3. *DC/DC converter requirements.*

The final solution achieved an efficiency of just over 98%, as shown in **Figure 18**.

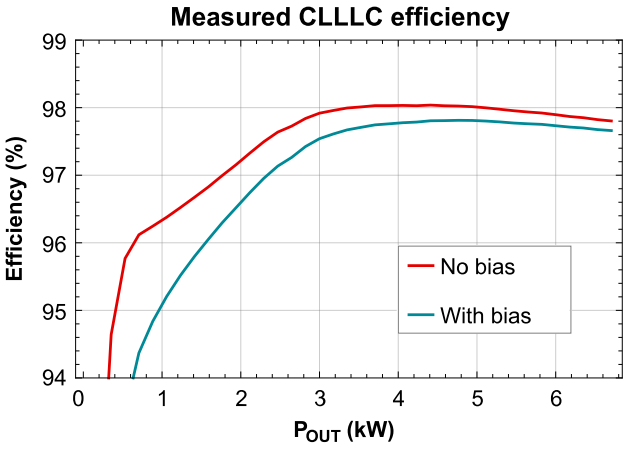


Figure 18. *Measured efficiency of the capacitor-inductor-inductor-inductor-capacitor (CLLLC) converter.*

For context, **Figure 19** shows some essential waveforms during operation at full load.

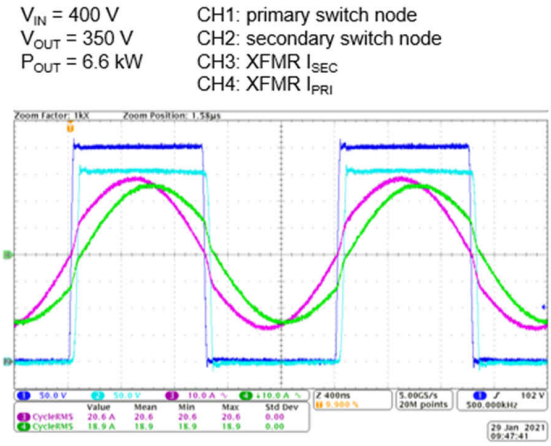


Figure 19. *CLLLC essential waveforms at full load.*

Topology selection, operating frequency, tank design, operating modes, thermal management, layout and control optimization are among some of the more significant design challenges that we solved in the course of the GaN-based OBC reference design. Now, let us explore these challenges more, along with the rationale behind our decision-making.

DC/DC Topology Selection

In order to determine how to meet size, efficiency and output voltage regulation requirements, we evaluated two topologies in detail: the CLLLC (**Figure 20**) and the dual active bridge (DAB) (**Figure 21**).

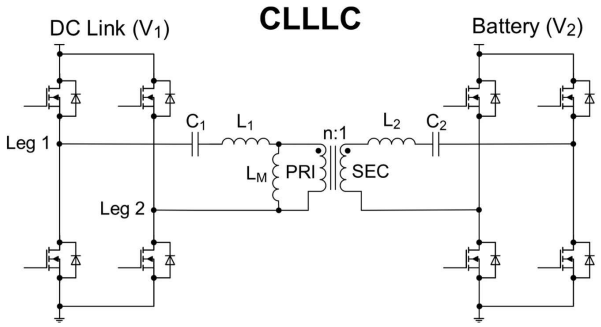


Figure 20. *CLLLC schematic.*

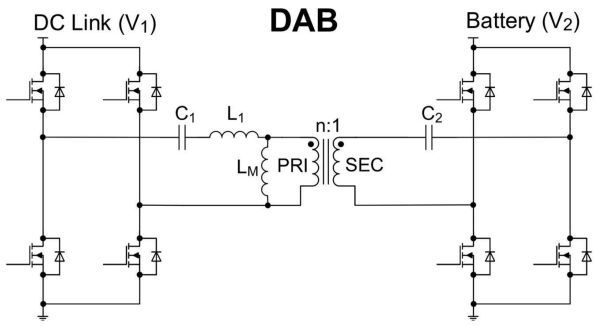


Figure 21. *DAB schematic.*

Both of these converters have the same fundamental structure. They both have a full bridge on the primary and secondary, and roughly the same reactive components. The fundamental differences are how the topologies are controlled, and the relative size of the reactive components.

It is beyond the scope of this paper to provide a detailed design procedure for both topologies. However, it is worth taking a look at the results of our comparison.

Figure 22 shows two sets of graphs: one for the CLLLC and the other for the DAB. The plot on the left shows the RMS current in the GaN switch. The plot on the right shows the GaN FET drain-to-source voltage (V_{DS}) at turnon. These plots provide essential information on how efficient the switches will be in each topology. A low RMS current means fewer I^2R losses, while a lower V_{DS} means lower switching losses. In the end, the highest efficiency will occur when the RMS currents are as small as possible and V_{DS} at turnon is as close to zero as possible.

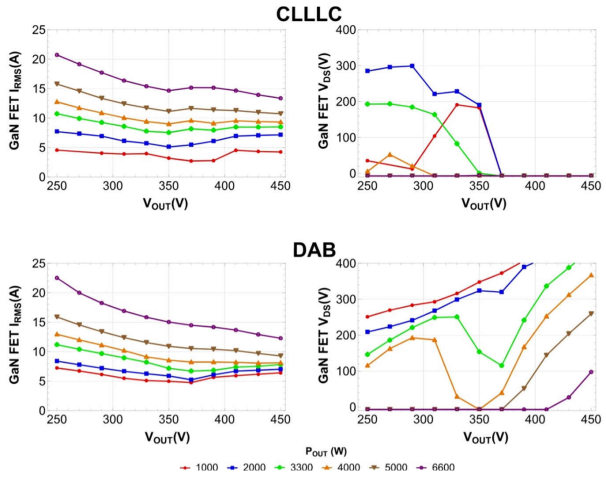


Figure 22. *CLLLC and DAB performance comparisons.*

Examining the plots in **Figure 22** reveal that the CLLLC converter has lower RMS current when the output voltage is smaller. The reduced RMS current is critical to enabling the charger to put out as much power as possible at low voltages. Additionally, the CLLLC operates with more conditions where zero voltage switching (ZVS) is maintained.

These facts imply that the CLLLC converter will be more efficient, and therefore easier to cool. The CLLLC converter will also result in a smaller solution.

Frequency Selection

Raising the frequency of a switched-mode power supply results in a size reduction of many of the reactive components. The transformer is typically the largest single component in the DC/DC converter, and its physical size is highly dependent on operating frequency. The high efficiency of a GaN switch at elevated frequencies is the fundamental tool for reducing solution size.

Figure 23 shows how the operating frequency affects the transformer volume in a CLLLC converter. The transformer volume is normalized to the volume at 100 kHz, which means that at 500 kHz, the volume of the transformer should be about 35% of what a 100-kHz design would be. This enormous volumetric reduction means that designers will need to consider a few other factors before deciding on the exact switching frequency.

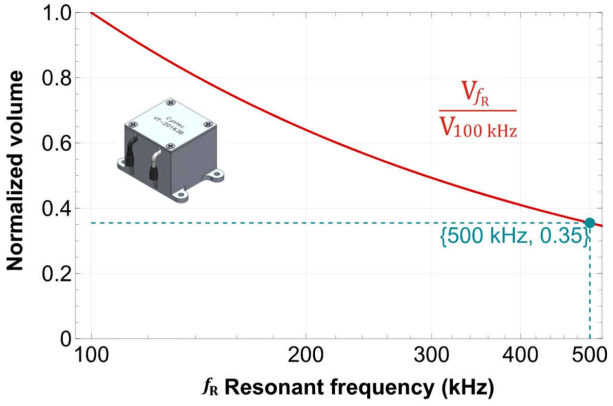


Figure 23. *Transformer volume vs. frequency.*

Core Loss

Controlling transformer core loss is a priority, especially high-frequency transformers. **Equation 2**, the Steinmetz equation, shows the relationship between loss density in the core and frequency:

$$P_{FE} = k\, f^{\alpha} B_{PK}^{\beta} \qquad (2)$$

where P_{FE} is the loss per unit volume; f is the excitation frequency; B_{PK} is the peak flux density in the core; k, α and β are material constants.

From **Equation 2**, it is apparent that as the frequency increases, so will the losses. The losses in modern magnetic materials start to become difficult to manage when the switching frequency goes much above 1 or 2 MHz.

Loss of ZVS

While the CLLLC converter does an excellent job maintaining ZVS over a wide range of conditions, there are still many situations in which it cannot. **Figure 21** shows several operating points that partially or even fully lose ZVS. The ability to maintain ZVS is complicated by the fact that a CLLLC converter uses frequency modulation as the primary control mechanism for maintaining output regulation. It turns out that most, if not all, of the conditions where the CLLLC converter loses ZVS are at a lighter load and at frequencies well above resonance (more on this later). The switching losses in these conditions will be proportional to that

operating frequency. Fundamentally, if the operating frequency gets too high, the converter may overheat at a light load.

Dead Time

The time required for ZVS is a function of the parasitic capacitance connected to the switch node and the current source driving that capacitance, which tends to be dominated by the GaN FET short-circuit output capacitance (C_{OSS}). In order to avoid hard switching, the CLLLC converter needs to allow this voltage to transition in a resonant manner. Since facilitating these transitions consumes a significant portion of the tank energy, the dead time essentially reduces the efficiency since no meaningful power transfer occurs. As the switching frequency becomes large, the overall dead time can become a significant percentage of the overall switching period.

ISR Bandwidth

The interrupt service routine (ISR) is a software routine that performs the time-sensitive calculations necessary to regulate the converter output and manage system-level protection. There are limits on how many instructions the microcontroller can do during its ISR. A single 200-MHz C2000 core can provide approximately 170 million instructions per second, with which it can comfortably control both a two-phase 120-kHz PFC and a 500-kHz resonant CLLLC. Higher operating frequencies might require the use of an additional processor, which could make the design both larger and more expensive.

Overall

Taking into consideration the volumetric benefits of GaN and the aforementioned frequency-related challenges, we decided that a 500-kHz resonant frequency with an upper frequency limit of 800 kHz would provide the best overall size without the negative side effects.

Resonant Tank Design

After selecting the operating frequency, we needed to determine six tank elements, shown in the highlighted boxes in **Figure 24**. Although the procedure we are about to describe will create a very reasonable starting point, it will not provide an exact solution. In general, it is difficult, if not impossible, to come up with an exact solution without detailed simulation and analysis. Real hardware always reveals subtleties not evident in the design phase. Still, it is almost always helpful to get to a reasonable starting point quickly, from which you can fine-tune a design as necessary through simulation and then hardware.

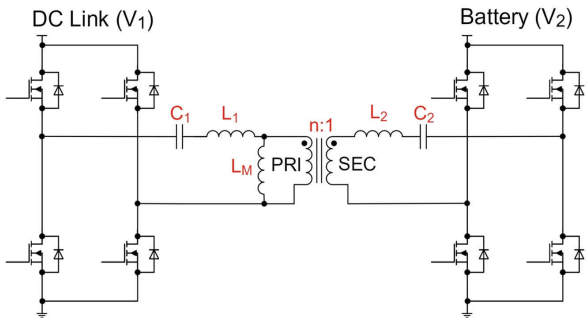


Figure 24. *CLLLC essential parameters.*

The design of the tank elements will have a profound effect on converter efficiency, thermal performance and size. Our primary considerations included:

- Core losses:
  - Impacted by frequency, turns ratio and core size.
- Winding losses:
  - The tank elements determine the winding currents.
  - Inductances may drive larger gaps that can induce more losses caused by fringing.
- FET conduction losses:
  - The tank elements determine the FET current.
- Maintaining ZVS:
  - The tank current (and in particular the magnetizing inductance) determine whether it's possible to maintain ZVS.

- Magnetics integration:
  - Only realistic ratios of leakage inductance to magnetizing inductance can make magnetics integration physically realizable.

Consider the gain required in order to supply the necessary output voltage and current during charging and discharging. Both the turns ratio (n) and the magnetizing inductance (L_M) have the largest influence on the required gains. The best designs often require iteration to see which combination yields the highest efficiency. It usually makes sense to start with n, since it has a bigger influence than L_M.

Resonant converters are most efficient when operating at or near the resonant frequency. Battery-charger requirements dictate that the converter charge with as much power or current as possible, meaning that the required current will be greatest when the output voltage is at its lowest. Choose n such that the converter operates with the lowest tank current possible when the required charge current is greatest. The converter will then operate close to resonance, and most importantly at its highest efficiency.

Figure 25 illustrates the operating point for the design where the secondary current is largest. This point dictates how to choose n.

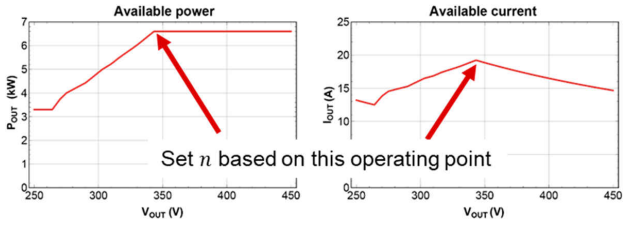


Figure 25. *Turns ratio selection.*

While L_M affects both ZVS and gain, look at its impact on ZVS. **Equation 3** through **Equation 7** quantify the behavior during the switching transient, illustrated in **Figure 26**.

Equation 3 is the basic differential equation that defines how the magnetizing current evolves with time during a one-half cycle of switching:

$$V_{DC\_LINK} = L_M \times \frac{dI_{L_M}(t)}{dt} \quad (3)$$

where V_{DC_LINK} is the converter input voltage and $I_{L_M}(t)$ is the magnetizing current.

Since the applied voltage is constant, it is possible to simplify **Equation 3** to **Equation 4**:

$$V_{DC\_LINK} = L_M \times \frac{\Delta I_{L_M}}{T_S/2} \quad (4)$$

where ΔI_{L_M} is the change in the magnetizing current during a one-half cycle.

Equation 5 is the differential equation that defines how the GaN FET V_{DS} will evolve over time. A common assumption is that $I_{L_M}(t)$ is a constant during the dead time, but this is in fact not true. Making this assumption, however, will get you to a reasonable starting point.

$$I_{L_M}(t) = 2 \cdot C_{OSS} \times \frac{dV_{DS}(t)}{dt} \quad (5)$$

where $V_{DS}(t)$ is the GaN FET V_{DS}.

Since the current driving the FET is one-half the total delta, you can simplify **Equation 5** to **Equation 6**:

$$\Delta I_{L_M}/2 = 2 \times C_{OSS} \times \frac{V_{DC\_LINK}}{t_d} \quad (6)$$

where t_d is the dead time.

Simultaneously solving **Equation 5** and **Equation 6** results in **Equation 7** – the L_M that will facilitate ZVS in the targeted dead time:

$$L_M = \frac{t_d \times T_s}{8 \times C_{OSS}} \quad (7)$$

where T_S is the switching period.

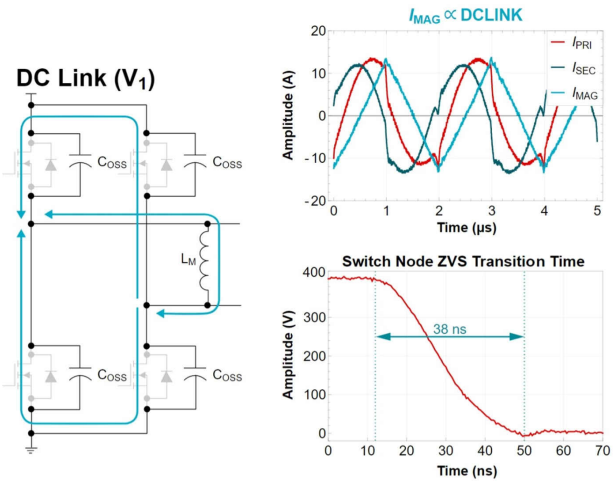


Figure 26. *ZVS considerations.*

Figure 26 illustrates the path that the current takes in the LM to charge and discharge the C_{OSS} capacitances of the GaN FETs. The measured waveforms show the primary, secondary and magnetizing currents. The switch-node transition time achieved with a 14-µH LM was 38 ns.

As a side note, **Equation 3** through **Equation 7** predict an L_M value of 20 µH. 14 µH was used in order to better enhance ZVS over a wider range of operating points and help achieve the necessary gain.

Then, first harmonic analysis (FHA) was used to assess the converter's overall ability to meet the charge and discharge profiles. **Figure 27** illustrates the method. Essentially, replacing the switch networks with sinusoidal equivalents makes it possible to analyze the tank elements using classic S-domain frequency analysis.

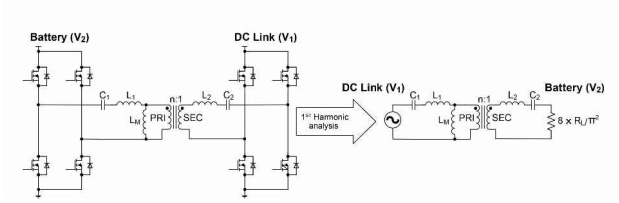


Figure 27. *FHA method.*

From here, some assumptions were made to reduce the number of variables. First, that the inductance on both sides of the isolation barrier is equivalent through the turns ratio. Mathematically, this means $n^2 = \frac{L_1}{L_2}$.

Next, the capacitance ratio was set, $m = \frac{C_2}{n^2 \cdot C_1}$, such that $f_1 = f_2$. This means that $m = 1$.

With these assumptions, all that remains is to select the ratio, $k = \frac{L_M}{L_1}$, which will adjust the tank gain such that it is possible to meet the charge and discharge profiles. Plotting the charge and discharge curves for various values of k and selecting the design point that best maps to the required gain will determine k. **Figure 28** illustrates the values.

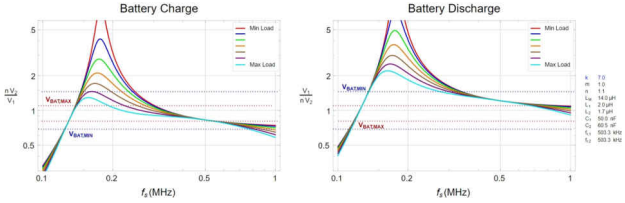


Figure 28. *FHA gain curves.*

Thermal Solution

Figure 29 shows the complete solution with the cold plate attached. The solution uses liquid cooling with a maximum coolant temperature of 65°C. All hot components access the cold plate from the back side of the printed wiring board (PWB).

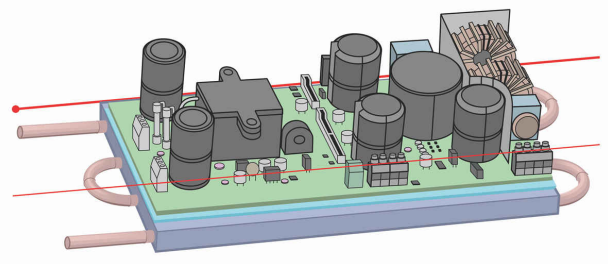


Figure 29. *3D image of the complete solution.*

Figure 30 shows a cross-section of this solution illustrating how the GaN FETs interface to the PWB and cold plate. Using a thermal interface material (TIM) will facilitate heat transfer from all hot spots.

Figure 30 also shows the placement of the TIM relative to the cold plate and GaN FETs. The FETs themselves have a $\theta_{Junction\text{-}Case}$ of 0.15°C/W. The TIM has a thermal impedance of 1.2 to 1.25°C/W. Overall, $\theta_{Junction\text{-}ColdPlate}$ is 1.35 to 1.5°C/W.

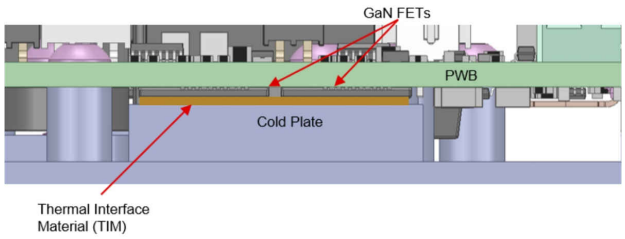


Figure 30. *Magnified cross-section of the 6.6-kW OBC reference design PWB.*

Figure 31 shows the bottom side of the PWB, while **Figure 32** shows the top side of the cold plate. By comparing these images, you can see how the cold-plate features provide access to the thermally significant components highlighted in **Figure 31**.

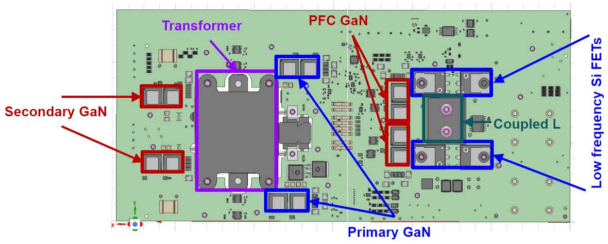


Figure 31. *Bottom view of the 6.6-kW OBC reference design PWB.*

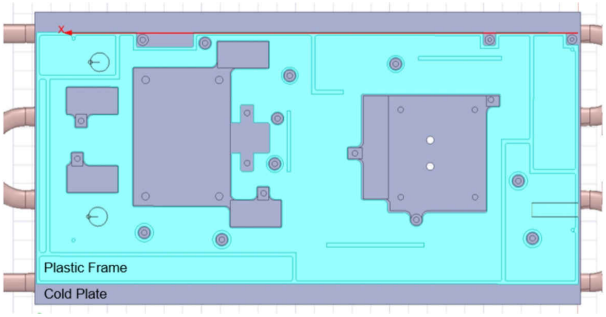


Figure 32. *Top view of the liquid-cooled cold plate.*

Figure 33 is a thermal scan of the top side of the board. Given that the significantly hot components are located on the bottom side, there is very little of interest to see here.

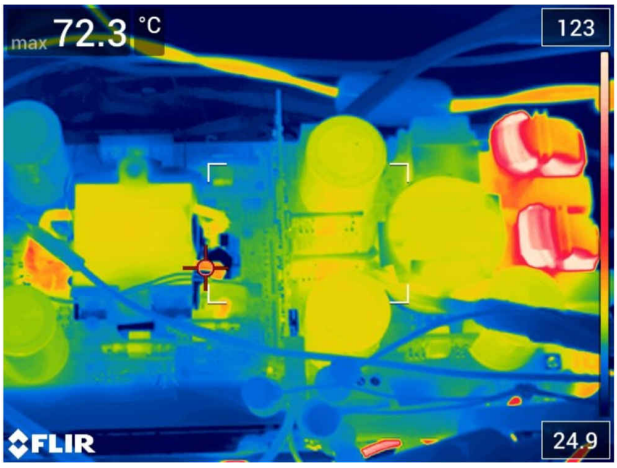


Figure 33. *Thermal scan of the top side of the 6.6-kW OBC.*

Layout Best Practices

As the power density increases, an optimal layout becomes even more important in order to guarantee a low noise floor and good signal integrity. In addition, GaN FETs have a much higher switch-node transient voltage (dv/dt) than silicon or SiC. Preventing dv/dt from coupling unwanted noise into sensitive nodes requires careful layout planning.

The first step in a high-quality layout is to ensure that the GaN FETs have a low inductance decoupling loop in order to minimize switching losses and minimize V_{DS} overshoot. Without this, excessive ringing on the drain-to-source can negatively impact stability, signal integrity and EMI.

Figure 34 shows the layout of one of the CLLLC's half bridges that uses a vertically oriented switching loop with high-frequency decoupling capacitors on the left, a low-side GaN FET in the center, a high-side GaN FET on the right, and two resonant capacitors above the high-side GaN FET.

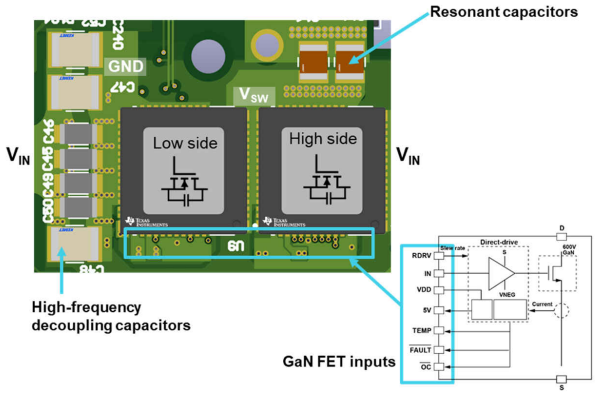


Figure 34. *GaN FET PWB component placement and decoupling.*

In order to visualize the benefits of this layout, **Figure 35** shows the conduction paths when the high-side device turns on with hard switching. The fast rate at which these switches turnon and off results in very large transient currents (di/dt). If these conduction paths have an appreciable inductance, excessive voltage spikes will occur.

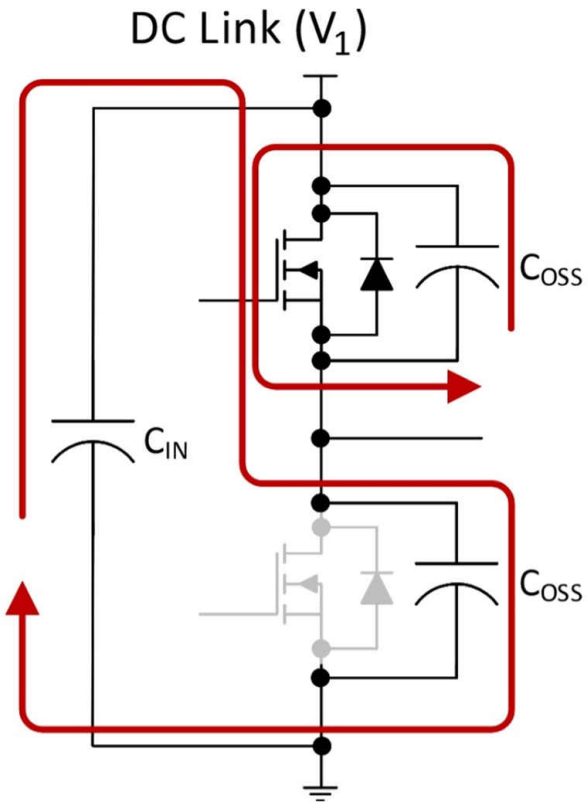


Figure 35. *Schematic of hard-switching turnon current-loop conduction path.*

Equation 8 estimates the inductance:

$$L = \frac{\mu_0 \mu_r N^2 A_e}{l_e} \quad (8)$$

where μ_0 is the permeability of free space ($4 \times \pi \times 10^{-7}\ H/m$), μ_r is the relative permeability (in this case, 1), N is the number of turns (in this case, one), A_e is the area of the conduction path and l_e is the magnetic path length.

Figure 36 is a simplified cross-section of the PWB bottom-side components, with the hard-switching turnon edge-conduction current shown in red. The vertical scale of the image was exaggerated to make it easier to see; in reality, the total board thickness is about 90 mils. Notice that the loop created by the current has a very small area, which implies that the inductance is very small, as shown in **Equation 8**.

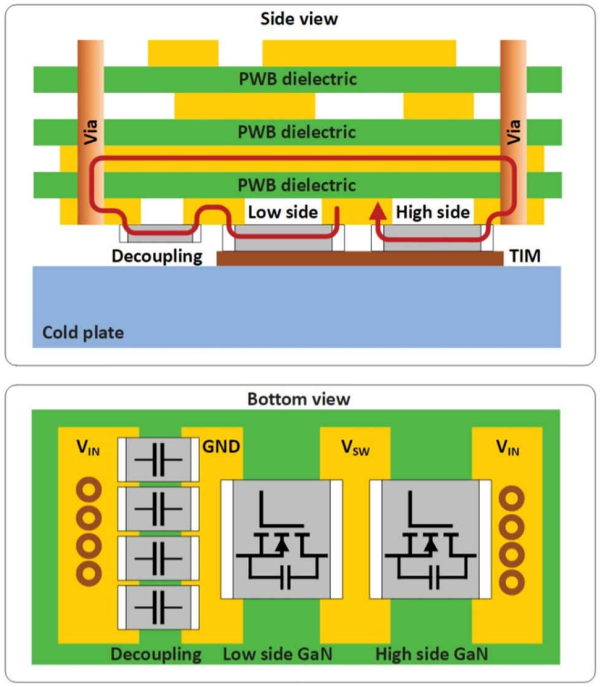


Figure 36. *Simplified low-inductance decoupling loop: views from the side (top) and above (bottom).*

Figure 37 shows the actual bottom-side component placement and routing for layer 8. This placement and routing reflects the same concept for the power loop illustrated in **Figure 36**. Red indicates the switch node, green indicates the primary-side ground, blue is the DC

link, and gray indicates the different input signals to the GaN FETs. The cold plate electrically connects to ground.

None of the signals shown on the snippet of layer 8 are equal to the voltage potential of the cold plate. Essentially, the cold plate acts as one side of a large capacitor. Since the GaN FET switch nodes create very large dv/dt, minimizing the influence of this parasitic capacitance must be a priority. Extra capacitance on the switch node will slow down the switching transition and create more losses.

Additionally, all of the inputs of the high-side GaN FET are referenced to the switch node, which means that they experience the same dv/dt with respect to ground and the cold plate.

There are no components on the bottom side associated with the GaN FET inputs. There are also minimal copper features on the inputs so as to avoid any coupling to the cold plate that might induce noise.

Layer 7 provides the power-loop decoupling return path from **Figure 36**, shown in blue. Adding a shield protects any coupling to pins and traces on layer 8. This shield also protects the vias on layer 7 from noise coupling to the input voltage plane.

Layer 6 creates a void in the same location of layer 7's shield to prevent capacitive coupling to the inputs.

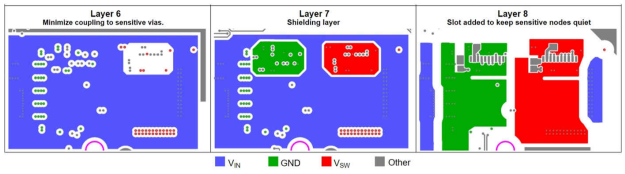


Figure 37. *GaN half-bridge layout – bottom-side considerations.*

Figure 38 shows the top-side features, with sensitive components and traces added to the top of the PWB. Keeping these components within a small area avoids any additional noise coupling. Layer 2 is used for interconnect, while layer 3 contains another shield to protect the components and traces on layers 1 and 2 from noisy signals not referenced to the switch node.

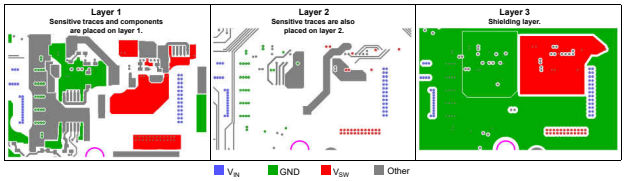


Figure 38. *GaN half-bridge layout: top-side considerations.*

Control-Loop Considerations

Figure 39 shows the control system block diagram for the DC/DC converter. Because the system is isolated, it is necessary to cross the isolation barrier twice: once to deliver the control signals to the secondary-side GaN FETs and once to provide feedback to the MCU residing on the primary side.

The purpose of the feedback control loop is to minimize the impact of the PFC 100-/120-Hz output voltage ripple on the CLLLC output current, maintain stability and prevent jitter. Essentially, the control loop needs to manage the bandwidth to charge the battery while preventing excessive currents in that battery. In general, it is possible to achieve low ripple battery currents with 1 to 2 kHz of bandwidth.

Given that GaN enables a higher switching frequency, the bandwidth is mostly limited by the need to prevent unwanted jitter. One of the biggest limiters to bandwidth is noise pickup on the board. Since the noise travels a long distance through many stages across the secondary, it's critical to filter this path. The long noise-sensitive routing is compounded by the fact that both the PFC and CLLLC are using one MCU, thus necessitating both good layout and proper filtering.

Noise-free feedback is essential to jitter-free operation. Proper layout is always the best line of defense; however, practical layout constraints always results in the pickup of noise. Once that noise is on the feedback node, the large gains in the compensator can produce significant pulse-width jitter. Fortunately, adding capacitance can suppress this noise.

One good place to add capacitance is at the output of the voltage divider. The high-voltage output requires the use of large resistor values to create the divider.

In addition to filtering noise, the capacitance at the feedback point creates a pole with those resistors. Preventing this pole from interfering with the required bandwidth necessitates a relatively small capacitor. The constraints on current feedback are not the same as voltage feedback.

This design uses a low-ohmic resistor for sensing, which enables the use of larger capacitors on the current feedback lines. Using a high-quality high-quality operational amplifier (op amp) to properly condition the signal will enable more heavy filtering of the analog-to-digital converter (ADC) input when placed directly on the ADC pin inputs. The ability to put capacitance on the ADC input pins is dependent on the op amp's ability to drive a capacitive load, which should be listed in the data sheet. It is best to place some capacitance in each location (**Figure 38**); however, with proper op-amp selection selection, the ADC pins may be the most effective location to filter.

In addition to capacitance, the MCU also uses oversampling and averaging of the ADC measurements to further reduce noise and increase the effective number of bits.

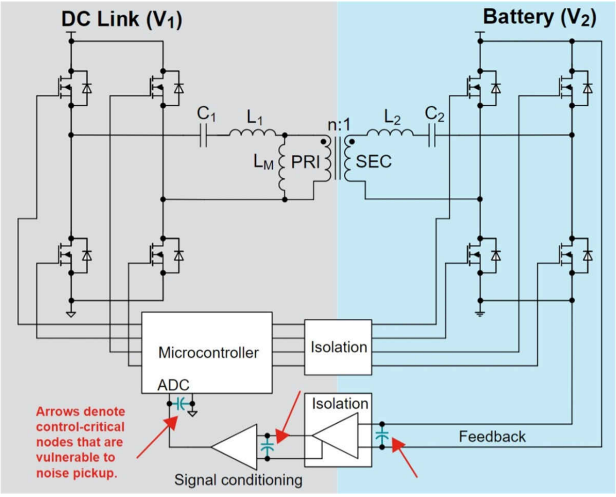


Figure 39. *Control-loop block diagram.*

Figure 40 shows what the MCU ADC output looks like after adding proper filtering to the system. Notice that the error floor is roughly within ±0.1%, a percentage that was definitely sufficient for the design, but on the surface might also seem small.

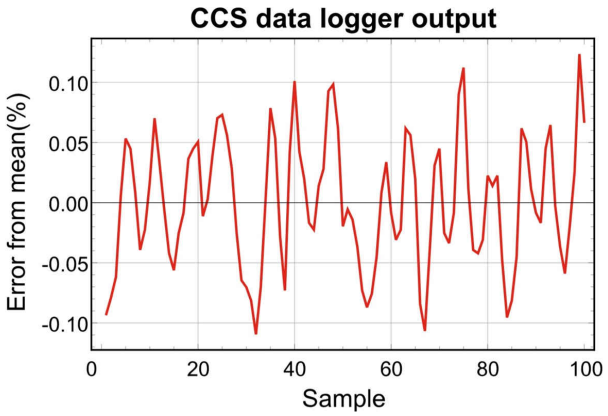


Figure 40. *ADC feedback noise floor.*

Figure 41 shows the gain and phase of the compensator as designed to deliver the required performance. When controlling a large output voltage (400 V) a large attenuation is required to get the signal to a level that the MCU can sense (typically less than 3.3 V). In order to get a reasonable bandwidth out of the system, the compensator may require a gain of 30 dB or more. A gain that large can make the system sensitive to very small noise variations.

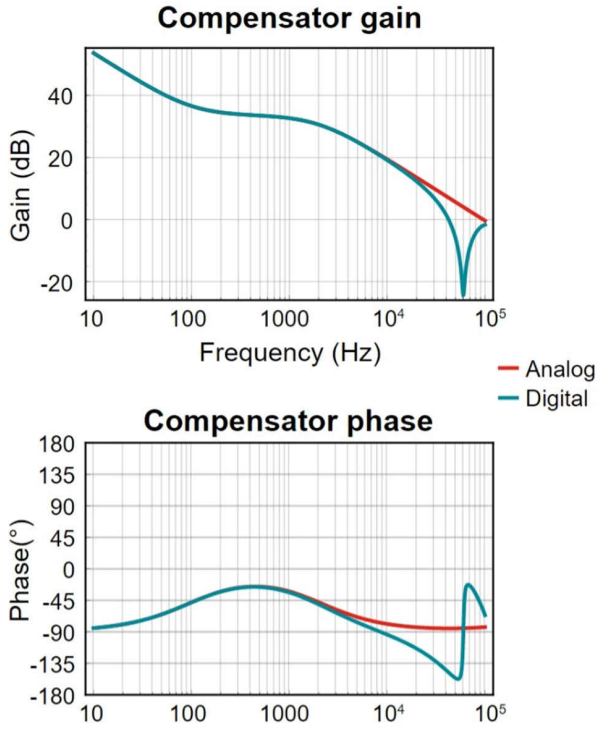
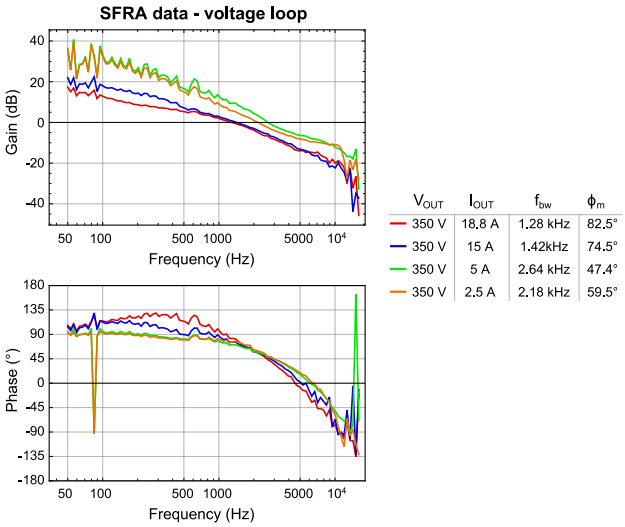


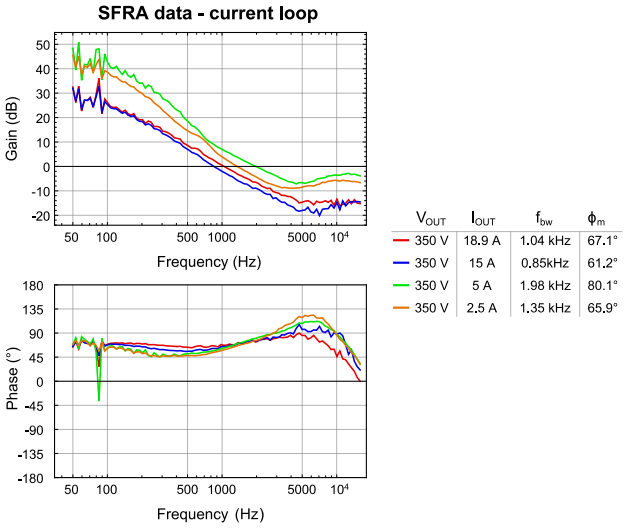
Figure 41. *Compensator Bode plot.*

Figure 42 shows the final Bode plots across load for both voltage and current feedback operation, with the former operating into a constant current load and the latter operating into a constant voltage load. What you cannot see with these plots is that in all cases, the duty-cycle modulation is well controlled without excessive jitter.



V_{OUT}	I_{OUT}	f_{bw}	ϕ_m
350 V	18.8 A	1.28 kHz	82.5°
350 V	15 A	1.42kHz	74.5°
350 V	5 A	2.64 kHz	47.4°
350 V	2.5 A	2.18 kHz	59.5°

Figure 42. *Bode plot loop dynamics for voltage control.*



V_{OUT}	I_{OUT}	f_{bw}	ϕ_m
350 V	18.9 A	1.04 kHz	67.1°
350 V	15 A	0.85kHz	61.2°
350 V	5 A	1.98 kHz	80.1°
350 V	2.5 A	1.35 kHz	65.9°

Figure 43. *Bode plot loop dynamics for current control.*

Conclusions

Figure 44 shows a picture of the final converter, while **Figure 45** shows the end-to-end efficiency operating at the highest output current condition. The power density of the design came out at 62.5 W/inch^3, or 3.8 kW/L.

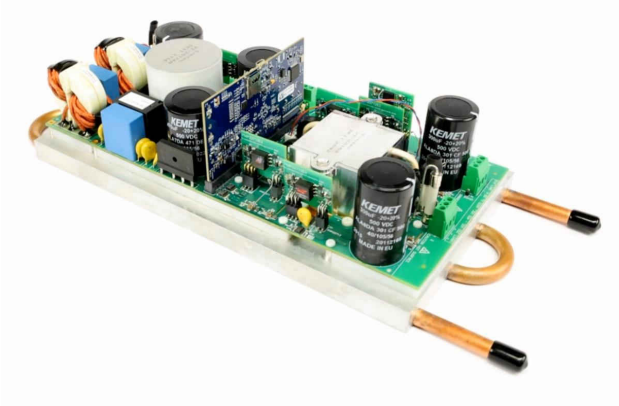


Figure 44. *6.6-kW OBC with liquid-cooled cold plate.*

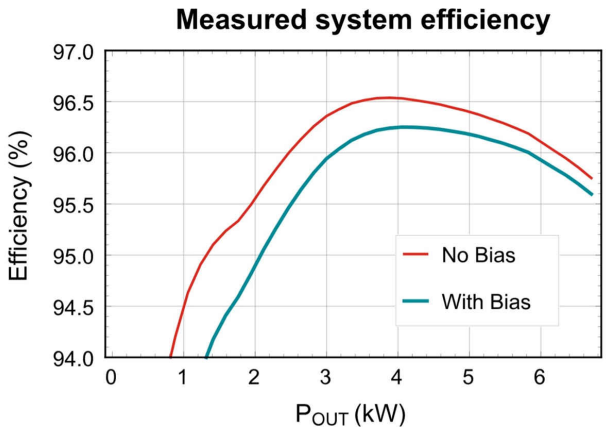


Figure 45. *Measured system efficiency of the 6.6-kW OBC.*

GaN's fast switching performance enables high-frequency power supplies that reduce size while maintaining high efficiency. With these high frequencies, a variety of challenges emerge, requiring cost-effective countermeasures that help maximize the benefits that come from high-speed switching.

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