

TI new battery pack solutions for light EV (LEV) and battery backup unit (BBU)

應用於輕型電動車 (LEV) 和後備電池組 (BBU) 的 TI 電池組解決方案

August 2021

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10s-16s Li-ion/LiFePO₄ battery pack with accurate cell voltage measurement and high-side MOSFET control: [TIDA-010208](#)

Features

- **High cell voltage and pack current sensing for accurate battery status data:**
 - $\pm 5\text{mV}$ @25°C; $\pm 10\text{mV}$ @0-60°C; $\pm 15\text{mV}$ @-40-85°C
 - $\pm 10\text{mA}$ (worse case $\pm 40\text{mA}$) @25°C, $< 2\text{A}$; $\pm 0.5\%$ error @25°C, $> 2\text{A}$.
- **Robust and programmable battery cell protections** COV, CUV, 2 levels OCD, OCC, SCD, OT and UT
- **Low power consumption**
 - Typical: Standby 100uA and ship mode 10uA.
- **Survive 120V PACK side voltage and reverse charger fault.**
- Unified platform for 10s, 14s and 16s mainstream system architecture
- Passive cell-balancing (effective current: 90 mA)
- ESD: Contact $\pm 8\text{kV}$ per IEC 61000-4-2

Target applications

- Server / telecom battery
- E-bike/scooter battery pack
- backup unit battery pack
- Garden tool battery pack

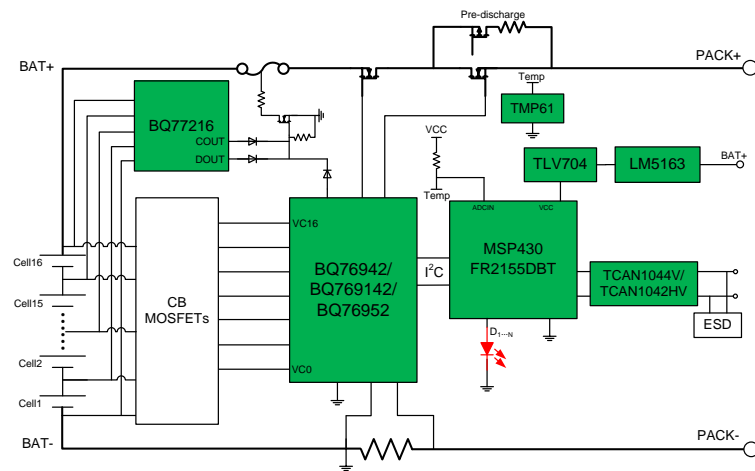
Tools and resources



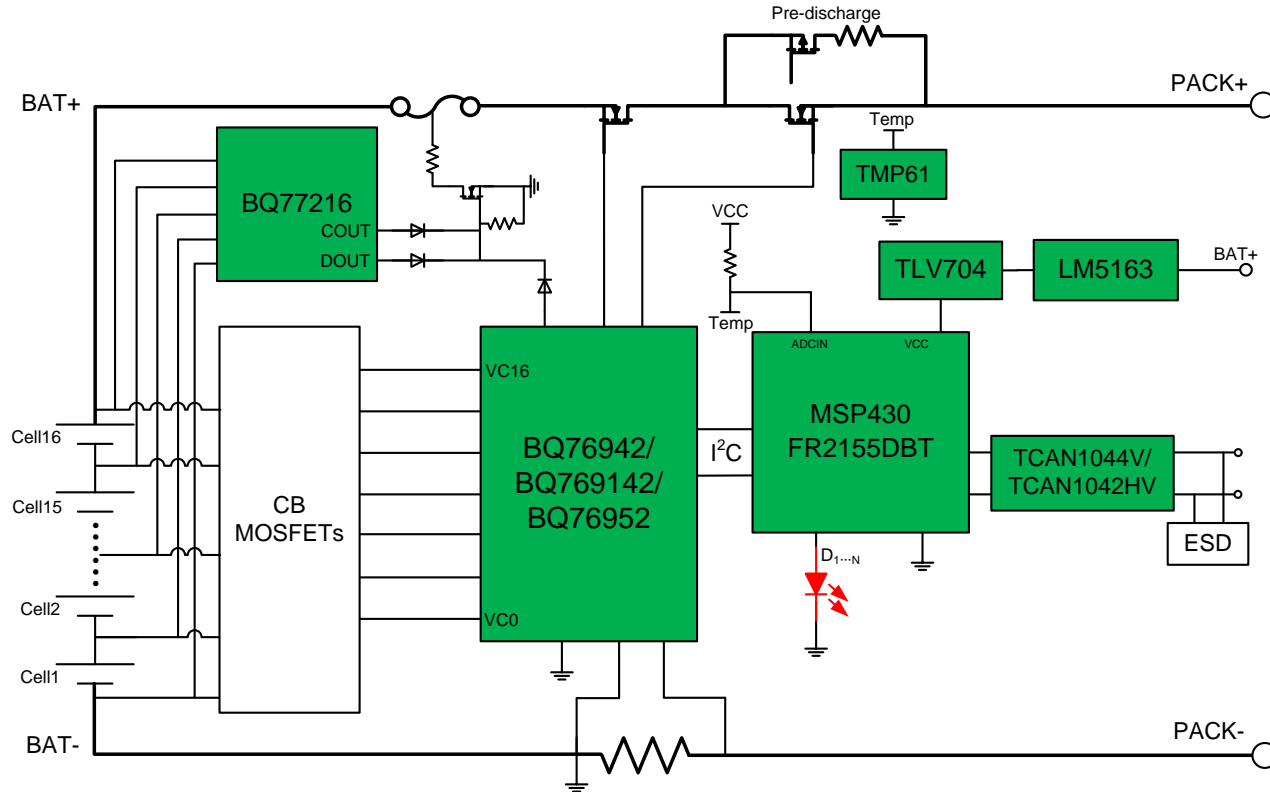
- **Design files:** Schematics, BOM, gerber
- **Device datasheets:**
 - [BQ76952/BQ76942/BQ769142](#), [BQ77216](#), [MSP430FR2155](#), [LM5163](#), [TMP61](#), [TLV704](#), [TCAN1042V/TCAN1044HV](#)

Benefits

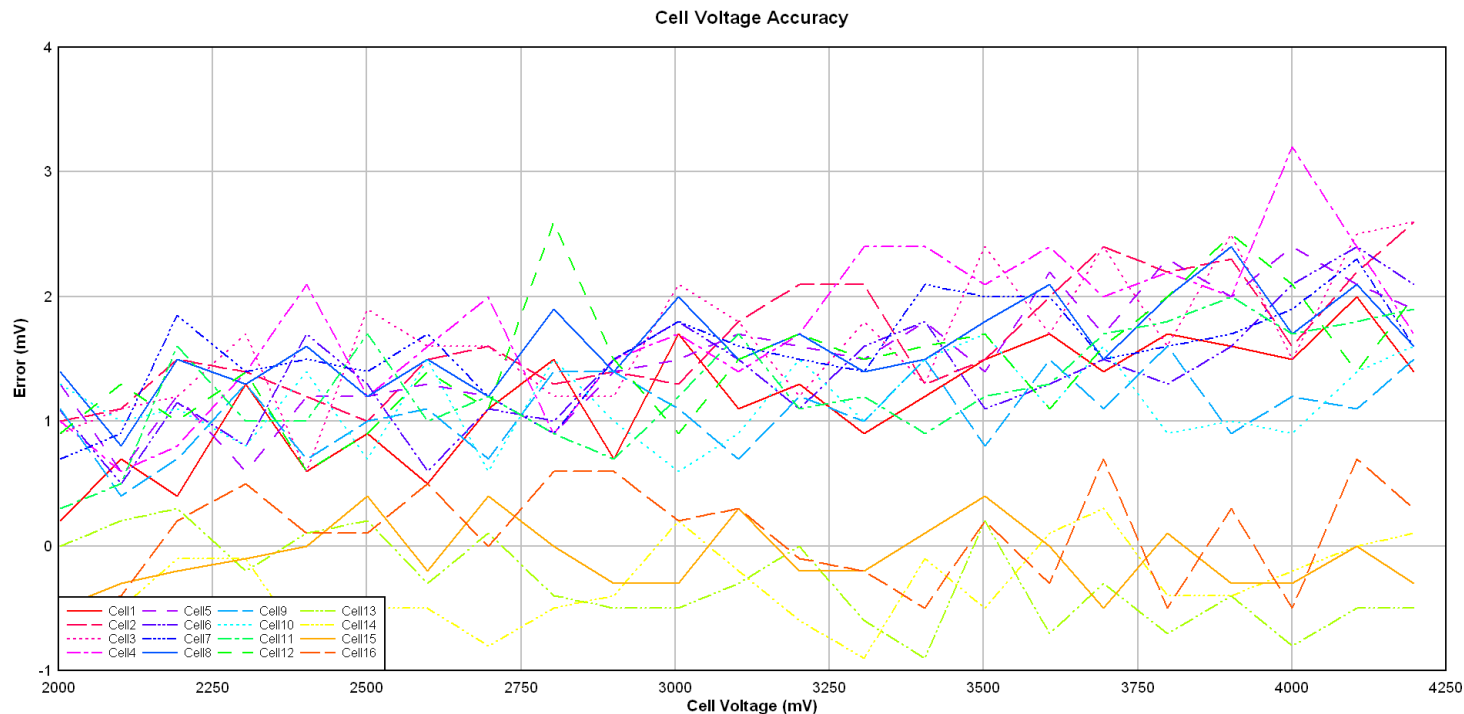
- Accurate voltage, current and temperature information of battery
- Robust full set protection to help ensure safety
- Low system-level current consumption to save power
- Highly integrated solution for system design
- Safe and effective cell balancing
- Cost effective
- One board to cover multiple platforms with P2P devices



System block diagram TIDA-010208



Cell voltage accuracy – before calibration



Cell Voltage Error < $\pm 5\text{mV}$

Input resistor: 100 Ω @Room temperature

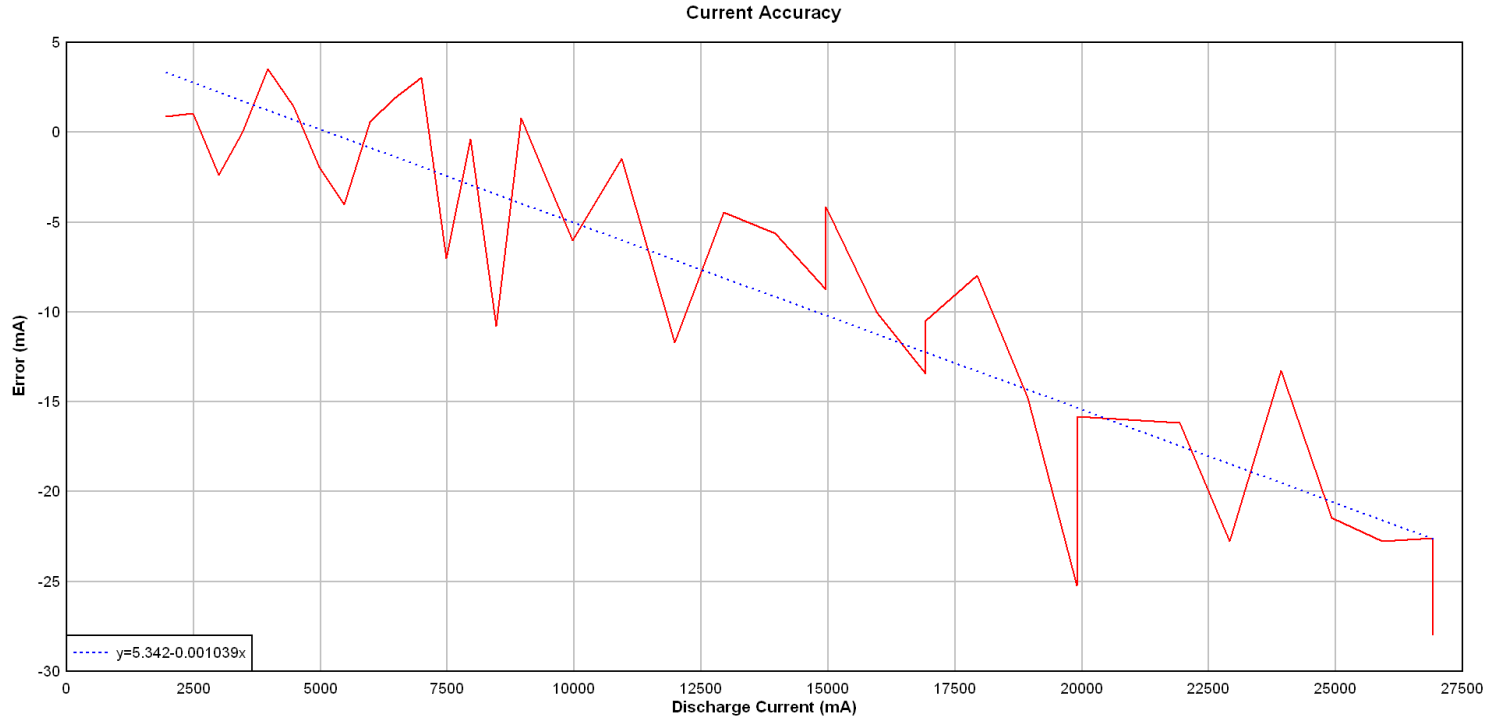
Pack current accuracy – discharge current <2A



Current Error < ±10mA @<2A

Shunt resistor 1mΩ 50ppm @Room temperature

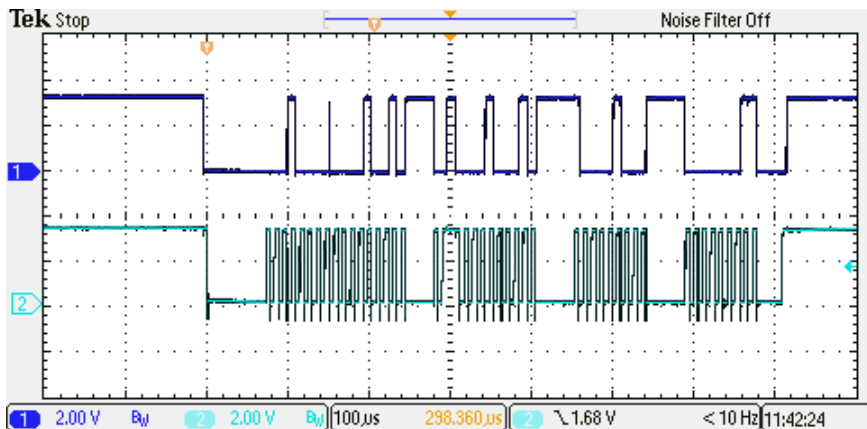
Pack current accuracy – discharge current >2A



Current Error <1% @>2A

Shunt resistor 1m Ω 50ppm @Room temperature

I2C Curve – 100kHz

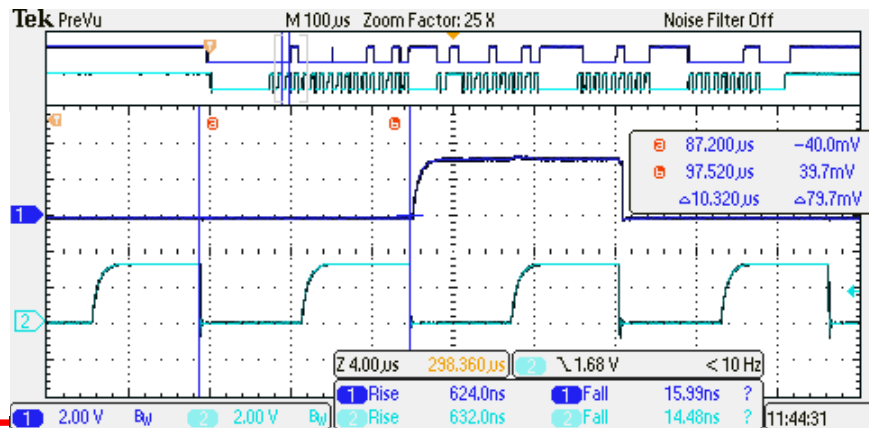
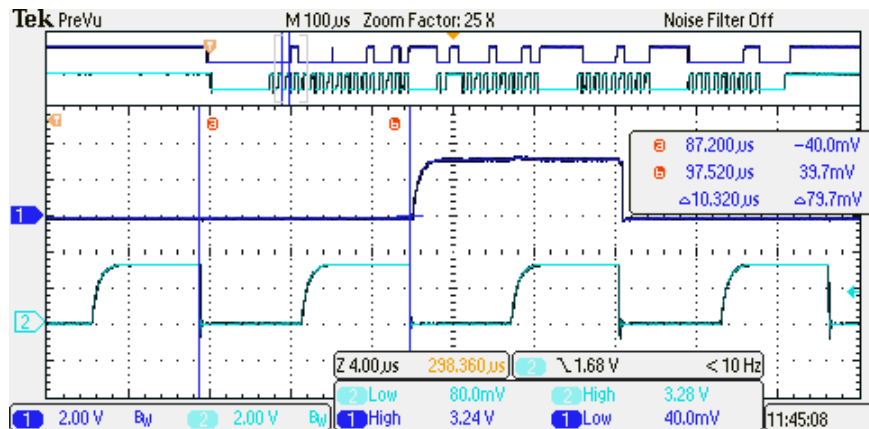


Test conditions

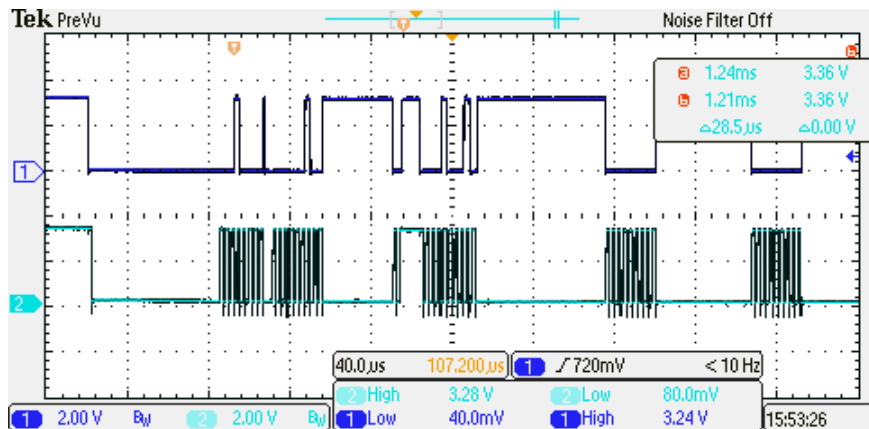
- I2C pull up: 10k Ω . I2C frequency: 100kHz.

Results

- Rise time: SCL: 632ns, SDA: 624ns
- Fall time: SCL: 14.48ns, SDA: 15.99ns
- High level: SCL: 3.28V, SDA: 3.24V
- Low level: SCL: 80mV, SDA: 40mV
- SCL frequency: 96.9kHz.



I2C Curve – 400kHz

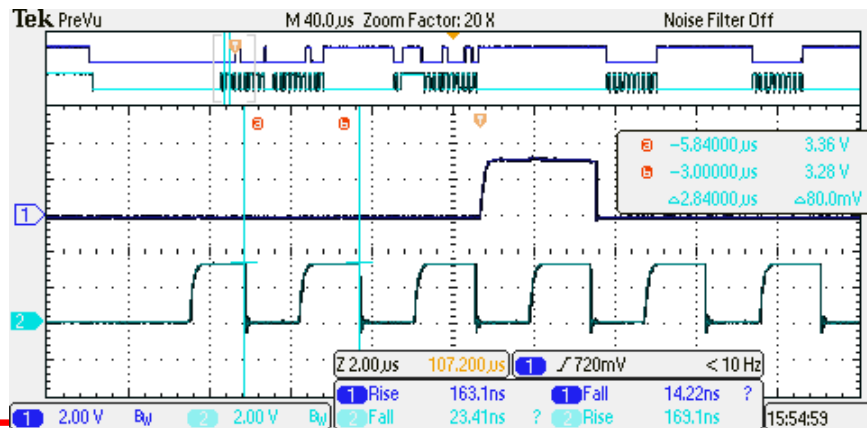
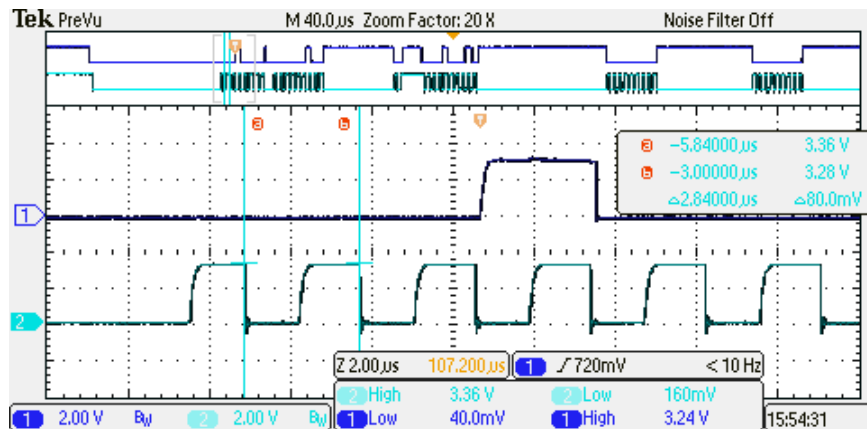


Test conditions

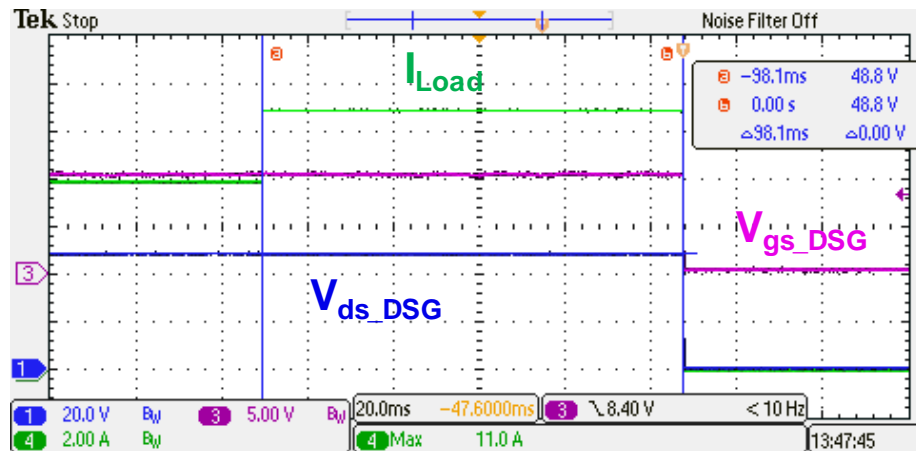
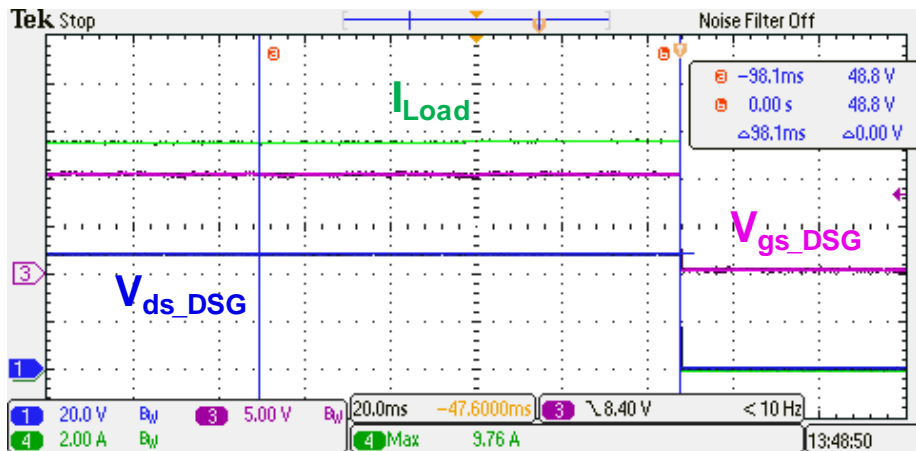
- I2C pull up: 2.49kΩ. I2C frequency: 350kHz.

Results

- Rise time: SCL: 169.1ns, SDA: 163.1ns
- Fall time: SCL: 23.41ns, SDA: 14.22ns
- High level: SCL: 3.36V, SDA: 3.24V
- Low level: SCL: 160mV, SDA: 40mV
- SCL frequency: 352kHz.



Over Current Discharge



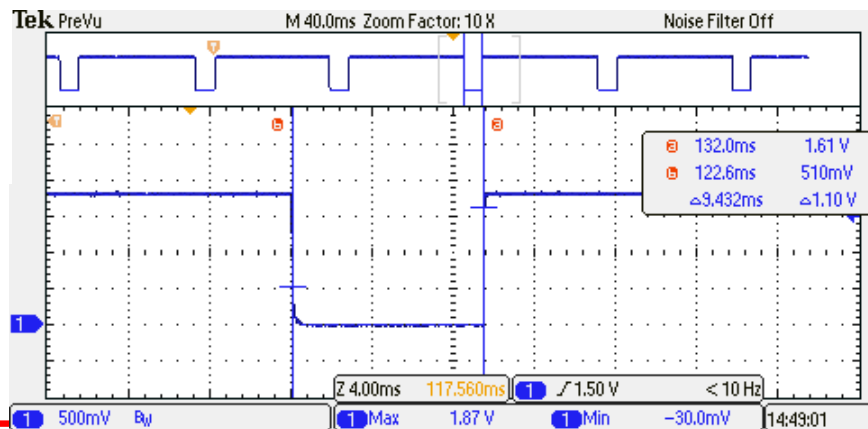
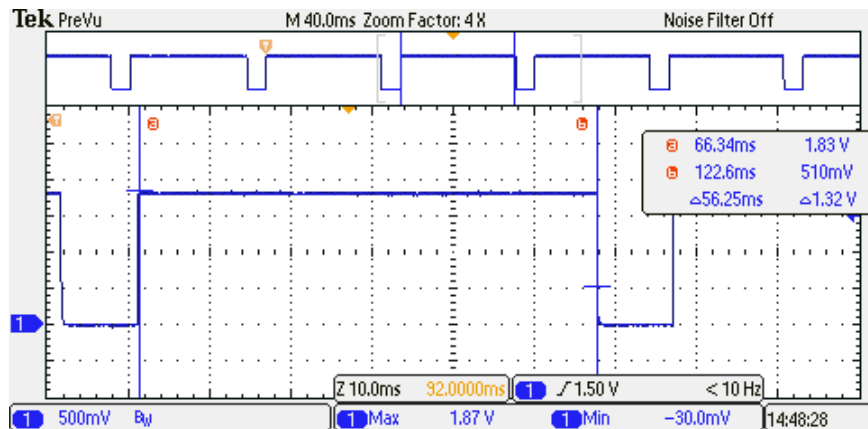
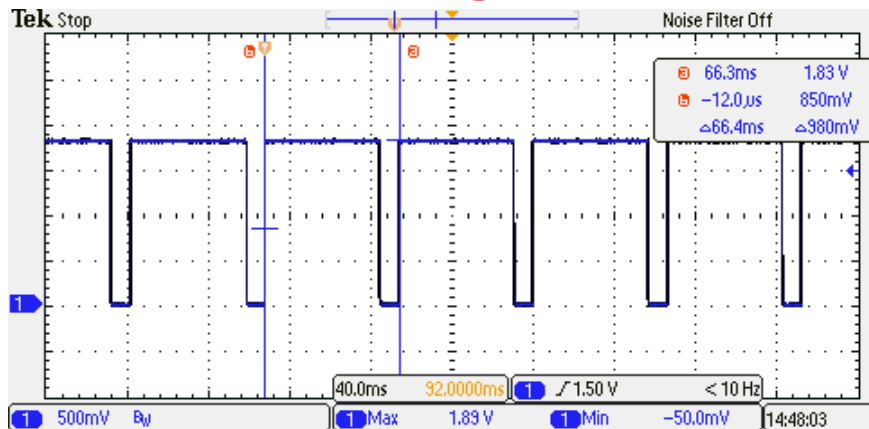
Test conditions

- V_{in} : 48V DC source + 4900uF e-cap
- OCD2 configuration:
 - 10A threshold, 100ms delay
- @ Room temperature

Results

- Protection threshold: 9.76 with -0.24A error (2A max).
- Delay time: 98.1ms with -1.9ms error (4% max).

Cell balancing in normal mode



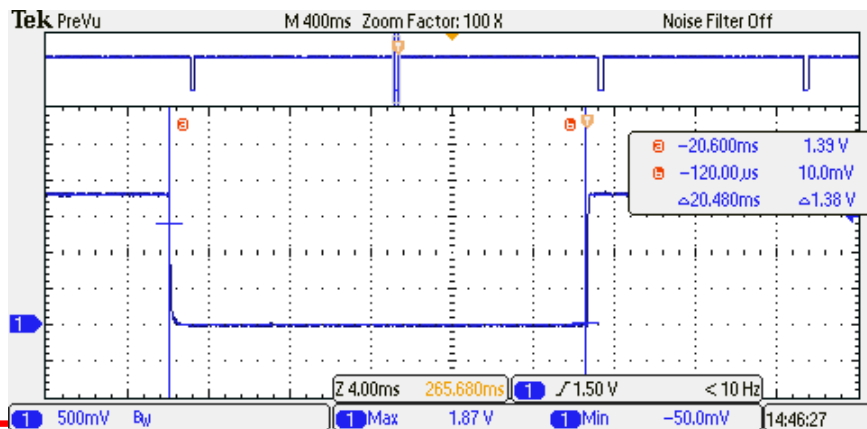
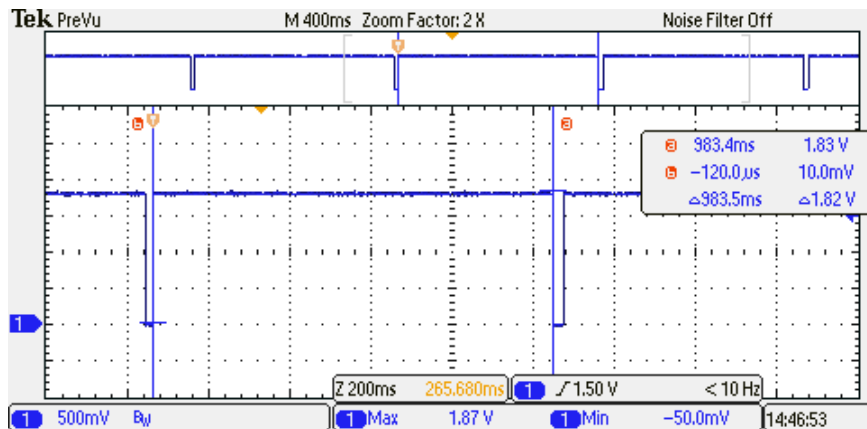
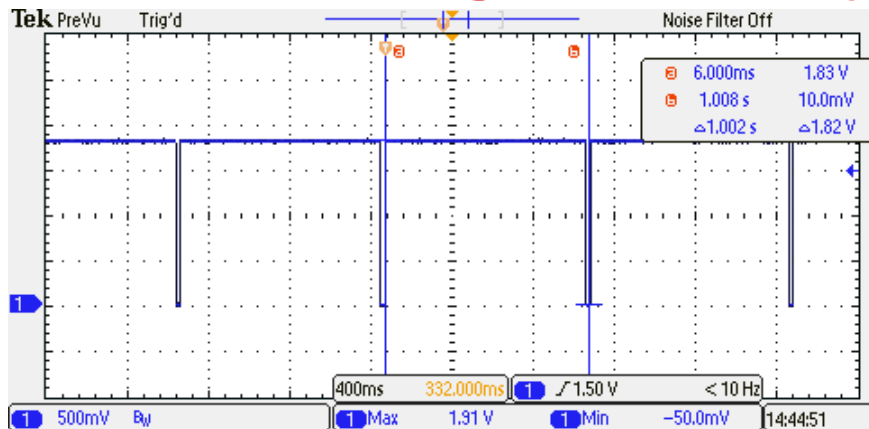
Test conditions

- Max cell count: 1s
- Minimum CB cell voltage: 3500mV

Results

- Cell balancing period: 66.4ms
- Cell balancing last time: 56.25ms
- Cell balancing duty: 84.7%

Cell balancing in standby mode



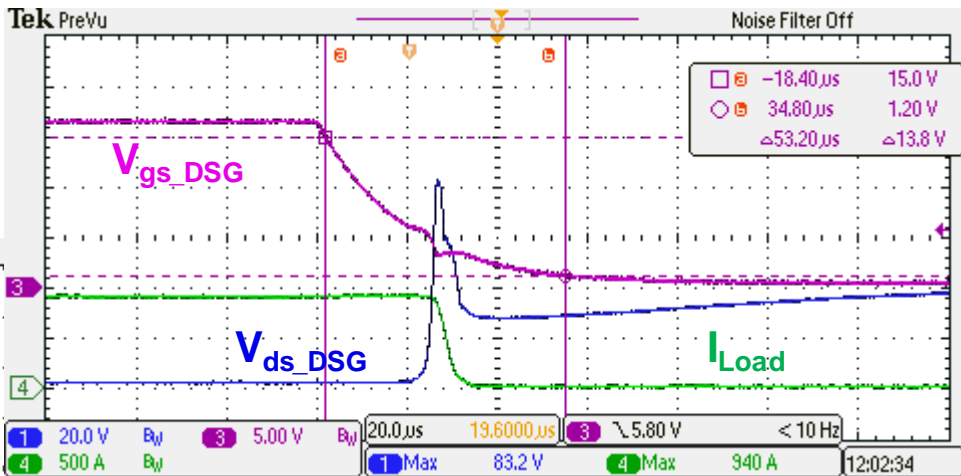
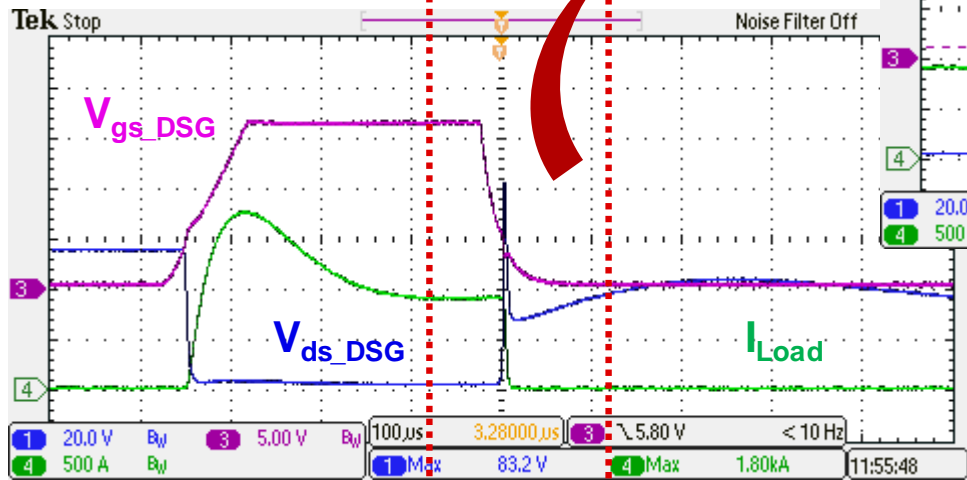
Test conditions

- Max cell count: 1s
- Minimum CB cell voltage: 3500mV

Results

- Cell balancing period: 1.002s
- Cell balancing last time: 983.5ms
- Cell balancing duty: 98.1%

Short circuit discharge



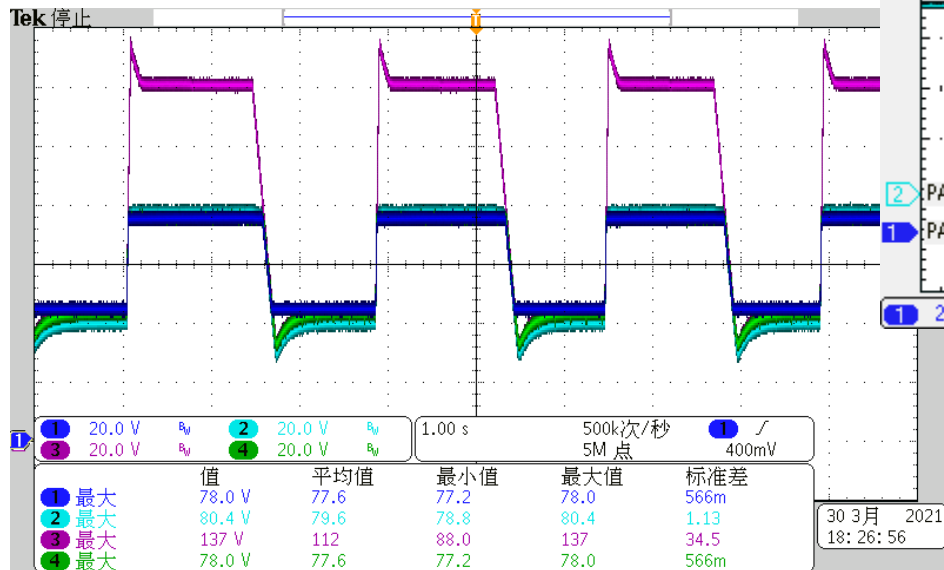
Test conditions

- Vin: 55V DC source + 4900uF e-cap
- SCD: 200A threshold, 300us delay

Results

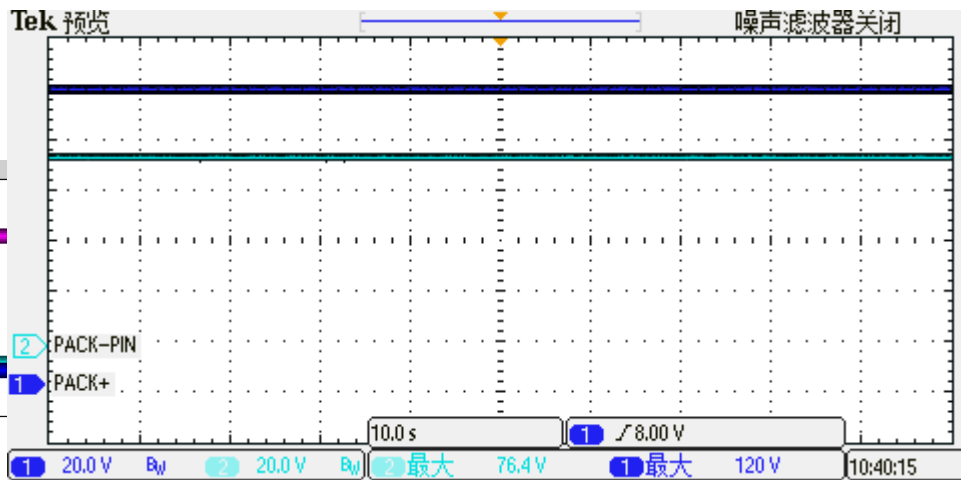
- DSG MOSFET peak V_{DS} : 83.2V, peak current: 940A
- DSG MOSFET off time: V_{GS_drop} : 53.2us, I_{D_drop} : ~10us

120V on Pack-Side



Channel 1: LD-PIN
Channel 2: DSG-PIN

Channel 3: PACK-Side
Channel 4: PDSG-PIN



Results

- BQ76952 Pins maximum voltage < 80V.
- Maximum temperature rise < 20°C after working 2 minutes.

ESD tests - contact

Applied to	ESD test signal amplitude (\pm)	Results	Notes
PACK+	2kV	PASS	Both charge and discharge MOSFET are on.
	4kV	PASS	Both charge and discharge MOSFET are on.
	6kV	PASS	Both charge and discharge MOSFET are on.
	8kV	PASS	Both charge and discharge MOSFET are on.
PACK-	2kV	PASS	Both charge and discharge MOSFET are on.
	4kV	PASS	Both charge and discharge MOSFET are on.
	6kV	PASS	Both charge and discharge MOSFET are on.
	8kV	PASS	Both charge and discharge MOSFET are on.

Test conditions

- PACK side have 2 series 0.1uF cap only;
- ESD equipment: ESS-S3011;
- IEC 61000-4-2: 150pF \pm 10%, 330 Ω \pm 10%;

16s Li-ion/LiFePO₄ battery pack with accurate cell voltage measurement and low-side MOSFET control for large capacity applications

On-going

Features

- **High cell voltage and pack current sensing for accurate battery status data:**
 - $\pm 5\text{mV}$ @25°C; $\pm 10\text{mV}$ @0-60°C; $\pm 15\text{mV}$ @-40-85°C
 - $\pm 20\text{mA}$ (worse case $\pm 80\text{mA}$) @25°C, $< 2\text{A}$; 0.5% error @25°C, $> 2\text{A}$.
- **Full set protections:** COV, CUV, OCC, OCD1/2, SCD, OT, UT, OW.
- **Low power consumption**
 - Typical: Standby 100uA and ship mode $< 10\text{uA}$.
- Low-side MOSFET control with 32A max current
- Automatic charger and discharge control
- Effective passive cell balancing with BJT (effective current: 90 mA)
- Isolated RS-485 communication available

Target Applications

- Telecom / server battery
- E-bike / e-motor battery pack
- backup unit battery pack
- Garden tool battery pack

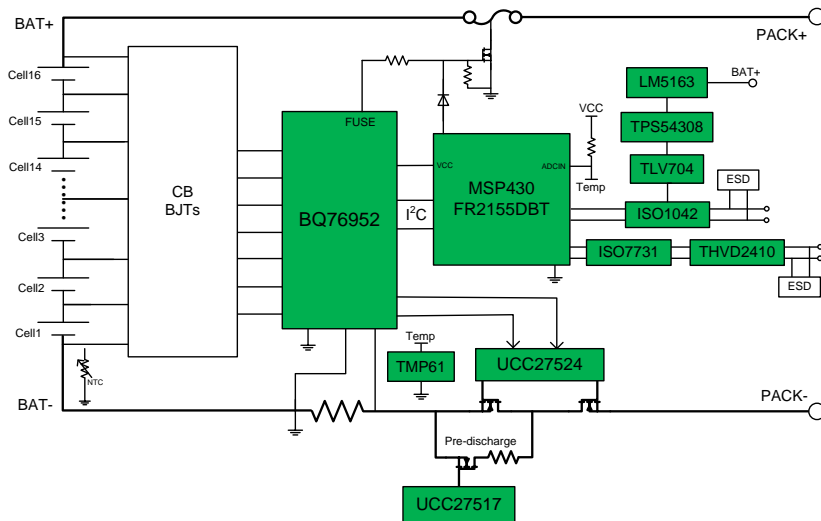
Tools and resources



- **Design guide**
- **Design files:** Schematics, BOM, gerber
- **Device datasheets:**
 - [BQ76952](#), [MSP430FR2155](#), [LM5163](#), [TPS54308](#), [ISO1042](#), [THVD1400](#), [UCC27517](#), [UCC27524](#), [TLV704](#), [TMP61](#), [ISO7731](#)

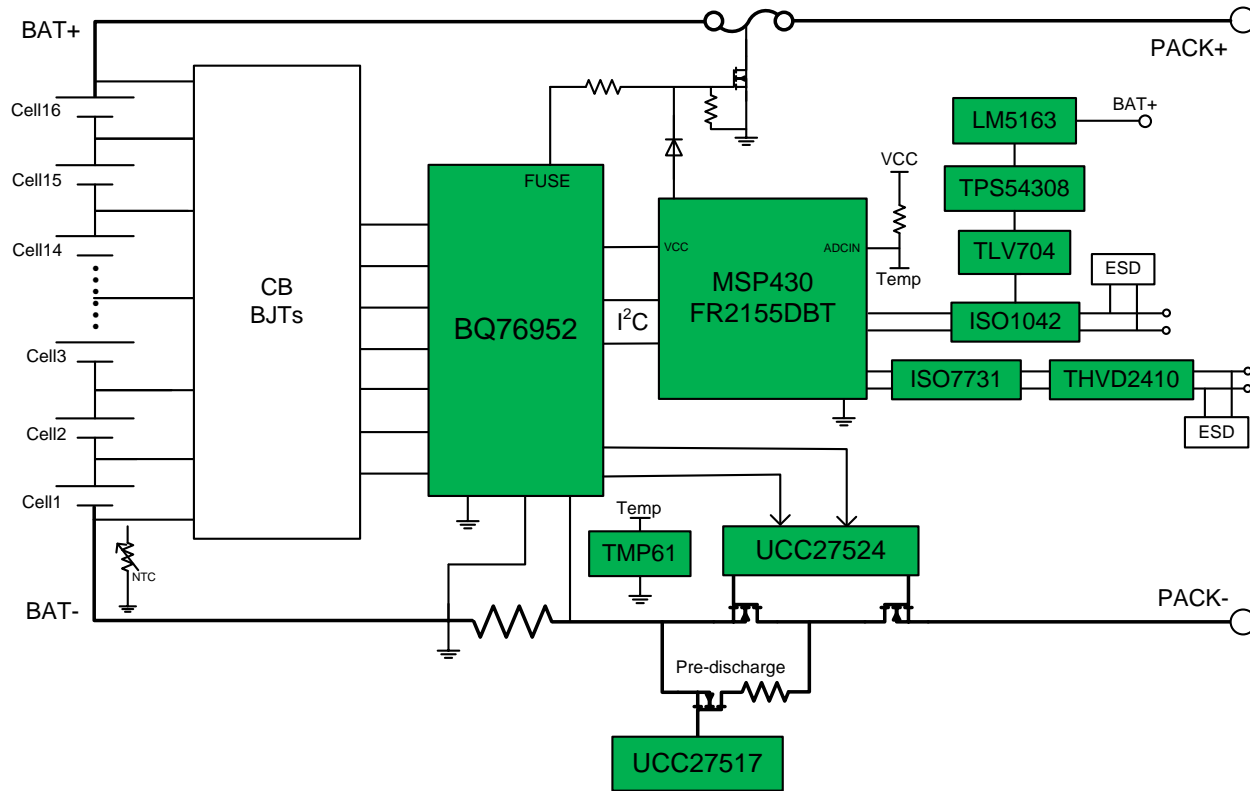
Benefits

- Accurate voltage, current and temperature information of battery
- Robust full set protections to ensure safety
- Strong MOSFET driver to enable larger pack capability
- Highly integrated solution for system design
- Low cost and effective cell balancing



System block diagram

On-going



Q & A

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