Power Supply Design Seminar

Choosing the Right Variable Frequency Buck Regulator Control Strategy

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TEXAS INSTRUMENTS

Choosing the Right Variable Frequency Buck Regulator Control Strategy

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ABSTRACT

The choice of using a non-isolated buck converter topology to reduce a distribution voltage to a lower one for point-of-load applications is an easy one. The buck is simple, has relatively few components and may be configured for a wide variety of applications. The choice of how to manage the control of the converter is not quite as straightforward a decision. This topic continues Topic 1: "Choosing the Right Fixed Frequency Buck Regulator Control Strategy" and shifts to the variable frequency realm with discussion of constant on-time control and its enhancements with various versions of the D-CAP architecture. The highlights and challenges for each technique are discussed and select design examples are presented.

I. INTRODUCTION

This paper shifts focus to variable frequency control with a discussion of constant on-time control and its enhancements, along with various versions of the D-CAP architecture. The highlights and challenges for each technique are discussed. For a complete introduction to buck converters and the various control variations, please refer to Topic 1: "Choosing the Right Fixed Frequency Buck Regulator Control Strategy."

II. VARIABLE FREQUENCY CONTROL TECHNIQUES

A. Constant On-Time Control

Figure 1(A) shows the block diagram for constant on-time (COT) control of buck converters. The output voltage is sensed via a resistor divider as the feedback voltage and then compared with the reference voltage. Whenever the feedback voltage is below the reference voltage, a fixed on-time pulse is generated to charge the output capacitor as illustrated in Figure 1(B). The implementation of COT control is quite simple since there is no complicated compensation required, only a simple comparator. Due to the direct output voltage feedback path to the comparator, any change in the output voltage is reflected to the comparator without delay, providing faster load transient performance compared to fixed frequency control.

Figure 2 compares load transient performance in an example for COT control and the conventional voltage mode control. With the same load transient steps, COT control easily achieves faster response due to the load feed-forward characteristic of the directly coupled comparator. Compared to voltage mode control, COT control requires fewer external components for loop compensation since only a simple comparator is required while a type 3 compensator is required for voltage mode control, as shown in Figure 3.

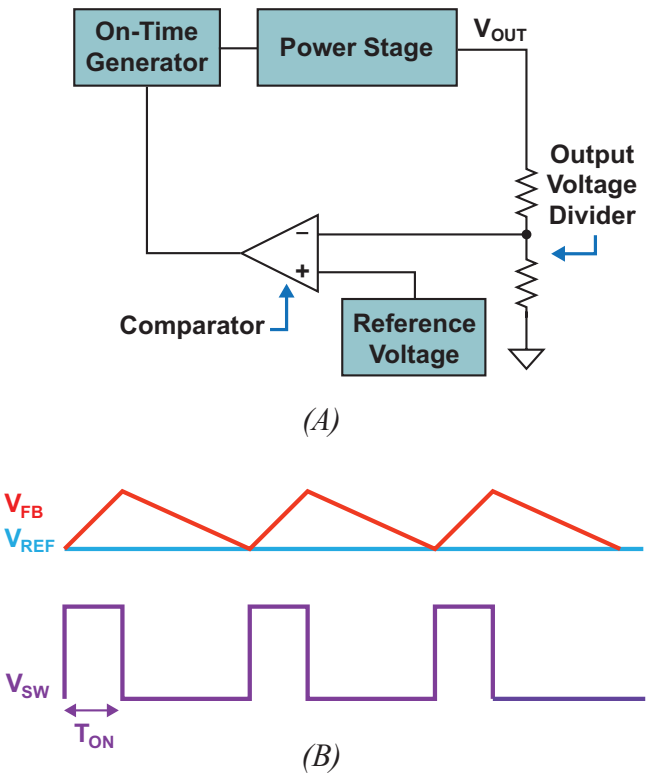
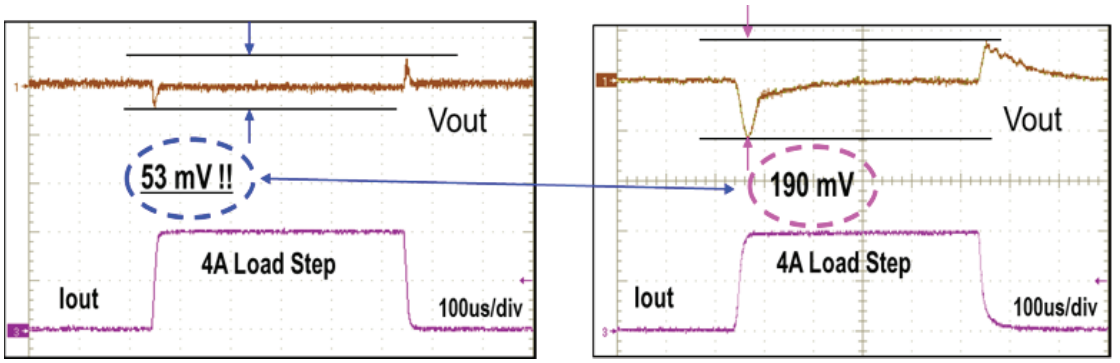
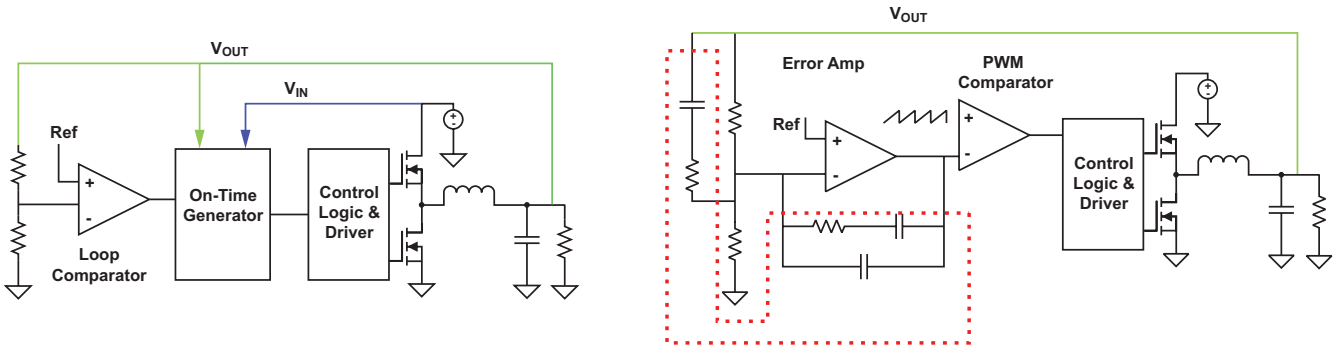


Figure 1 – Constant on-time (COT) control for buck converters: (A) block diagram; (B) illustrated operational waveforms.



(A) *(B)*

Figure 2 – Load transient performance comparisons: (A) COT control with 22 µFx3 output capacitors; (B) voltage mode control with 100 µFx4 output capacitors.



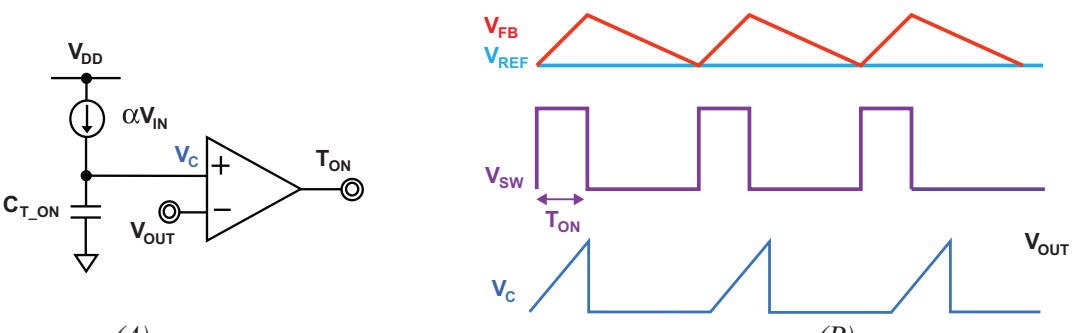
(A) *(B)*

Figure 3 – External component comparisons: (A) COT control; (B) voltage mode control with type 3 compensations.

B. Adaptive On-Time Control

Since on-time is fixed with COT control, the switching frequency is based on the duty ratio, which will result in very high switching frequency with low duty-ratio conditions. By making on-time a function of the input voltage and output voltage, COT control achieves "pseudo" fixed-frequency during steady state operation. Figure 4 shows an on-time generator and its related waveforms. An input voltage controlled current source charging a capacitor to generate a control voltage, V_C, is compared with the output voltage. The pulse width (on-time) is varied based on the duty ratio while maintaining switching frequency relatively constant as follows:

$$F_{SW} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{T_{ON}} = \frac{V_{OUT}}{V_{IN}} \times \frac{\alpha V_{IN}}{V_{OUT}} \times \frac{1}{C_{TON}} = \frac{\alpha}{C_{TON}} = \text{Constant}$$



(A) *(B)*

Figure 4 – Adaptive on-time generator: (A) block diagram; (B) illustrated operational waveforms.

Figure 5 shows a comparison of the switching frequencies between COT control and adaptive on-time control at a steady state load and over a range of input voltages.

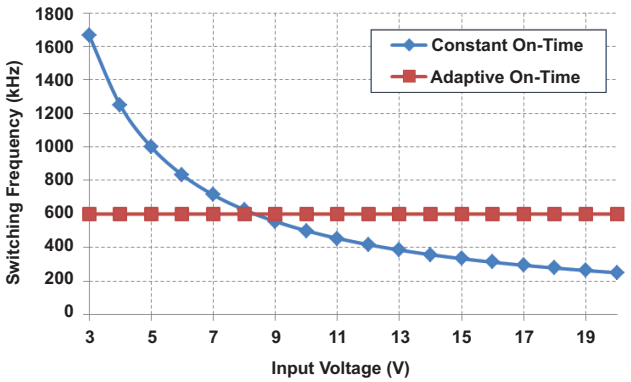


Figure 5 – Switching frequency comparisons of COT and adaptive on-time control over input voltage.

It should be noted that the "fixed-frequency" feature of adaptive on-time control is only valid during steady-state operation. During line or load transients, the switching frequency varies even with adaptive on-time control. In addition, due to the inherent variable switching frequency nature of the control method, COT and adaptive on-time control provide seamless transition between discontinuous conduction mode (DCM) and forced continuous conduction mode (FCCM) without any control mode change. As shown in Figure 6, the switching frequency is reduced at light loads, which improves light-load efficiency. Figure 7 shows the efficiency improvement by enabling DCM at light loads and allowing frequency reduction (i.e., SKIP mode).

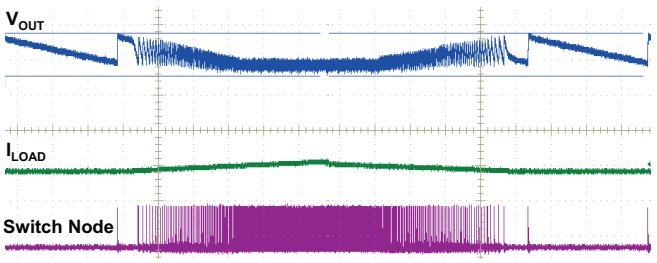


Figure 6 – Seamless DCM/CCM transitions with COT or adaptive on-time control.

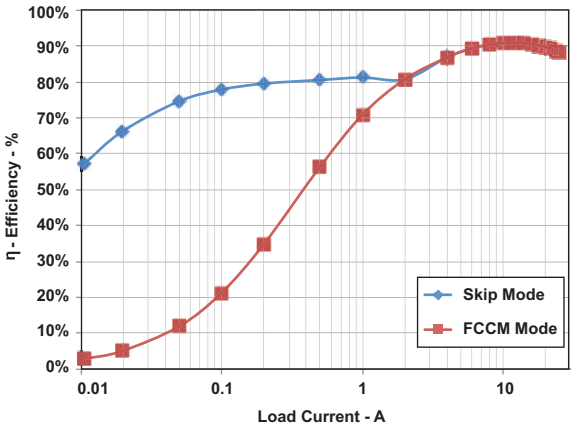


Figure 7 – Efficiency curves with DCM enabled at light loads (TPS53219+CSD86350 with 12 V to 1.1 V @ 500 kHz switching frequency).

C. TI D-CAP™ Control

TI D-CAP control adopts the concept of adaptive on-time control as shown in Figure 8. One difference compared to adaptive on-time control is that a ramp voltage is summed into the comparator to be compared with the feedback voltage and the control voltage. This ramp compensation improves the jitter performance of the control scheme by reducing the noise band in the application. Figure 9 shows the concept of the ramp compensation and compares jitter performance with and without ramp compensation. The ramp is reset and generated at each switching cycle, and the slope is adaptive by maintaining ramp height constant regardless of switching frequency.

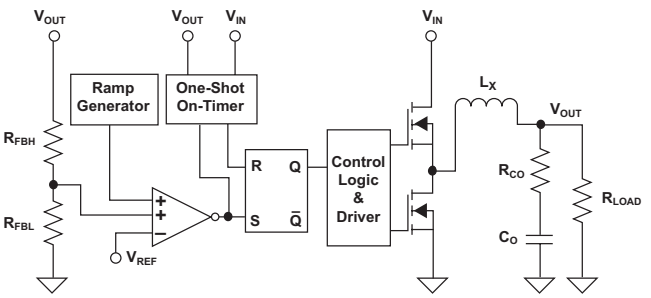
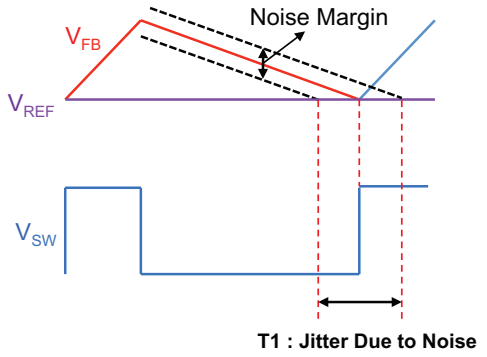
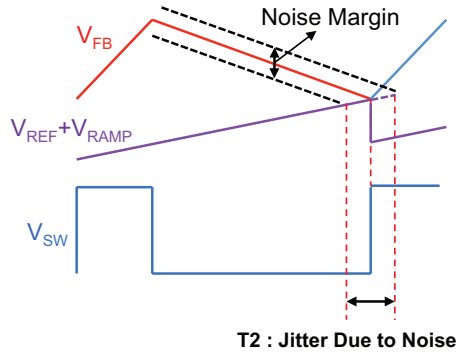


Figure 8 – Block diagram of TI D-CAP control architecture.



(A)



(B)

Figure 9 – Jitter performance comparisons: (A) without ramp compensations and (B) with ramp compensations.

For voltage feedback, the D-CAP control architecture utilizes output ESR voltage ripple and capacitor ripple voltage:

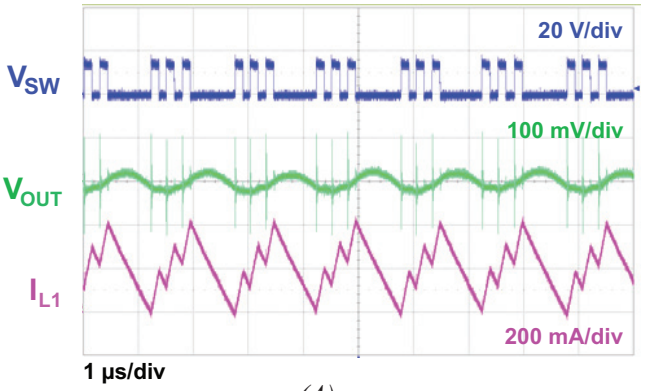
$$\Delta V_{OUT} = \Delta I_L \cdot R_{CO} + \frac{\Delta I_L}{8 \cdot f_{SW} \cdot C_O} = V_{ESR} + V_C$$

In order to stabilize the system, minimum ESR (R_{Co}) is chosen to fulfill the stability criteria below [9]:

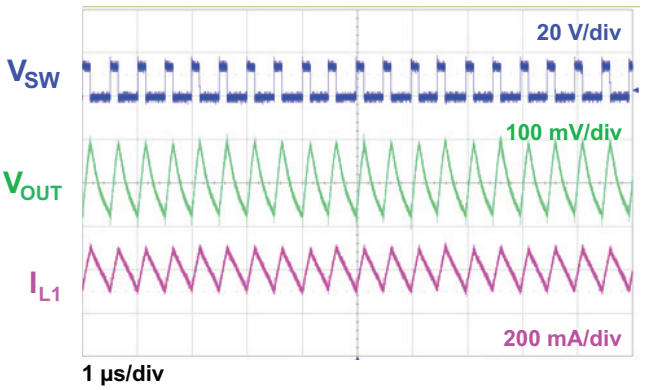
$$R_{Co} \cdot C_O \geq \frac{T_{ON}}{2}$$

Figure 10 shows comparisons with and without enough ESR at steady state operation.

Due to the ESR limitation there is the possibility of a stability issue when applying TI D-CAP control to systems with low-ESR output capacitors, such as MLCCs. To ensure stability when using low-ESR output capacitors with D-CAP control, an external ripple injection circuit directly feeds inductor current ripple to the comparator as shown in Figure 11.



(A)



(B)

Figure 10 – Steady-state operation: (A) without enough ESR; (B) with enough ESR.

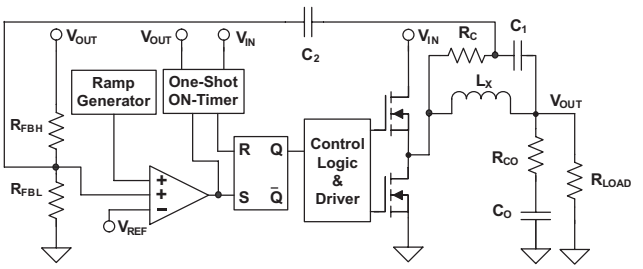


Figure 11 – D-CAP control architecture with external ripple injections.

D. TI D-CAP2™ Control

Though the external ripple injection circuit solves the stability issue for D-CAP control when used with low-ESR output capacitors, it requires more external components. In order to simplify the implementation, the ripple injection circuit is implemented internally in the TI D-CAP2 control architecture. Figure 12 shows the block diagram. By using the built-in ripple injection circuit, there is no minimum requirement for the ESR.

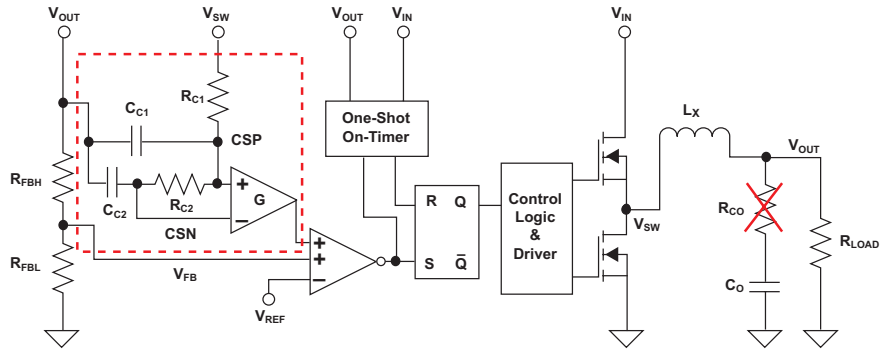


Figure 12 – Block diagram of D-CAP2 control architecture.

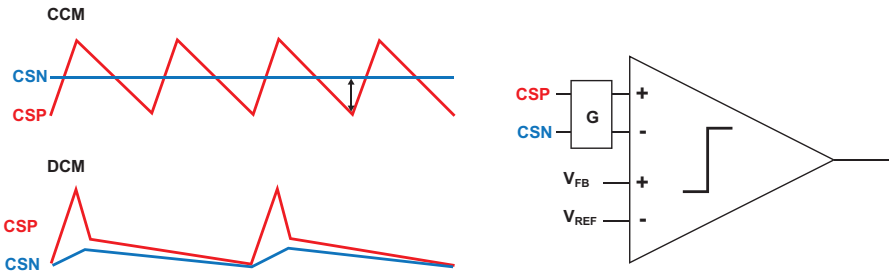


Figure 13 – Offset differences in CCM and DCM of the ripple injection circuit.

The switching, VSW, and output voltage, VOUT, generate a triangle waveform in phase with the inductor current and implement the ripple injection circuit. This signal is AC coupled to remove the DC voltage. Unfortunately, there are different offsets in CCM and DCM, as shown in Figure 13, and these offsets result in poor output voltage accuracy.

Since the $R_{C1}C_{C1}$ network of the ripple injection circuit is implemented with fixed values, the performance varies when applying D-CAP2 control architecture to different input and output conditions. Figure 14 shows an example of using a fixed $R_{C1}C_{C1}$ time constant (30 µs) in the ripple injection circuit for applications with different duty ratios. The same $R_{C1}C_{C1}$ networks may not be the optimal solution.

E. TI D-CAP3™ Control

To improve on the D-CAP2 control architecture, the D-CAP3 control architecture adds a couple of features. These features include a sample-hold circuit for improving the DC accuracy and an adaptive ripple injection circuit. Figure 15 shows the block diagram of the D-CAP3 control architecture.

By using the sample-hold concept for the ripple injection circuit, the offset difference between DCM and CCM, shown in Figure 13, is eliminated as shown in Figure 16.

To ensure better performance over wide range applications, the RC time constant for the ripple injection circuit is no longer a fixed number but is adaptive for different applications by checking the output voltage and the switching frequency. As shown in the comparison in Figure 17, better load transient performance is achieved by using different RC time constants for different applications.

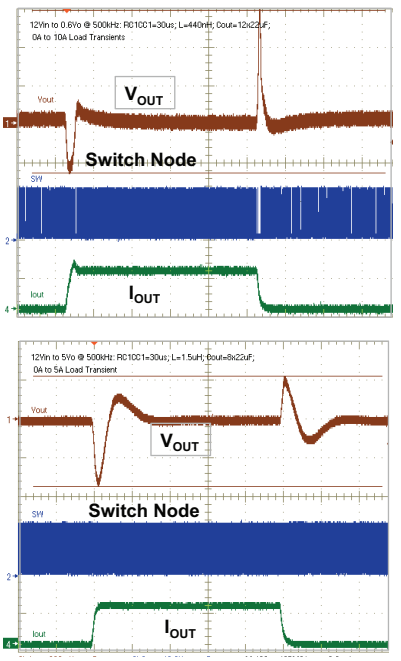


Figure 14 – Comparison of transient performance with the same $R_{C1}C_{C1}$ time constant with different duty cycles.

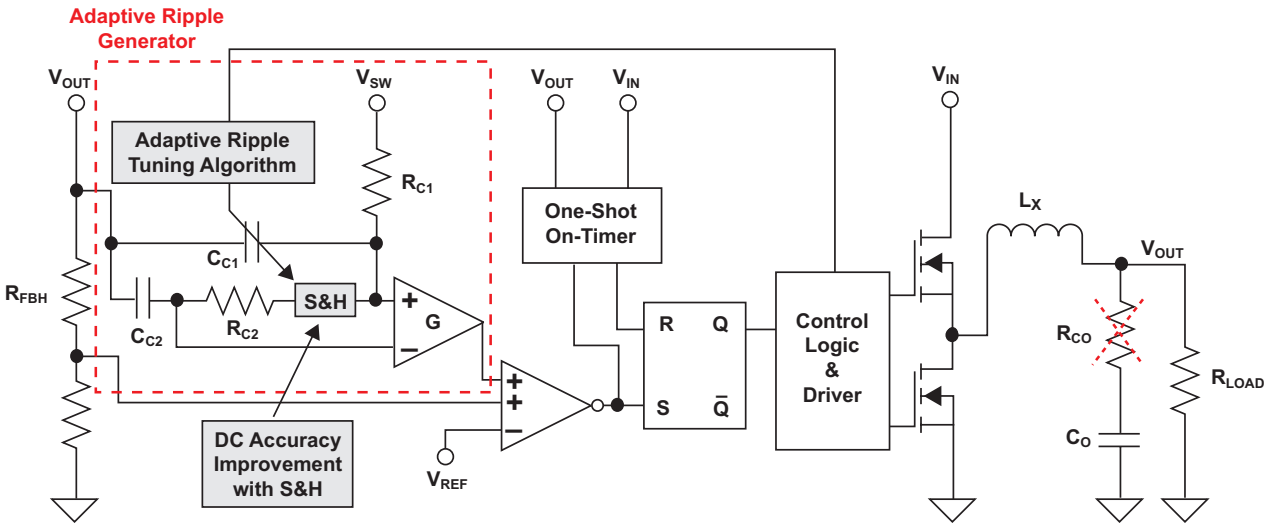
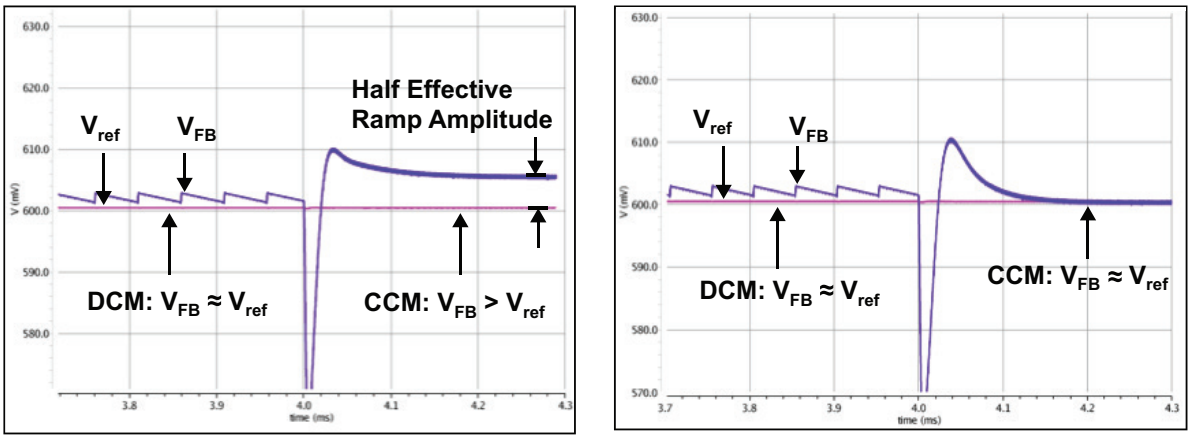
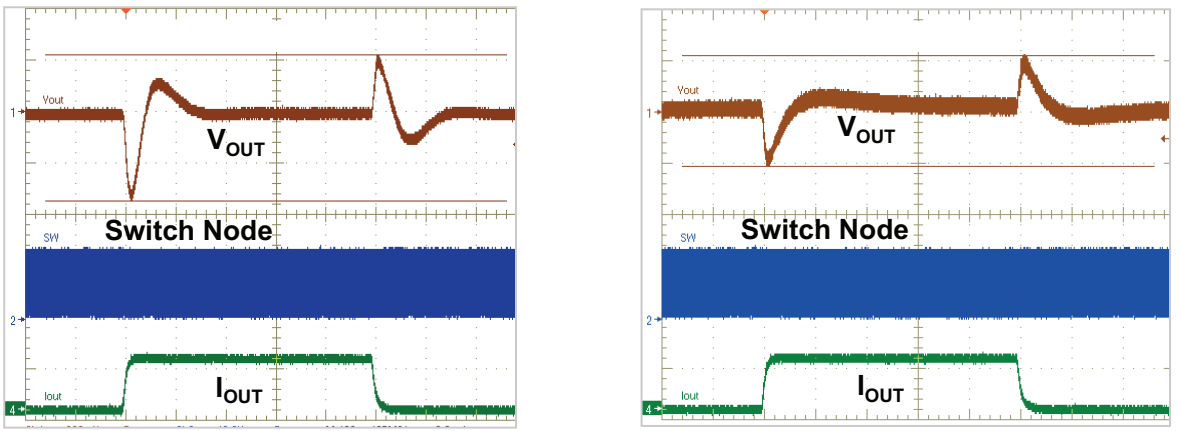


Figure 15 – Block diagram of the D-CAP3 control architecture.



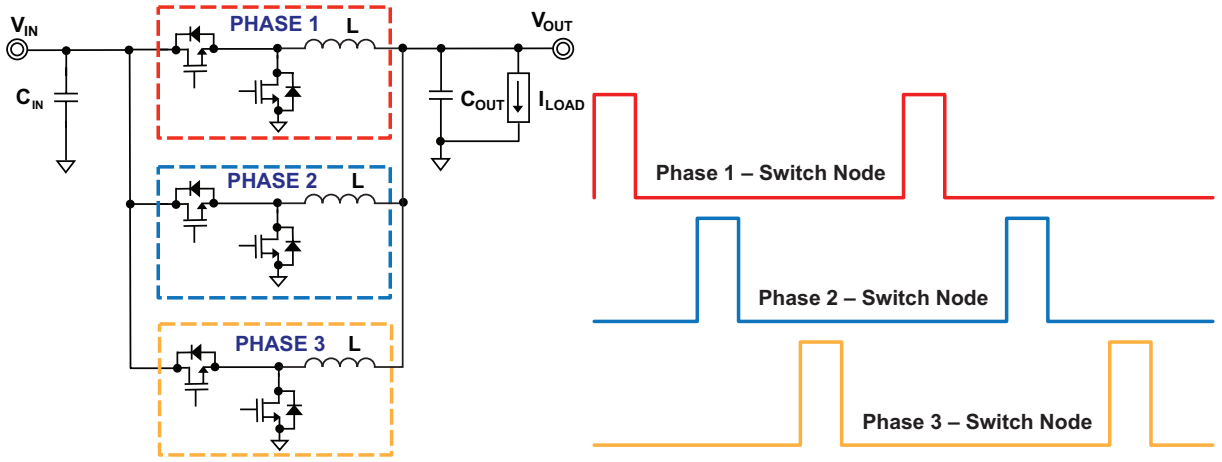
(A) *(B)*

Figure 16 – Offset comparisons in DCM and CCM: (A) without sample-hold circuit; (B) with sample-hold circuit.



(A) *(B)*

Figure 17 – Load transient comparisons of 12 V to 5 V applications with: (A) fixed $R_{C1}C_{C1}$ time constant; (B) adaptive $R_{C1}C_{C1}$ time constant.



(A) *(B)*

Figure 18 – Multiphase buck converter: (A) block diagram; (B) illustrated phase interleaving waveforms.

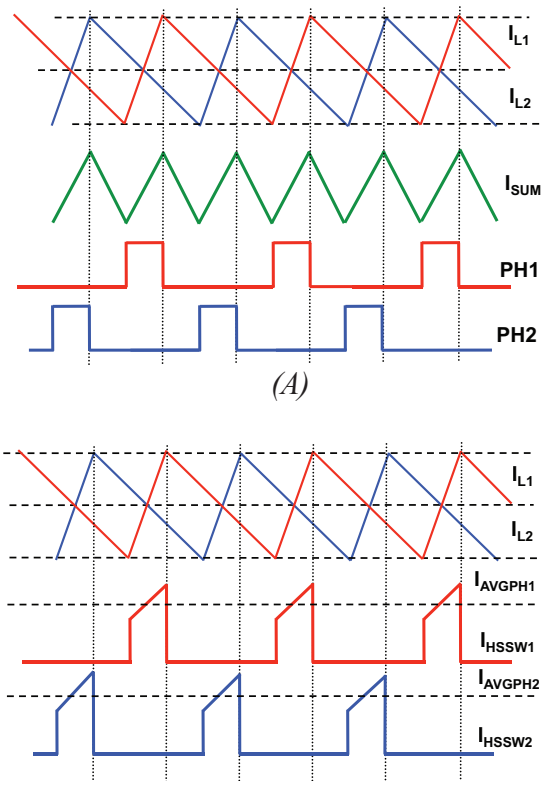
III. Variable Frequency Control for Multiphase Converters

A. Multiphase DC-DC Converters

Multiphase DC-DC converters are typically used to provide higher current outputs than a single-phase power converter can source. Figure 18 shows the block diagram and illustrated phase interleaving waveforms of a multiphase buck converter. Multiple phases are interleaved to reduce input ripple, output ripple and to reduce the output capacitance required to maintain an equivalent output voltage ripple, as shown in Figure 19. The reduced input RMS current yields higher efficiency and better thermal conditions. Figure 20 shows the ripple cancellation effects with different phase numbers and duty ratios. More operational phases result in lower ripple amplitudes with the same duty ratio.

During load step-up transients, all phases are overlapped to equivalently reduce the inductance L by phase number N. This allows the converter to deliver N times the inductor current to charge the output capacitors and to deliver current to the load, as shown in Figure 21. Hence, the load transient performance is improved with multiphase converters.

In addition, with multiphase converters, high efficiency is achieved over wide load ranges by adjusting the number of phases based on the load conditions. Figure 22 provides examples of the efficiency curves with different operational phase numbers. At heavy-load conditions, more phases are operated to reduce conduction loss. As load current decreases, the number of operational phases is reduced, optimizing efficiency. At extreme light-load conditions, the converter is operated in single-phase DCM to reduce the switching frequency further to maintain high efficiency.



(A)

(B)

Figure 19 – Ripple reduction in 2-phase operations: (A) output ripple; (B) input ripple.

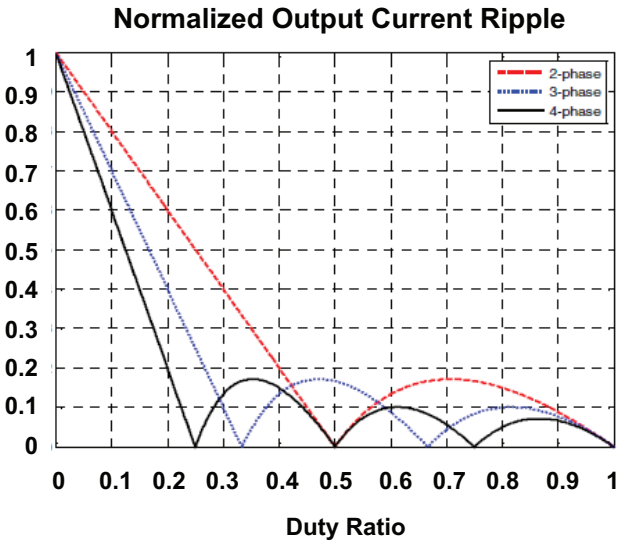


Figure 20 – Ripple cancellation effects with different phase numbers and duty ratios.

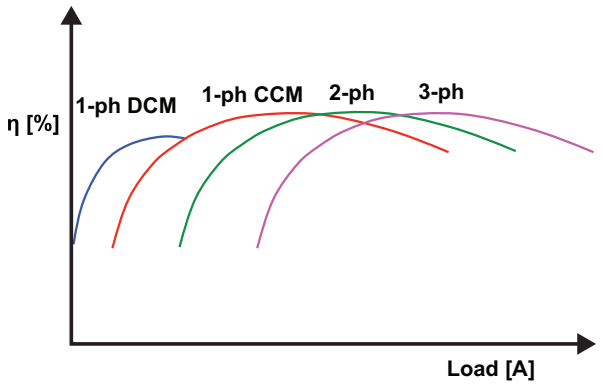


Figure 21 – Load step-up transient with phase overlapping of a multiphase buck converter.

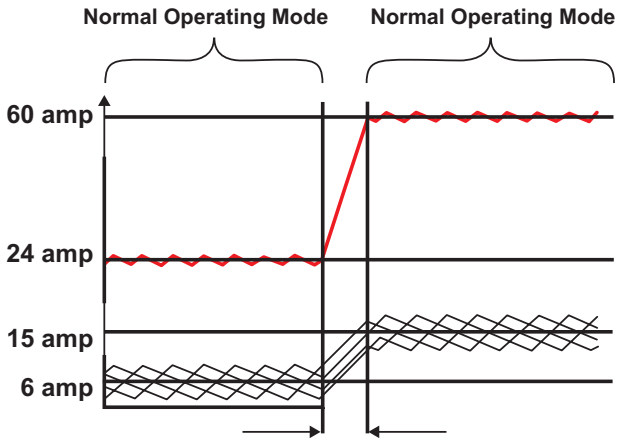


Figure 22 – Illustrated efficiency curves with different operational phase numbers.

B. TI D-CAP+™ Control

For high current applications, D-CAP+ control architecture, as shown in Figure 23, combines the benefits of D-CAP constant on-time control with those of multiphase converters. The major differences compared to the previous D-CAP families for single-phase converters are:

- Inductor currents of individual phases are fed back so the system has accurate droop control and good current-sharing performance
- An error amplifier is utilized to improve DC accuracy over load and line

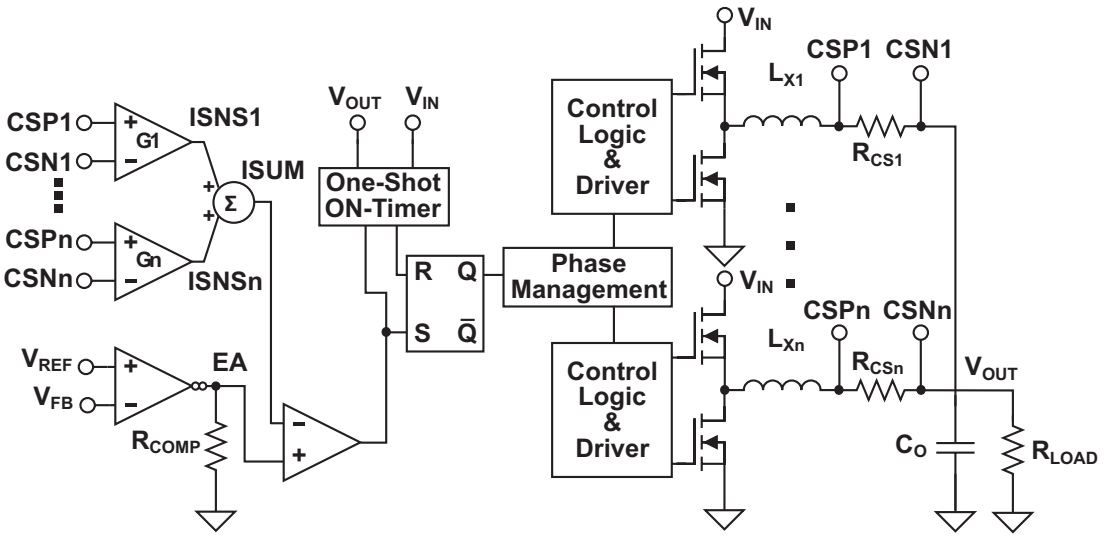


Figure 23 – Block diagram of D-CAP+ control architecture.

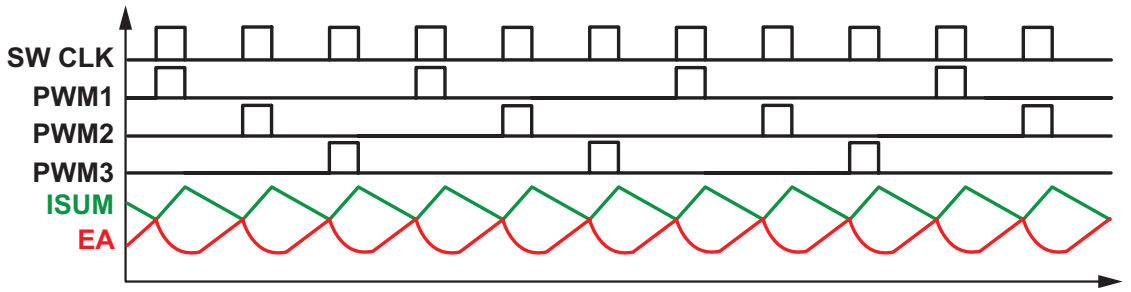
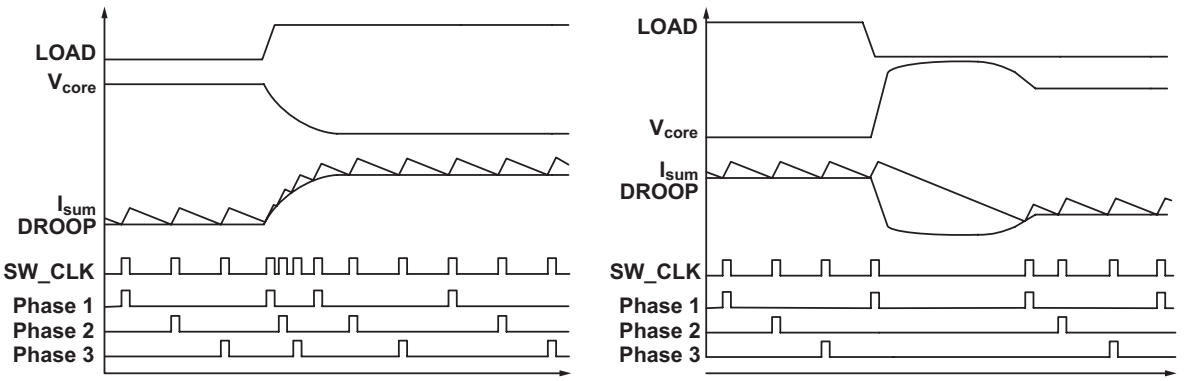


Figure 24 – Illustrated operational waveforms of D-CAP+ control architecture with 3 phases in steady state.

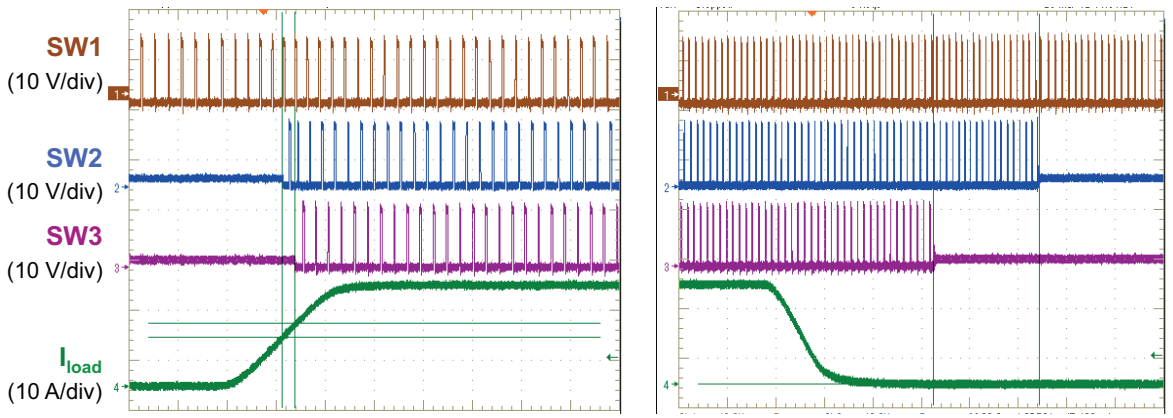


(A) *(B)*

Figure 25 – Illustrated load transient waveforms of D-CAP+ control architecture with 3-phase operation: (A) load step up; (B) load step down.

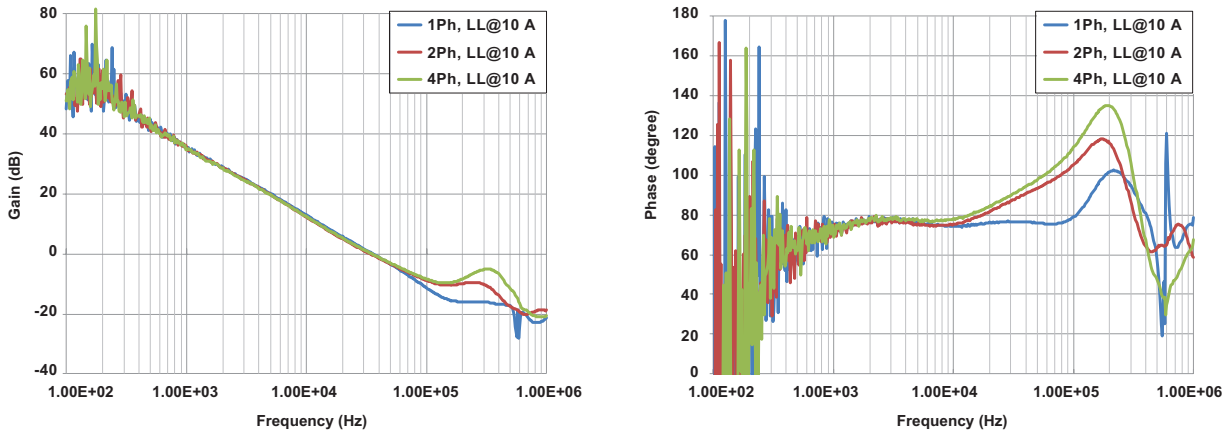
Figure 24 illustrates the operational waveforms of D-CAP+ control architecture with 3 phases in steady state. By using the adaptive on-time control concept, a pseudo fixed switching frequency of SW_CLK is generated by comparing the summed inductor currents, ISUM, and the error amplifier output, EA, signal. By distributing the switching signal to different phases, all phases can be perfectly interleaved in steady state. During load transients, the switching frequency is varied to improve the transient performance as shown in Figure 25. Variable switching frequencies of different phases can be observed in Figure 25.

One important feature of a multiphase converter is the capability to dynamically add or drop the number of operational phases based on load conditions. The goal is to optimize efficiency while maintaining good load transient performance. Figure 26 shows waveforms of dynamic phase adding and shedding performance when adjusting load currents. While monitoring the summed inductor currents, ISUM, the operational phase



(A) *(B)*

Figure 26 – Experimental waveforms of dynamic phase shedding: (A) phase adding; (B) phase shedding.



(A) *(B)*

Figure 27 – Experimental waveforms of dynamic phase shedding: (A) phase adding; (B) phase shedding.

number is adjusted automatically while keeping the phase interleaving according to the number of phases. More importantly, due to the characteristics of current-mode control, by feeding the inductor current to the modulator, the double poles formed by the inductor and the output capacitors are split, hence the loop gain characteristics become less sensitive to the operational phase numbers, as shown in Figure 27. By having a dynamic phase adding/shedding feature, high efficiency is achieved over wide load ranges. Figure 28 shows the high-efficiency curves of a 5-phase buck converter with dynamic phase shedding enabled.

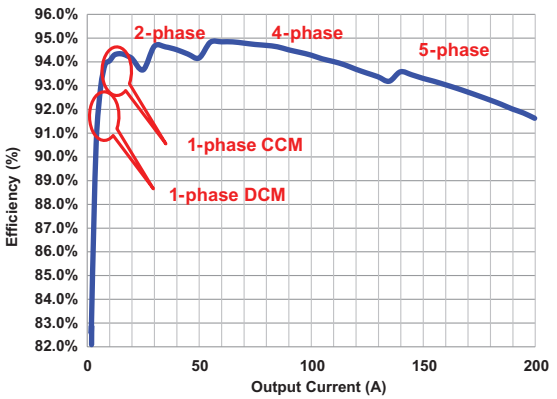


Figure 28 – Efficiency curves of a 5-phase converter with dynamic phase adding/shedding enabled.

Typically there is a tradeoff between high efficiency, with enabling dynamic phase shedding, and load transient performance due to the delay of adding phases. However, fast phase adding performance is achievable with the D-CAP+ control architecture as, not only the summed inductor currents used to determine the phase adding timing, but also the output voltage are utilized to avoid excessive undershoot caused by the delay of phase adding. Figure 29 shows waveforms of fast phase adding performance during load step up.

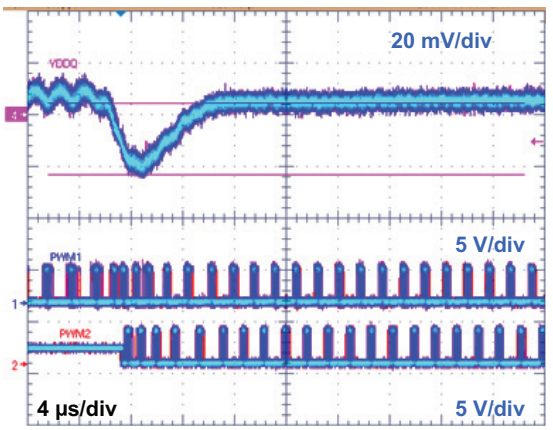


Figure 29 – Fast phase adding during load transients.

Current sharing is important for multiphase converters, and is achieved in both steady-state and dynamic load conditions. Figure 30 shows the block diagram of dynamic current sharing used in D-CAP+. Individual phase currents are amplified, filtered and compared with the average current to generate an error signal proportional to the level of current sharing. This signal is used to adjust the on-time for each of the phases. With a small filter time constant (5 µs), fast load transients achieve dynamic current sharing. Figures 31-32 show the waveforms of current sharing performance with a four-phase buck converter. The current of each phase is balanced dynamically to avoid stressing any of the phases during load transients.

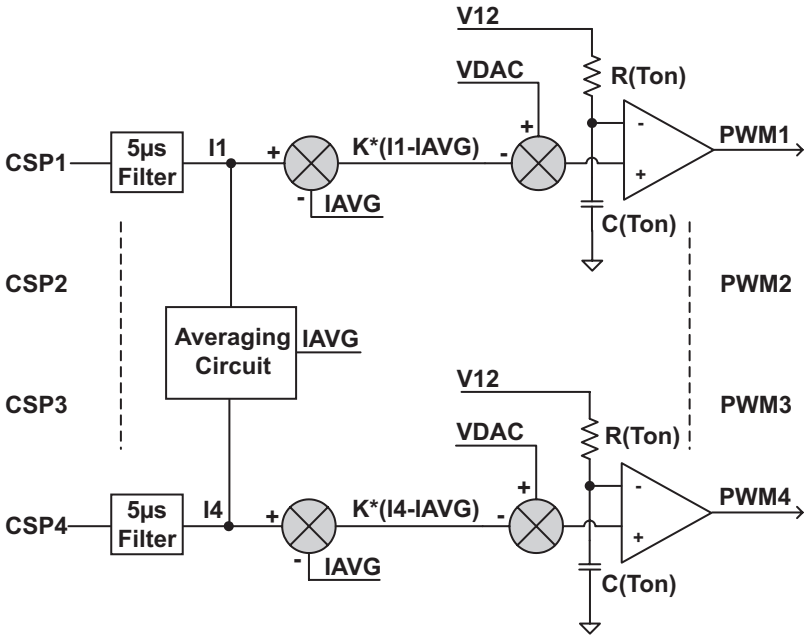
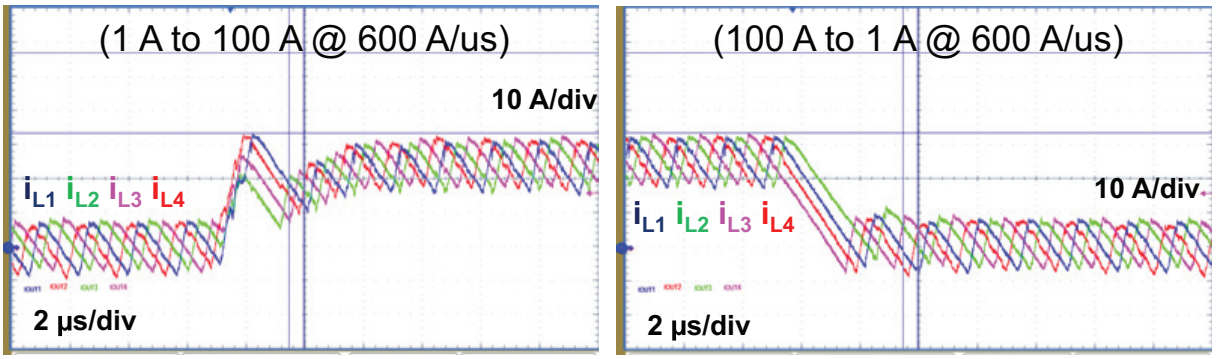


Figure 30 -Block diagram of dynamic current sharing with D-CAP+ control architecture.



(A) *(B)*

Figure 31 – Dynamic current sharing performance of D-CAP+ control architecture: (A) load step-up; (B) load step-down.

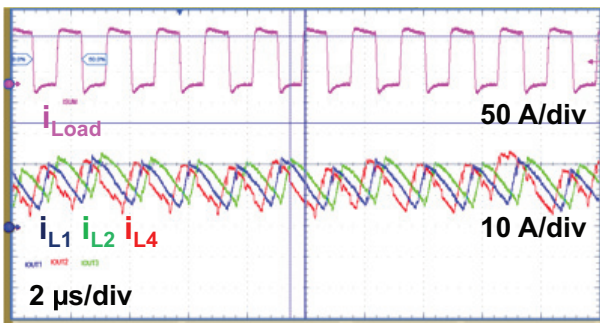


Figure 32 – Dynamic current sharing performance of D-CAP+ control architecture with fast load transients (1 A-100 A load steps with 600 kHz load frequency).

IV. Summary of D-CAP Control Methods

Table 1 compares different D-CAP control architectures. The original D-CAP control architecture maintains the advantages of COT control, such as fast load transients and no compensation, and introduces adaptive on-time and ramp compensation for jitter improvement. The D-CAP2 control architecture builds in a ramp generation circuit to solve the stability issue when using MLCC output capacitors. The D-CAP3 control architecture further improves on D-CAP2 by including a sample-and-hold circuit, thereby improving the DC regulation accuracy between DCM/CCM. An adaptive ripple compensation circuit improves performance for wide ranging applications. Finally, the D-CAP+ control architecture introduces inductor current feedback for accurate load-line control as well as capability for multiphase applications for high-power solutions. The D-CAP+ control architecture also features good dynamic phase shedding and dynamic current sharing performance.

Control Architecture	Features
D-CAP™	• Adaptive On-Time Control • Fast Load Transients • Ramp Compensation • High Efficiency @ Light Loads
D-CAP2™	• Internal Ripple Compensation for MLCCs
D-CAP3™	• Sample-and-Hold for DC Accuracy Improvement for CCM/DCM • Adaptive Ripple Compensation
D-CAP+™	• With Actual Current Feedbacks • Extension to Multi-Phase Applications • Dynamic Current Sharing • Dynamic Phase Shedding

Table 1 – Comparison of D-CAP control architectures.

Table 2 summarizes the advantages of the COT control mentioned in this paper, and also addresses disadvantages of the original COT control and its solutions.

Advantages	Disadvantages
Simple design, no compensation required	Variable switching frequency (Solution: D-CAP/D-CAP2/D-CAP3/D-CAP+)
Excellent load transient response	Sensitive to PCB design for jitter (Solution: D-CAP/D-CAP2/D-CAP3/D-CAP+)
Excellent line transient response	Minimum ripple requirement or output capacitor type limitations (Solution: D-CAP2/D-CAP3/D-CAP+)
Seamless DCM/CCM transitions for good light-load efficiency	Poor load/line regulation (Solution: D-CAP3/D-CAP+)
	Not easy for multi-phase configurations (Solution: D-CAP+)

Table 2 – Advantages and disadvantages of COT control and its solutions.

V. Summary

While this topic has only covered the variable frequency control portion of the whole picture, Table 3 below outlines the fundamental differences between both fixed frequency (covered in Topic 1) and variable frequency control for comparison. Both offer good output regulation, though, with a variable frequency approach, an amplifier is a necessary addition to the basic control approach.

	Fixed Frequency Control	Variable Frequency Control
Output voltage regulation	Yes	Yes
Synchronize to system clock	Yes	No
Fast transient response	Latency of at least one period	Low latency
EMI spectrum	High peaks, low average	Low peaks, higher average
Minimum controllable pulse width	An issue with high frequency and high conversion ratios	May be fixed (COT)
Loop compensation	Relatively fixed to an application circuit	May be used in multiple applications with little “tuning”

Table 3 – Summary of fixed frequency versus variable frequency control.

VI. References

[1] Lynch, Brian, "Under the Hood of Low Voltage DC/DC Converters," SEM-1500 Power Supply Design Seminar, Texas Instruments, 2004.

[2] Lynch, Brian, "Feedback in the Fast Lane," SEM-1700 Power Supply Design Seminar, Texas Instruments, 2006.

[3] Dixon, Lloyd H., "Current-Mode Control of Switching Power Supplies," slup075, Texas Instruments.

[4] Dixon, Lloyd H., "Average Current Mode Control of Switching Power Supplies," slup091, Texas Instruments.

[5] Sheehan, Robert, "Current-Mode Modeling For Peak, Valley and Emulated Control Methods," Texas Instruments.

[6] Erickson, Robert W., "Fundamentals of Power Electronics."

[7] Ridley, Ray, "A More Accurate Current-Mode Control Model," slup122, Texas Instruments.

[8] Betten, John and Kollman, Robert, "Easy Calculation Yields Load Transient Response," Power Electronics Technology, February 2005.

[9] Li, J. and Lee, F. C., "Modeling of V2 Current-Mode Control," IEEE Trans. Circuit and Systems: Part I, vol. 57, no. 9, pp. 2552-2563, Sept. 2010.

Appendix A – Design Examples

There are a number of tools useful in the design of the power supply. The first step is to decide on a control scheme. Examples here include voltage mode (with feed forward), emulated current mode, and D-CAP3. Once the control scheme is defined, the input voltage, output voltage and output current help narrow the choice of a power supply IC. The first major step after choosing the controller is to define the switching frequency (or estimated frequency for D-CAP).

Once the frequency is defined, the power stage components are calculated. The power stage choice is largely independent of controller choice. There are a number of choices to aid in these calculations:

1. WEBENCH® - www.ti.com/webench

WEBENCH calculates all of the necessary components for a design. It allows the engineer to optimize the design based on goals. The tool provides performance estimates, a complete schematic and bill of materials. Below are sample screen shots of the interface.

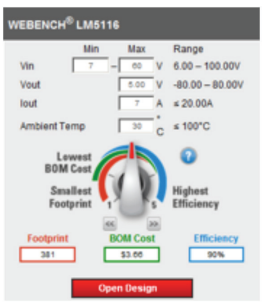


Figure A1 – WEBENCH design entry interface.

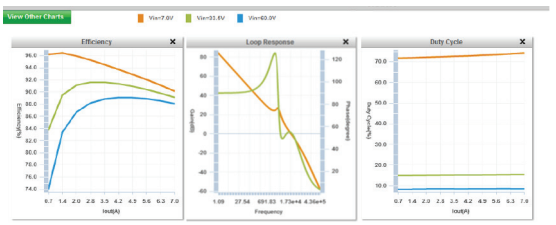


Figure A2 – WEBENCH simulated plots (efficiency, loop response, duty cycle).

2. Power Stage Designer™ - http://www.ti.com/tool/powerstage-designer

Power Stage Designer is a tool that provides all of the necessary parameters to calculate the components of the power stage. These values are necessary to pick the output filter for a buck converter. Shown below are sample screen shots of the interface:

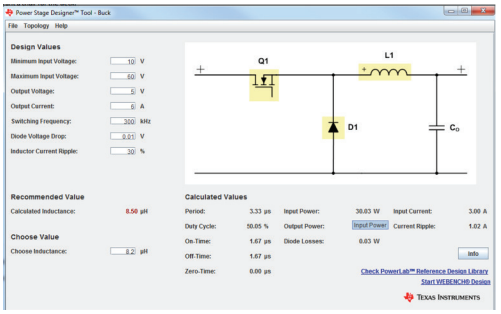


Figure A3 – Power Stage Designer for buck converters.

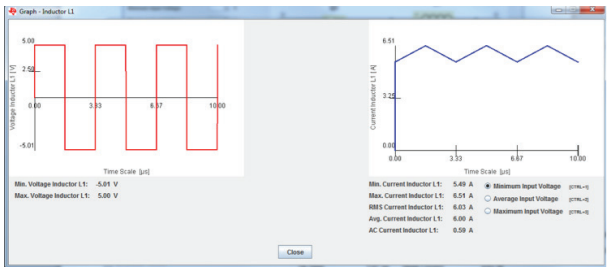


Figure A4 – Inductor waveforms from Power Stage Designer.

Voltage Mode Design Example

Design Specifications:

- V_{IN} = 10-60 V
- V_{OUT} = 5 V
- I_{OUT} Max = 6 A
- Switching Frequency = 300 kHz

Based on the above set of specifications, the TPS40170 is chosen for the controller. The full details of the calculations can be found on pages 31-41 of the following document:

http://www.ti.com/lit/gpn/tps40170

Below are sample plots from the completed design:

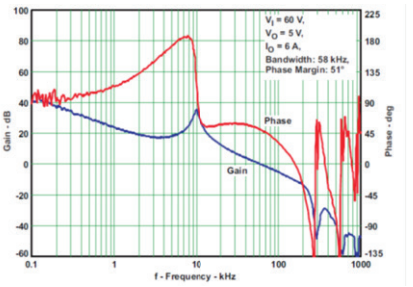


Figure A5 – Loop response of the TPS40170 design example.

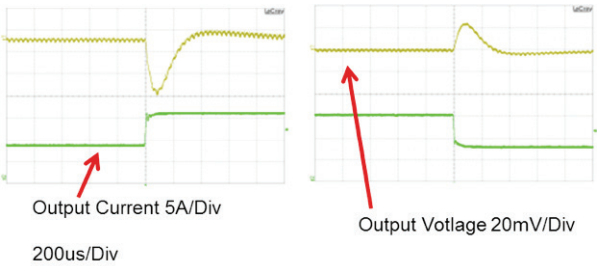


Figure A6 – Transient response of the TPS40170 design example.

Emulated Current Mode Design Example

Design Specifications:

- V_{IN} = 7-60 V
- V_{OUT} = 5 V
- I_{OUT} Max = 7 A
- Switching Frequency = 250 kHz

Based on the above set of specifications, the LM5116 is chosen for the emulated current mode design example. The detailed procedure for calculating the external components can be found on pages 19-26 of the following document:

http://www.ti.com/product/LM5116

Below are sample plots from the completed design:

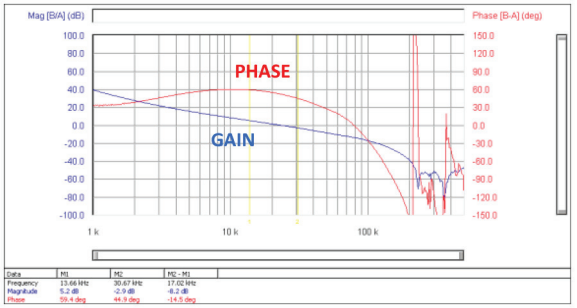


Figure A7 – Loop response of the LM5116 design example.

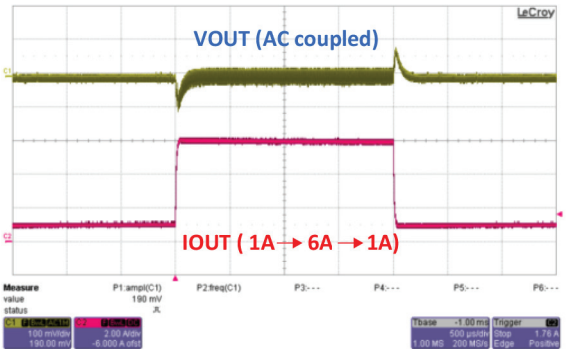


Figure A8 – Load transient response of the LM5116 design example.

D-CAP3 Design Example

Design Specifications:

- V_{IN} = 5-18 V
- V_{OUT} = 1.2 V
- I_{OUT} Max = 6.6 A
- Switching Frequency = 500 kHz

Based on the above set of specifications, the TPS53515 is chosen for this D-CAP3 design example. The detailed procedure for calculating the external components can be found on page 23 of this document:

http://www.ti.com/lit/gpn/tps53515

Below are example waveforms from the completed design:

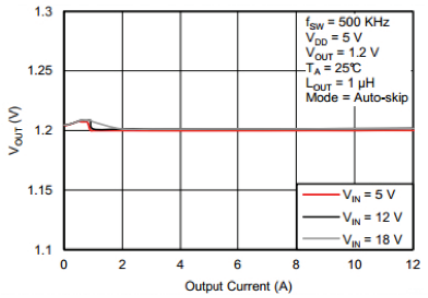


Figure A9 – Load regulation of T PS53515 design example.

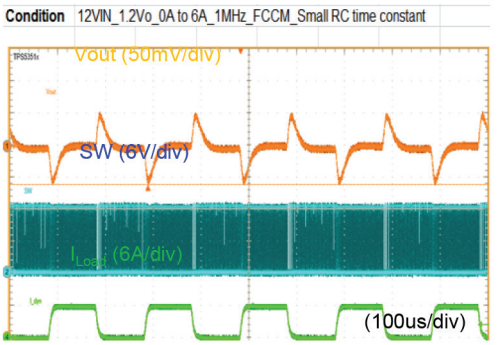


Figure A10 – Load transient response of the TPS53515 design example.

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