Control Challenges for
Low Power AC/DC Converters

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Control Challenges for Low Power AC/DC Converters

Brian King and Rich Valley

Abstract

Low power flyback AC/DC conversion is used extensively in consumer and industrial markets today. A growing segment of these converters is using primary side regulation (PSR) with magnetic feedback because of the cost and size benefits it offers. PSR flyback achieves good voltage and current regulation while at the same time it reduces standby power dissipation below 30 mW.

This topic covers some fundamentals of the flyback power supply and examines advantages, tradeoffs and challenges typically associated with a PSR flyback design. The impact of design choices along with fundamental insights are shared as they pertain to key performance attributes: static and dynamic voltage regulation, current limiting, efficiency, standby power consumption, size and cost. Measurement results highlight these trade-offs relative to more conventional control approaches.

I. Introduction

There are many papers that cover the design and operation of the flyback converter. Other than a review of the basics this is not rehashed here. What this paper attempts to provide is some insight into the characteristics and design trade-offs of low power AC/DC power supplies. It is hard to do this without focusing on AC/DC adapter circuits, since the sheer volume of this application drives performance standards and circuit innovations that naturally find their way into other applications. Regardless, the common performance goals of higher efficiency, smaller size and lower cost are very familiar to all power supply designers and hopefully some discussion here is of interest. Special consideration is given to no-load, or standby power consumption, recognizing that this is becoming a more common design concern, particularly in consumer electronics. For those interested in more general details on the art of flyback design there are several excellent references cited at the end of this topic that cover such things as magnetic design and loop compensation [1] [2] [3].

II. The Low Power Flyback Converter

For AC/DC conversion from 3 W to 30 W, the flyback topology is dominant. It provides a relatively simple and low cost solution to efficient isolated, or non-isolated, power conversion. The flyback accommodates the worldwide 85 VAC to 265 VAC outlet voltage levels over which many electrical systems must operate, particularly if they are intended to go into a suitcase. At these low power levels a well-designed flyback is very compact due to a combination of low parts count, higher operating frequencies (up to 130 kHz) and efficiencies in the 80-90% range. The flyback converter is also used to generate multiple isolated outputs, if needed, with little overhead. For these reasons both consumer and industrial equipment with power requirements in these ranges are taking advantage of this topology.

A. Performance Standards

The high volume nature of AC/DC adapters, or external power supplies (EPS), has resulted in state, government and international regulations that drive energy conservation policies – examples include the Department of Energy (DOE) in the United States and the European Commission Code of Conduct (COC) for energy consumption standards on external power supplies [4] [5]. These standards set minimum requirements for the efficiency and standby power consumption for the EPS. As illustrated in Figure 1, the efficiency requirements for these standards depend on the nameplate output power ratings of the supplies.
and specify an average efficiency based on measurements at 100%, 75%, 50% and 25% of the nameplate power. Both the DOE and COC specifications include separate standards for low voltage supplies – those with output voltages less than 6 V (indicated by the “LV” labels in Figure 1). In addition, the COC requirement includes an efficiency standard at 10% of the rated power. The more stringent, Tier 2, COC standards are scheduled to become effective starting in 2016 (“T2” labels in Figure 1). Meeting these requirements is driving the adoption of new control methodologies across the industry.

The standby, or no-load, power limits covered by these standards intend to reduce energy consumption of the power supplies when they are powered but disconnected from a load or are powered and connected to a load that is off. The COC includes the following table on standby (no-load) power requirements. A similar table exists in the DOE standard with the maximum no-load power for 1 W to 49 W output power ratings equal to 0.100 W.

<table>
<thead>
<tr>
<th>Rated Output Power (P_{no})</th>
<th>No-Load Power Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tier 1</td>
<td>Tier 2</td>
</tr>
<tr>
<td>≥ 0.3 W and &lt;49 W</td>
<td>0.150 W</td>
</tr>
<tr>
<td>≥ 49 W and &lt; 250</td>
<td>0.250 W</td>
</tr>
<tr>
<td>Mobile handheld battery driven &lt; 8 W</td>
<td>0.075 W</td>
</tr>
</tbody>
</table>

Table 1 – Code of Conduct, no-load power consumption, version 5, October 2013. Tier 1 levels effective January 2014, Tier 2 levels effective January 2016.

Pushing no-load power even lower for cell phone chargers is the 5-Star program introduced by leading cellphone manufacturers together with the European Commission’s Integrated Product Policy program. This standard for mobile-device chargers has a no-load power maximum of less than 30 mW to qualify for the highest, 5 star, rating. Finally, there are OEMs who are specifying 10 mW and others are pushing for less than 5 mW – this is commonly referred to as zero no-load power.

While these standards explicitly apply to “external power supplies” up to power levels of 250 W, there are initiatives targeted at a broad range of consumer end equipment with similar goals of energy conservation. Examples include the European Union’s Ecolabel and the United States’ Energy Star programs.
B. Common Implementation

A compact physical design and a V-I response curve for a 5 V, 10 W flyback converter are shown in Figure 2. Tight control of output current as well as voltage is desirable to maximize the current availability for a given thermal capability and/or to accommodate current limitations of connectors between the adapter and its load. As a result, the manufacturers of these supplies have been leaders in the adoption of innovative topology and control methods that shrink a bill of materials and maximize the efficiency of the low power AC/DC converter.

![Image of a 5 V, 10 W AC/DC converter](image)

Some widely adopted innovations used in these converters include:

1) Valley switching or quasi-resonant switching to reduce switching losses and EMI filtering.
2) Variable frequency control that reduces switching losses at fractional output power levels, particularly important to reduce standby power consumption.
3) Higher frequency operation that reduces the size of magnetic components.
4) Magnetic versus optical feedback that reduces part count and cost. This is also known as primary side regulation (PSR) implying that the voltage reference for the system is located within the PWM controller on the primary side of the power supply.
5) Primary based output current control – with knowledge of the primary-side switch current and the timing of the transformer current an accurate output current limit is obtained.
6) Feed-forward output compensation, also known as cable compensation, improves output voltage regulation at the end of a resistive cable that connects the supply to its load.

The basic components of a common low power AC/DC flyback converter are shown in Figure 3. The key elements of the supply are:

1) The flyback transformer, which includes a primary winding, a secondary winding and a bootstrap, or auxiliary, winding used to power the primary control circuitry. The auxiliary winding voltage also contains information about the input and output voltage and output rectifier conduction time. The transformer provides voltage transformation and galvanic isolation between the primary and secondary circuits.
2) A PWM controller and power switch. The controller uses peak current and frequency control for regulation and requires a means to start-up when a line voltage (VAC) is first applied.
3) In many non-PSR flybacks a TL431 and optical coupler provide a reference and amplified/filtered feedback signal to the controller. The optical coupler is used when galvanic isolation must be maintained between the primary and secondary domains.

Figure 2 – A highly compact 5 V, 10 W AC/DC converter is shown along with the corresponding V-I response curve.

![V-I response curve](image)

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1 Technically, the correct term for the magnetic device in a flyback supply is “coupled-inductor, as the device is used to store and transfer magnetic energy. However, due to popular convention and for the sake of consistency, it is referred to as a transformer in this paper.
Not shown in Figure 3 is the EMI filter, which at lower power levels, typically consists of a simple Pi-filter at the bulk supply for differential noise reduction.

Figure 3 – A historically popular AC/DC flyback converter circuit.

C. Modes of Operation

When discussing the operation of the flyback a good place to start is with mode of operation of the transformer current. There are three modes of operation – continuous conduction mode (CCM), discontinuous conduction mode (DCM) and a third mode referred to as transition mode, boundary mode or critical conduction mode. This paper refers to this third mode as transition mode (TM). In TM the current falls to zero each switching cycle, like in DCM, but the next cycle starts immediately – meaning that there is no discontinuous time but the output diode has gone to zero current before the power switch is turned on.

Operation in CCM implies that the transformer current does not go to zero between on-times of the power switch. This mode of operation, outlined in Figure 4, is typically used with a fixed frequency control method where only the duty-cycle of the power switch is used to ramp up or down the operating level of the transformer. The steady state average duty-cycle is set by the ratio of input to output voltages and the turns ratio – the level of

Figure 4 – Continuous conduction mode (CCM) flyback operation.
power transfer is proportional to a net integral of a duty-cycle deviation.

In DCM operation, shown in Figure 5, the total flux in the core, or net winding current, goes to zero between switching cycles. Here the switching period is broken into three components, \( T_{\text{ON}} \), \( T_{\text{DM}} \) and \( T_{\text{DIS}} \). The on-time of the power switch, \( T_{\text{ON}} \), now controls an energy level that is stored each cycle in the transformer. The remainder of the switching period is divided into two parts, \( T_{\text{DM}} \), or demagnetization time, and \( T_{\text{DIS}} \), or discontinuous time. During \( T_{\text{DM}} \) the energy that was stored in the transformer is delivered to the secondary output. Once the stored energy has diminished to zero, the transfer is complete. During \( T_{\text{DIS}} \) the energy in the transformer remains at zero.

TM operation is a special case; it designates operation at the boundary of CCM and DCM. In transition mode the control law of the converter forces the turn-on of the power switch immediately following a zero current condition on the secondary winding.

By inspection one sees the triangular waveforms in DCM and TM have somewhat higher RMS losses versus the trapezoidal shape of the CCM waveforms for a given power throughput. These losses are seen in the power switch, transformer core and transformer windings. From an efficiency standpoint this may seem to give an edge to the CCM mode of operation. In actuality, the diode reverse recovery losses associated with turning on the power switch while the output diode is still conducting and switching losses associated with the non-zero starting primary current are generally high enough to more than overcome the increased RMS losses, commonly giving the efficiency edge to the TM or DCM modes.

This simple advantage of the non-CCM mode of operation drives most AC/DC adapters to be designed to operate in the discontinuous mode of operation at rated power levels. This is further reinforced by several associated characteristics of a CCM supply. These are radiated electro-magnetic interference (EMI) associated with the diode reverse recovery, possibly larger magnetic size needed for the higher inductance values and a more complex loop compensation [1].

There are cases where peak and momentary (relative to the thermal time constants of the system) power levels greater than the continuous rating are needed out of the converter. Here a temporary transition from DCM to CCM can have the advantage of delivering up to twice the output power.

- **Single switch control**
- \( T_{\text{ON}} \):
  - Switch on-time
  - Energy taken from \( V_{\text{IN}} \) and stored in primary
  - Core is “magnetized”
- \( T_{\text{DM}} \):
  - Switch is off
  - Stored energy is fully transferred to \( V_{\text{OUT}} \)
  - Core is “demagnetized”
- \( T_{\text{DIS}} \):
  - Discontinuous time
  - Currents are zero
  - \( T_{\text{DIS}} = 0 \) \( \rightarrow \) transition mode

Figure 5 – Discontinuous conduction mode (DCM) flyback operation.
power for a given transformer size and peak current operating level.

D. Valley Switching

The power lost in the switch is further reduced in discontinuous systems by using valley switching. Referring to Figure 6, in DCM operation at the end of the demagnetization period the windings are at known voltages, and momentarily held there by the parasitic capacitance of the connecting circuits. For the purposes of this paper it assumes ideal magnetic coupling and lumps the scaled parasitic capacitances from all the windings to a single switch-node capacitance, $C_{SWN}^2$. The switch-node voltage is at the bulk voltage plus the reflected output secondary voltage (referred to as the flyback voltage, $V_{FB}$).

$$V_{SWN}(\text{during } T_{DM}) = V_{BULK} + \frac{N_P}{N_S} (V_{OUT} + V_D) = V_{BULK} + V_{FB} \quad (1)$$

Where $N_P$ and $N_S$ are the number of turns of the primary and secondary transformer windings, respectively. In CCM operation the switch-node is approximately this voltage at turn-on.

When the power switch is turned on, energy proportional to the capacitance and the square of the switch-node voltage is dissipated by the switch. If the turn-on of the switch is delayed, then the voltage on the switch-node naturally resonates to a voltage, the valley voltage, approaching:

$$V_{SWN} \text{ @ end of } T_{DM} + \frac{T}{2} = V_{BULK} - V_{FB} \quad (2)$$

Here $T_R$ is the natural resonant frequency of the LC tank formed by the primary winding inductance and $C_{SWN}$. Turning on the switch at this lower voltage reduces the switch dissipation by an amount equal to the energy difference in $C_{SWN}$. As long as the bulk voltage is greater than the flyback voltage, a converter operating at a switching frequency, $f_{SW}$, has a savings in power equal to:

$$\frac{1}{2} C_{SWN} \times (V_{BULK} + V_{FB})^2 - (V_{BULK} - V_{FB})^2 \times f_{SW} = 2 \times C_{SWN} \times V_{BULK} \times V_{FB} \times f_{SW} \quad (3)$$

$C_{SWN}$ is generally dominated by the total output capacitance of the power switch, COSS, the inter-winding transformer capacitance, heat-sink capacitance and the junction capacitance of the rectifiers tied to the secondary and auxiliary windings. An easy way to estimate $C_{SWN}$ is to observe the resonant frequency, $1/T_R$. Knowing the primary inductance of the transformer, an effective value of $C_{SWN}$ is calculated. When doing this, be aware that $C_{SWN}$ may have some non-linear components depending on the type of switch being used. Particularly, the commonly used super-junction MOSFETs have a highly non-linear $C_{OSS}$ when the drain voltage is below approximately 25 V.

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$Figure 6 – Idealized switch-node waveforms in CCM and DCM with valley switching.$
This savings cannot be realized with CCM operation since the voltage on the switch-node is always equal to the flyback voltage plus the bulk voltage at turn-on. In a DCM supply without valley switching, turn-on theoretically happens anytime during a resonant cycle, resulting in some fraction of this energy savings. Thus the savings, if any, depend on the specific operating point of the converter. If the discontinuous time of a switching cycle is long then the potential for recovering this energy is lost, as the energy that was available to resonate the switch-node is instead dissipated by the damping elements in the resonant tank.

In a discontinuous supply with valley switching the switch-node waveform has three basic shapes. These are shown in Figure 7. The first of these waveforms shows the turn-on at the first valley after the end of the demagnetization time. Since the discontinuous time is minimal it is essentially transition mode. A converter that operates in this mode of first valley switching over a range of peak currents and frequencies is commonly referred to as a quasi-resonant flyback converter.

The middle waveform in Figure 7 shows valley switching in a DCM supply where the operating frequency is reduced such that switching takes place on the valley following the expiration of a forced minimum period, $1/f_{SW}\text{(limit)}$. This mode of frequency control with valley switching is sometimes referred to as “valley skipping”. The last waveform in this figure shows a low frequency case, where the resonant ringing is fully dissipated within the operating period. Here the next switching cycle is initiated by the timer expiration since no resonant valleys remain.

An additional benefit of valley switching is the reduction of the high frequency elements in the conducted and radiated EMI that are associated with the turn-on edge of the power switch. The reduction of the high dv/dt portion of the falling drain voltage and high di/dt from reverse recovery and capacitive discharge are both helpful in reducing EMI.

**E. Control Law**

In the discontinuous flyback converter a controlled amount of energy is taken from the input and stored in the transformer during the switch on-time and, minus some losses, delivered to the load before the next switching cycle. The cycle energy, $CE_{ST}$, stored in the transformer at the end of a switch on-time is equal to:

$$CE_{ST} = \frac{1}{2} L_P \times I_{PRI\text{ (peak)}}^2 \tag{4}$$
Where $L_p$ is the inductance of the transformer primary winding and $I_{PRI(peak)}$, also referred to as $I_{PP}$, is the current level in this winding at the end of the switch on-time.

The product of the cycle-energy and the switching frequency approximates the input power level, ignoring leakage inductance, input rectifier and other losses:

$$P_{IN} = CE_{ST} \times f_{SW} \quad (5)$$

The output power level is related to the input power with an efficiency factor. This overall efficiency varies with the supply’s load, input voltage and operating temperature.

$$\eta = \frac{P_{OUT}}{P_{IN}} \quad (6)$$

From this it is easy to see that the converter’s output power level modulates by controlling the switching frequency, i.e. frequency modulation (FM), or controlling the energy/cycle, i.e. peak current amplitude modulation (AM), or both.

In a PWM regulator the control law is the rule that is applied to the amplified error voltage to control the converter output power level. Typically the amplified error voltage is simply the output of an inverting amplifier that compares a measurement of the output, the output voltage in this case, to a reference voltage level. While there are many subtle differences in how discontinuous mode controllers regulate, they are generalized into three commonly used categories: fixed frequency DCM, variable frequency DCM and variable frequency TM/DCM. The last is also known as quasi-resonant (QR) when the controller includes valley switching.

### i. Fixed Frequency DCM

A controller operating in DCM with a fixed frequency control law will vary the peak primary current at mid and high power loads to regulate the output. The peak current is generally controlled by comparing the amplified error voltage with the drop across a current sense resistor in the return of the power switch – terminating the switch on-time when the current sense signal crosses the error amplifier output.\(^3\) Since only the peak switch current is controlled, the dynamic range of the converter is limited to the square of the ratio of the maximum to minimum switch currents. This “AM” dynamic range limitation is imposed primarily by the operating range of the bulk supply, the maximum operating frequency, and the minimum controllable on-time of the controller/switch combination.

![Control Law Profile](image)

*Figure 8 – Fixed frequency control law.*

A control law profile for a fixed frequency DCM controller is shown in Figure 8. The actual PWM controller may or may not allow CCM operation. During normal conditions, the proper choice of the transformer inductance relative to the operating frequency and power level achieves DCM. Unless prevented by the controller it is difficult to avoid CCM operation during situations when $V_{OUT}$ is low, such as in a start-up or an overload condition.

\(^3\) This describes traditional current mode PWM control that became very common in the 1980s. This variant happens to be operating with discontinuous inductor current. In this type of power supply, current mode control over a variable on-time controller has several advantages, including a transfer function that is independent of the input voltage and inherently good control of the peak switch and transformer magnetizing currents.
Figure 9 – Switching frequency and peak primary current versus output power for a DCM fixed frequency control law.

With this control law the resulting peak primary current varies as the square root of the output power, illustrated in Figure 9 and implied by the following expression:

\[ P_{\text{OUT}} = P_{\text{OUT}}(\text{max}) \times \left( \frac{I_{\text{PP}}}{I_{\text{PP}}(\text{max})} \right)^2 \]  \hspace{1cm} (7)

Here \( I_{\text{PP}}(\text{max}) \) is the peak primary current at \( P_{\text{OUT}}(\text{max}) \).

The main benefit of this control law is the known operating frequency at mid and higher loads. This is important in systems where spectral interference must be minimized. It suffers with lower fractional load efficiency and standby power dissipation primarily since much of the switching losses remain constant with output power.

**ii. Variable Frequency DCM**

Figure 10 shows the second control law, variable frequency DCM. In this control law the high power region of operation is controlled purely with frequency modulation while the peak switch current is held constant. Mid to very low power levels are then controlled with an AM region. Very light, or standby, regions of operation are accommodated with a second FM region, or alternatively a cycle skipping or burst mode of operation.

Figure 10 – Variable frequency DCM control law.

The response of the peak primary current and switching frequency, Figure 11, illustrates the dynamic range benefit of using both AM and FM control. The converter regulates the output smoothly to very low fractional or standby power levels. Like the fixed frequency control law, full load power is a function of the product of the switching frequency, primary inductance and the square of the primary peak current. Again like the fixed frequency controller, RMS losses at full load are minimized if transition mode operation is approached at the minimum input voltage level. This constrains the peak primary current at \( P_{\text{max}} \) conditions to be

\[ I_{\text{PP}}(\text{max}) = \frac{2 \times P_{\text{OUT}}(\text{max})}{\eta} \times \frac{1}{V_{\text{FB}}} + \frac{1}{V_{\text{BULK}}(\text{min})} \]  \hspace{1cm} (8)

Valley switching slightly raises the needed peak primary current beyond this level.

Figure 11 – Switching frequency and peak primary current versus output power for a DCM variable frequency control law.
iii. Variable Frequency TM/DCM

If the control law is modified in the high power region to use AM modulation then transition mode operation is realized, but only in this region of operation. This offers some potential improvement in full load efficiency by allowing the reduction of RMS levels of the primary and secondary currents relative to the output power across an input voltage range. The operating frequency and the peak primary current vary with both the input voltage and load. This implies a larger inductance in the transformer to allow a lower operating frequency at full load and low line (input voltage). This is necessary to keep switching losses at bay as the operating frequency increases as either the load is decreased or the input voltage is raised.

A control law that allows transition mode at full load and DCM operation at lighter loads is shown in Figure 12. The control law has an upper AM region of operation for heavy loads (high VCL), an FM region for medium power loads, and an additional AM region and burst region for lighter loads. Either or both of the low power AM and burst regions may not be needed depending on the type of light load performance required.

The upper AM region, or QR region, is the only place where the power supply operates in transition, or quasi-resonant, mode. In this region the controller linearly varies the peak primary current, reducing it in response to a decreasing load. Since the next switching cycle starts when the previous cycle ends this causes the frequency to change inversely, increasing with decreasing load. This is illustrated in Figure 13 and detailed in the expressions below. A potential drawback to this control law is that its operating point in the QR region is input voltage dependent, i.e. the peak primary current must change with the input to maintain a constant load. For the control variable, IPP, to change the time constants of the overall voltage loop come into play. This makes rejection of ripple on the input voltage more difficult if the loop bandwidth is not much greater than the input ripple frequency.

In the QR region the output power is given by:

\[ P_{OUT}(QR \text{ region}) = \frac{\eta \times I_{PP} \times V_{FB} \times V_{BULK}}{2} \]  

And the operating frequency is:

\[ f_{SW}(QR \text{ region}) = \frac{1}{L_{P} \times I_{PP}} \times \frac{V_{FB} \times V_{BULK}}{V_{FB} + V_{BULK}} \]  

Here again this paper does not take into account the impact of valley switching on the operating period, which has the effect of slightly raising the peak current needed.

The \( f_{SW}(max) \) limit shown in the control law of Figure 12 is there to constrain the maximum operating frequency. This limit is factor if a larger upper AM range, than illustrated, is utilized or if the power supply is designed to have full-power operating frequencies closer to this limit. In the example illustrated in Figure 13, the supply stays in transition mode until \( I_{PP} \) reaches \( I_{PP(mid)} \). At that point the controller responds to any further decrease in load by moving immediately down the FM region of Figure 12 until it intercepts the supply’s transition mode frequency of Equation 10 and pulls the supply into DCM operation with a reduced switching frequency. If the transition mode frequency does hit \( f_{SW}(max) \) then the supply also goes into DCM and the frequency stays at \( f_{SW}(max) \) until \( I_{PP} \) reaches its mid-level and FM control takes over.
II. PRIMARY SIDE REGULATION

Most AC/DC flyback power supplies that operate independently of a larger system include an extra transformer winding, connected in phase with the output winding but referenced to the primary circuit, as in Figure 3. This winding is commonly referred to as an auxiliary or bootstrap winding. As mentioned earlier, this winding serves several purposes. Revisiting them in a bit more detail, they are:

- **Bias power**: Most commonly, this winding voltage is rectified and used to provide bias power to the primary circuit during regulation.
- **Demagnetization sensing**: The primary controller uses the transitions of this waveform to know when, or if, the demagnetization of the transformer core is completed. This is useful to guarantee DCM or TM operation or to achieve valley switching.
- **Input (bulk) voltage sensing**: During the power switch on-time the voltage across the winding is proportional, by the appropriate turns ratio, to the bulk input voltage.
- **Output voltage sensing**: During the demagnetization time when the secondary current is flowing, the voltage at this winding is proportional to the output voltage plus any series secondary voltage drop such as the output rectifier.

The phrase “primary side regulation” (PSR) generally describes the use of magnetic feedback via this auxiliary winding to close the voltage feedback loop. This allows the output voltage to be regulated completely from the primary side of an isolated supply. More specifically, primary side voltage regulation is referred to as PSR-CV, where the CV is for constant voltage. PSR-CC, on the other hand, refers to the control of output current from the primary. Here CC is for constant current.

PSR-CV and -CC regulation use a combination of the timing information and reflected voltage available at the auxiliary winding to target a square V-I load response, such as shown in Figure 14. A well regulated output current, \( I_{OCC} \), in Figure 14, is useful to control power dissipation in the converter, or to limit current to the load. Generally in an AC/DC isolated supply, as noted above, the primary circuit is powered from an auxiliary winding. This implies that no, or limited, bias voltage is available when the converter is not running, or when the output voltage is near zero. Considering this, it is apparent that a special start-up circuit is needed to initiate operation when power is first applied, or after various fault or shutdown scenarios. As seen in Figure 14, this also results in a minimum sustained operating, or hold-up, voltage, \( V_{OHU} \). When \( V_{OUT} = V_{OHU} \), the minimum voltage to operate the primary circuits is present at the auxiliary winding; below that level the converter stops normal operation.

\[
\begin{align*}
\text{V}_{OCV} & \quad \text{V}_{OHU} \\
\text{Output Voltage} & \quad \text{Output Current} \\
0 & \quad I_{OCC}
\end{align*}
\]

*Figure 14 – PSR-CV and PSR-CC regulation when combined can results in an essentially square V-I characteristic.*
A. The Benefits of PSR
An important advantage of PSR-CV is the elimination of the secondary-based feedback circuit and the need to provide a separate feedback path across the isolation boundary to the controller. This is illustrated in Figure 15.

A summary of the benefits and trade-offs of PSR-CV operation are given here. Some of these are discussed in more detail in the following sections, including operational examples and measurements.

**PSR-CV Advantages:**
- Reduced bill of materials helping to reduced cost, size and complexity
- Potential for improved reliability by eliminating parts and optical coupler
- Simple and often fully integrated loop compensation
- Easy implementation of output droop compensation to deal with series resistance to the load, commonly called cable compensation for AC/DC adapter applications\(^4\)
- Easy extension to add PSR-CC control

**PSR-CV Disadvantages:**
- Voltage regulation tolerance is typically limited to no better than +/-3% to +/-5% specifications
- Transient response is dependent on the operating frequency, recovery from light loads to full load can result in large output voltage droop
- Ability to accommodate CCM operation is possible, but more difficult – controller product options are more limited
- Not compatible with Kelvin load sensing

B. PSR-CV, Voltage Regulation

\(i.\) **Voltage Sampling**

The voltage sensing utility of the auxiliary winding, as it is used for magnetic feedback, is illustrated below in Figure 16. This figure shows idealized voltage waveforms for the auxiliary winding voltage. The most obvious challenge to using the winding for regulation is sampling the non-continuous voltage during the T\(_{DM}\) period. In addition, good regulation implies accurate control of the auxiliary to secondary transformer turns ratio, \(N_A/N_S\) and a repeatable rectifier forward voltage, \(V_D\).

\(^4\)In a PSR-CV isolated supply, this is more important since Kelvin connection to a load is not possible as it would be with a secondary based feedback system. Although, in many “cable connected” load scenarios the cable itself does not support dedicated lines for load sensing, leaving feed-forward compensation still useful.
Getting a good feedback signal becomes a bit more daunting when some of the common “second order” realities are considered. There are a number of obstacles in trying to get a good feedback signal from a transformer winding. A basic description of these follows:

- **Leakage inductance**: Non-ideal coupling between the secondary and primary windings results in leakage inductance that also stores energy proportional to \( I_{PP} \) during each cycle. This energy causes a spike in voltage at the switch-node (primary winding driven terminal) that is largely seen as a reduced spike at the auxiliary winding. This spike in voltage resets the leakage inductance and allows the primary current to transfer to the secondary circuit. After the current in the leakage inductance goes to zero, the primary winding is left charged to an elevated voltage by the node capacitance. The energy results in a high frequency ringing that is seen at the auxiliary winding.

  The magnitude and shape of this “leakage spike” is generally controlled by an RCD clamp circuit whose primary job is to limit the peak voltage that the primary switch sees. If a slow diode is used to rectify the auxiliary winding, this also impacts the shape of the auxiliary winding voltage by absorbing some of the leakage energy as it is forward biased or by its reverse recovery current interacting with the output impedance at the auxiliary winding.

  Both the spike and the ringing, or any other induced voltage perturbations, must be dealt with by the sampling circuit to capture an accurate output voltage representation.

- **Equivalent series resistance (ESR) and inductance (ESL)**: During the demagnetization period, \( T_{DM} \), the reflected voltage from the secondary contains additional offsets due to resistance or inductance in series with the secondary current loop. Generally the inductance impact, which causes a voltage offset proportional to the approximately constant \( di/dt \) during \( T_{DM} \), is small and may be neglected. The effect of the resistance cannot. The secondary winding, the output capacitor and output diode have enough ESR that the reflected auxiliary winding voltage during \( T_{DM} \) may have a significant slope.

Although…..

1. \( V_{OUT} + V_D \), scaled by a turns ratio, at Aux during \( T_{DM} \)
2. Use for voltage feedback (at VS input)

- Signal is not continuous
- \( N_A / N_S \) must be controlled
- \( V_D \) (output diode voltage) is a source of error
- Nothing is this simple

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**Figure 16 – PSR feedback concept.**
An example of the impact of ESR, leakage inductance and equivalent switch-node capacitance is shown in Figure 17. The figure suggests that there is an ideal point in time, “VS Sample”, to capture the feedback signal. This is the point in time when the output rectifier’s current reaches zero.

As long as a sample is referenced in time to the zero-current event and some averaging is applied, the dependence of the feedback to changes in a modulated peak primary current are avoided. Sampling with a time referenced to the leading edge of $T_{DM}$ results in degraded load regulation unless the ESR induced errors are otherwise compensated. An added difficulty in compensating for ESR errors is their time and temperature dependence. The lifetime variation of the output capacitor’s ESR, for example, is significant.

**ii. The Voltage Loop and Transient Performance**

Once an accurate feedback sample is available, the remaining voltage regulation loop is straightforward and conventional, as illustrated in Figure 18. Most of the available controller products with PSR integrate the loop filter, $M(s)$, function. This is beneficial for most applications, reducing parts and design complexity. On the other hand, it can be a source of frustration for those who prefer to do their own loop compensation. An interesting characteristic of these flyback loops is the absence of the output zero in the Laplace transfer expression that is often used as a phase lead source in the loop compensation. This zero is not present in these loops if the sampling takes place at a consistent secondary current level, e.g. zero.

An important limitation of primary side control for voltage regulation is the impact of the feedback method on transient load regulation. Since the output voltage is only sampled during a power
cycle the controller becomes “blind” to what is happening at the output between switching cycles. This is not a problem if the switcher is operating at a high frequency for load steps in either direction, as is the case for negative load steps or load steps from modest to high loads. But when the power supply is at a very light load and operating at a greatly reduced switching frequency, the output droop for a positive load step is dramatic. The timing of the load step within the switching cycle impacts this as well as the size of the step and output capacitor value.

### Transient Response
- Low switching frequencies when $I_{OUT}$ is very low
- Feedback is only available during a switching event
- Poor transient performance, or a very large output capacitor is needed

*Figure 19 – Transient performance: A PSR supply is blind to load steps between switching cycles.*

The magnitude of the maximum potential output droop, depending on the timing of the load step relative to power cycles, is given below:

$$V_{OUT} = \frac{I_{OUT}(\text{step})}{C_{OUT} \times f_{SW}}$$

This is a clear trade-off when using primary side regulation if tight transient regulation is needed. As will be discussed later, this is also impacted by the desire to reach low standby power, which drives the switching frequencies very low.

### iii. Voltage Regulation Error Sources

With care, static output voltages with PSR are controlled to better than +/- 5%, and more tightly in some cases. Some sources of voltage error that have to be considered include:

1) **Reference, error amplifier and resistors:** Tolerances, drift and offsets, as always, are a key source of manageable error, but no more so with PSR than with traditional feedback.

2) **Output rectifier drop:** Since the circuit is regulating the sum of $V_{OUT} + V_D$, the diode forward voltage needs to be accounted for. A difficulty with procuring the diode is the fact that most manufacturers do not specify the forward drop at low currents with any type of precision. For a given diode technology and current rating this drop should be reasonably consistent. Limiting sourcing of the diode to a specific manufacturing flow is still better.

   One characteristic of the diode forward voltage that needs consideration is its temperature variation. Schottky diodes have a temperature coefficient of about -1.2 mV/ºC and silicon diodes about -2 mV/ºC. The potential output drift is significant when 100 ºC operating ranges are needed at lower output voltages. Compensation for this effect normally has to take place in the control IC.

3) **Transformer:** Automated manufacturing yields consistent results on the winding counts and winding coupling, which impacts the equivalent turns ratios. As long as a good sampling method is used, the impact of leakage inductance on voltage regulation is small.

4) **Winding voltage sampling errors:** Primarily at light loads, when the demagnetization time is short and when the output load approaches that of the primary circuit, sampling errors may be significant.

   - The effects of the auxiliary rectifier or primary clamping diode recoveries are a problem if they crowd the trailing edge of the flyback voltage.
   - Cross regulation of the auxiliary to secondary windings is degraded when the current flowing in the auxiliary diode becomes significant or greater than the current in the secondary circuit.
• Excess filtering of the VS signal can result in shifts in the sampling circuit, again at light loads where a narrow flyback pulse must be dealt with.

C. PSR-CC, Current Regulation

The need to accurately control output current in a flyback power supply is driven by 5 W and 7 W USB battery chargers that are designed to provide a maximum current in a minimum form factor. USB charging standards and resulting OEM specifications also limit the maximum output current across the full range of the output voltage. Each of these is supported by the square V-I characteristic shown in Figure 14.

Regulating the output current from the primary side relies upon controlling the peak primary current and the duty-cycle of the secondary circuit. The primary and secondary winding currents are shown in Figure 20, followed by the important control expressions.

![Figure 20 – Primary side current control: Shown are the primary and secondary winding currents of the transformer.](image)

By keeping the product of the demagnetization duty-cycle, $T_{DM}/T_{SW}$, and the peak primary current, $I_{PRI}(peak)$, constant, good output current regulation is achieved – typically as good as +/-5%.

Sources of error in the output current come from:

$$I_{PRI}(peak) \times \frac{T_{DM}}{T_{SW}}$$

1) **tolerance:** This is specified as a single current sense threshold voltage parameter that includes the tolerance of the duty-cycle term, or as a current parameter in the case of an integrated current sense and/or power switch. There is some output current dependence on line voltage unless compensation is implemented to account for power switch turn-off delay.

2) **Leakage inductance:** Leakage inductance, and its snubbing or clamping, impacts the level of the secondary peak current versus the peak primary current. This impact is generally low since leakage inductance must be kept low for efficiency reasons.

3) **Transformer:** As with PSR-CV, automated manufacturing of the transformer can minimize associated errors.

PSR-CC controllers achieve the best tolerance on output current by keeping $I_{PRI}(peak)$ at its maximum value, minimizing current sense errors during CC regulation, and then limiting the demagnetization duty-cycle to a maximum value, $D_{DM}(max)$. Now there are two constraints in the peak primary current, recalling that in order to optimize the converter’s efficiency the peak primary current level is chosen according to Equation 8. To satisfy both constraints on the current, a given primary to secondary turns ratio is used. Combining Equation 14 and Equation 8 and making a simplifying assumption that the overall efficiency is approximated simply as $V_{OUT} / (V_{OUT} + V_D)$ results in an expression for an optimum primary to secondary turns ratio for a given $D_{DM}(max)$.

$$N_{PS}(opt) = \frac{V_{BULK}(min)}{V_{OUT} + V_D} \times \frac{1 - D_{DM}(max)}{D_{DM}(max)}$$
If a turns ratio larger than this is used, the converter reaches transition mode above the minimum input voltage at full load. If the ratio is lower, then the converter operates more deeply discontinuous than necessary, increasing RMS losses. Valley switching forces slightly lower ratios. In practice, the turns ratio of the flyback primary and secondary must also satisfy restrictions on the voltage capability of the output rectifier or power switch. Fixed values of the demagnetization duty-cycle must therefore be done with care to be reasonably optimum for the intended application.

### III. STANDBY POWER

Many power supplies, particularly those for consumer applications, spend much time in a standby mode. Plugged into the wall 24/7, just waiting for the need to “wake up” and do their thing. The need to be immediately ready to throttle from a no-load or nearly zero load condition to full load conditions results in a continuous level of standby energy consumption. Building a supply that is able to deal with a mWatts to Watts load range while minimally adding to the mWatts is a challenge.

#### A. Contributions to Standby Power

The contributors to standby power, PSB, are generalized into three main components.

$$P_{SB} = P_{LKG} + P_{STRT} + f_{SW}(sb) \times CE_{IN}(min) \quad (16)$$

where:

- $P_{LKG}$ = Capacitor and junction leakage losses
- $P_{STRT}$ = Start-up power
- $f_{SW}(sb)$ = Converter switching frequency during standby
- $CE_{IN}(min)$ = Converter minimum input cycle energy

The leakage of the input bridge rectifiers, the main and auxiliary output rectifiers, any snubbing or clamping rectifiers and the bulk and output capacitors may be a concern at very low target standby power, or at higher temperatures. In the low power AC/DC space, these tend not to be limiting items even down to 10 mW $P_{SB}$ levels.

As discussed earlier, off-line stand-alone AC/DC power supplies require some means to start. In some cases this start-up circuit results in a continuous supply drain off the AC mains or the rectified input bulk voltage, $V_{BULK}$.

In most cases the last term, which is the product of the input cycle-energy and the standby switching frequency, is dominant. A limited range on the amplitude of the peak primary current results in a minimum cycle-energy at the input. The resulting product must satisfy any standby loading on the supply summed with the losses directly associated with delivering it.

#### B. Start-Up Impact on Standby Power

The method for start-up has a large bearing on the standby power, particularly when targeting standby levels below 100 mW. There are two basic start-up methods, as illustrated in Figure 21. The resistive start-up method results in an increase in standby power, while active start-up ideally does not.

An active start-up circuit generally contains a “normally on” high voltage active device, such as a depletion mode MOSFET or JFET, that supplies the needed charging current when the PWM controller is not yet “intelligent”. Once the PWM controller VDD voltage has reached its UVLO(on) level it can turn the active device off, eliminating any addition to standby power. To appreciate the benefits of active start-up we can examine the standby impact of the resistive solution.

The goal of the start-up circuit is to allow the converter to start within a specified maximum start up time, $t_{START}(max)$. This start time is dominated by the time it takes to charge the VDD capacitor, $C_{DD}$, to the turn-on threshold of the primary controller, generally specified as an under-voltage lockout threshold, $V_{UVLO}(on)$, after an input voltage is applied. In order to estimate the charging time we have to first determine the minimum size of $C_{DD}$.
The value of $C_{DD}$ is determined by how much charge it must hold for a given $\Delta V$ across it. After $C_{DD}$ is charged by the start-up circuit to $V_{UVLO(on)}$, the input capacitor has to stay above the controller’s $V_{UVLO(off)}$ threshold long enough for the supply’s output voltage to come up to the minimum hold-up voltage – this is a function of the converter’s maximum output current, the output capacitor size and any load on the converter during start-up. Referring to this output charging time as $t_{CHRG}$ it is estimated by:

$$t_{CHRG} = \frac{C_{OUT}}{I_{OUT(max)} - I_{LOAD(start)}} \times \frac{V_{ULVO(off)} + V_{DAUX}}{N_{AS}} - V_D$$

(17)

where $V_{DAUX}$ and $V_D$ are, respectively, the auxiliary and output rectifier drops and $N_{AS}$ is the auxiliary to secondary turns ratio.

Then the size of the minimum VDD capacitor is calculated:

$$C_{DD}(min) = \frac{t_{CHRG} \times I_{RUN}}{V_{ULVO(on)} - V_{ULVO(off)}}$$

(18)

$I_{RUN}$ is the normal bias current of the primary circuit.

Finally the minimum charging current from the start-up source (resistor or active device) is calculated:

$$I_{CHRG}(min) = \frac{C_{DD}(min) \times V_{ULVO(on)}}{t_{STRT(max)} - t_{CHRG}} + I_{START}$$

(19)

where $I_{START}$ is the current draw of the primary circuit as VDD is moving from 0 V to $V_{UVLO(on)}$.

Here is a good point to put some numbers to this. Below is a table with some relevant start-up parameters and typical values that may be needed for a 25 W, 12 V AC/DC supply.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{OUT(max)}$</td>
<td>2.3</td>
<td>A</td>
</tr>
<tr>
<td>$I_{LOAD(start)}$</td>
<td>2.1</td>
<td>A</td>
</tr>
<tr>
<td>$C_{OUT}$</td>
<td>470</td>
<td>$\mu$F</td>
</tr>
<tr>
<td>$N_{AS}$</td>
<td>1</td>
<td>-</td>
</tr>
<tr>
<td>$V_{UVLO(on)}$</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>$V_{UVLO(off)}$</td>
<td>8</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DAUX}$</td>
<td>0.7</td>
<td>V</td>
</tr>
<tr>
<td>$V_{D}$</td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td>VDD(run)</td>
<td>12</td>
<td>V</td>
</tr>
<tr>
<td>$I_{RUN}$</td>
<td>2</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{START}$</td>
<td>10</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$t_{START(max)}$</td>
<td>1</td>
<td>s</td>
</tr>
<tr>
<td>VAC RMS(min)</td>
<td>85</td>
<td>V</td>
</tr>
<tr>
<td>VAC RMS(max)</td>
<td>240</td>
<td>V</td>
</tr>
</tbody>
</table>

Table 2 – Relevant start-up parameters and typical values for a 25 W, 12 V AC/DC power supply.
Using the values from Table 2, $t_{\text{CHRG}}$ is estimated to be 19.3 ms. Note $t_{\text{CHRG}}$ is much lower if the load at start-up is reduced, but it is always good to consider this case where start-up into a full rated output load is required. Using the expressions above, $C_{\text{DD(min)}}$ is calculated to be 3.2 μF and $I_{\text{CHRG(min)}}$ to be 75.5 μA for one second start-up time.

If a resistive network to the bulk voltage is used, 75.5 μA would dictate a value for resistor $R_{\text{STR}}$ in Figure 21 of approximately $85 \times \sqrt{2} / 75.5 \mu\text{A} = 1.59 \text{ MΩ}$. Using a 1.5 MΩ resistor then has a standby power impact ranging from 9.6 mW at 85 VAC RMS to 77 mW at 240 VAC RMS using the peak of the line voltage minus the VDD run level as the static voltage across the start-up resistor.

These calculated values are summarized in Table 3.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{\text{CHRG}}$</td>
<td>19.3</td>
<td>ms</td>
</tr>
<tr>
<td>$C_{\text{DD(min)}}$</td>
<td>3.2</td>
<td>μF</td>
</tr>
<tr>
<td>$I_{\text{CHRG(min)}}$</td>
<td>75.5</td>
<td>μA</td>
</tr>
<tr>
<td>$R_{\text{STR}}$</td>
<td>1.5</td>
<td>MΩ</td>
</tr>
<tr>
<td>$P_{\text{STRT}}(85\text{V AC})$</td>
<td>&gt; 9.6</td>
<td>mW</td>
</tr>
<tr>
<td>$P_{\text{STRT}}(240\text{V AC})$</td>
<td>&gt; 77</td>
<td>mW</td>
</tr>
</tbody>
</table>

Table 3 – Resistive start-up dissipation.

Standby power levels of under 30 mW are possible with resistive start-up, but obviously only under certain circumstances – longer start time allowance, smaller relative output capacitor or load current, etc. When those relaxations are not possible, active start-up is needed.

C. Minimum Input Cycle-Energy and Achieving Low $P_{\text{SB}}$

i. Control Law Impacts

Once the static losses during standby are understood, the rest of the standby power is attributed to the minimum cycle-energy and the operating frequency of the power supply during standby. It should be noted that the minimum operating frequency for a given cycle-energy is set by the actual non-zero load within the converter both at the primary side (auxiliary) and at the secondary side outputs and by the fraction of the input cycle-energy that actually gets to an output.

The power consumption of the primary control circuit bias must obviously be low during standby, as it sets a minimum load on the auxiliary winding output. This load combines with any standby or “pre-load” at the main secondary output to form a total effective standby load.

The PWM controller must be able to operate at a low enough effective operating frequency, or regulation is not possible. It is also beneficial for the controller to reach the minimum switching frequency with a constant time/cycle – i.e. not by generating a burst of cycles with a long wait time between bursts, see Figure 22.

Figure 22 – To achieve low standby power, operation at low average switching frequencies is needed.

Beyond a low operating bias current and frequency, in standby situations the PSR-CV controller allows the supply to operate at a small cycle-energy. This allows a higher standby operating frequency, easing the transient response issue described earlier while still keeping $f_{\text{SW}} \times CE_{\text{IN(min)}}$ small. A first order estimate of the minimum input cycle-energy is given here by:

$$CE_{\text{IN(min)}} = \frac{P_{\text{OUT(max)}}}{\eta_{T} \times f_{\text{SW(@P max)}}} \times \frac{1}{K_{AM}} \quad (20)$$

where:

$$K_{AM} = \frac{I_{PRI(\text{peak@P max})}}{I_{PRI(\text{peak,min})}}$$

Here $\eta_{T}$ is an efficiency estimate of the converter when it is processing $I_{PRI(\text{peak,min})}$ and ignores the bias losses and capacitive switching losses. In most cases $\eta_{T}$ is approximately the same as the full load efficiency. The minimum cycle-energy expression also uses $f_{\text{SW(@P max)}}$, the power supply’s operating frequency at maximum load that is a function of the peak
primary current at full load, the primary inductance, $L_{PRI}$, and the overall converter efficiency.

$$f_{SW}(@ P_{\text{max}}) = \frac{2xP_{\text{OUT}}(\text{max})}{\eta \times L_{PRI} \times (I_{PRI}(\text{peak} @ P_{\text{max}}))^2}$$

(21)

From Equation 20 it would appear that by making $K_{AM}$ large, standby power is kept low and the standby operating frequency high, thus maintaining good no-load transient response. In reality the limitations imposed on operating frequency and, as discussed later, additional contributions to input cycle energy stemming from parasitic capacitance place a cap on practical AM ranges to as low as 3 to 5. In fact, for a given AM range, two restrictions on the full power operating frequency are used to “test” the choice of a targeted frequency. The frequency limitations that depend on the AM range come from the controller’s minimum controllable on-time, and from the minimum $T_{DM}$ required to sample the output in a PSR-CV situation.

The approximate limitation imposed on the switching frequency for a given AM range and minimum demagnetization time is:

$$f_{SW}(@ P_{\text{max}}, T_{DM(\text{min})}\text{imposed limit}) = \frac{T_{DM(\text{min})} \times K_{AM} + T_R}{D_{DM(\text{max})} \times 2^{-1}}$$

(22)

Here $T_R$ is the resonant period of the switch-node after the secondary current goes to zero. This is zero if valley switching is not being used. $D_{DM(\text{max})}$ is the duty cycle of the demagnetization time at full load. If the converter is optimized for efficiency reasons to operate at the transition mode boundary at full load and low line, the maximum duty-cycle for the demagnetization is estimated by:

$$D_{DM(\text{max})} = \frac{T_{DM(\text{max})}}{T_{SW}} = \frac{V_{BULK(\text{min})} / V_{FB}}{V_{BULK(\text{min})} + V_{FB}} \times 1 - \frac{T_R \times f_{SW}(@ P_{\text{max}})}{2}$$

(23)

Here again $T_R$ is set to zero if valley switching is not used. $V_{BULK(\text{min})}$ is the minimum bulk voltage where full output power is delivered.

The minimum controllable on-time of a PWM controller generally is pre-determined and specified by a leading edge blanking specification, $T_{LEB}$. Combined with $K_{AM}$ and the input voltage range, this puts a restriction on the maximum operating frequency given by:

$$f_{SW}(@ P_{\text{max}}, T_{LEB}\text{imposed limit}) = \frac{K_{AM} \times T_{LEB} \times V_{BULK(\text{max})}}{1 - D_{DM(\text{max})} \times V_{BULK(\text{min})} + T_R}$$

(24)

Here $V_{BULK(\text{max})}$ is the maximum operating voltage of the bulk input voltage, and again the $T_R$ term only applies if valley switching is used.

**ii. Switch-Node Capacitance Impact on Cycle-Energy**

In order to actually estimate the achievable standby power, the influence of the switch-node capacitance is studied. In Figure 23 a lumped switch-node capacitance, $C_{SWN}$, is shown with its voltage swing in a standby situation. Here, the switch is turned on until the peak primary current reaches a controlled minimum value followed by a short demagnetization time and then a long discontinuous time. The capacitance sees a large voltage excursion.

The switch-node capacitance increases the input cycle-energy by an amount given by:

$$CE_{IN(\text{cap, total})} = C_{SWN} \times V_{BULK}^2$$

(25)

A portion of this energy is dissipated immediately in the switch and then in the tank by the elements that damp the ringing. This portion is:

$$CE_{IN(\text{cap, dissipated})} = \frac{1}{2} \times C_{SWN} \left( V_{BULK}^2 + V_{FB}^2 \right)$$

(26)

The remaining energy ends up in the primary winding. During the demagnetization period it is then delivered to either the auxiliary or secondary output circuits with some associated loss. This remaining portion is:

$$CE_{IN(\text{cap, out})} = \frac{1}{2} \times C_{SWN} \left( V_{BULK}^2 - V_{FB}^2 \right)$$

(27)
Figure 23 – Switch-node capacitance.

Looking at an example gives additional appreciation of the relevance of this capacitance regarding standby operation. Consider the example of a typical 5 V, 10 W AC/DC with some appropriate values given in Table 4.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{\text{OUT}}(\text{max})$</td>
<td>10</td>
<td>W</td>
</tr>
<tr>
<td>$f_{\text{SW}}(\text{max})$</td>
<td>100</td>
<td>kHz</td>
</tr>
<tr>
<td>$V_{\text{BULK}}(\text{max})$</td>
<td>365</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{FB}}$</td>
<td>80</td>
<td>V</td>
</tr>
<tr>
<td>$K_{\text{AM}}$</td>
<td>4</td>
<td>A/A</td>
</tr>
<tr>
<td>$C_{\text{SWN}}$</td>
<td>70</td>
<td>pF</td>
</tr>
<tr>
<td>$\eta_{T}$</td>
<td>80</td>
<td>%</td>
</tr>
</tbody>
</table>

Table 4 – Parameters for a 10 W, 5 V supply used to illustrate the impact of $C_{\text{SWN}}$.

Using these values the minimum input and output cycle-energy are calculated with and without the impact of $C_{\text{SWN}}$. A good estimate of the fraction of the incremental input energy that is available to offset loads at the primary or secondary circuits is the efficiency estimate, $\eta_{T}$. The value of $\eta_{T}$ approaches, or exceeds, the full load efficiency of the converter since it ignores capacitive, static and bias losses. This is an approximation since not all power losses scale linearly with output power.

As shown in Table 5, the energy drawn from the input and delivered to the output per cycle are both significantly increased by a modest capacitance. In this example, the input cycle energy is more than doubled and the output cycle energy increases by more than 50%. The fact that this effect is significant indicates the diminishing returns in some applications of pushing the AM range in the control law to address very low standby power.

The ratio, $\frac{C_{\text{ENOUT}}(\text{min, total})}{C_{\text{ENIN}}(\text{min, total})} = \frac{9.8 \ \mu J}{17.14 \ \mu J} = 57.2\%$, is the effective incremental efficiency once the converter is operating at the bottom of the AM range(s) where the cycle-energy is at its minimum. If this is defined as a separate efficiency factor, $\eta_{\text{CE(min)}}$, the efficiency of the overall supply in this very low power region is predicted by:

$$
\eta_{\text{LP}} = \frac{P_{\text{OUT}}}{\eta_{\text{CE(min)}} P_{\text{OUT}} + P_{\text{B}} + P_{\text{STR}} + P_{\text{LKG}}} \quad \text{(28)}
$$

$P_{B}$ is the sum of the static loading at the auxiliary and secondary outputs, which is added to any utilized output power, $P_{\text{OUT}}$.

### Input minimum cycle-energy impact from $C_{\text{SWN}}$:

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum CE, ignoring $C_{\text{SWN}}$</td>
<td>$C_{\text{ENIN}}(\text{min, } C_{\text{SWN}}=0) = 7.81 \ \mu J$</td>
</tr>
<tr>
<td>Incremental input CE with $C_{\text{SWN}} @ 70 \ \text{pF}$</td>
<td>$\Delta C_{\text{ENIN}}(70 \ \text{pF, total}) = 9.33 \ \mu J$</td>
</tr>
<tr>
<td>Total minimum input CE with $C_{\text{SWN}} @ 70 \ \text{pF}$</td>
<td>$C_{\text{ENIN}}(\text{min, total}) = 17.14 \ \mu J$</td>
</tr>
</tbody>
</table>

### Split of incremental input cycle-energy due to $C_{\text{SWN}}$:

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dissipated portion of incremental CE</td>
<td>$\Delta C_{\text{ENIN}}(70 \ \text{pF, dissipated}) = 4.89 \ \mu J$</td>
</tr>
<tr>
<td>Portion available to output</td>
<td>$\Delta C_{\text{ENIN}}(70 \ \text{pF, output}) = 4.44 \ \mu J$</td>
</tr>
<tr>
<td>Total incremental input CE with $C_{\text{SWN}} @ 70 \ \text{pF}$</td>
<td>$\Delta C_{\text{ENIN}}(70 \ \text{pF, total}) = 9.33 \ \mu J$</td>
</tr>
</tbody>
</table>

### Output minimum cycle-energy impact from $C_{\text{SWN}}$:

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Incremental output CE = $\eta_{T} \times \Delta C_{\text{ENIN}}(70 \ \text{pF, output})$</td>
<td>$\Delta C_{\text{ENOUT}}(70 \ \text{pF, output}) = 3.55 \ \mu J$</td>
</tr>
<tr>
<td>Output CE, ignoring $C_{\text{SWN}} = \eta_{T} \times C_{\text{ENIN}}(\text{min, } C_{\text{SWN}}=0)$</td>
<td>$C_{\text{ENOUT}}(\text{min, } C_{\text{SWN}}=0) = 6.25 \ \mu J$</td>
</tr>
<tr>
<td>Total output minimum CE with $C_{\text{SWN}} @ 70 \ \text{pF}$</td>
<td>$C_{\text{ENOUT}}(\text{min, total}) = 9.80 \ \mu J$</td>
</tr>
</tbody>
</table>

Table 5 – This table quantifies the impact of the switch-node capacitance on input and output cycle energy for the 5 V, 10 W example. The input cycle energy increases by over 100% and the output cycle energy by over 50%.
iii. Minimum Load Current

During standby the voltage loop regulates the output by adjusting the switching frequency. If the controller has a minimum switching frequency, this results in a minimum load requirement. The total loading on the outputs, including all the bias loading on the secondary and auxiliary outputs, must be high enough to absorb a minimum power output. If the energy is not absorbed, the output and auxiliary voltages lose regulation and rise. This generally is addressed by applying an additional pre-load on the output, at the expense of increased standby power.

iv. A Low Standby Power Calculation

Accounting for the effects of the switch-node capacitance, the total output power, including internal consumption, of the converter in standby is:

$$P_{OUT\text{(sb,total)}} = f_{SW\text{(sb)}} \times \frac{P_{OUT\text{(max)}}}{f_{SW\text{(@Pmax)}}} \frac{1}{K_{AM}} + \frac{\eta_T \times C_{SW} (2 \times VAC_{RMS}^2 - V_{FB}^2)}{2}$$

The input power during standby, assuming the leakage and start-up overhead is negligible, is:

$$P_{IN\text{(sb,total)}} = f_{SW\text{(sb)}} \times \frac{P_{OUT\text{(max)}}}{\eta_T \times f_{SW\text{(@Pmax)}}} \frac{1}{K_{AM}} + C_{SW} (2 \times VAC_{RMS}^2)$$

Here the term $V_{BULK}^2$ is substituted with the equivalent expression, $2 \times VAC_{RMS}^2$.

Transient performance is adjusted by increasing the size of the output capacitor for a given standby switching frequency. If size or cost is constraining the output capacitor, then alternatively, the standby switching frequency is increased. This comes at the expense of added standby power.

One needs to be careful when using this technique. While it works very well for a single load step, periodic load transients, whose period is close in time relative to the voltage loop’s settling time, still suffer poor transient performance since the loop likely is in a lower frequency state for some time following a fast reduction in the load.

A procedure to make the transient versus standby power trade-off starts with the determination of a minimum switching frequency to achieve the desired transient response using Equation 11. Then Equation 29 is used to pick the necessary total standby load to force the desired switching frequency. This is done at the highest line voltage since this is where the switching frequency is at its lowest. A pre-load is then determined from the difference of this calculated power minus the pre-existing load requirements, such as the primary controller, or other circuits on the primary or secondary. The resulting standby input power is then estimated using Equation 30. The following example illustrates this process for the 5 V, 10 W supply outlined in Table 4, where a target is set to meet a <10% output drop with a 0.5 A load step from standby using an output capacitor of 820 μF.

1) Using Equation 11, a minimum switching frequency of 1200 Hz is determined.

2) Solve Equation 29 at the highest line and the desired $f_{SW\text{(sb)}}$ to determine the total standby load that results in the needed minimum switching frequency. With $VAC_{RMS} = 260$ V,
switching at 1200 Hz results in delivered output power of 12 mW (see Figure 24).

3) Once a total standby load is determined, the actual input power and resulting switching frequency is estimated versus line voltage using Equation 29 and Equation 30. This is shown graphically in Figure 25. In the example, across a typical input voltage range, 85 V_{RMS} to 235 V_{RMS}, the standby switching frequency ranges from 1800 Hz to 1300 Hz and the input standby power changes from about 16.5 mW to just over 20 mW.

![Figure 24](image)

**Figure 24 – Making a trade-off between standby power and transient response starts with determining the standby load needed to drive the correct switching frequency.**

![Figure 25](image)

**Figure 25 – Standby power and switching frequency.**

This analysis is most applicable to cases where

the objective is to keep standby power below 100 mW for output ratings up to 30 W. The effective switch-node capacitance tends to go up at higher power levels following the size of the power switch and output rectifier. To achieve low standby power in these cases the operating frequency needs to be further reduced. This drives the need for some type of direct load feedback path, such as the optocoupler.

### III. RESULTS AND COMPARISON

To see how the choice of control method impacts different aspects in the performance of a flyback power supply, consider the example of a USB charger for tablets. The present-day power requirements for tablet chargers are fairly consistent across different manufacturers and models. Tablet devices typically charge from a USB port that provides 5 V at 10 W. The regulation requirements on the 5 V bus usually allow for a +/-5% variation. The load transient requirements tend to be fairly loose, as severe changes in load levels are not expected in battery charging applications. Minimizing the standby power consumption is important for marketing and adds value to the product. Over-current protection requirements tend to vary. Most tablet manufacturers put limits on the maximum current that can be sourced from the charger, while the current limit requirements from after-market charger manufacturers tend to be less stringent. Obviously, the product is very portable, and it is expected that customers will take the charger with them as they travel to various countries. As a result, the charger must accept a universal AC input range of 85 VAC to 265 VAC at 50 Hz or 60 Hz.

### A. Converter Design

To compare control methods, three tablet charger designs were developed using different controllers. DCM is the operating mode of choice for this power level, as it eliminates turn-on switching losses and diode reverse recovery losses and it simplifies the control loop. Keeping the comparison fair, all designs use the same transformer design, power MOSFET and output diode. Additionally, all controllers operate at approximately 100 kHz in the full load condition.
i. Fixed-Frequency with Optocoupler Feedback

The first controller in the comparison is a fixed frequency PWM controller with optocoupler feedback. For conciseness, this design example is referred to as DCM/FF/Opto. The control law used is like that shown in Figure 8. This control method is considered as “legacy” and it is common to flyback controllers developed over the past several decades. The schematic for the DCM/FF/Opto design example is shown in Figure 26. The internal clock is programmed to 100 kHz through the external components of R7, R8, and C14. The values of R7 and R8 also set the maximum duty cycle of the controller.

The output capacitors, C4 and C5, are sized to hold up the output voltage during transient load events. Multiplying the magnitude of the expected load step by the closed-loop output impedance of the power supply (at the unity gain crossover frequency, \( F_{BW} \)) gives a good approximation for the resulting change in output voltage \([6]\). This is shown numerically in Equation 31. Assuming a 2 kHz bandwidth, at least 320 \( \mu F \) are required to keep the output voltage from dropping more than 250 mV due to a 2 A load step. A total of 440 \( \mu F \) was used in this design. Of course, these capacitors see fairly high ripple current and must be sized appropriately. The capacitance and ESR of the output capacitors also determine the output ripple voltage. Aluminum polymer capacitors are used here because they provide a large amount of capacitance in a small case size, have very low ESR and can handle a large amount of ripple current. Placing a small ferrite bead between the two output capacitors forms a pi output filter and further reduces the output ripple and noise as shown in Figure 26.

\[
\Delta V_{\text{TRANSIENT}} = \frac{1}{2} \times \frac{1}{2\pi C_{\text{OUT}} F_{BW}} \times \Delta I_{\text{TRANSIENT}}
\]  

(31)

Figure 26 – Traditional flyback controllers implement a fixed-frequency PWM control method. Key components and sub-circuits affected by the choice of controller include: 1. Startup resistors, 2. Bias hold-up capacitor, 3. Optocoupler and error amplifier circuit, 4. Output capacitors, and 5. Gate drive conditioning circuitry.
The controller used in this design contains a soft-start circuit, which dictates the charging time of the output capacitors during startup. As discussed earlier, this charging time restricts the minimum amount of capacitance that is used on the bias rail, capacitor C3 in the schematic. Equation 18 is used to size the bias capacitor. For this design, $I_{\text{RUN}}$ is composed of the operating current of the controller, the gate drive current and the optocoupler current. With 6 V of hysteresis provided by the controller, at least 8 $\mu$F is required to hold up under a total load of 5 mA for at least 10 ms. A 22 $\mu$F bias capacitor is selected to provide enough overhead to ensure a proper startup.

The series combination of resistors R1 and R2 provides the startup current for the controller in the DCM/FF/Oppto design example. This resistance is low enough to ensure that the controller is guaranteed to start with a minimum input condition. The controller requires at least 110 $\mu$A of current at startup and has a start threshold of 15.6 V. Applying Equation 19, using 300 kΩ of startup resistance ensures that the converter starts within 1.2 seconds at the worst case minimum input condition of 85 VAC. The selection of these components is crucial in modern adapter designs, as using a resistance that is unnecessarily low will negatively impact the no-load power loss.

The TL431 shunt regulator, U2, provides regulation in the DCM/FF/Oppto design. This circuit is commonplace in isolated power supplies. Inside the TL431 is a 2.5 V reference and an error amplifier. The error signal feeds across the isolation boundary by the optocoupler, U3. Because the error amplifier directly senses the output voltage, it is able to provide excellent load regulation. However, this good regulation comes at the cost of at least seven components.

Peak current mode controllers, like the one used here, usually have a minimum on-time. This minimum on-time often is a result of leading-edge blanking, which prevents the PWM comparator from falsely triggering on spikes in the current sense signal that occur immediately after the FET turns on. With the controller in this example, the minimum on-time is due to the propagation delay of the comparator and is specified as 100 ns maximum. The minimum on-time causes the output voltage to float higher as the load tends toward zero. The traditional way of combating this problem is to simply add a resistor across the output to set a minimum load. This is often referred to as “pre-loading” the output. However, adding a pre-load greatly increases the standby power consumption. An alternative solution to this problem is to add a resistor and diode in the gate drive path (R100 and D100 in Figure 26). This puts delay in the turn-on path (through the resistor) yet does not affect the turn-off path (through the diode). By adjusting the resistor value, the minimum on-time is essentially cancelled out. Because this converter operates in DCM, the starting current when the FET turns on is 0 A, so switching losses and ringing due to the turn-on event are minimally affected by adding these components.

**ii. Valley Switching with Primary Side Regulation**

The second control method in this comparison uses a modern controller that implements valley switching and PSR, with a control law similar to that shown in Figure 10. The schematic for this design example is shown in Figure 27 and is referred to as DCM/VS/PSR. The PSR feature eliminates the TL431, optocoupler and associated discrete components. Instead, the auxiliary winding voltage is monitored by the VS pin of the controller through R15 and R16. As discussed earlier, the winding voltage is sampled at the end of the output diode conduction time to achieve the most accurate reading of the output voltage. The relationship between R15, R16 and the output voltage is given by:

$$V_{\text{VS}} = V_{\text{OUT}} + V_D \times N_{AS} \times \frac{R_{16}}{R_{15} + R_{16}}$$ (32)

Where: $V_{\text{VS}}$ is the regulating voltage level of the sampled auxiliary winding voltage, equal to 4.05 V for this controller. $V_D$ is the output diode drop at the end of the demagnetization period.

With a 4:1 ratio of the auxiliary winding to the secondary winding and assuming a 0.3 V drop for the output diode, using 133 kΩ and 31.6 kΩ for the resistor divider nominally sets the output voltage at 4.97 V.
Similar to the previous design, the desired load transient response determines the amount of output capacitance required for the PSR design. However, it is now the sampling rate of the controller that determines how long the output capacitors must hold up the output voltage. According to Equation 11, if this controller is allowed to run at its absolute minimum frequency of 600 Hz prior to a 2 A load step, 3300 μF is required to guarantee that the output never drops more than 1 V. In order to keep the output capacitance to a lower amount, a small preload resistor (R18) is added to increase the no load switching frequency to around 1 kHz.

An important difference between this design and the previous example is the lack of startup resistors. Instead, an active startup is provided through the HV pin of the IC and gates the startup current. By eliminating the power loss associated with the startup resistors, the light load efficiency is greatly increased. Active startup functions like this are becoming commonplace in contemporary power supply controllers. Some devices implement this function through a signal that turns an external JFET on and off, rather than incorporating a high voltage device into the same package as the controller.

Another simple improvement offered by this controller over the legacy controller is the widened startup hysteresis. Additionally, with PSR, the burden of supplying the optocoupler current during startup is removed. Rather than relying on a soft-start circuit to control the ramp up of the output voltage, this controller starts in current regulation while the output capacitors are charged, which greatly shortens the startup time. All of these factors help to reduce the size of the bias capacitor.

Since our adapter expects to start in very light load conditions, the entire 2 A capability is available to charge the output capacitors at startup. Using Equation 17, with 1640 μF, an 8.5 V turn-off level and a 4:1 ratio between the auxiliary winding and output winding, the charging time is 2 ms. Using Equation 18, at least 0.6 μF is required to provide 4 mA for 2 ms with 13 V hysteresis. A 1 μF ceramic capacitor is selected for C3.
iii. Valley Switching with Optocoupler Feedback

The third example in the comparison is a compromise between the first two designs and is shown in Figure 28. This final design uses a modern controller that implements valley switching and variable frequency operation, with the same control law as used by the controller in our DCM/VS/PSR example, but uses a TL431 and optocoupler for the output regulation. This example is referred to as DCM/VS/Opto.

Like the DCM/FF/Opto example, a smaller bank of output capacitors is used because the output voltage is continually monitored by the TL431. This controller is able to reduce the switching frequency to minimize no-load losses and the TL431 can immediately alert the controller to changes in output voltage, even between switching events. The tradeoff for providing this function is not only the obvious cost of the extra components, but also some residual power consumption at no-load that arises from providing bias the optocoupler and TL431.

Like the DCM/VS/PSR example, this design provides an active startup circuit and has a wide startup hysteresis. With only 440 μF on the output, from Equation 17 the output charging time is only 0.5 ms for this design. Unlike the DCM/VS/PSR example, the bias capacitor must also supply the optocoupler current at startup. Using Equation 18, to hold up to 5 mA for 0.5 ms with 13 V hysteresis, only 0.2 μF is required during startup. However, the combination of this control law and the optocoupler feedback places an additional restriction on the size of the bias capacitor. During load transients that slew from a heavy load to no-load, the output voltage temporarily overshoots as the TL431 is not able to respond instantaneously. This is shown in Figure 29. Once the TL431 is able to respond, it saturates and forces maximum current through the optocoupler. The controller then enters a state where it is switching at its absolute minimum frequency (170 Hz with this controller). This state endures until the output

---

Figure 28 – This modern controller implements valley switching with optocoupler feedback, and provides a compromise between traditional fixed frequency PWM controllers and modern controllers with PSR. Advantages include: 1. No startup resistors, 2. Reduced bias capacitance, and 4. Minimal output capacitance. One trade-off is: 3. Circuitry needed to provide output regulation and feedback.
voltage falls back to its steady state value and normal no-load operation is restored. During this time, the optocoupler current and the controller operating current drain the maximum bias capacitor voltage. To make matters worse, little energy is replenished into the bias capacitor due to the very low operating frequency. The bias capacitance must be large enough to prevent the bias voltage from falling below the turn-off threshold of the controller during this event [7]. The amount of capacitance required is given by:

\[
C_{BIAS} > \frac{I_{CC} + I_{OPTP} \times \Delta T_{OV}}{VDD(operating) - VDD(off)} \tag{33}
\]

To hold up 2 mA for 25 ms, with less than a 10 V drop, at least 4.2 μF is required. A 10 μF ceramic capacitor is used in this design.

**B. Layout and Assembly**

Photographs of the assembled circuits are shown in Figure 30, and give a sense of scale for the designs and the individual components. The assemblies for all three designs have the same l x w x h dimension of 2” x 1” x 0.8” (50 mm x 25 mm x 20 mm). The only major physical differences of the designs are:

1) The DCM/FF/Opto design requires startup resistors, while the other two designs do not.
2) The size of the bias capacitor is different on all three designs.
3) The TL431/optocoupler circuit is eliminated on the design with PSR.
4) PSR forces larger output capacitors for hold up during load transients.

**C. Performance**

Now that this paper has investigated how the choice of control method affects the component selection, an examination of how each design performs in different key aspects is performed.

**i. Output Voltage Accuracy**

Output voltage accuracy is a measure of how much statistical variation in output voltage set-point is expected from unit to unit in a production environment and is determined by the tolerances of components within the power supply. For the two designs with optocoupler feedback, the circuit...
designer chooses the accuracy of the output voltage by choosing the tolerance of the reference and feedback resistors. Components with tolerances better than 1% tend to be more expensive and are usually avoided in consumer products. The accuracy of the feedback divider has a strong dependency on the ratio of the output voltage to the reference voltage, and is determined by [8]:

$$\text{Error} = 2 \times \text{Tol} \times \frac{V_{\text{OUT}}}{V_{\text{REF}}}$$ (34)

Where Error is the accuracy of the divider, and Tol is the tolerance of the resistors.

With a 2:1 divider ratio, 1% resistors and a 1% reference, this results in an overall accuracy of 2%.\(^5\) By comparison, the design with PSR is limited to +/-5% accuracy. As described earlier, the reference and resistor tolerances are still factors, but additional error sources include the output rectifier drop, variations in transformer construction and sampling errors.

**ii. Load Regulation**

Load regulation, not to be confused with output voltage accuracy, is a measure of how much the output voltage of a single unit varies over the full load range. The output voltage versus load for all three of the designs is plotted in Figure 31. With the error amplifier and reference located on the secondary side, the designs that contain an optocoupler and TL431 are able to provide excellent load regulation, within +/-0.1%. The design with PSR implements feed-forward (cable compensation) which offsets resistive drops in the power path that would otherwise cause the output voltage to vary more substantially. The amount of cable compensation is set by the value of R17 in the schematic of Figure 27. The amount of cable compensation is usually estimated during the design phase and adjusted once prototypes are built, as the parasitic resistances are cumbersome to calculate ahead of time. With cable compensation, the DCM/VS/PSR design is able to keep the load regulation within +/-0.6%.

\(^5\) There are numerous statistical methods for calculating accuracy. Here the simple method of assuming the worst case values (within the specified tolerances) for the resistors and reference is used.

![Figure 31](image1.png) **Figure 31** – The designs that use an optocoupler and TL431 provide excellent load regulation. PSR provides load regulation that has more deviation, but can still be better than +/-1%.

**iii. Overload Protection**

The DCM/VS/PSR design and the DCM/VS/Opto designs use controllers that provide a constant current regulation mode. As discussed earlier, once the peak primary current reaches its maximum value, these controllers hold constant the duty cycle of the transformer demagnetization time. Both of these designs enter current regulation mode when the load is increased to 2.3 A. The output voltage then drops as the load resistance is decreased. The V-I characteristics of all three designs are shown in Figure 32.

![Figure 32](image2.png) **Figure 32** – The designs with modern controllers provide constant current regulation, whereas the legacy fixed frequency controller uses peak current limit as protection from overload conditions.
The fixed-frequency design, by contrast, simply limits the peak primary current during overload events. The controller continues to operate at 100 kHz as the load resistance drops further. Eventually, the power supply enters CCM as not all of the energy stored in the core is removed before the start of the next switching cycle. Although the power delivered to the load decreases, the current continues to rise as the output voltage drops. This may be undesirable or even unacceptable for some adapter manufacturers.

iv. Efficiency

The efficiency and power loss for the design examples, measured at 230 V AC input, are shown in Figure 33. Differences in efficiency are most significant at light loads. The DCM/FF/Opto design is burdened by the static losses of the startup resistors, while the reduced switching frequency and valley switching minimize losses in the other two designs. The control law of the DCM/VS/PSR and DCM/VS/Opto designs allows for variable frequency operation and keeps the efficiency plot flat as the load is increased past the 500 mA level.

The efficiency of all three converters starts to converge at the maximum load level. This is not surprising, considering that all three designs use the same power stage and operate at approximately the same switching frequency at maximum load. However, at the 2 A level, the DCM/FF/Opto design still has about 300 mW more loss than the other two designs because of losses in the startup resistors and the absence of valley switching.

v. Standby Power Consumption

A clear difference in the no-load power loss for these design examples is seen in Figure 34. The higher switching frequency of the DCM/FF/Opto design and startup resistors cause the power loss to range from around 150 mW at minimum input voltage to around 750 mW at maximum input voltage. The startup resistors are the largest contributor. In this case, 100 mW is lost in these resistors with 120 V AC input and 350 mW is lost with 230 V AC input.
The DCM/VS/Opto design keeps the standby power loss below 70 mW due to the low switching frequency at no-load and the active startup circuit. A majority of the losses in this design are due to biasing the optocoupler and TL431 circuit. By eliminating these losses, the DCM/VS/PSR design is able to further reduce the no-load losses to below 20 mW.

vi. Load Transients

For the two designs with optocouplers, the response to a 0 A to 2 A step is very similar. The response of the DCM/FF/Opto design is shown in Figure 35 (B). The output voltage only drops around 200 mV while the feedback loop takes time to respond. This response is predictable, and does not vary much with line and initial load conditions.

![Figure 35](image)

**Figure 35** – These plots show the output voltage response to a 2 A load step.

The response of the design with PSR is very different. It is dependent on the sampling rate of the controller and when in the switching cycle the transient occurs. If the transient occurs just prior to a switching event, and hence sampling of the output, the output voltage deviation is minimal. If it occurs just after a switching event, more time elapses before a sampling occurs and the output voltage drop is more severe. As shown in Figure 35 (A), a no-load to 2 A step could possibly result in a voltage drop of around 1 V. However, with a small starting load, the switching frequency (and sampling rate) is higher which greatly improves the transient response. Starting with only 10 mA keeps the voltage drop to around 300 mV. Clearly a trade-off is made between standby power consumption and load transient response in the PSR design.

D. Summary of Design Examples

A summary of the test results for all three designs is provided in Table 6. When the only concern is cost, as is sometimes the case in consumer products, PSR is the obvious choice. The TL431 and optocoupler account for the increased cost of the other two designs. This cost is slightly offset by the cost of the larger output capacitors in the PSR design.

Using a controller with variable frequency and PSR also offers the best solution with regards to standby power consumption. However, the low cost and low standby power come with a trade-off regarding output voltage accuracy, regulation and transient response. A controller with a variable frequency control law and optocoupler feedback offers a good compromise. With this approach, excellent regulation and transient response is provided and the standby power is kept below 75 mW. This is low enough to qualify for Tier 2 status according to the COC, referring back to Table 1.

The DCM/FF/Opto design performs similarly to the DCM/VS/Opto in all categories except standby power and current regulation. However, it did not outperform the other two designs in any of the categories evaluated. For consumer products, like the tablet charger example, it makes more sense to use a modern controller with a variable frequency control law. Fixed-frequency controllers are used in noise-sensitive applications where it is advantageous to have a determined switching frequency.
Iv. conclusions

In summary, global energy standards are driving the need for reduced standby loss and higher efficiency. At the same time, manufacturers of consumer products are looking for new ways to reduce the cost of the power supply.

Power supplies for consumer products tend to implement low power flybacks operating with a discontinuous versus continuous current because they benefit from reduced switching losses and EMI. There are several control methodologies (DCM, TM, QR and valley switching) that have the potential benefit of further reducing losses, improving EMI and reducing transformer size.

Primary-side regulation offers a way for manufacturers to reduce cost and improve reliability and still provide good output voltage and current regulation. However, transient response may suffer relative to conventional feedback methods.

Standby power is impacted by static leakages, start-up (or other) overhead and by ability of the controller to get to low cycle energies. The transient performance trade-off and the impact of switch-node capacitance can become dominant when very low standby power operation is targeted.

Traditional flyback controllers implement a fixed-frequency DCM control law. Modern controllers that implement energy saving features of active startup circuits, valley switching and PSR make it possible to meet aggressive energy standards and reduce cost at the same time.

<table>
<thead>
<tr>
<th></th>
<th>DCM/FF/Opto</th>
<th>DCM/VS/PSR</th>
<th>DCM/VS/Opto</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Voltage Accuracy</td>
<td>+/-2%</td>
<td>+/-5%</td>
<td>+/-2%</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>+/-0.1%</td>
<td>+/-0.6%</td>
<td>+/-0.1%</td>
</tr>
<tr>
<td>Max. Load Efficiency (115 VAC/230 VAC)</td>
<td>82.0%/80.4%</td>
<td>82.2%/82.5%</td>
<td>81.3%/81.7%</td>
</tr>
<tr>
<td>Standby Power (115 VAC/230 VAC)</td>
<td>216 mW/584 mW</td>
<td>14 mW/16 mW</td>
<td>57 mW/64 mW</td>
</tr>
<tr>
<td>Load Transients (0 A to 2 A)</td>
<td>-200 mV</td>
<td>-1100 mV</td>
<td>-200 mV</td>
</tr>
<tr>
<td>Current Regulation</td>
<td>Not Provided</td>
<td>+/-5%</td>
<td>+/-5%</td>
</tr>
<tr>
<td># of Components</td>
<td>41</td>
<td>27</td>
<td>37</td>
</tr>
<tr>
<td>Relative Cost</td>
<td>Low</td>
<td>Lowest</td>
<td>Low</td>
</tr>
</tbody>
</table>

Table 6 – A summary of the design examples shows that significant performance improvements are obtained by using a modern controller with valley switching and other enhanced features.

**IV. CONCLUSIONS**

In summary, global energy standards are driving the need for reduced standby loss and higher efficiency. At the same time, manufacturers of consumer products are looking for new ways to reduce the cost of the power supply.

Power supplies for consumer products tend to implement low power flybacks operating with a discontinuous versus continuous current because they benefit from reduced switching losses and EMI. There are several control methodologies (DCM, TM, QR and valley switching) that have the potential benefit of further reducing losses, improving EMI and reducing transformer size.

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Standby power is impacted by static leakages, start-up (or other) overhead and by ability of the controller to get to low cycle energies. The transient performance trade-off and the impact of switch-node capacitance can become dominant when very low standby power operation is targeted.

Traditional flyback controllers implement a fixed-frequency DCM control law. Modern controllers that implement energy saving features of active startup circuits, valley switching and PSR make it possible to meet aggressive energy standards and reduce cost at the same time.
V. REFERENCES


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<th>Brazil</th>
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<th>Asia</th>
</tr>
</thead>
<tbody>
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