

2N7002L-Q1 6V N-channel MOSFET

1 Features

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Operating Junction and Storage Temperature:
 - –65°C to +150°C
- 2kV Gate-Source ESD Rating

2 Applications

- [Personal Electronics](#)
- [Building Automation](#)
- [Industrial Automation](#)

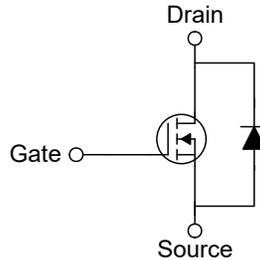
3 Description

This device is a N-channel Field-Effect Transistor in a plastic package. It has been designed to minimize the on-state resistance while maintaining fast switching performance.

Package Information

| PART NUMBER | PACKAGE ⁽¹⁾ | BODY SIZE (NOM) |
|-------------|------------------------|--------------------|
| 2N7002L-Q1 | DBZ (SOT-23) | 2.92mm × 2.37mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Block Diagram



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4 Pin Configuration and Functions

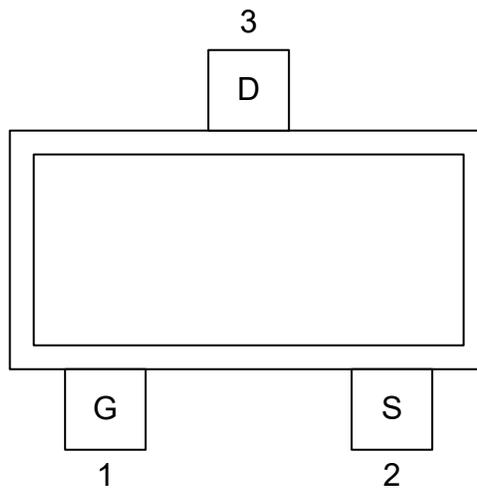


Figure 4-1. DBZ Package 3-Pin SOT-23 Top View

Table 4-1. Pin Functions

| PIN | | DESCRIPTION |
|------|-----|-------------|
| NAME | DBZ | |
| G | 1 | Gate |
| S | 2 | Source |
| D | 3 | Drain |

ADVANCE INFORMATION

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) ⁽¹⁾

| | | MIN | MAX | UNIT |
|-----------------------------------|--|-----|------|------|
| V _{DS} | Drain-to-Source Voltage | | 6 | V |
| V _{GS} | Gate-to-Source Voltage | | 7 | V |
| I _D | Drain Current T _A = 25°C | | 1.4 | A |
| I _D | Drain Current T _A = 85°C | | 437 | mA |
| I _{DM} | Pulsed Drain Current (t _p = 1s) | | 1.43 | A |
| T _J , T _{STG} | Operating Junction and Storage Temperature Range | -65 | 150 | °C |
| I _S | Source Current | | 1.4 | A |
| T _L | Lead Temp for Soldering Purpose | | 260 | °C |
| ESD | Gate-Source / Gate-Drain ESD Rating | | 2000 | V |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 Electrical Characteristics

over operating free-air temperature (unless otherwise noted) ⁽¹⁾

| | PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|---------------------------------------|---|--|-----|------|------|-------|
| OFF CHARACTERISTICS | V _{(BR)DSS} | Drain-to-Source Breakdown Voltage | V _{GS} = 0V, I _D = 1μA | 9.7 | 11.7 | 13.7 | V |
| | V _{(BR)DSS} / T _J | Drain-to-Source Breakdown Voltage Temperature Coefficient | | | 4 | | mV/°C |
| | I _{DSS} | Zero Gate Voltage Drain Current | V _{GS} = 0V, V _{DS} = 6V, T _J = 25°C | | | 2.5 | nA |
| | I _{DSS} | Zero Gate Voltage Drain Current | V _{GS} = 0V, V _{DS} = 6V, T _J = 125°C | | | 0.26 | μA |
| | I _{GSS} | Gate-to-Source Leakage Current | V _{DS} = 0V, V _{GS} = +7.0V | | | 384 | nA |
| ON CHARACTERISTICS | V _{GS} | Gate Threshold Voltage | V _{GS} = V _{DS} , I _D = 250μA | 0.4 | 0.7 | 0.95 | V |
| | V _{GS(TH)} | Negative Threshold Temperature Coefficient | | | -1.4 | | mV/°C |
| | R _{DSON} | Drain-to-Source On Resistance | V _{GS} = 5V, I _D = 64mA | 1.2 | | 3 | Ω |
| | R _{DSON} | Drain-to-Source On Resistance | V _{GS} = 3.3V, I _D = 64mA | 1.6 | | 4.5 | Ω |
| | G _{FS} | Forward Transconductance | V _{DS} = 5V, I _D = 64mA | 57 | | 181 | mS |

over operating free-air temperature (unless otherwise noted) ⁽¹⁾

| | PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------------|---------------------|------------------------------|---|-----|-------|------|------|
| CHARGES AND CAPACITANCE | C _{ISS} | Input Capacitance | V _{GS} = 0V, f = 1MHz, V _{DS} = 6V | | 4.8 | 5 | pF |
| | C _{OSS} | Output Capacitance | | | 7.4 | 8.5 | |
| | C _{RSS} | Reverse Transfer Capacitance | | | 5 | 5.5 | |
| | Q _{G(TOT)} | Total Gate Charge | V _{GS} = 0 to 5V, V _{DS} = 6V (see figure) | | 0.034 | | nC |
| | Q _{G(TH)} | Threshold Gate Charge | V _{GS} = 0 to 5V, V _{DS} = 6V (see figure) | | 0.007 | | |
| | Q _{GS} | Gate-to-Source Charge | V _{GS} = 0 to 5V, V _{DS} = 6V (see figure) | | 0.019 | | |
| | Q _{GD} | Gate-to-Drain Charge | V _{GS} = 0 to 5V, V _{DS} = 6V (see figure) | | 0.17 | | |
| SWITCHING CHARACTERISTIC | t _{d(ON)} | Turn-On Delay Time | V _{GS} = 5V, V _{DD} = 6V, R _G = 25Ω, R _D = 2.49kΩ | | | 1.4 | nS |
| | t _r | Rise Time | | | | 1.1 | |
| | t _{d(OFF)} | Turn-Off Delay Time | | | | 7.0 | |
| | t _f | Fall Time | | | | 55 | |
| DRAIN-SOURCE DIODE CHARACTERISTICS | V _{SD} | Forward Diode Voltage | V _{GS} = 0V, I _S = 20mA, T _J = 25°C | | | 0.97 | V |
| | | | V _{GS} = 0V, I _S = 20mA, T _J = 85°C | | | 0.93 | |

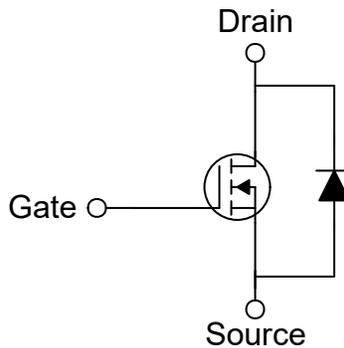
(1) All typical values are at T_A = 25°C.

6 Detailed Description

6.1 Overview

The 2N7002L-Q1 is an N-channel enhancement-mode MOSFET designed for general purpose switching in low-voltage , low-current applications. In a typical low-side configuration, the source is tied to ground and the gate is driven by a logic-level signal. When the gate voltage exceeds the threshold voltage, the MOSFET turns on and provides a low on-resistance path between drain and source.

6.2 Functional Block Diagram



6.3 Feature Description

6.4 Device Functional Modes

Table 6-1 lists the functional modes of the device.

Table 6-1. Function Table

| MODE | DESCRIPTION |
|------|---|
| OFF | $V_{GS} < \text{threshold}$; device does not conduct |
| ON | $V_{GS} > \text{threshold}$; device conducts |

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The 2N7002L-Q1 device can be used in level-translation applications for interfacing between devices or systems that are operating at different interface voltages. In the below example, the System Controller drives the gate of the 2N7002L. When the controller outputs a high logic level, the MOSFET turns on and pulls the EN pin of the system device low. When the controller output is low, the MOSFET turns off and the pull-up resistor brings the EN pin high to 5V. This creates an open-drain style interface for level shifting or for driving enable signals at a higher voltage than the controller's logic domain.

7.2 Typical Applications

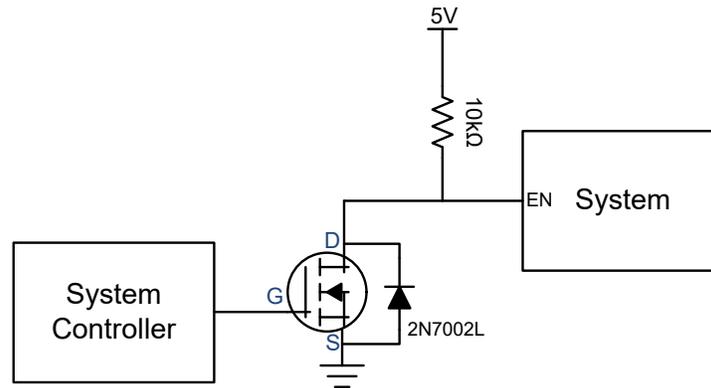


Figure 7-1. Typical Application using 2N7002L-Q1

7.2.1 Design Requirements

For proper operation of the 2N7002L, the design must remain within the limits defined in the *Absolute Maximum Ratings* and *Electrical Characteristics* tables.

7.2.2 Detailed Design Procedure

Designing with the 2N7002L requires selecting appropriate operating conditions for gate drive, load current, and switching behavior while ensuring all parameters remain within the limits defined in the *Absolute Maximum Ratings* and *Electrical Characteristics* tables.

1. Select the operating V_{DS} : ensure the supply voltage applied to the drain does not exceed the abs max ratings.
2. Choose a valid V_{GS} : use a logic-level gate voltage that falls within the recommended V_{GS} limits.
3. Confirm load current capability: make sure the drain current is within the device's continuous current and thermal capabilities.
4. Check switching capabilities: verify that the gate-drive strength and switching frequency are compatible with the device's gate charge and capacitances.

8 Power Supply Recommendations

Operate the 2N7002L-Q1 within the limits defined in the *Absolute Maximum Ratings* and *Electrical Characteristics* tables. Use a 5V drain supply, and ensure that V_{DS} never exceeds 6V, including during transient events. Drive the gate from logic rails (1.8V, 3.3V, or 5V) and ensure the V_{GS} never exceeds 7V under any condition. Place decoupling capacitors near the device or load to reduce switching-related voltage spikes.

9 Layout

9.1 Layout Guidelines

Minimize trace lengths on the drain, source, and gate connections to reduce parasitic inductance and switching noise.

- Route the gate-drive signal away from noisy switching nodes to prevent coupling.
- Provide adequate copper area on the source or drain pads for thermal dissipation.
- If switching small inductive loads, place any flyback or clamp components close to the device to minimize transient stress.

9.2 Layout Example

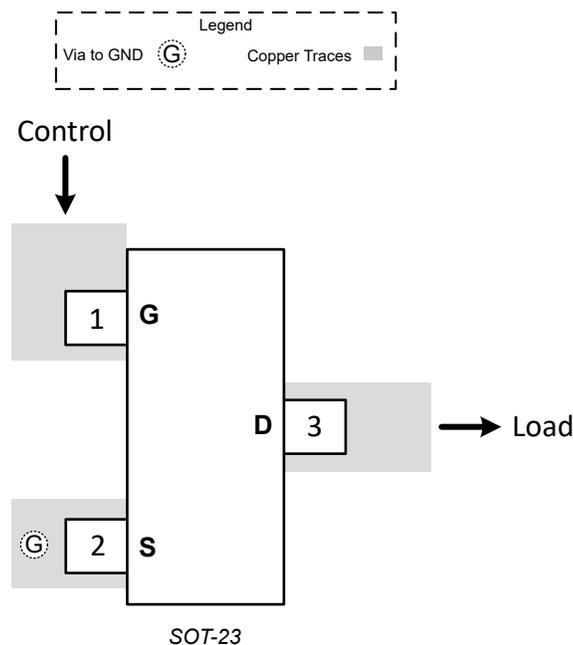


Figure 9-1. Example Layout for the SOT-23 Package

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs](#)
- Texas Instruments, [Designing and Manufacturing with TI's X2SON Packages](#)

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---------------|----------|-----------------|
| December 2025 | * | Initial Release |

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|--------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| P2N7002LDBZRQ1 | Active | Preproduction | SOT-23 (DBZ) 3 | 3000 LARGE T&R | - | Call TI | Call TI | -40 to 125 | |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF 2N7002L-Q1 :

- Catalog : [2N7002L](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

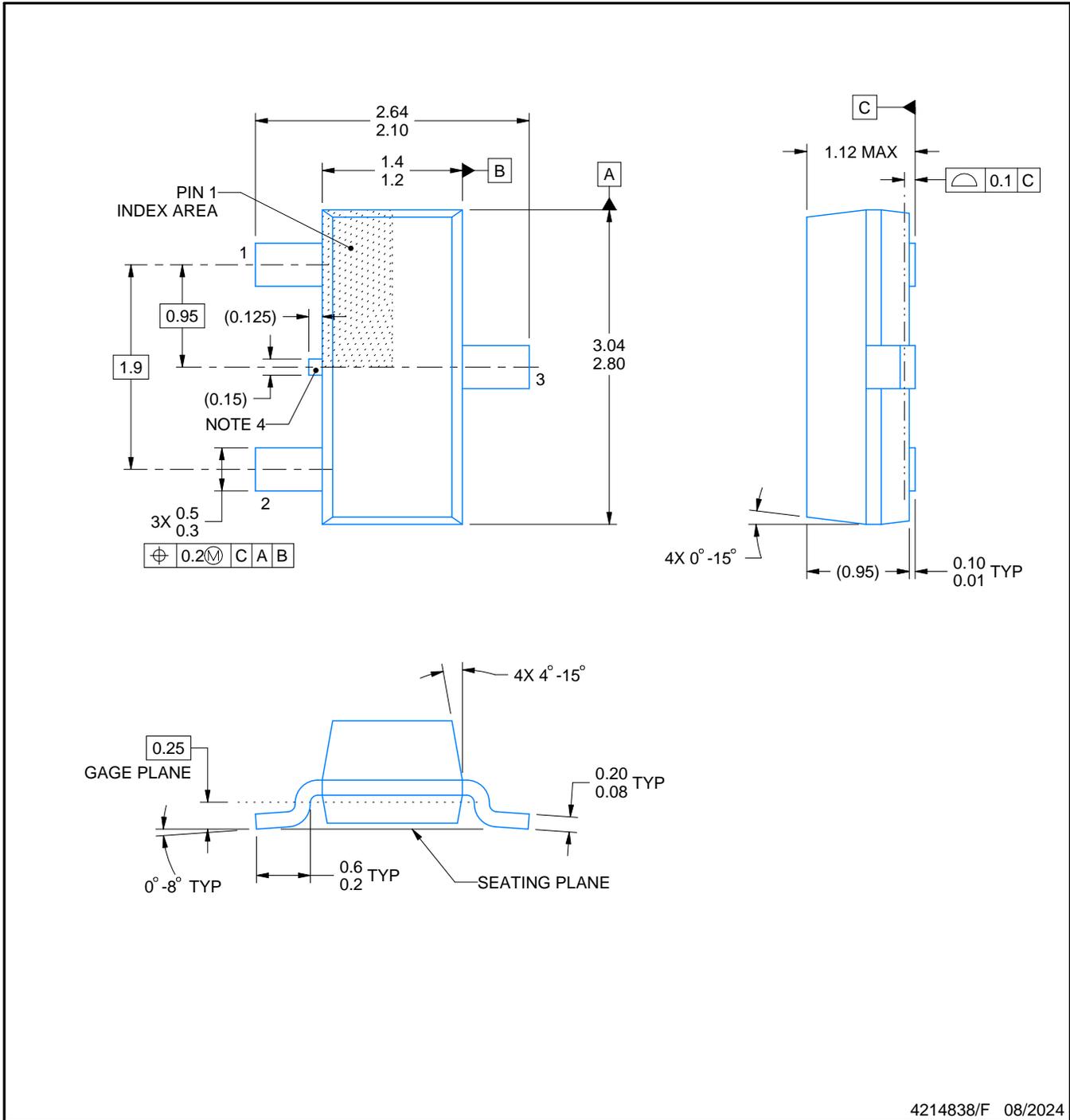
DBZ0003A



PACKAGE OUTLINE

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



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NOTES:

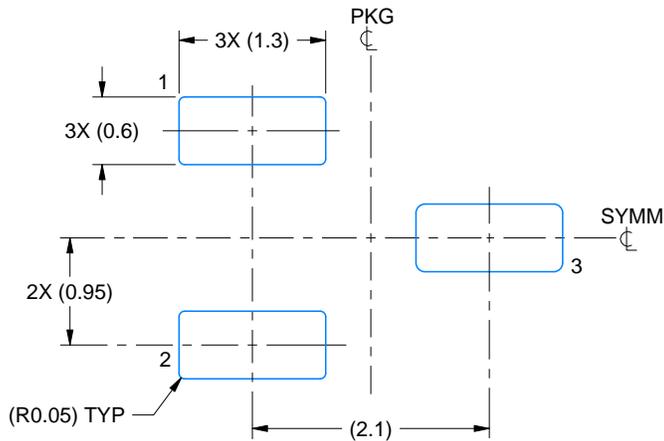
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

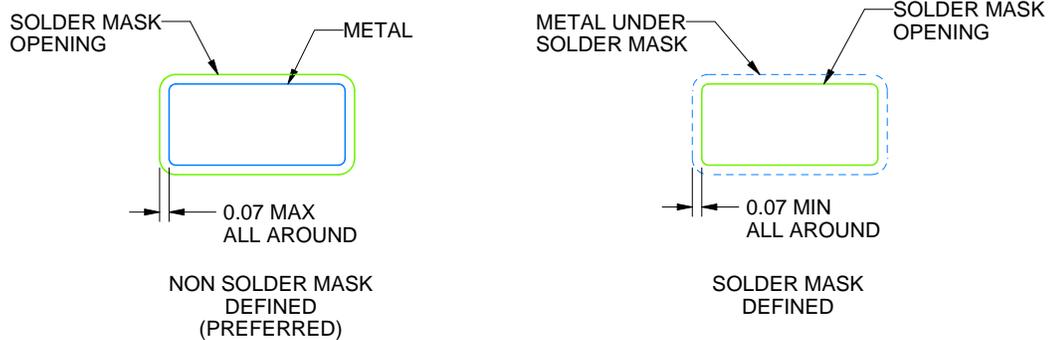
DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

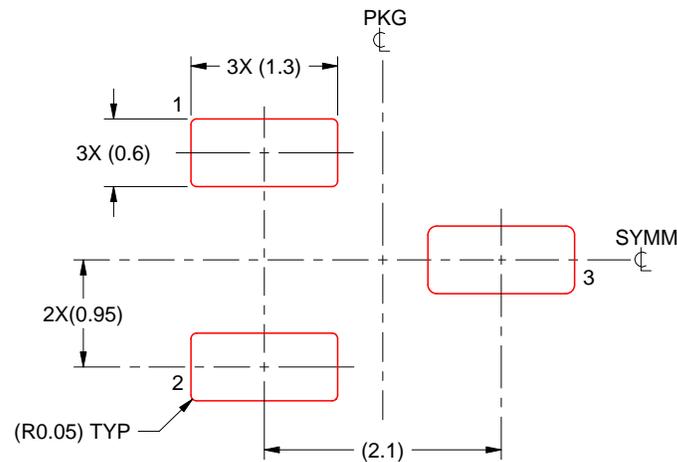
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025