ADS9324C 16-Bit, 1MSPS, 16-Channel, Precision ADC With 80Vpp Common-Mode Difference Amplifier

ADVANCE INFORMATION

1 Features

- 16-channel, 16-bit Simultaneous Sampling ADC
  - 1MSPS throughput on each channel
- Integrated programmable gain amplifier
  - 1MΩ analog input impedance
  - Supports single-ended and differential inputs
  - Input ranges:
    - Differential input voltage: ±50V, ±25V, ±12.5V, ±10V, ±6.25V, ±5V, ±2.5V
    - Common mode voltage: ±40V
- Analog bandwidth options: 25kHz and 400kHz
- Open-wire safe inputs
  - Near zero ADC output code for floating inputs
- Typical performance:
  - INL: ±0.5LSB; DNL: ±0.5LSB
  - SNR: 88dB; THD: –103dB; DC CMRR: 100dB
- Low-drift, on-chip reference (4.096V) and buffer
  - 15ppm/°C typical temperature drift
- Digital features
  - On-chip digital filters for oversampling
  - System offset, gain and phase calibration
  - Digital window comparators
  - ADC output data randomizer
- Power Supply
  - Analog supplies: 5V and 1.8V
  - Digital I/O supply: 1.8V to 3.3V
- Temperature range: –40°C to +125°C

2 Applications

- Test and measurement
  - Battery cell formation and test
- Industrial automation
  - Analog input module
  - Mixed module (AI, AO, DI, DO)
- Series stacked cell voltage monitoring
- Multi-axis motor control

3 Description

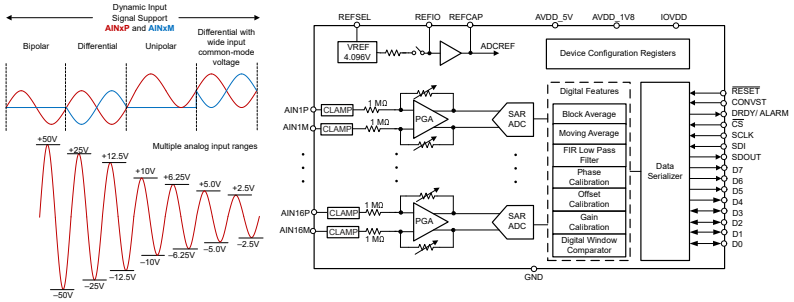
The ADS9324C is a 16-channel, integrated data acquisition (DAQ) system based on a simultaneous-sampling, 16-bit successive approximation (SAR) analog-to-digital converter (ADC) operating at a maximum of 1MSPS per channel. The device features a complete analog front-end for each channel, including a programmable gain amplifier (PGA) with input impedance of 1MΩ, input clamp, low-pass filter, and an ADC input driver. The device also features a low-drift, precision reference with a buffer to drive the ADC. The high input impedance allows direct connection with sensors and transformers, thus eliminating the need for external driver circuits. The device supports both differential and single-ended inputs, allowing the device to be used with various sensor outputs.

The ADS9324C includes a flexible digital interface allowing the device to be used with a variety of host controllers. Users can configure the serial interface to read the ADC output on 1-lane, 2-lane, 4-lane, and 8-lane. The device also has flexibility to operate the ADC as 2-CH, 4-CH, 8-CH and 16-CH simultaneous sampling ADC.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
ADS9324C	RSK (VQFN, 64)	8.00mm × 8.00mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Device Block Diagram

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4 Device Comparison Table

PRODUCT	RESOLUTION (Bits)	CHANNELS	COMMON MODE VOLTAGE	SAMPLE RATE (kSPS)
ADS9324	16	16, single-ended, differential	±12.5V	1000
ADS9324C	16	16, single-ended, differential	±40V	1000
ADS9344	12	16, single-ended, differential	±12.5V	1000

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5 Pin Configuration and Functions

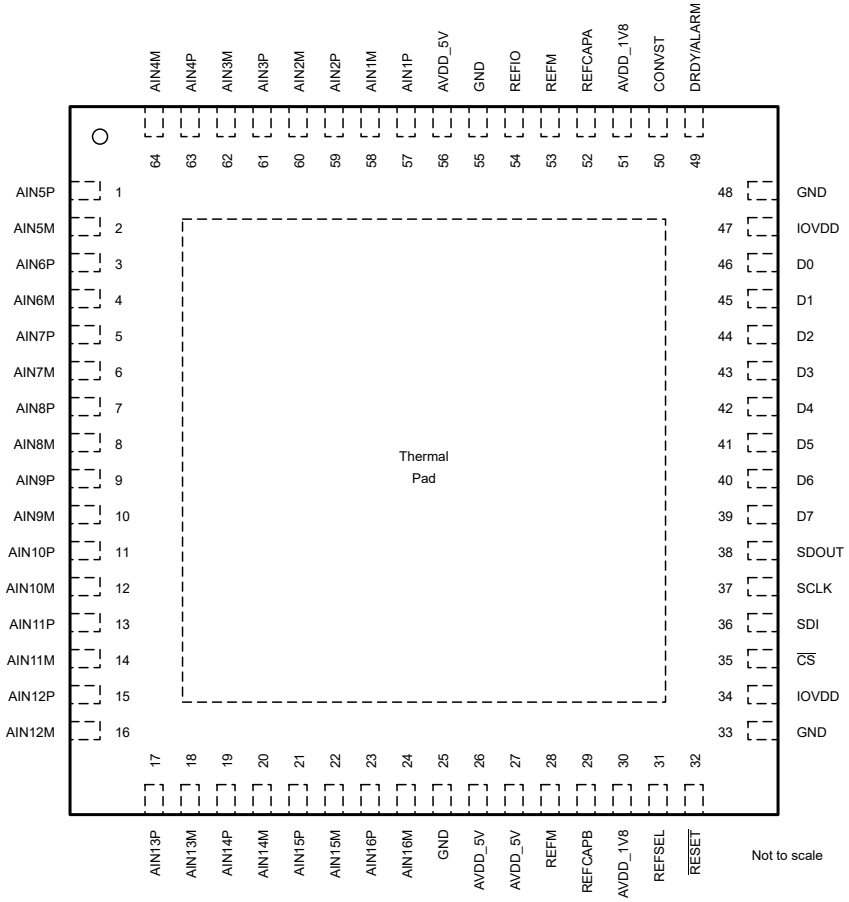

Figure 5-1. RSK Package, 64-Pin VQFN (Top View)

Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
AIN1P	57	AI	Analog input channel 1, positive input.
AIN1M	58	AI	Analog input channel 1, negative input.
AIN2P	59	AI	Analog input channel 2, positive input.
AIN2M	60	AI	Analog input channel 2, negative input.
AIN3P	61	AI	Analog input channel 3, positive input.
AIN3M	62	AI	Analog input channel 3, negative input.
AIN4P	63	AI	Analog input channel 4, positive input.
AIN4M	64	AI	Analog input channel 4, negative input.
AIN5P	1	AI	Analog input channel 5, positive input.
AIN5M	2	AI	Analog input channel 5, negative input.
AIN6P	3	AI	Analog input channel 6, positive input.
AIN6M	4	AI	Analog input channel 6, negative input.
AIN7P	5	AI	Analog input channel 7, positive input.
AIN7M	6	AI	Analog input channel 7, negative input.
AIN8P	7	AI	Analog input channel 8, positive input.
AIN8M	8	AI	Analog input channel 8, negative input.
AIN9P	9	AI	Analog input channel 9, positive input.
AIN9M	10	AI	Analog input channel 9, negative input.

Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
AIN10P	11	AI	Analog input channel 10, positive input.
AIN10M	12	AI	Analog input channel 10, negative input.
AIN11P	13	AI	Analog input channel 11, positive input.
AIN11M	14	AI	Analog input channel 11, negative input.
AIN12P	15	AI	Analog input channel 12, positive input.
AIN12M	16	AI	Analog input channel 12, negative input.
AIN13P	17	AI	Analog input channel 13, positive input.
AIN13M	18	AI	Analog input channel 13, negative input.
AIN14P	19	AI	Analog input channel 14, positive input.
AIN14M	20	AI	Analog input channel 14, negative input.
AIN15P	21	AI	Analog input channel 15, positive input.
AIN15M	22	AI	Analog input channel 15, negative input.
AIN16P	23	AI	Analog input channel 16, positive input.
AIN16M	24	AI	Analog input channel 16, negative input.
AVDD_1V8	30, 51	P	1.8V power-supply. Connect 1µF and 0.1µF decoupling capacitors to GND.
AVDD_5V	26, 27, 56	P	5V analog supply. Connect 1µF and 0.1µF decoupling capacitors to GND.
DRDY/ALARM	49	DIO	Data ready or alarm; active high
CONVST	50	DI	Logic input to control start of conversion.
$\overline{CS}$	35	DI	Chip-select input for the SPI configuration; active low.
D0	46	DIO	Serial output data lane 0 or daisy-chain input 0.
D1	45	DIO	Serial output data lane 1 or daisy-chain input 1.
D2	44	DIO	Serial output data lane 2 or daisy-chain input 2.
D3	43	DIO	Serial output data lane 3 or daisy-chain input 3.
D4	42	DO	Serial output data lane 4.
D5	41	DO	Serial output data lane 5.
D6	40	DO	Serial output data lane 6.
D7	39	DO	Serial output data lane 7.
GND	25, 33, 48, 55	P	Ground.
IOVDD	34, 47	P	Digital I/O supply for the data interface. Connect 1µF and 0.1µF decoupling capacitors to GND.
REFCAPA	52	AO	Reference amplifier output pin. Connect a low ESR 1µF, X7R decoupling capacitor between pin 52 and 53.
REFIO	54	AIO	This pin acts as an internal reference output when REFSEL is high; this pin functions as input pin for the external reference when REFSEL is low; decouple with REFM on pin 53 using a 4.7µF capacitor.
REFCAPB	29	AO	Reference amplifier output pin. Connect a low ESR 1µF, X7R decoupling capacitor between pin 29 and 28.
REFM	28, 53	P	Reference GND pins. Shorted these pins to GND plane external to the device on the PCB.
REFSEL	31	DI	Logic input to select reference voltage source for the ADC.
$\overline{RESET}$	32	DI	Reset input for the device; active low.
SCLK	37	DI	Serial clock input for the data interface.
SDI	36	DI	Serial data input for the data interface.
SDOUT	38	DO	Serial data output for the user registers or single lane data output.
Thermal Pad	-	P	Exposed thermal pad. Connect to GND.

(1) AI = analog input; AO = analog output; AIO = analog input or output; DI = digital input; DO = digital output; DIO = digital input or output; P = power supply; and NC = no connect.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
AVDD_5V to GND	–0.3	6	V
AVDD_1V8 to GND	–0.3	2.1	V
IOVDD to GND	–0.3	3.6	V
AINnP - AINmM, between any adjacent analog pins	–50	50	V
AINnP and AINnM to GND	–50	50	V
REFIO to GND	GND – 0.3	VREF (4.096) + 0.3	V
Digital inputs to GND	GND – 0.3	3.6	V
Input current to any pin except supply pins(2)	–10	10	mA
Junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–60	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Limit pin current to 10mA or less.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	Analog input pins (AINnP and AINnM)	±8000	V
			All other pins	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)		±500	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
AVDD_5V	Analog power supply	AVDD_5V to GND	4.75	5	5.25	V
AVDD_1V8	Power supply	AVDD_1V8 to GND	1.7	1.8	1.9	V
IOVDD	Digital interface power supply	IOVDD to IOGND	1.7		3.6	V
REFERENCE VOLTAGE						
V_{REF}	Reference voltage to the ADC	External reference	4.086	4.096	4.106	V
ANALOG INPUTS						
AINnP	Operating input voltage, positive input		–50		50	V
AINnM	Operating input voltage, negative input		–50		50	V
	Voltage difference between adjacent analog pins (AINnP - AINmM)		–50		50	V
V_{CM}	Common mode input range, (AINnP + AINnM)/2	Differential input CM_RANGE_AINn = 0	–40		40	V
TEMPERATURE RANGE						
T_A	Ambient temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		ADS93x4, ADS93x4C RSK (VQFN) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	22.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	8.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	6.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

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6.5 Electrical Characteristics

at AVDD_5V = 4.75V to 5.25V, AVDD_1V8 = 1.7V to 1.9V, IOVDD = 1.7V to 3.6V, V_{REF} = 4.096V (internal or external), and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
R_{IN}	Input impedance	All input ranges		1		MΩ
	Input impedance thermal drift	All input ranges		10		ppm/°C
	Input capacitance			10		pF
V_{FSR}	Full-scale input range (AINnP – AINnM)	RANGE_n[2:0] = 010b	–2.5		2.5	V
		RANGE_n[2:0] = 000b	–5		5	V
		RANGE_n[2:0] = 011b	–6.25		6.25	V
		RANGE_n[2:0] = 100b	–10		10	V
		RANGE_n[2:0] = 101b	–12.5		12.5	V
		RANGE_n[2:0] = 001b	–25		25	V
		RANGE_n[2:0] = 110b	–50		50	V
V_{CM}	Common mode input range	Differential input CM_RANGE_AINn = 0	–40		40	V
ANALOG INPUT FILTER						
$BW_{(-3\ dB)}$	Analog input LPF bandwidth –3 dB	Low-bandwidth filter, all input ranges		25.5		kHz
		Wide-bandwidth filter, V_{FSR} = ±2.5V		280		kHz
		Wide-bandwidth filter, V_{FSR} = ±5V		325		kHz
		Wide-bandwidth filter, V_{FSR} = ±6.25V		300		kHz
		Wide-bandwidth filter, V_{FSR} = ±10V, ±12.5V		350		kHz
		Wide-bandwidth filter, V_{FSR} = ±25V, ±50V		400		kHz
	Phase delay	Low-bandwidth filter, all input ranges		6.2		µs
		Wide-bandwidth filter, all input ranges		0.5		µs
DC PERFORMANCE - SINGLE-ENDED						
	Resolution	No missing codes	16			Bits
DNL	Differential nonlinearity	All ranges		±0.5		LSB
INL	Integral nonlinearity	All ranges		±0.5		LSB
	Offset error(1) (4)	V_{FSR} = ±2.5V		±15		LSB
		V_{FSR} = ±5V, ±6.25V, ±10V, ±12.5V, ±25V		±8		LSB
		V_{FSR} = ±50V		±16		LSB
	Offset error thermal drift(2)	V_{FSR} = ±2.5V		1		ppm/°C
		V_{FSR} = ±5V, ±6.25V, ±10V, ±12.5V, ±25V		1		ppm/°C
		V_{FSR} = ±50V		1		ppm/°C
	Gain error(2) (3) (4)	V_{FSR} = ±2.5V, ±5V, ±6.25V, ±10V, ±12.5V, ±25V		±0.012		%FSR
		V_{FSR} = ±50V		±0.025		%FSR
	Gain error thermal drift(2) (3)	V_{FSR} = ±2.5V, ±5V, ±6.25V, ±10V, ±12.5V, ±25V		0.8		ppm/°C
		V_{FSR} = ±50V		2		ppm/°C
DC PERFORMANCE - DIFFERENTIAL						
	Resolution	No missing codes	16			Bits
DNL	Differential nonlinearity	All ranges		±0.5		LSB
INL	Integral nonlinearity	All ranges		±0.5		LSB

at AVDD_5V = 4.75V to 5.25V, AVDD_1V8 = 1.7V to 1.9V, IOVDD = 1.7V to 3.6V, V_{REF} = 4.096V (internal or external), and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Offset error(1) (4) (5)	V_{FSR} = ±2.5V		±15		LSB
		V_{FSR} = ±5V, ±6.25V, ±10V, ±12.5V, ±25V		±8		LSB
	Offset error thermal drift(2) (5)	V_{FSR} = ±2.5V		1		ppm/°C
		V_{FSR} = ±5V, ±6.25V, ±10V, ±12.5V, ±25V		1		ppm/°C
	Gain error(2) (3) (4) (5)	V_{FSR} = ±2.5V, ±5V, ±6.25V, ±10V, ±12.5V, ±25V		±0.012		%FSR
	Gain error thermal drift(2) (3) (5)	V_{FSR} = ±2.5V, ±5V, ±6.25V, ±10V, ±12.5V, ±25V		0.8		ppm/°C
DC PERFORMANCE - SINGLE-ENDED, OPEN WIRE SAFE						
	Resolution	No missing codes	16			Bits
DNL	Differential nonlinearity	All ranges		±0.5		LSB
INL	Integral nonlinearity	All ranges		±0.5		LSB
	Offset error(1) (4)	V_{FSR} = ±2.5V		±15		LSB
		V_{FSR} = ±5V, ±6.25V, ±10V, ±12.5V		±8		LSB
	Offset error thermal drift(2)	V_{FSR} = ±2.5V, ±5V, ±6.25V, ±10V, ±12.5V		1		ppm/°C
	Gain error(2) (3) (4)	V_{FSR} = ±2.5V, ±5V, ±6.25V, ±10V, ±12.5V		±0.012		%FSR
	Gain error thermal drift(2) (3)	V_{FSR} = ±2.5V, ±5V, ±6.25V, ±10V, ±12.5V		0.8		ppm/°C
AC PERFORMANCE - SINGLE-ENDED						
SNR	Signal-to-noise ratio in low-bandwidth mode (–0.1dBFS input at 1kHz)	V_{FSR} = ±2.5V		86		dB
		V_{FSR} = ±5V, ±6.25V		87		dB
		V_{FSR} = ±10V, ±12.5V, ±25V, ±50V		88		dB
	Signal-to-noise ratio in wide-bandwidth mode (–0.1dBFS input at 1kHz)	V_{FSR} = ±2.5V		77		dB
		V_{FSR} = ±5V		79.5		dB
		V_{FSR} = ±6.25V		81.5		dB
		V_{FSR} = ±10V		82.5		dB
		V_{FSR} = ±12.5V		84		dB
		V_{FSR} = ±25V		86		dB
		V_{FSR} = ±50V		87		dB
SINAD	Signal-to-noise + distortion ratio in low-bandwidth mode (–0.1dBFS input at 1kHz)	V_{FSR} = ±2.5V		84.7		dB
		V_{FSR} = ±5V, ±6.25V		86		dB
		V_{FSR} = ±10V, ±12.5V		86.4		dB
		V_{FSR} = ±25V, ±50V		87		dB
	Signal-to-noise + distortion ratio in wide-bandwidth mode (–0.1dBFS input at 1kHz)	V_{FSR} = ±2.5V		76.5		dB
		V_{FSR} = ±5V		78.9		dB
		V_{FSR} = ±6.25V		80.7		dB
		V_{FSR} = ±10V		81.6		dB
		V_{FSR} = ±12.5V		83		dB
		V_{FSR} = ±25V		85		dB
		V_{FSR} = ±50V		86		dB
THD	Total harmonic distortion (–0.1dBFS input at 1kHz)	All ranges		–103		dB
SFDR	Spurious-free dynamic range (–0.1dBFS input at 1kHz)	All ranges		100		dB
	Isolation crosstalk	At dc		–100		dB
AC PERFORMANCE - DIFFERENTIAL						

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at AVDD_5V = 4.75V to 5.25V, AVDD_1V8 = 1.7V to 1.9V, IOVDD = 1.7V to 3.6V, V_{REF} = 4.096V (internal or external), and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio in low-bandwidth mode (–0.1dBFS input at 1kHz)	V_{FSR} = ±2.5V		78		dB
		V_{FSR} = ±5V, ±6.25V		83		dB
		V_{FSR} = ±10V, ±12.5V, ±25V		86.5		dB
	Signal-to-noise ratio in wide-bandwidth mode (–0.1dBFS input at 1kHz)	V_{FSR} = ±2.5V		70		dB
		V_{FSR} = ±5V		74		dB
		V_{FSR} = ±6.25V		76		dB
		V_{FSR} = ±10V		79		dB
		V_{FSR} = ±12.5V		80		dB
		V_{FSR} = ±25V		84		dB
SINAD	Signal-to-noise + distortion ratio in low-bandwidth mode (–0.1dBFS input at 1kHz)	V_{FSR} = ±2.5V		77.2		dB
		V_{FSR} = ±5V, ±6.25V		81.6		dB
		V_{FSR} = ±10V, ±12.5V, ±25V		84.5		dB
	Signal-to-noise + distortion ratio in wide-bandwidth mode (–0.1dBFS input at 1kHz)	V_{FSR} = ±2.5V		70		dB
		V_{FSR} = ±5V		73.5		dB
		V_{FSR} = ±6.25V		75.3		dB
		V_{FSR} = ±10V		78.3		dB
		V_{FSR} = ±12.5V		78.8		dB
		V_{FSR} = ±25V		82		dB
THD	Total harmonic distortion (–0.1dBFS input at 1kHz)	All ranges		–103		dB
SFDR	Spurious-free dynamic range (–0.1dBFS input at 1kHz)	All ranges		100		dB
	CMRR	At dc, no CM error correction		74		dB
		At dc, CM error correction enabled, measured with ΔV_{CM} = 80V		100		dB
	Isolation crosstalk	At dc		–100		dB
AC PERFORMANCE - SINGLE-ENDED, OPEN WIRE SAFE						
SNR	Signal-to-noise ratio in low-bandwidth mode (–0.1dBFS input at 1kHz)	V_{FSR} = ±2.5V,		80		dB
		V_{FSR} = ±5V, ±6.25V		85.5		dB
		V_{FSR} = ±10V, ±12.5V		87.5		dB
	Signal-to-noise ratio in wide-bandwidth mode (–0.1dBFS input at 1kHz)	V_{FSR} = ±2.5V		71.5		dB
		V_{FSR} = ±5V		76		dB
		V_{FSR} = ±6.25V		78		dB
		V_{FSR} = ±10V		80		dB
		V_{FSR} = ±12.5V		81.5		dB
SINAD	Signal-to-noise + distortion ratio in low-bandwidth mode (–0.1dBFS input at 1kHz)	V_{FSR} = ±2.5V		79.3		dB
		V_{FSR} = ±5V, ±6.25V		84		dB
		V_{FSR} = ±10V, ±12.5V		86		dB
	Signal-to-noise + distortion ratio in wide-bandwidth mode (–0.1dBFS input at 1kHz)	V_{FSR} = ±2.5V		71.2		dB
		V_{FSR} = ±5V		75.6		dB
		V_{FSR} = ±6.25V		77.5		dB
		V_{FSR} = ±10V		79.3		dB
		V_{FSR} = ±12.5V		80.7		dB
THD	Total harmonic distortion (–0.1dBFS input at 1kHz)	All ranges		–103		dB

ADVANCE INFORMATION

at AVDD_5V = 4.75V to 5.25V, AVDD_1V8 = 1.7V to 1.9V, IOVDD = 1.7V to 3.6V, V_{REF} = 4.096V (internal or external), and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SFDR	Spurious-free dynamic range (–0.1dBFS input at 1kHz)	All ranges		100		dB
	Isolation crosstalk	At dc		–100		dB
INTERNAL REFERENCE						
V_{REF} (1)	Voltage on REFIO pin (configured as output)	1µF capacitor on REFIO pin, T_A = 25°C		4.096		V
	Reference temperature drift			15		ppm/°C
	Reference buffer output impedance			1		kΩ
	Reference turn-on time	1µF capacitor on REFCAP pin			30	ms
EXTERNAL REFERENCE INPUT						
REF_{LKG}	Reference input leakage current				±10	nA
DIGITAL INPUTS						
V_{IL}	Input low logic level threshold				0.3 IOVDD	V
V_{IH}	Input high logic level		0.7 IOVDD			V
DIGITAL OUTPUTS						
V_{OL}	Output low logic level	I_{OL} = 200µA sink	0		0.4	V
V_{OH}	Output high logic level	I_{OH} = 200µA source	IOVDD-0.4		IOVDD	V
POWER SUPPLY						
	Total power dissipation	Maximum throughput		230		mW
I_{AVDD_5V}	Supply current from AVDD_5V	Maximum throughput, internal reference		30		mA
I_{AVDD_1V8}	Supply current from AVDD_1V8	Maximum throughput, internal reference		32		mA
I_{IOVDD}	Supply current from IOVDD	Maximum throughput		6		mA

(1) Does not include the variation in voltage resulting from solder shift effects.
(2) The specifications include the full operating temperature range after offset error calibration at T_A = 25°C.
(3) These specifications include the full temperature range variation but not the error contribution from internal reference.
(4) ADC_CAL is performed at the power up.
(5) Common mode error correction is enabled (CME_CORR_EN_AINn =1b).

ADVANCE INFORMATION

6.6 Timing Requirements

at AVDD_5V = 4.75V to 5.25V, AVDD_1V8 = 1.7V to 1.9V, IOVDD = 1.7V to 3.6V, V_{REF} = 4.096V (internal or external), and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

		MIN	MAX	UNIT
CONVST				
t_{CONVST}	Sampling time interval (1 / f_{CONVST})	1		µs
t_{PL_CV}	CONVST pulse low time	50		ns
t_{PH_CV}	CONVST pulse high time	50		ns
$t_{su\_CV\_hi\_DRDY\_hi}$	Setup time: CONVST rising to the DRDY rising(1)	50		ns
SERIAL INTERFACE				
f_{SCLK}	Maximum SCLK frequency		60	MHz
t_{SCLK}	Minimum SCLK time period	16		ns
t_{PH_SCLK}	SCLK high time	0.45	0.55	t_{SCLK}
t_{PL_SCLK}	SCLK low time	0.45	0.55	t_{SCLK}
t_{hi_CS}	Pulse duration: $\overline{CS}$ high	16		ns
t_{su_CSCK}	Setup time: $\overline{CS}$ falling to the first SCLK capture edge	16		ns
t_{ht_CSCK}	Hold time: last SCLK falling edge to $\overline{CS}$ rising time	16		ns
t_{su_CKDI}	Setup time: SDI data valid to the corresponding SCLK rising edge	3		ns
t_{ht_CKDI}	Hold time: SCLK rising edge to corresponding data valid on SDI	1		ns
t_{su_DRDYCS}	Setup time: DRDY rising edge to CS falling edge	0		ns
t_{ht_DRDYCS}	Hold time: DRDY rising edge to CS rising edge	0		ns

(1) Applicable only for internal clock oversampling mode.

ADVANCE INFORMATION

6.7 Switching Characteristics

at AVDD_5V = 4.75V to 5.25V, AVDD_1V8 = 1.7V to 1.9V, IOVDD = 1.7V to 3.6V, V_{REF} = 4.096V (internal or external), and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
RESET					
t_{PU}	Power-up time for device	1-µF capacitor on REFCAP pin		30	ms
SERIAL INTERFACE					
t_{d_CSDO}	Delay time: CS falling edge to data valid on SDOUT and D[7:0]			16	ns
t_{dz_CSDO}	Delay time: CS rising edge to SDOUT and D[7:0] going Hi-Z			7.5	ns
t_{vt_CKDO}	Valid time: SCLK launch edge to previous data valid on SDOUT and D[7:0]		7.6		ns
t_{d_CKDO}	Delay time: SCLK launch edge to corresponding data valid on SDOUT and D[7:0]			17	ns
DRDY AND ALARM					
t_{CYC}	ADC cycle time period		1 / f_{CONVST}		µs
$t_{d\_CVDRDY\_hi}$	Data ready time, time delay between CONVST falling edge to DRDY rising edge			t_{CONV}	µs
$t_{d\_CVDRDY\_lo}$	Time delay between CONVST falling edge to DRDY falling edge			350	ns
t_{d_ALARM}	Time delay between CONVST falling edge to new ALARM valid			t_{CONV}	µs

6.8 Timing Diagrams

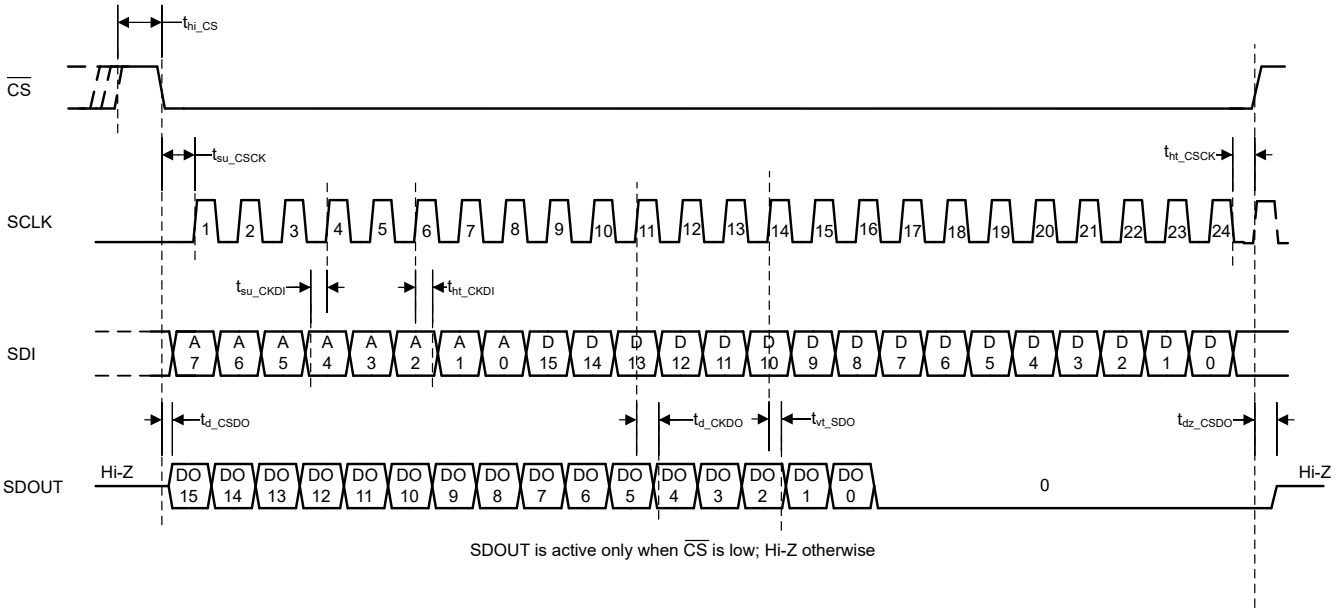


Figure 6-1. Timing for Register Read and Write Operations

ADVANCE INFORMATION

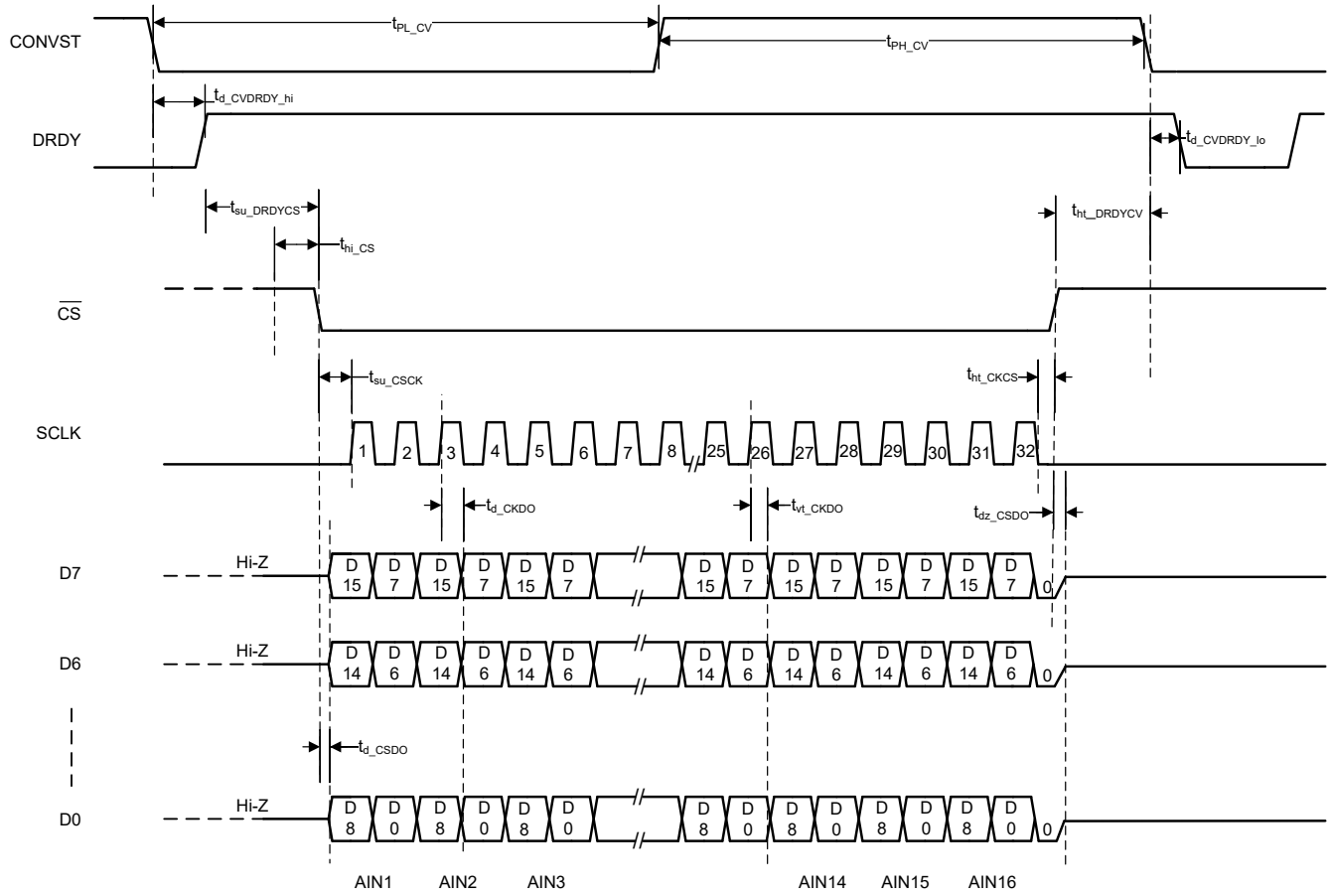


Figure 6-2. ADC Conversion Data Read Timing: 8-Lane (Default Operation)

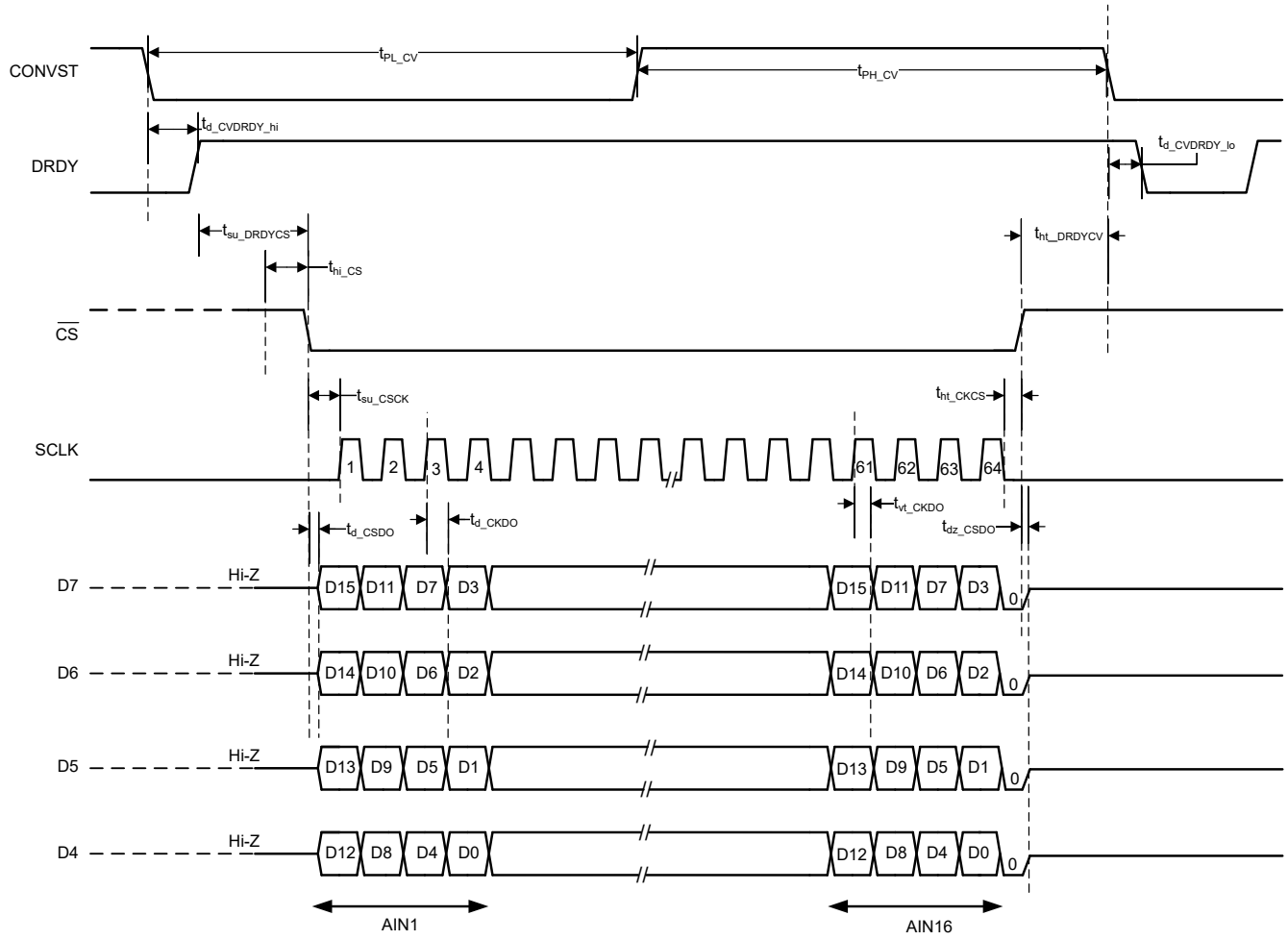


Figure 6-3. ADC Conversion Data Read Timing: 4-Lane

ADVANCE INFORMATION

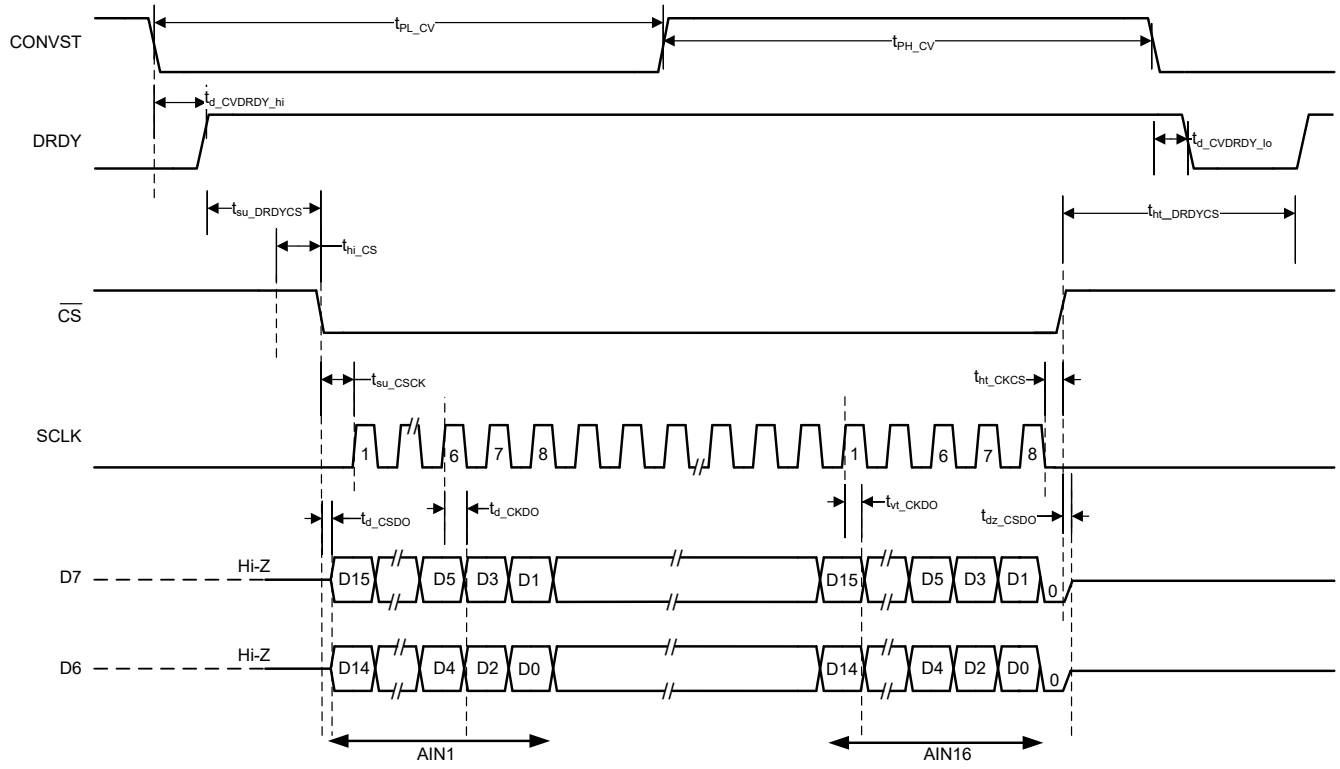


Figure 6-4. ADC Conversion Data Read Timing: 2-Lane

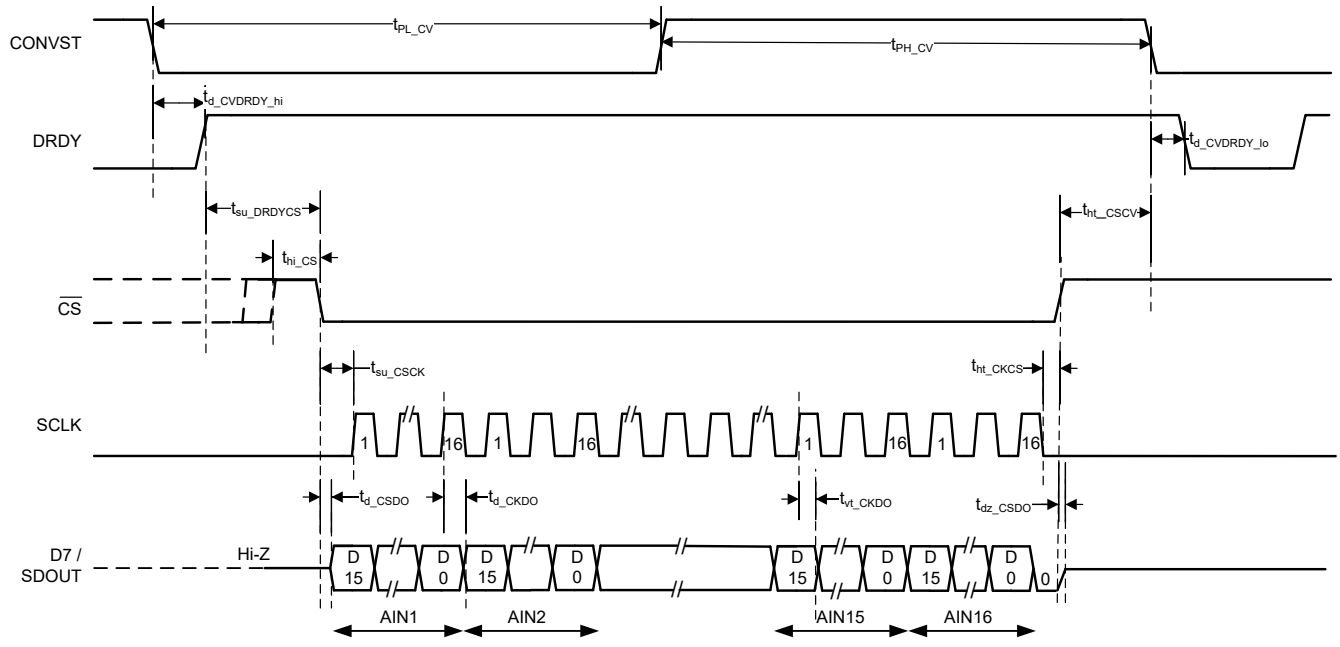
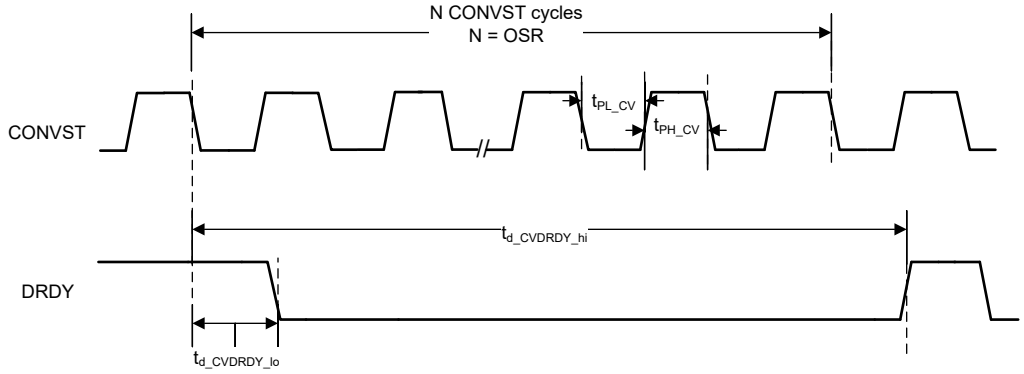


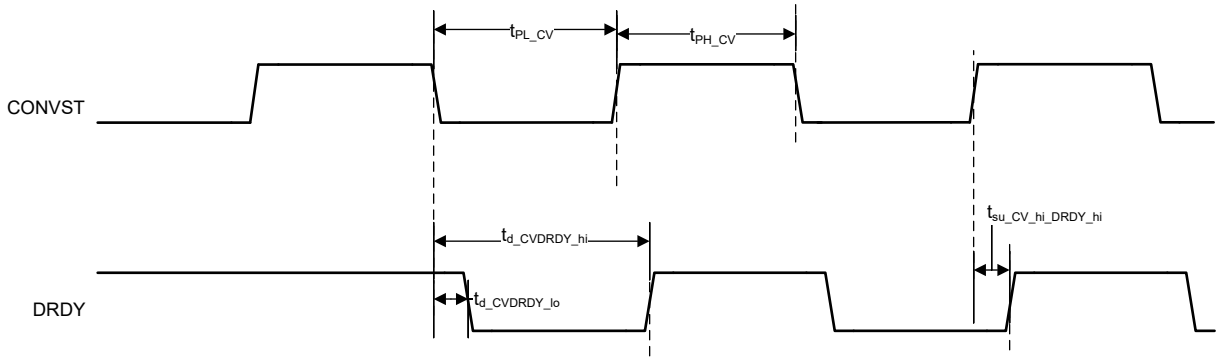
Figure 6-5. ADC Conversion Data Read Timing: 1-Lane



Note

1. Applicable when using block average filter with external clock oversampling mode and FIR filters. For FIR filters, N is the decimation factor.

Figure 6-6. CONVST and DRDY, External Clock Oversampling



Note

1. In the internal clock oversampling mode, CONVST must go high before the rising edge of the DRDY for proper device operation. The timing requirement is defined by $t_{su\_CV\_hi\_DRDY\_hi}$. This limits the minimum t_{PH_CV} of the CONVST signal. The minimum value of t_{PH_CV} is given by $t_{PH\_CV} = t_{CONVST} - 1.2\ \mu s$, applicable for $f_{CONVST} \leq \frac{800kHz}{N}$, where N is the oversampling ratio.
2. Applicable for block average filter with internal clock oversampling mode.

Figure 6-7. CONVST and DRDY, Internal Clock Oversampling

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7 Detailed Description

7.1 Overview

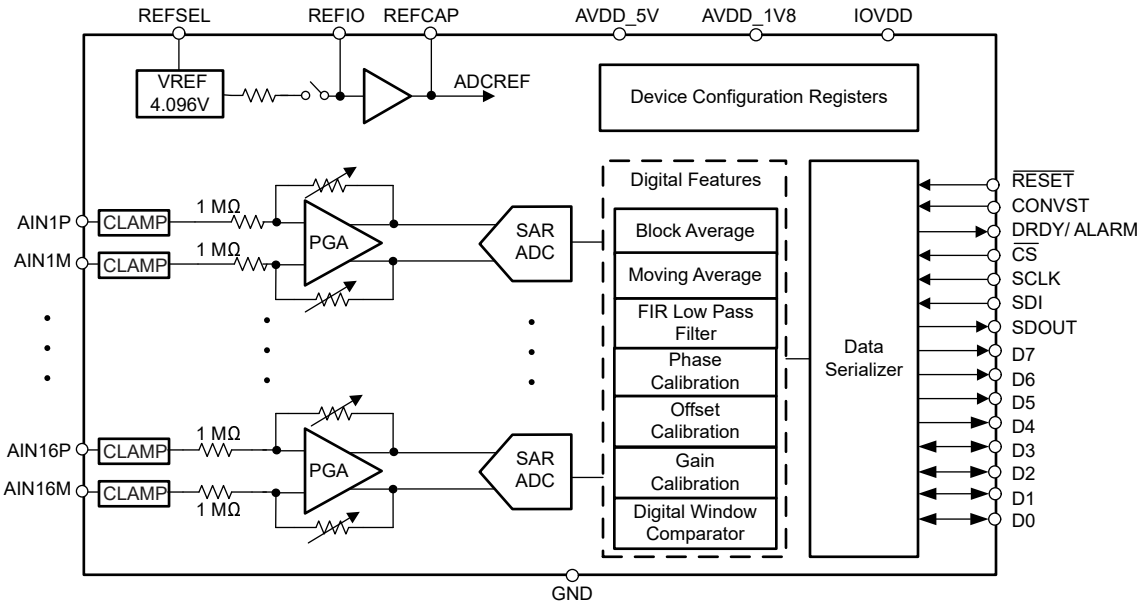
The ADS9324C is a 16-bit simultaneous sampling data acquisition (DAQ) system with sixteen analog input channels configurable as either single-ended or differential. Each analog input channel consists of an input clamp protection circuit and a programmable gain amplifier (PGA) with user-selectable bandwidth options. The input signals are digitized with a 16-bit analog-to-digital converter (ADC), based on the successive approximation register (SAR) architecture. This overall system achieves a maximum throughput of 1MSPS per channel for all channels. The device has a 4.096V internal precision reference with a buffer to drive the ADC.

The device operates from 5V and 1.8V analog supplies and accommodates true bipolar input signals. The device offers a constant 1MΩ resistive input impedance irrespective of the sampling frequency or the selected input range. The ADS9324C offers a simplified end design without requiring external amplifiers, high-voltage bipolar supplies, and complicated driver circuits. The device supports both differential and single-ended inputs, allowing the device to be used with various sensor outputs. For single-ended inputs, the device includes an open-wire safe mode, which results in a near-zero ADC output code if a sensor is suddenly disconnected from the ADC inputs.

Each channel on the ADS9324C contains optional digital filters to improve noise performance of the ADC. The digital filter supports block average, moving average and low pass FIR modes. The ADS9324C also contains offset, gain and phase calibration features that can be programmed to automatically adjust the ADC output for measured offset, gain and phase errors. The device includes a ADC calibration (ADC_CAL) module to calibrate the ADC errors and reduces the channel to channel offset and gain mismatch. The ADC_CAL feature is useful when the user is not performing any system-level calibration, and requires low ADC offset and gain error at power-up.

The ADS9324C includes a flexible digital interface allowing the device to be used with a variety of host controllers. Users can configure the serial interface to read the ADC output on 1-lane, 2-lane, 4-lane, and 8-lane. The device also has flexibility to operate the ADC as 2-CH, 4-CH, 8-CH and 16-CH simultaneous sampling ADC. An ADC output randomizer feature is also provided to minimize interference between data transmission and analog performance of the ADC when the PCB layout does not minimize ground bounce.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Inputs

The ADS9324C incorporates sixteen, simultaneous sampling, 16-bit successive approximation register (SAR) analog-to-digital converters (ADCs). The device has a total of sixteen analog input pairs. The ADC digitizes the voltage difference between the analog input pairs AINnP – AINnM. Figure 7-1 shows the simplified circuit schematic for each analog input channel, including the input clamp protection circuit, PGA with selectable low-pass filter, and a precision 16-bit SAR ADC.

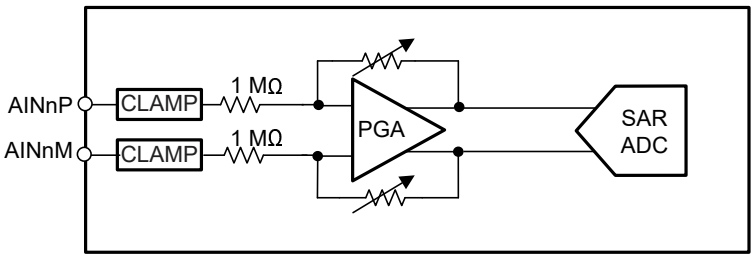


Figure 7-1. Front-End Circuit Schematic of the Analog Input Channel

7.3.2 Input Clamp Protection Circuit

As shown in Figure 7-1, the ADS9324C features an internal clamp protection circuit on each of the sixteen analog input channels. Use of external protection circuits is recommended as a secondary protection scheme to protect the device. Using external protection devices helps with protection against surges, electrostatic discharge (ESD), and electrical fast transient (EFT) conditions.

The ADS9324C allows each analog input to swing up to a maximum voltage of ±50V. In case of overvoltage condition, the input current increase linearly with the input voltage up to clamp voltage of ±105V. Figure 7-2 shows a typical current versus voltage characteristic curve for the input clamp. Beyond this voltage, the input clamp circuit turns on, and current increases exponentially.

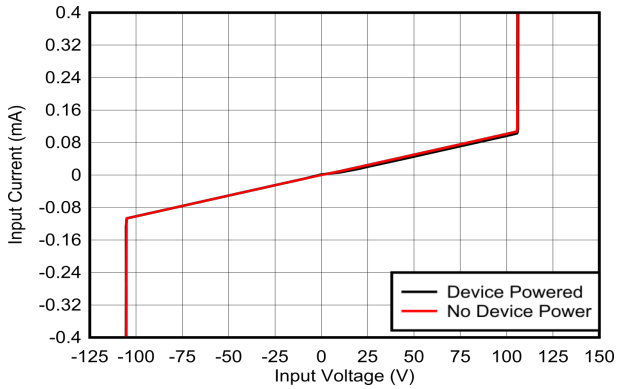


Figure 7-2. Input Clamp Protection Profile: Input Current vs Input Voltage

For input voltages exceeding the maximum input voltage ±50V, make sure that input current never exceeds the absolute maximum rating (see the *Absolute Maximum Ratings* table) of ±10mA to prevent any damage to the device. Figure 7-3 shows that a small series resistor placed in series with the analog inputs is an effective way to limit the input current. In addition to limiting the input current, this resistor can also provide an antialiasing, low-pass filter when coupled with a capacitor. To maintain the dc accuracy of the system, matching the external source impedance on the AIN*n*P input pin with an equivalent resistance on the AIN*n*M pin is recommended. This matching helps to cancel any additional offset error contributed by the external resistance.

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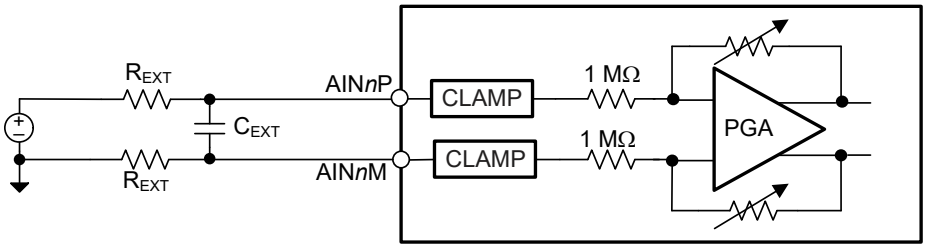

Figure 7-3. Matching Input Resistors on the Analog Inputs of Devices

The input overvoltage protection clamp on the ADS9324C is intended to control transient excursions on the input pins. Leaving the device in a state such that the clamp circuit is activated for extended periods of time in normal or power-down mode is not recommended because this fault condition can degrade device performance and reliability.

7.3.3 Analog Input Impedance

Each analog input channel in the device presents an input resistance of 1MΩ on both AIN*n*P and AIN*n*M pins. The input resistance for each channel is independent of either the input signal frequency, the configured range of the ADC, or the oversampling mode. The primary advantage of such high-impedance inputs is the ease of driving the ADC inputs without requiring driving amplifiers with low output impedance. Bipolar, high-voltage power supplies are not required in the system because this ADC does not require any high-voltage, front-end drivers. In most applications, the signal sources or sensor outputs can be directly connected to the ADC input, thus significantly simplifying the design of the signal chain.

To maintain the dc accuracy of the system, matching the external source impedance on the AIN*n*P input pin with an equivalent resistance on the AIN*n*M pin is recommended (see Figure 7-3). This matching helps to cancel any additional offset error contributed by the external resistance.

7.3.4 Programmable Gain Amplifier (PGA)

The ADS93x4C features a programmable gain amplifier (PGA) at the every analog input channel. The PGA supports both single-ended and differential inputs with a bipolar signal swing. In differential-input mode, the ADS93x4C can take maximum common mode voltage of ±40V. In signal-ended mode, the maximum common mode voltage supported is $\pm\frac{\text{RANGE}}{2}$. Table 7-1 lists the supported analog input ranges. Configure the analog input range independently for each channel with the INPUT_RANGE_AINn[2:0] register fields in PGA_CONFIG_AINx registers.

Each analog input channel features an antialiasing, low-pass filter (LPF) at the output of the PGA. Table 7-2 lists the various programmable LPF options available in the ADS9324C, corresponding to the analog input range. The following illustrates the frequency responses for low-bandwidth and wide-bandwidth LPF configurations. Select the analog input bandwidth for the each analog input channels with the PGA_SEL bit field in the PGA_BW_SEL_AINn registers. By default, the all PGA are in low-bandwidth mode.

Table 7-1. Analog Input Ranges

INPUT TYPE	RANGE	INPUT_RANGE_AINx	CM_RANGE_AINx
Single-ended	±50V	6	5
Single-ended	±25V	1	5
Single-ended	±12.5V	5	5
Single-ended	±10V	4	5
Single-ended	±6.25V	3	5
Single-ended	±5V	0	5
Single-ended	±2.5V	2	5
Differential	±25V	1	0
Differential	±12.5V	5	0
Differential	±10V	4	0

Table 7-1. Analog Input Ranges (continued)

INPUT TYPE	RANGE	INPUT_RANGE_AINx	CM_RANGE_AINx
Differential	±6.25V	3	0
Differential	±5V	0	0
Differential	±2.5V	2	0
Single-ended open wire safe	±12.5V	5	6
Single-ended open wire safe	±10V	4	6
Single-ended open wire safe	±6.25V	3	6
Single-ended open wire safe	±5V	0	6
Single-ended open wire safe	±2.5V	2	6

Table 7-2. Low-Pass Filter Corner Frequency

LPF	PGA_BW_SEL_AINn	ANALOG INPUT RANGE	CORNER FREQUENCY (–3dB)
Low-bandwidth	0	All input ranges	25.5kHz
Wide-bandwidth	1	±2.5V	280kHz
		±5V	325kHz
		±6.25V	300kHz
		±10V, ±12.5V	350kHz
		±25V, ±50V	400kHz

7.3.5 ADC Transfer Function

The ADS9324C outputs 16 bits of conversion data in either straight-binary or binary two's-complement formats. By default, ADC output is in binary two's-complement format. Set EN_OFS_BINARY to 1'b for straight-binary format. The format for the output codes is the same across all analog channels. Figure 7-4 show the transfer characteristics for the ADS9324C.

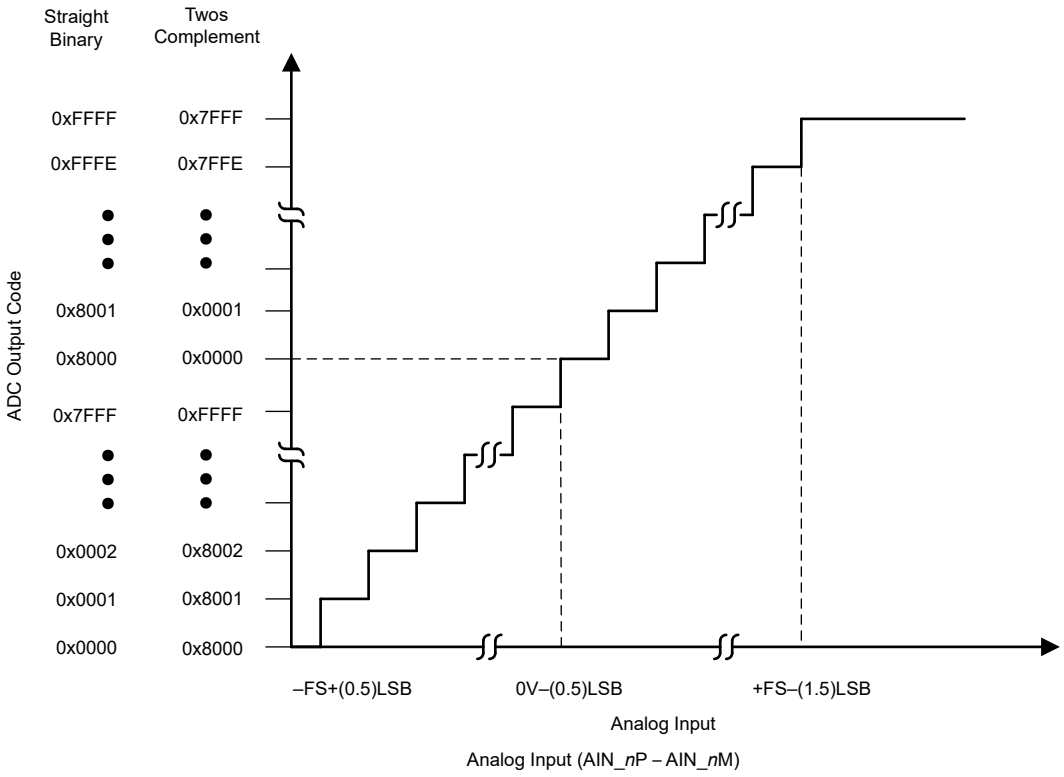

Figure 7-4. ADC Transfer Characteristics

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7.3.6 Reference

The ADS93x4C has a precision, low-drift voltage reference internal to the device. For best performance, filter the internal reference noise by connecting a 4.7µF ceramic bypass capacitor to the REFIO pin, and connect 1µF ceramic capacitors directly between REFCAPA and REFM pins, and between the REFCAPB and REFM pins, shows in the Figure 7-5 and Figure 7-6. On power-up, as described in Table 7-3, the reference source is selected by the REFSEL pin or by the values in the REFSEL_CTRL and EXT_REF_EN fields in address 0x10 in the ADS93x4C Common register bank.

Table 7-3. ADC Voltage Reference Source Selection

REFSEL INPUT	REFSEL_CTRL_DIS	EXT_REF_EN	ADC REFERENCE SOURCE
Low	0b	X	ADC reference is selected using REFSEL pin. External reference on REFIO pin.
High	0b	X	ADC reference is selected using REFSEL pin. Internal reference is active.
X	1b	0b	ADC reference is selected using EXT_REF_EN bit field in 0x10 register. Internal reference is active.
X	1b	1b	ADC reference is selected using EXT_REF_EN bit field in 0x10 register. External reference is selected. Force external reference on REFIO pin.

Note

1. If the external reference is not applied in the external reference operation, the device goes into power down mode.

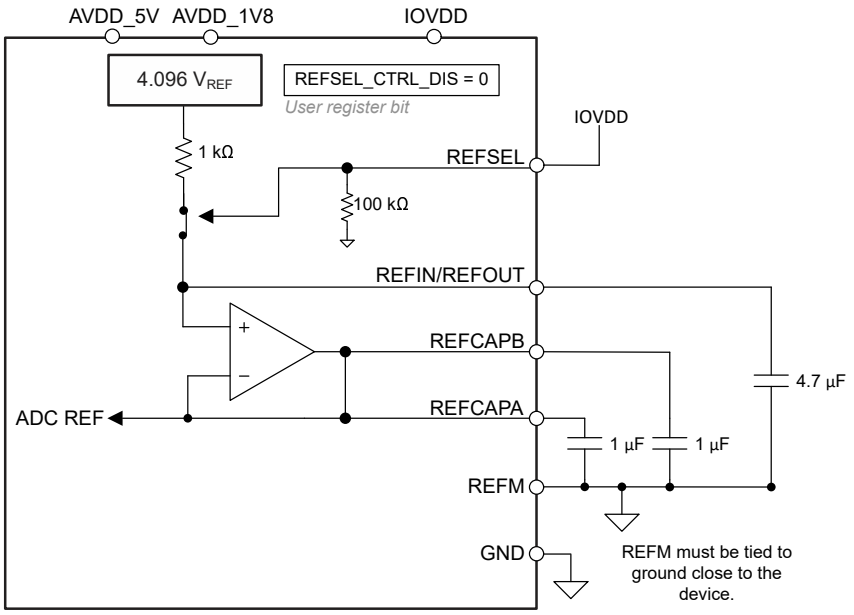

Figure 7-5. Internal Reference Voltage

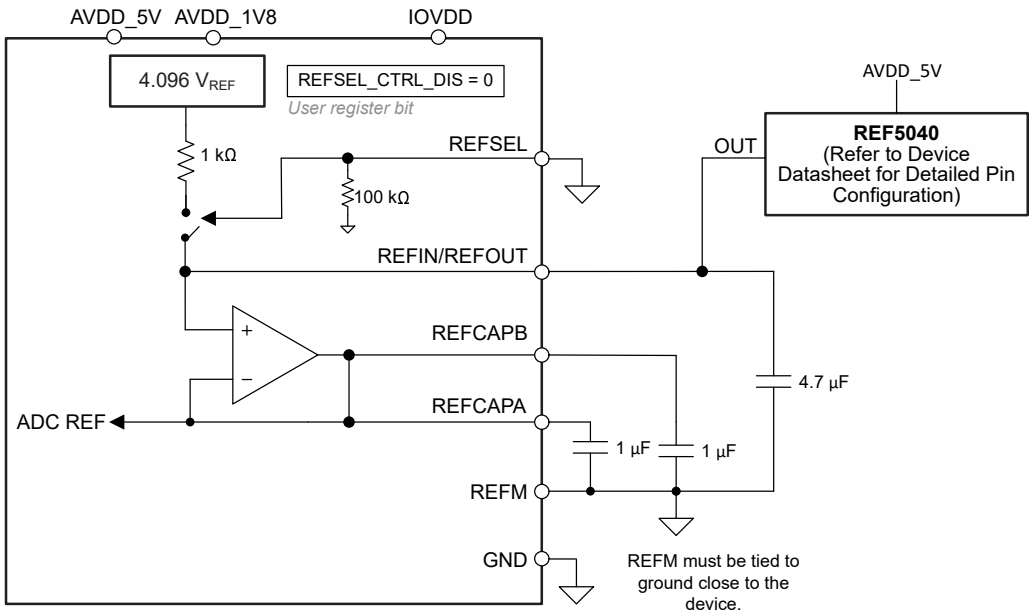

Figure 7-6. External Reference Voltage

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7.3.7 Open Wire Safe Mode

The ADS9324C is designed to handle open circuit inputs without producing erroneous conversion results. When both inputs AINnP and AINnM are left in an open circuit condition, the ADC output code remains within ±16LSB of the 0V reference code. In single-ended conditions, where AINnM is connected to ground, a pull-down resistor (R_{PD}) is needed to keep the ADC output close to zero code, shown in the Figure 7-7. There are three input modes in the devices: differential, single-ended, and single-ended open-wire safe. Open-wire safe mode produces the least change in the ADC output for a given pull-down resistor when the input signal source is floating. see the Table 7-4. To configure the analog inputs in the open-wire safe mode, set the CM_RANGE_AINn to 110b.

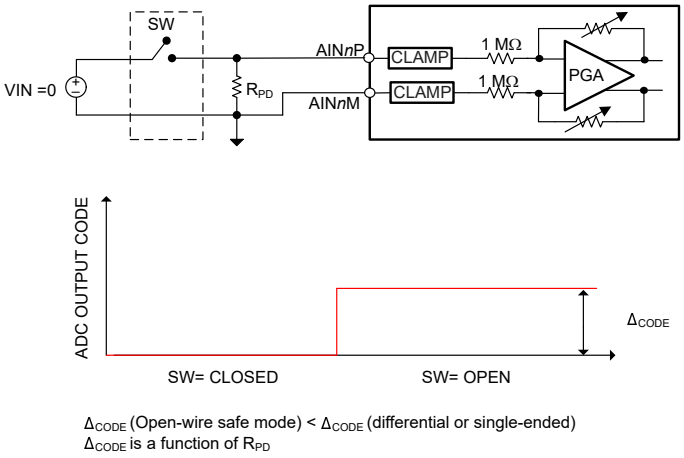

Figure 7-7. Open-Wire Safe Mode

Table 7-4. R_{PD} and Offset Increment (RANGE = ±10V, ±5V)

R_{PD} (kΩ)	Δ_{CODE} OPEN-WIRE SAFE	Δ_{CODE} SINGLE-ENDED
2.5	$2LSB_{16}$	$15LSB_{16}$
5	$4LSB_{16}$	$30LSB_{16}$
7.5	$6LSB_{16}$	$45LSB_{16}$
10	$8LSB_{16}$	$60LSB_{16}$
Open (Hi-Z)	≅0.18V (RANGE = ±5V) ≅0.36V (RANGE = ±10V	≅1.89V (RANGE = ±5V) ≅2.10V (RANGE = ±10V)

Figure 7-9 and Figure 7-8 show the ADC output with changes in the pull down resistor value.

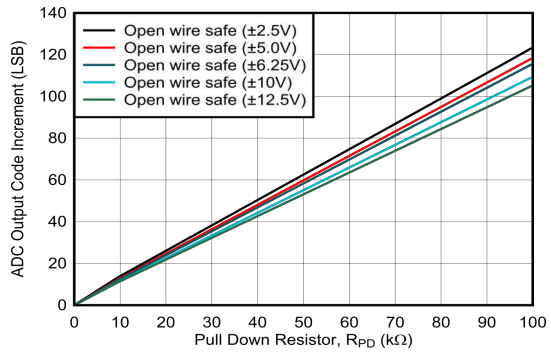

Figure 7-8. Open Circuit ADC Code Error With R_{PD}(Open Wire Safe Mode)

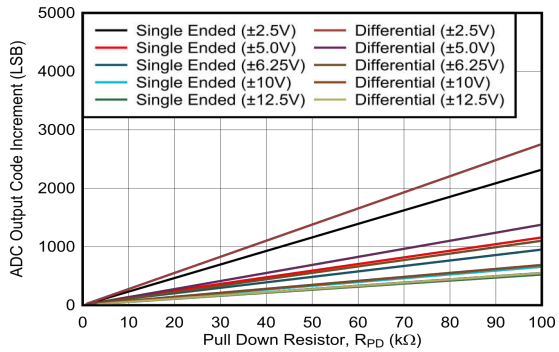

Figure 7-9. Open Circuit ADC Code Error With R_{PD}(Single-ended and Differential)

7.3.8 System Offset Calibration

Any offset present on the sensor, or offset error caused by mismatch between R_{EXT} (see Figure 7-3) used at the analog input pins can be compensated using ADS93x4C onchip offset calibration feature. The offset calibration value is a 10-bit value coded in two's-complement format, and is added to the ADC conversion data. The offset calibration operation precedes gain calibration operation. Equation 1 shows ADC output code after offset operation, and Table 7-5 shows ADC output with different offset calibration register values. By default, offset calibration is enabled, and OFS_AINx value is 000h. The offset calibration can be disabled by writing OFS_CAL_DIS to 1b in GEN_CFG5 register.

$$\text{ADC Output Code} = \frac{(16\text{−bit ADC Conversion Result}) \times 4 + \text{OFS\_AINx}}{4} \quad (1)$$

Table 7-5. Offset Calibration Example

OFS_AINx Register Code	ADC FINAL OUTPUT
1FFh	ADC Code + $127LSB_{16}$
100h	ADC Code + $64LSB_{16}$
001h	ADC Code + 0.25LSB
3FFh	ADC Code – $1LSB_{16}$
2FFh	ADC Code – $64LSB_{16}$
200h	ADC Code – $128LSB_{16}$

7.3.9 System Gain Calibration

Using external resistors at the analog input of the ADC creates a system gain error, which can be compensated using system gain calibration feature inside the ADS93x4C device. Table 7-6 shows example gain calibration values. The gain calibration can be disabled by writing GAN_CAL_DIS to 1b in GEN_CFG5 register.

$$\text{Gain Correction Applied} = \frac{(\text{Gain Register Value})}{65536} \quad (2)$$

$$\text{Gain Register Value} = \frac{(\text{Actual Code} - \text{ADC code})}{\text{ADC Code}} \times 65536 \text{ ; For 2's complement} \quad (3)$$

$$\text{Gain Register Value} = \frac{(\text{Actual Code} - \text{ADC code})}{\text{ADC Code} - 32768} \times 65536 \text{ ; For offset binary} \quad (4)$$

Table 7-6. Gain Calibration Example

GAN_AINx	GAIN CORRECTION APPLIED	ADC FINAL OUTPUT (TWO's COMPLEMENT)
1FFFh	0.124985	ADC Code × 1.124985
0CCDh	0.050003	ADC Code × 1.05003
0000h	0	ADC Code × 1.0
3333h	–0.050003	ADC Code × 0.949997
2000h	–0.124985	ADC Code × 0.875015

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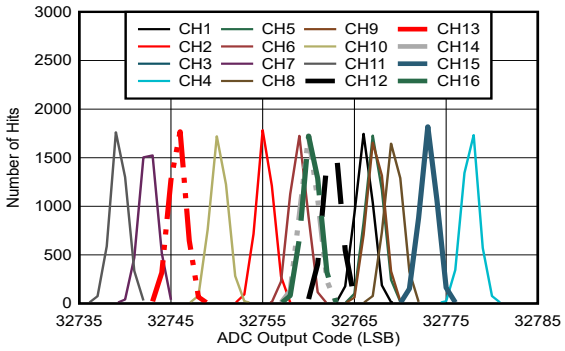
7.3.10 ADC Gain and Offset Error Calibration

The ADS93x4C includes a ADC calibration module (ADC_CAL) for every ADC channel. Any change in ADC gain and offset error due to changes in the ambient temperature can be calibrated using this calibration. When ADC_CAL is running, the ADC waits for T_{WAIT} time to calibrate the gain and offset error of the all channels (see the Table 7-7). The ADC calibration module does not affect the signals at the AINnP and AINnM input pins. ADC_CAL is an optional feature and requires user triggering to initiate operation. If the user is performing system-level offset and gain calibration, either using the on-chip system gain and offset error feature or in the host, ADC_CAL is not required. The ADC_CAL feature is useful when the user is not performing any system level calibration, and requires low ADC offset and gain error at power-up.

Table 7-7. ADC Calibration Time (T_{WAIT})

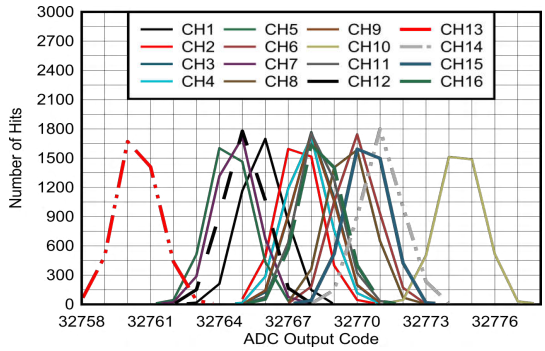
ADC_CAL MODE	INT_TRIG_MODE	T_{WAIT} TIME
Free running CONVST	0b	$100{,}000 \; x \; t_{CONVST}$
Single-shot	1b	125ms

Figure 7-10 and Figure 7-11 show ADC output code when input shorted to ground before and after ADC calibration is performed. Channel-channel to offset error gets reduced from $40LSB_{16}$ to $15LSB_{16}$, and offset error is reduced from $\pm30LSB_{16}$ to $\pm8LSB_{16}$ after calibration is performed.



RANGE = ±5V, low-bandwidth, single-ended, V_{IN} = 0V, channel-to-channel offset mismatch = $40LSB_{16}$, offset error = $\pm30LSB_{16}$

Figure 7-10. Offset Error Before ADC Calibration



RANGE = ±5V, low-bandwidth, single-ended, V_{IN} = 0V, channel-to-channel offset mismatch = $15LSB_{16}$, offset error = $\pm8LSB_{16}$

Figure 7-11. Offset Error After ADC Calibration

ADC calibration block is configured using ADC_CAL register in the ADS93x4C Common register bank. Before running ADC calibration module, enable common mode error correction feature if required and disable digital filters. By default digital filters are disabled. ADC calibration module requires user to provide analog input configuration. Depending on the single ended or differential analog mode, update SE_DIFF_MODE_AIN9_16 and SE_DIFF_MODE_AIN1_8 bit fields in the ADC_CAL register. See below for steps required to run the ADC gain and offset error calibration module.

ADC Calibration (Single-shot Mode):

1. Set the INT_TRIG_MODE to 1b.
2. The ADC calibration module supports three calibration modes, offset calibration, gain calibration, and offset and gain calibration. Update ADC_CAL_MODE bit field to 01b, 10b and 11b for offset only, gain only and, offset and gain calibration. Writing 00b on the ADC_CAL_MODE disables the automatic calibration block and calibration value applied to the ADC data output. Verify that this field is set to 01b, 10b or 11b if the ADC calibration feature is used.
3. Write 0b to 1b for a rising edge transition on the ADC_CAL_TRIG bit.
4. Wait for 10µs.

5. Write ADC_CAL_TRIG bit to 0b.
6. Send a single clock pulse to the device. At least one falling edge must be provided. If the clock idle state is low, the device requires a low-high pulse sequence. End state of the CONVST must be high.
7. Wait for 125ms. Alternatively, the user can read the CALIB_BUSY flag status to determine when calibration is complete.
8. User can now operate the ADC in normal operation.

ADC Calibration With Continuous CONVST Signal: Use the below programming sequence to configure the ADC_CAL block if INT_TRIG_MODE is programmed to 0b.

1. Verify that a free running CONVST clock is provided to the ADC.
2. The ADC calibration module supports three calibration modes, offset only calibration, gain only calibration, and offset and gain calibration. Update ADC_CAL_MODE bit field to 01b, 10b and 11b for offset only, gain only and, offset and gain calibration. Writing 00b on the ADC_CAL_MODE disables the automatic calibration block and calibration value applied to the ADC data output. Verify that this field is set to 01b, 10b or 11b if the ADC calibration feature is used.
3. Write 0b to 1b for a rising edge transition on the ADC_CAL_TRIG bit.
4. Verify that at least one t_{CONVST} delay time.
5. Write ADC_CAL_TRIG bit to 0b.
6. Wait for 100,000 CONVST clock cycles. For 1MHz CONVST, the wait time required is 100ms.
7. User can now operate the ADC in normal operation.

7.3.11 Digital Filter

The ADS93x4C includes four digital filter options as shown in the Figure 7-12. At a time only one filter path is selected, and is applied to all channels. Digital filter is selected using DIG_FILTER register in the ADS93x4C Common register bank.

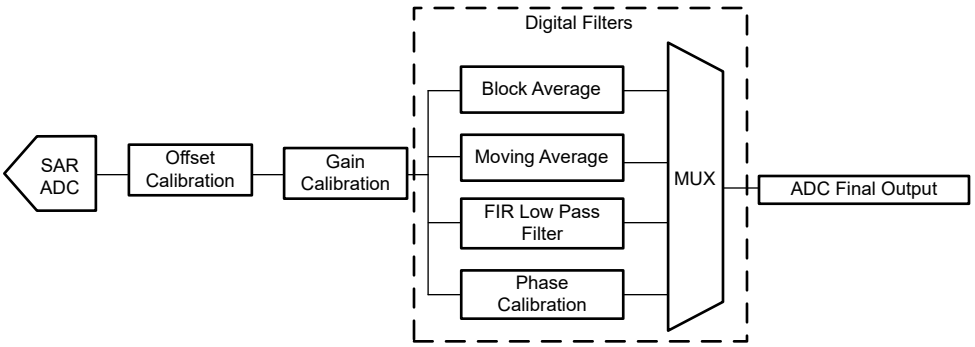


Figure 7-12. ADC Output Data Path

7.3.11.1 System Phase Calibration

The phase mismatch between channels can be compensated, on a per-channel basis, using the phase calibration feature present inside the device. The phase calibration is done using digital delay, and has minimum resolution of 1µs at CONVST of 1MSPS. Phase delay is introduced using 8-bit field in PHASE_DELAY_AINx registers in AIN1 - AIN8 Channel and AIN9 - AIN16 Channel register banks. Equation 5 calculates the phase calibration value.

$$\text{Phase Calibration Applied} = \frac{\text{PHASE\_DELAY\_AINx}}{\text{ADC Sampling Frequency}} \quad (5)$$

Phase Calibration Filter Configuration:

1. Calculate the PHASE_DELAY_AINx field value using Equation 5.
2. Program the PHASE_DELAY_AINx register for the respective channels.
3. Set the PHASE_DELAY_EN bit in the DIG_FILTER register to 1b.
4. Write 0b to 1b on the DIGITAL_FILT_SYSREF bit field in the DIGITAL_FILTER register. Verify that at least one t_{CONVST} delay time, and then write DIGITAL_FILT_SYSREF bit to 0b, shown in Figure 7-13.

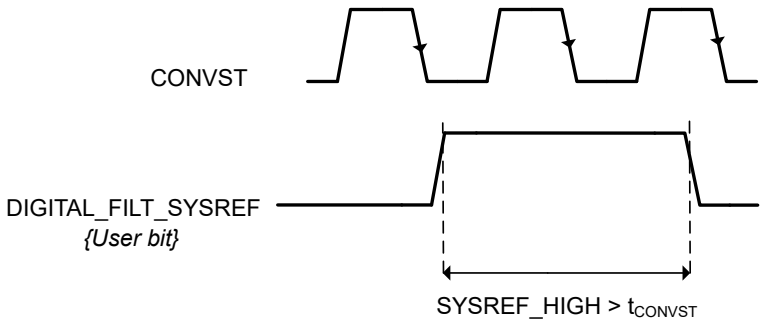
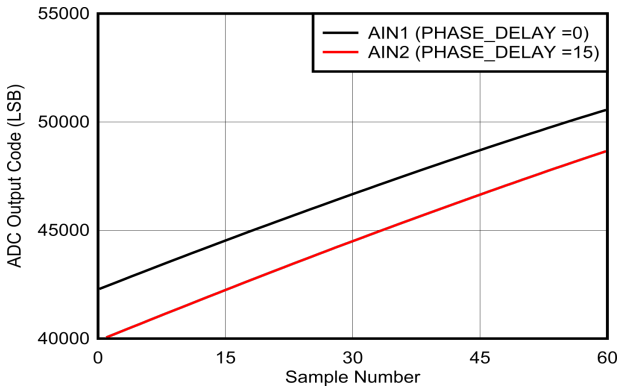


Figure 7-13. Digital Filter SYSREF and CONVST



Same input single applied on AIN1 and AIN2

Figure 7-14. Phase Adjustment Example

7.3.11.2 Block Average Filter

The ADS9324C features an optional block averaging digital filter that can be used in slower throughput applications requiring lower noise and higher dynamic range. The overall throughput of the ADC decreases proportionally with increase in the oversampling ratio of the block average filter. Oversampling can be done using both external or internal oversampling clock, as shown in Figure 7-15 and Figure 7-16. By default, oversampling works with external clock where ADC takes samples for each channel on the falling edge of the CONVST clock before reporting out the average value. In the external clock oversampling, the input signal is sampled at regular intervals, providing optimal antialiasing performance. Initialize the GEN_CFG5 register field before using the on-chip digital filters of the ADS9324C. First, set the AVG_MODE_OVR_EN bit field in the GEN_CFG5 register to 1b. Then, set the AVG_MODE bit field in the GEN_CFG5 register to 1b.

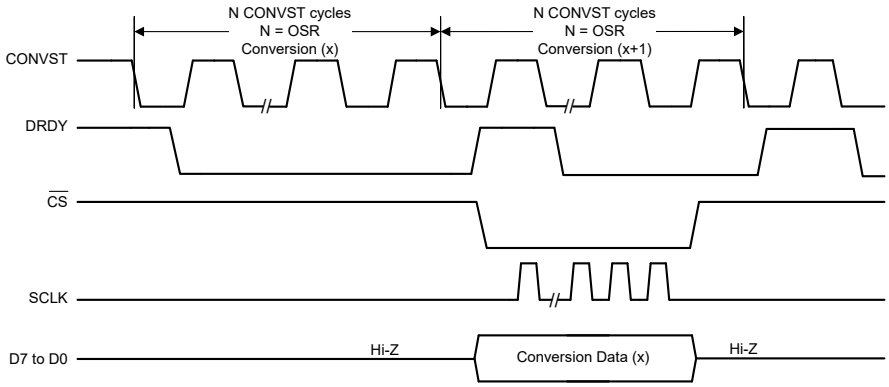


Figure 7-15. External Oversampling Clock

In the internal oversampling clock mode, ADC automatically triggers the conversion after the first CONVST falling edge. To use internal oversampling clock mode, set the INT_TRIG_MODE bit to 1b in the DIG_FILTER register in the ADS93x4C Common regbank. A rising edge transition, 0b to 1b, on the DIGITAL_FILT_SYSREF bit field of the DIGITAL_FILTER register is required for the oversampling filter to work properly (see the Figure 7-13).

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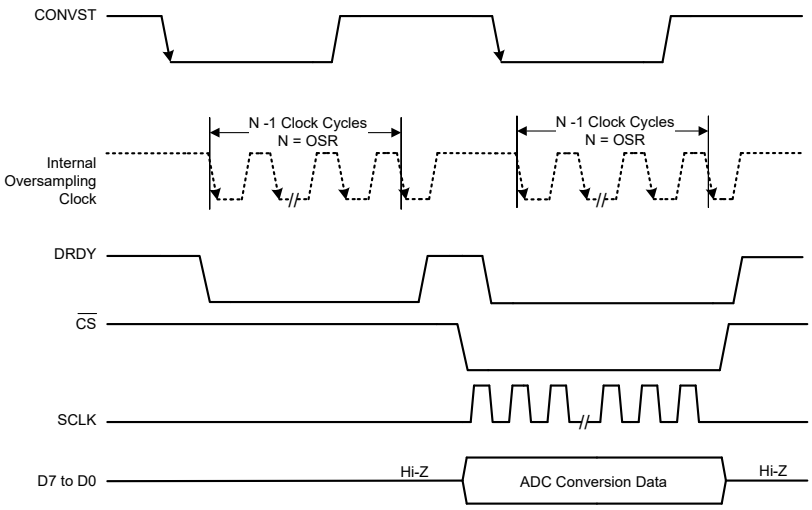


Figure 7-16. Internal Oversampling Clock

7.3.11.3 Moving Average Filter

The ADS9324C has a programmable simple moving average filter for each channel. The moving helps with reducing random white noise while maintaining the sharpest possible step response. The moving average filter length can be adjusted using MVG_AVG_LENGTH bit field in the DIGITAL_FILTER register. The maximum length of the moving average filter is 128. The frequency is mathematically described by Equation 6. Figure 7-17 shows moving average filter frequency response for length of 10. A SYSREF pulse is required after programming and configuring the moving average filter for the filter to work properly. Write 0b to 1b on the DIGITAL_FILT_SYSREF bit field in the DIGITAL_FILTER register (see the Figure 7-13).

$$H[f] = \frac{\sin(\pi f N)}{N \sin(\pi f)} \tag{6}$$

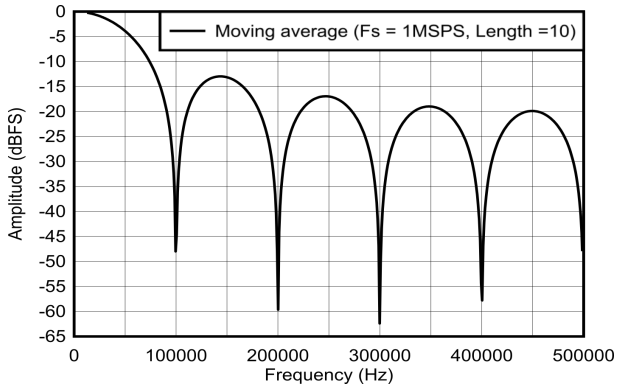
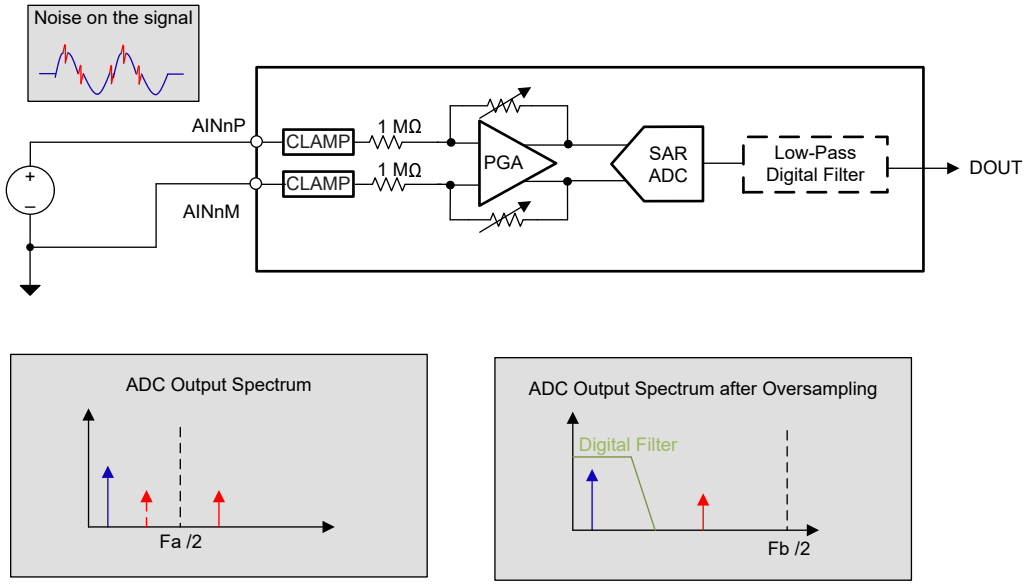


Figure 7-17. Frequency Response of Moving Average (Length =10)

7.3.11.4 Low-Pass FIR Filter

Each analog input channel of the features an integrated low-pass filter (LPF) at the output of the PGA for anti-aliasing. If the anti-aliasing provided by the analog low-pass filter is not sufficient, the user can utilize ADS93x4C on-chip digital filters to achieve desired anti-aliasing effect. The ADS93x4C on-chip digital filter oversamples the input signal and then uses a digital low-pass filter to attenuate the high-frequency noise on the signal (see the Figure 7-18). The ADS9324C has six selectable low-pass FIR filters. The FIR filter can be selected using FIR_FILT_SEL bit field in the DIGITAL_FILTER register as shown in the Table 7-8. A SYSREF pulse is required after programming the digital filter. Write 0b to 1b transition on the DIGITAL_FILT_SYSREF bit field in the DIGITAL_FILTER register (see the Figure 7-13).



Fa and Fb are sampling frequency of the ADC; Fb > Fa

Figure 7-18. Anti-aliasing using Low-Pass Digital Filter

Table 7-8. Low Pass FIR Filter Options

FILTER OPTION	FIR_FIL_SEL	DECIMATION	-3dB CUT-OFF FREQUENCY	GROUP DELAY (T_{CONVST})
FIR1	001b	2	0.218x F_{CONVST}	5
FIR2	010b	2	0.205x F_{CONVST}	3
FIR3	011b	4	0.108x F_{CONVST}	13
FIR4	100b	2	0.205x F_{CONVST}	3
FIR5	101b	Not supported.		
FIR6	110b	4	0.100x F_{CONVST}	9
FIR7	111b	8	0.540x F_{CONVST}	29

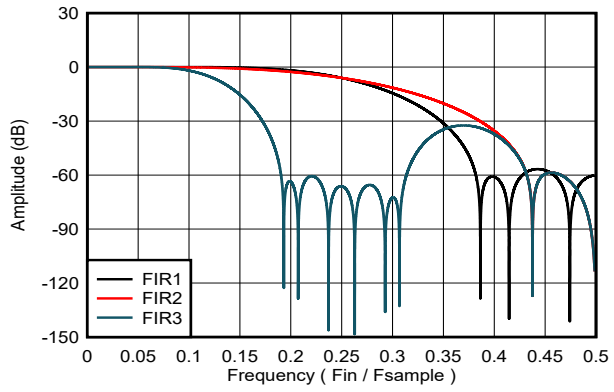


Figure 7-19. FIR1, FIR2 and FIR3 Filter Frequency Response

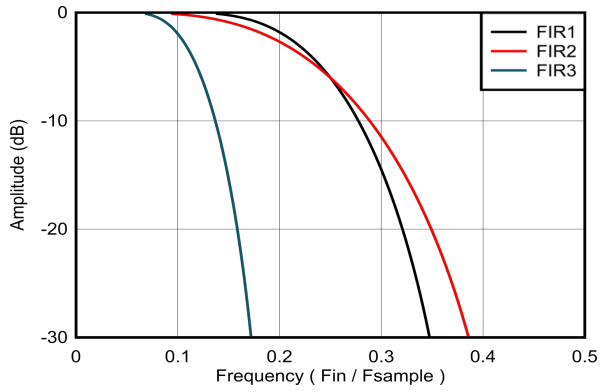


Figure 7-20. FIR1, FIR2 and FIR3 Filter Frequency Response, Pass-Band Detail

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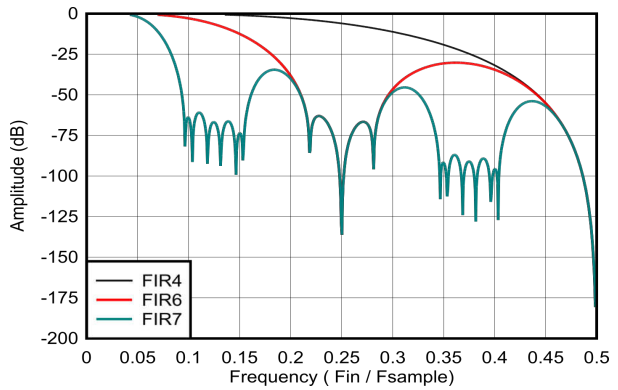

Figure 7-21. FIR4, FIR6 and FIR7 Filter Frequency Response

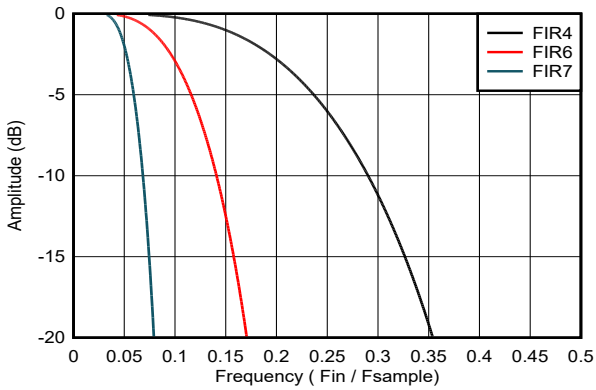

Figure 7-22. FIR4, FIR6 and FIR7 Filter Frequency Response, Pass-Band Detail

ADVANCE INFORMATION

7.3.12 Digital Window Comparator

The ADS93x4C has an 8-bit digital window comparator (DWC) for each input channel. Figure 7-23 shows the block diagram of the digital comparator. The low-side threshold, high-side threshold, and hysteresis parameters are independently programmable for each input channel. By default, hysteresis is 0, the high threshold is 127 (0x7F), and the low threshold is -128 (0x80). The DWC sets the DWC output to HIGH when the ADC output exceeds the high threshold or goes below the low threshold. The hysteresis field is an 8-bit field, and users can set the field to be from 0 to 255. The DWC also includes a glitch reject filter inside each DWC. The glitch reject filter is a 4-bit counter that counts if the ADC data exceeds the high or low thresholds for a consecutive number of ADC conversion clocks before asserting HIGH at the low and high comparator output. The glitch reject filter and user DWC reset bit are common for AIN1 to AIN8, and AIN9 to AIN16 channel groups. A rising edge transition on the DWC_RSTx user bit resets the digital window comparator flags.

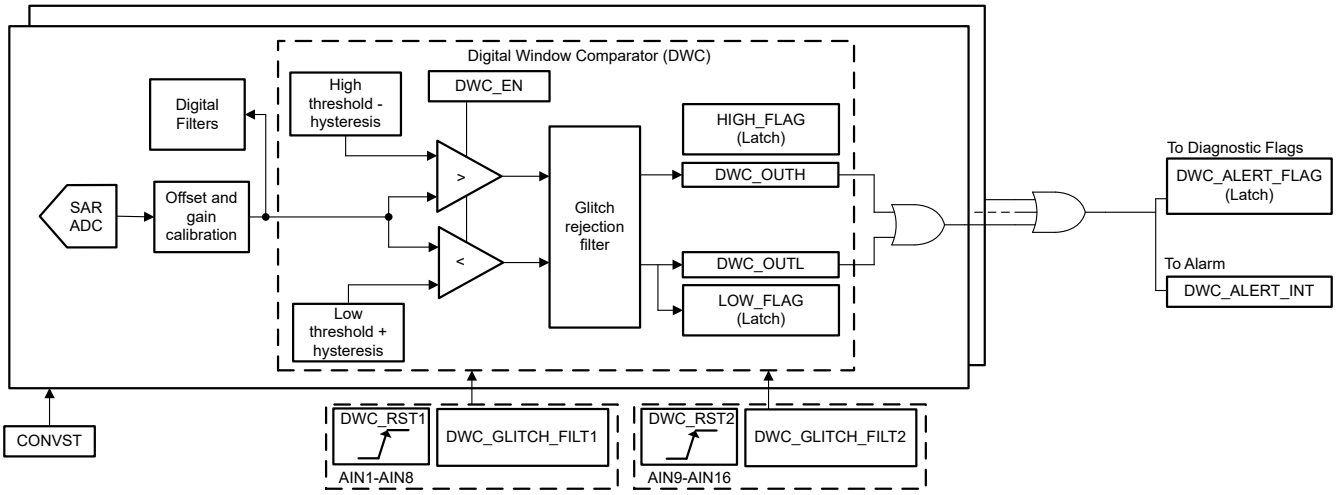

Figure 7-23. Digital Window Comparator Functional Block Diagram

To enable the digital window comparator, set the DWC_EN bit in the DWC_CFG registers in AIN1 - AIN8 Channel and AIN9 - AIN16 Channel regbank. High and low flag status of each window comparator can be read using DWC_FLAG_AIN1_8 and DWC_FLAG_AIN8_16 registers. By default, the glitch reject counter is set to 0000'b. In case of an event, the glitch reject filter counts the number of high or low threshold violations before setting HIGH and LOW flags. The DWC also provides interrupt output, DWC_ALERT_INT, which is ORed output of high and low comparators. DWC_ALERT_INT signal goes to ALARM pin, and can be provided as output on the DRDY/ALARM pin by configuring the ALARM pin (see the Section 7.3.13). The DWC_ALERT_INT can be programmed as a level based (ALRM_TYP = 0b) or a pulse output (ALRM_TYP = 1b). High or low alert interrupt signals can be selected by setting high or low thresholds to maximum or minimum values. The behavior of the digital comparator is illustrated in Figure 7-24 .

- If only HIGH_FLAG or HIGH_ALERT signals are required, program the LOW_TH_AINn to -128 (negative maximum value).
- If only LOW_FLAG or LOW_ALERT signals are needed, program the HIGH_TH_AINn to 127 (positive maximum value).

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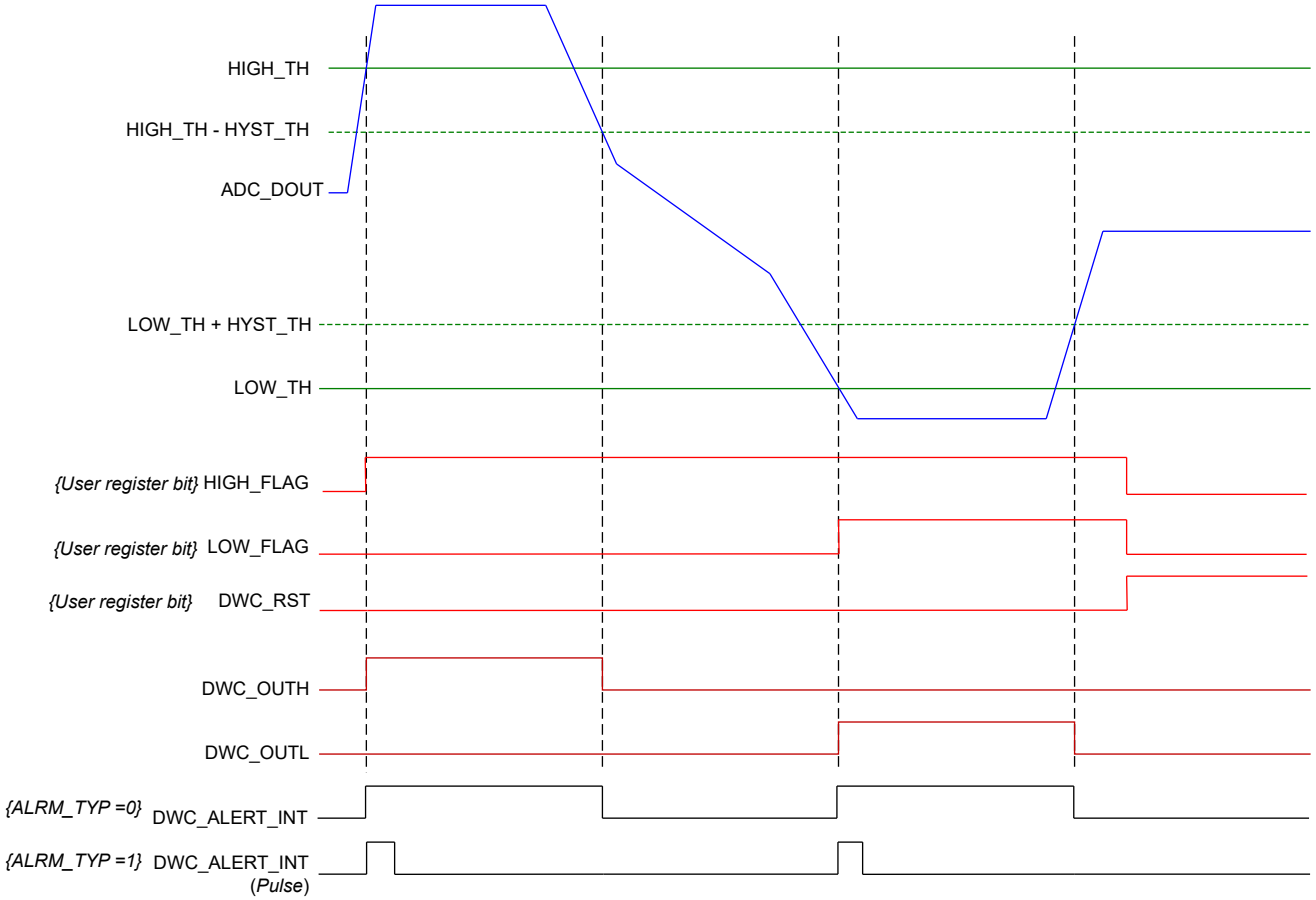

Figure 7-24. Digital Window Comparator Behavior

7.3.13 Alarm Modes

The ADS93x4C DRDY/ALARM is a multifunction pin, shown in theFigure 7-25. User can program the DRDY/ALARM pin to output DRDY, DWC_ALERT_INT, and ADC_CAL_DONE signals. By default, DRDY/ALARM operates as ADC data ready pin, DRDY. Table 7-9 shows ALARM_SEL values for different alarm modes. The ALARM is an active high pin by default, and can be programmed to active low by setting the ALRM_POL bit field to 1'b1 in the DRDY_ALARM_SEL register of the ADS93x4C Common register bank. DWC_ALERT_INT is by default a level-based interrupt, and can be programmed as pulse-based by setting ALRM_TYP to 1b. Pulse mode is only applicable for DWC_INT signal.

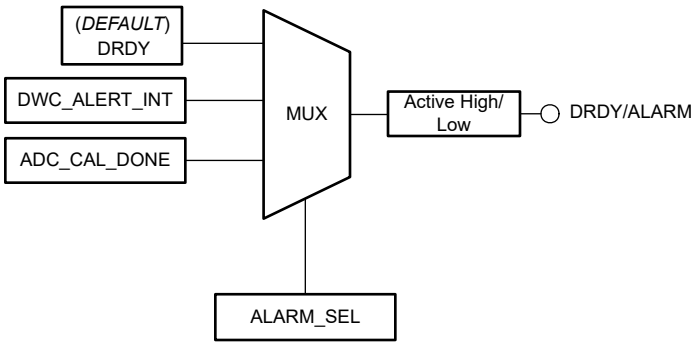

Figure 7-25. Alarm Functional Block Diagram

Table 7-9. Alarm Modes

ALARM_SEL[3:0]	ALARM NAME	DESCRIPTION
0000b	DRDY	ADC conversion done interrupt
0001b	DWC_ALERT_INT	DWC alert interrupt
0110b	ADC_CAL_DONE	ADC calibration done

ADVANCE INFORMATION

7.3.14 Data Interface

The ADS9324C supports 1-lane, 2-lane, 4-lane and 8-lane mode data read serial interface. Select the data interface as described in Table 7-10. The ADC supports 16-bit and 24-bit ADC data length. The ADC data length is configured using DOUT_LENGTH[1:0] field in the GEN_CFG3 register (0x0A). The 16-bit ADC conversion result is output MSB first in a 24-bit data packet and the last eight bits are zeroes when oversampling is disabled.

Use the registers in Table 7-10 to configure the data interface.

Table 7-10. Register Configurations For Data Interface Modes

INTERFACE MODE	FIGURE	DOUT_LANE_SEL[1:0] (ADDRESS = 0x0A)	ADC_DATA_SDOUT_EN (ADDRESS = 0x0A)
8-lane, D[7:0]	Figure 6-2	0	0
4-lane, D[7:4]	Figure 6-3	1	0
2-lane, D[7:6]	Figure 6-4	2	0
1-lane, D7	Figure 6-5	3	0
1-lane, SDOUT	Figure 6-5	3	1

7.3.14.1 ADC Channel Modes

ADS93x4C contains a digital feature to select number of ADC channels on the data interface. Table 7-11 shows the possible combinations supported in the device. In all modes, the lowest channel number gets transmitted first. Figure 7-26 shows an 8-channel ADC data read mode when ADC_CH_SEL = 0xxb.

Table 7-11. ADC Channel Modes

ADC_NUM_SEL	ADC_CH_SEL	ADC CHANNELS REPORTED	ADC OUTPUT
00b (Default)	xxxb	16 (Default)	AIN1, AIN2, AIN3, AIN4, AIN5, AIN6, AIN7, AIN8, AIN9, AIN10, AIN11, AIN12 AIN13, AIN14, AIN15, AIN16
01b	0xxb	8	AIN1, AIN2, AIN3, AIN4, AIN13, AIN14, AIN15, AIN16
01b	1xxb	8	AIN5, AIN6, AIN7, AIN8, AIN9, AIN10, AIN11, AIN12
10b	00xb	4	AIN1, AIN2, AIN15, AIN16
10b	01xb	4	AIN3, AIN4, AIN13, AIN14
10b	10xb	4	AIN5, AIN6, AIN11, AIN12
10b	11xb	4	AIN7, AIN8, AIN9, AIN10
11b	000b	2	AIN1, AIN16
11b	001b	2	AIN2, AIN15
11b	010b	2	AIN3, AIN14
11b	011b	2	AIN4, AIN13
11b	100b	2	AIN5, AIN12
11b	101b	2	AIN6, AIN11
11b	110b	2	AIN7, AIN10
11b	111b	2	AIN8, AIN9

Figure 7-26. 8 Channel ADC Data Read, ADC_NUM_SEL =01b, ADC_CH_SEL = 0xxb

Figure 7-27. 8 Channel ADC Data Read, ADC_NUM_SEL =01b, ADC_CH_SEL = 1xxb

7.3.14.2 Daisy Chain

Figure 7-28 shows a typical connection diagram with two devices in a daisy-chain topology.

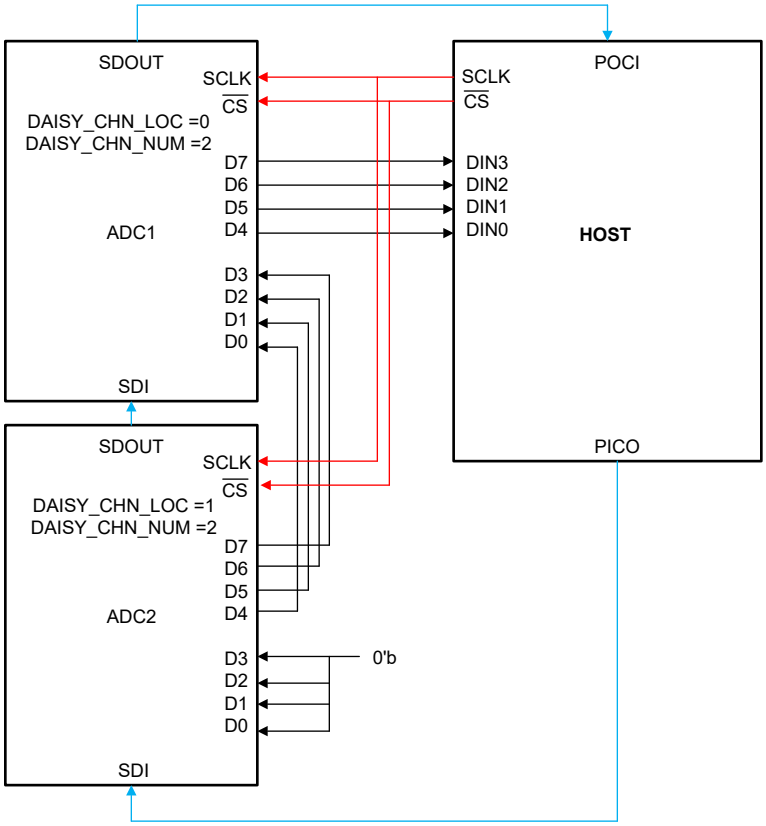

Figure 7-28. Daisy-Chain Connections for Configuration SPI

The $\overline{CS}$ and SCLK inputs of both ADCs are connected together and controlled by a single $\overline{CS}$ and SCLK pin of the controller, respectively. The SDI input pin of the bottom ADC in the chain (ADC2) is connected to the peripheral IN controller OUT (PICO) pin of the controller. Then, the SDO output pin of ADC2 is connected to the SDI input pin of ADC1. The SDO output pin of the top ADC in the chain (ADC1) is connected to the peripheral OUT controller IN (POCI) pin of the controller. The data on the PICO pin passes through ADC1 with a 32-SCLK delay, as long as $\overline{CS}$ is active. The register read and write requires 24-SCLK when daisy chain is not used. In daisy chain mode, register read and write requires 32-SCLK per ADC device. The MSB of the SPI commands are padded with zeros.

Daisy chain mode in ADS93x4C supports 1-lane, 2-lane, and 4-lane data transfer. Daisy chain is not supported with ADC data on SDOUT in 1-lane mode data transfer. Below are register configurations required to program the ADC in the daisy chain configuration.

1. Set the DAISY_CHN_NUM and DAISY_CHN_LOC bit field for all devices.
2. Set the number of lanes, DOUT_LANE_SEL, for all the devices. Number of lanes in the daisy chain configuration can only be 4, 2 and 1.
3. Program the DAISY_CHN_EN to 1b for the devices.

7.3.14.3 Diagnostic Flags

The diagnostic flag status is a 8-bit value, shown in the Table 7-12. The status bits can be reported out along with ADC data output, shown in the Figure 7-29. To enable diagnostic status bits, set the EN_STATUS_BITS bit field in the GEN_CFG register to 1b.

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Table 7-12. DIAG_FLAG Bit Field

DIAG_FLAG[7:0]	FIELD NAME	DESCRIPTION
7	Reserved	Reserved
6	DWC_ALERT_FLAG	ORed output all digital comparators ALERT_FLAG
5	Reserved	Reserved
4	Reserved	Reserved
3	Reserved	Reserved
2	Reserved	Reserved
1	Reserved	Reserved
0	RESET_DETECT_FLAG	Reset value of this bit is 1b. User program RESET_DETECT_FLAG to 0b after ADC power up. Any glitch that resulted in device reset, sets this bit to 1b.

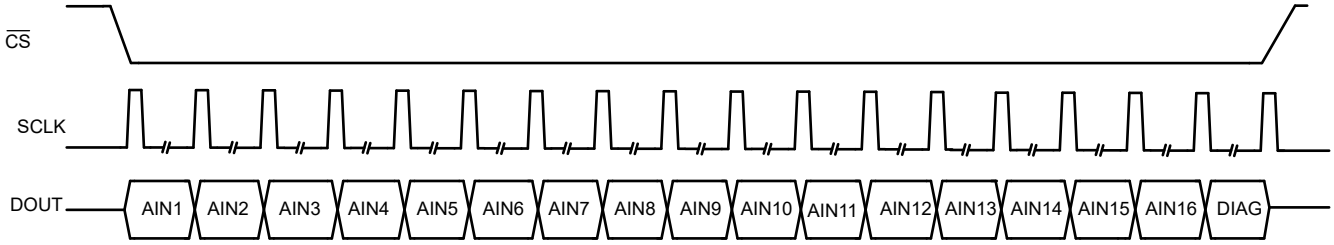

Figure 7-29. ADC Data Output Frame, DIAG_FLAG Enabled

7.3.14.4 ADC Output Data Randomizer

The ADS93x4C features a data output randomizer. When enabled, the ADC conversion result is bit-wise exclusive-ORed (XOR) with 8-bit pseudo-random binary sequence (PRBS) field, shown in the Figure 7-30. The PRBS bits can be appended to the ADC data output, shown in the Figure 7-32, Figure 7-33, Figure 7-34 and Figure 7-35. The XOR PRBS bits have equal probability of being either 1 or 0. As a result of the XOR operation, the data output from the ADS93x4C is randomized. The ground bounce created by the transmission of this randomized result over the data interface is uncorrelated with the analog input voltage. This uncorrelated transmission helps minimize interference between data transmission and analog performance of the ADC when the PCB layout does not minimize ground bounce.

Equation 7 and Equation 8 shows how to compute ADC conversion result from the ADC randomized output code when data output randomizer is enabled. Let's say the ADC randomized output value is 0x1234 and PRBS bits are 0x1f, the computed MASK_BITS value is 0x1fff and ADC conversion results is 0x1234 ^ 0x1fff. XOR mode is not supported for 24-bit ADC output frame.

$$\text{MASK\_BITS} = (\text{PRBS 8–bit Value}) \times 256 + (\text{PRBS0} \times 255) \tag{7}$$

$$\text{ADC Conversion Result} = (\text{ADC Randomized Code}) \ \hat{} \ (\text{MASK\_BITS}) \tag{8}$$

To enable the data output randomizer following register writes are required:

1. Write EN_XOR_PATT bit field of the GEN_CFG3 register to 1b.
2. Configure the XOR_CTL register: Program XOR_BIT_SEL to 1b, NUM_XOR_BITS to 11b, and XOR_MODE to 11b.

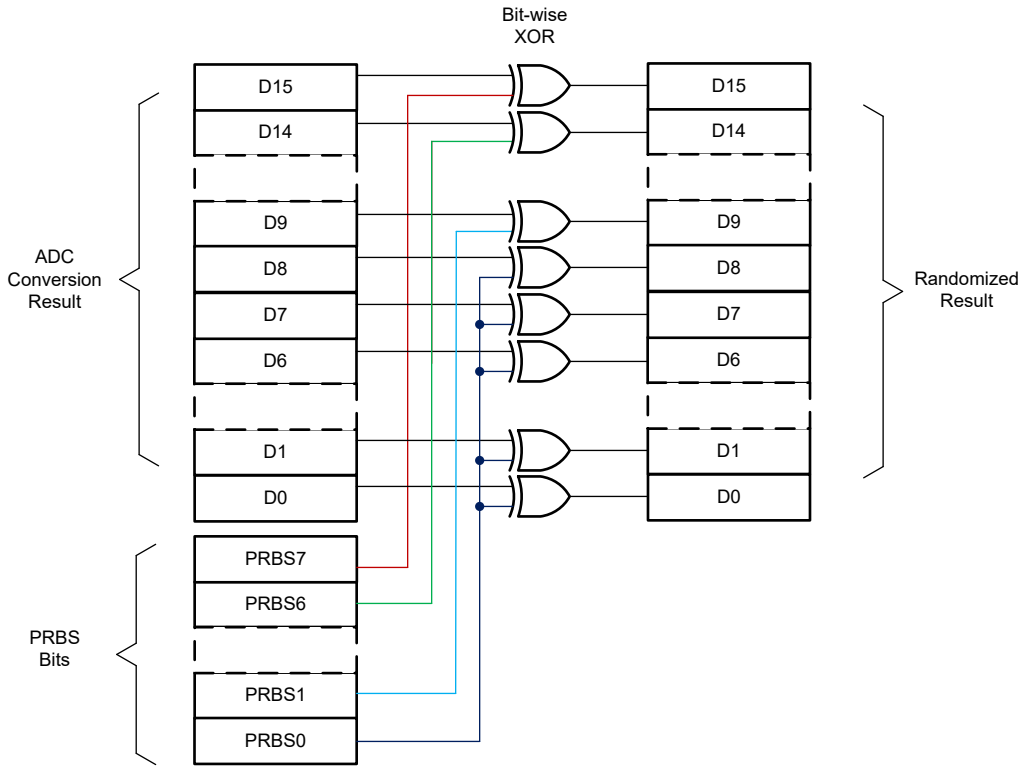

Figure 7-30. ADC Data Output Randomizer

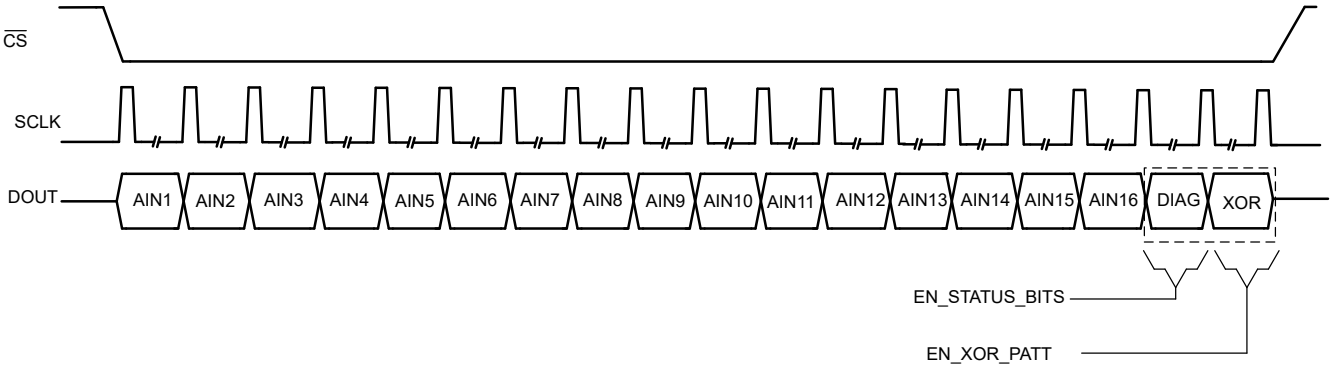

Figure 7-31. ADC Data Output Frame, DIAG_FLAG and XOR_PATT Enabled

ADVANCE INFORMATION

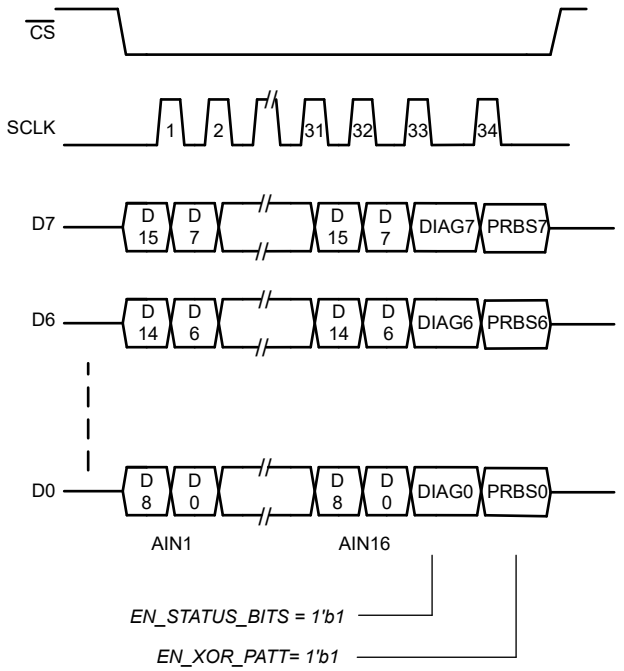

Figure 7-32. ADC Output Frame, 8-Lane Mode

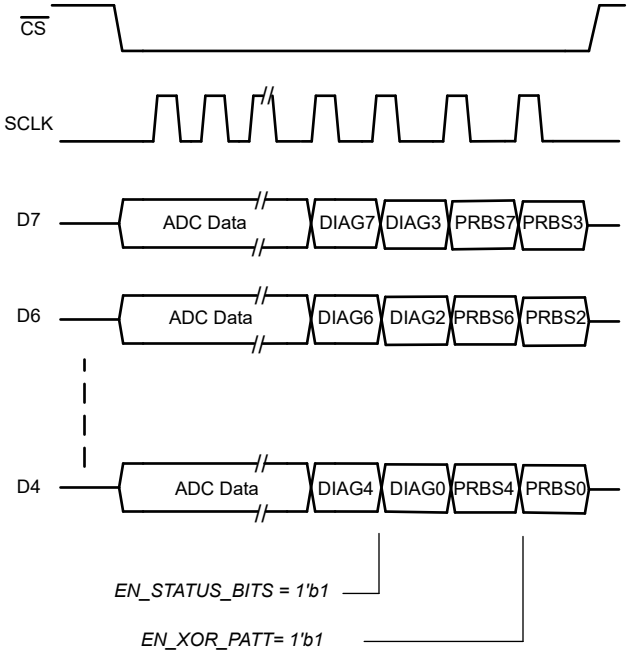

Figure 7-33. ADC Output Frame, 4-Lane Mode

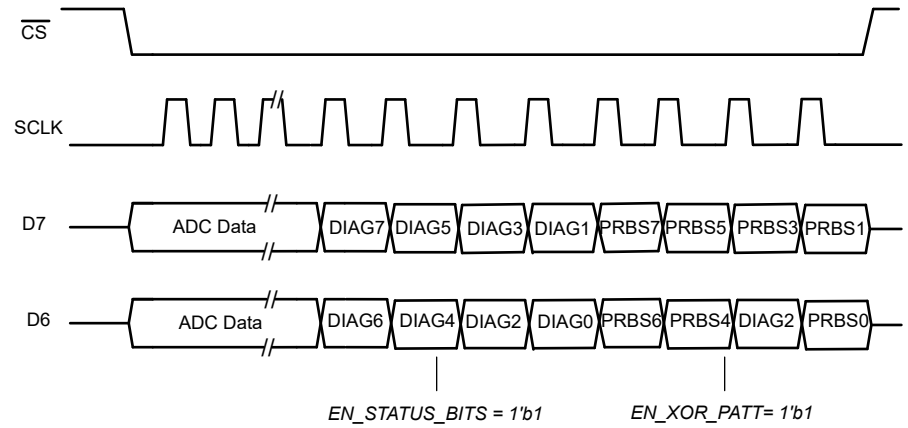

Figure 7-34. ADC Output Frame, 2-Lane Mode

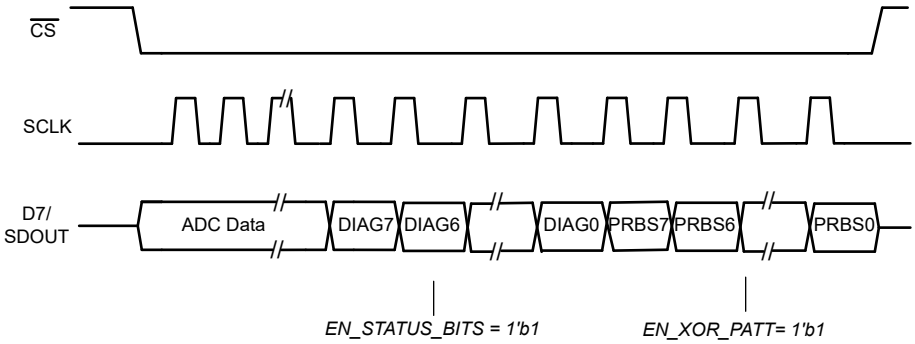

Figure 7-35. ADC Output Frame, 1-Lane Mode

7.3.14.5 Test Patterns for Data Interface

The test pattern is a 16-bit value that replaces the ADC output data MSB with predefined digital data. Enable the test patterns by configuring the TP_CFG register (0x2E) in theAIN1 - AIN8 Channel and AIN9 - AIN16 Channel register banks.

Table 7-13 lists the test patterns supported by the ADS93x4C.

Table 7-13. Test Pattern Configurations

TP_EN	TP_MODE[2:0]	TP_DIS_IDX	TP_UPD_MODE	ADC OUTPUT	RESULT (See the notes)
0	X	X	0	ADC conversion result	ADC conversion result
1	0	1	0	Fixed pattern	AIN1 = TP_AIN1, AIN2 = TP_AIN2, .., AIN15 = TP_15, AIN16 = TP_16.
1	0	0	0	Fixed pattern	AIN1 = 0x0000+TP_AIN1, AIN2 = 0x1000+TP_AIN2, .. , AIN15 = 0xE000+TP_15,AIN16 = 0xF000+TP_16.
1	1	1	0	Ramp pattern	Ramp pattern increments at channel frame boundary (see the Figure 7-36 and Figure 7-38).
1	2	1	1	Ramp pattern	Ramp pattern increment at sample frame boundary. AIN1=AIN2=AIN3.. =AIN8; AIN9=AIN10=AIN11.. =AIN16; See the Figure 7-37 and Figure 7-39

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Note

1. Configure the test patterns for two separate channel groups AIN1_8 and AIN9_16.
2. When using 24-bit ADC output, last 8-bits are zeros.
3. TP_AIN1 and TP_AIN16 control the ramp step for AIN1 to AIN8 and AIN9 to AIN16 respectively.
4. Ramp step is TP_AIN1 +1 and TP_AIN16 +1 for AIN1 to AIN8 and AIN9 to AIN16 respectively.

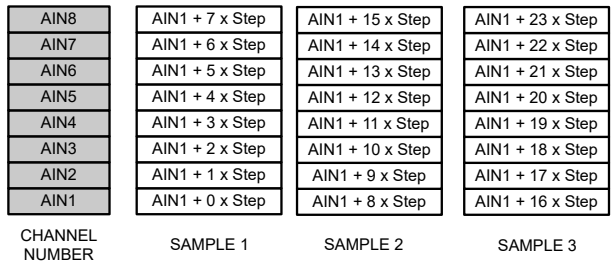

Figure 7-36. Digital Ramp Test Pattern, Increment at Channel Frame Boundary (TP_UPD_MODE =0)

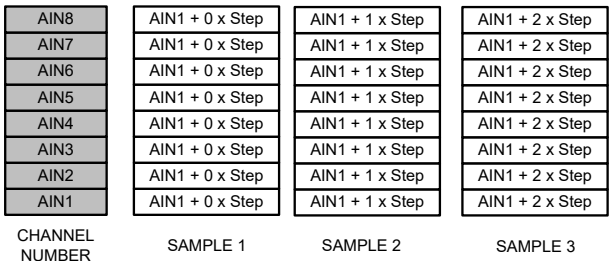

Figure 7-37. Digital Ramp Test Pattern, Increment at Sample Frame Boundary (TP_UPD_MODE =1)

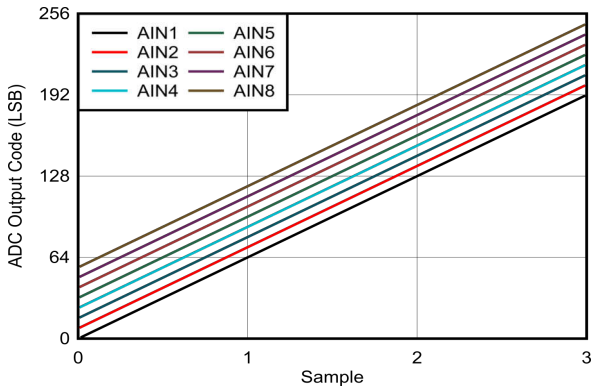

Figure 7-38. Ramp Test Pattern Example, Step = 8 (TP_AIN1 =7, TP_UPD_MODE =0)

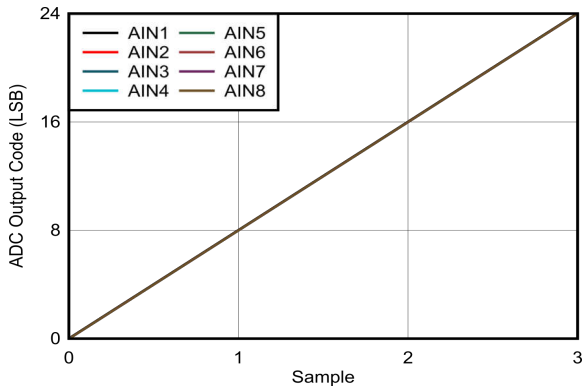

Figure 7-39. Ramp Test Pattern Example, Step = 8 (TP_AIN1 =7, TP_UPD_MODE =1)

7.3.14.6 Digital Output Drive Strength Control

The digital output drive strength can be adjusted using DRIVE_STRENGTH bit field in the GEN_CFG4 register of ADS93x4C Common register bank. See the Digital Output Drive Strength Control.

Table 7-14. Drive Strength Control

DRIVE_STRENGTH	DESCRIPTION
00b	Normal device operation
01b	0.5x Normal Operation
10b	2x Normal Operation
11b	1.5x Normal Operation

7.3.14.7 Digital Output Delay Adjustment

ADS93x4C includes a feature to add delay on ADC data output pins, SDOUT and D7, D5, D6, D5, D4, D3, D2, D1 and D0. Use DIG_DELAY_CFG1 and DIG_DELAY_CFG2 registers in the ADS93x4C Common register bank to program the delay.

7.4 Device Functional Modes

7.4.1 Reset

Reset the ADS9324C with a logic 0 on the $\overline{\text{RESET}}$ pin or write 1b to the SW_RST bit field of address 0x01 in the ADS93x4C Common register bank. The device registers are initialized to the default values after reset and the device is initialized with a sequence of register write operations.

The $\overline{\text{RESET}}$ pin is an active-low digital input. A dedicated reset pin allows the device to be reset at any time in an asynchronous manner. All digital circuitry in the device is reset when the $\overline{\text{RESET}}$ pin is set to logic low and this condition remains active until the pin returns high.

7.4.2 Normal Operation

After the ADS9324C is powered-up, the ADS9324C converts analog input voltages to digital output voltages at the falling edge of CONVST signal. A minimum delay time, t_{PU}, is needed after device reset (see the Section 6.7).

7.4.3 Standby Mode

The device supports a low-power standby mode in which only part of the circuit is powered down. The analog front-end, signal-conditioning circuit for each channel and the internal reference is powered down in this mode. In standby mode, the total power consumption of the device is typically equal to 6.5mW. To put the device in the low-power standby mode, set the DEVICE_PDN bit field of the PDN_CTL register to 1b.

7.4.4 Programming

7.4.4.1 Register Write Operation

The ADS9324C 16-bit registers are grouped in 3 register banks, ADS93x4C Common, AIN1 - AIN8 Channel, and AIN9 - AIN16 Channel, and are addressable with an 8-bit register address. ADS93x4C Common register bank is selected for read or write operation by writing 0x0001 to BANK_SEL register, address 0x02. PAGE_SEL register, address 0x2, is unique among all register banks, and always accessible irrespective PAGE_SEL bits. A 24-bit serial communication frame is required to write data to configuration registers. The 24-bit register read frame consists of an 8-bit register address and new 16-bit register value. The data on SDI is latched on the rising edge of SCLK. The write command is decoded on the $\overline{CS}$ rising edge and the specified register is updated with the 16-bit data specified in the register write operation. The 24-bit SPI frame for a register write is shown in Figure 7-40, and the steps required to write a register are described in Table 7-15.

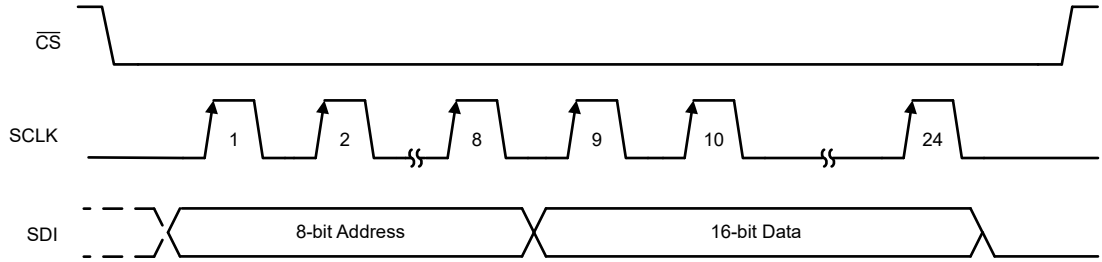

Figure 7-40. Register Write Frame

Table 7-15. Register Write Sequence

FRAME NUMBER	SDI[23:0]		DESCRIPTION
	SDI[23:16] = REG_ADDR	SDI[15:0] = REG_ADDR DATA	
1	0x02	0x0001	Selects register bank 0. For register bank 1 and 2, write 0x02 and 0x04 respectively.
2	REG_ADDR	REG_ADDR DATA	Writes user data to the desired address. Repeat this step for the required number of register writes.

7.4.4.2 Register Read Operation

The register banks for register read operation is selected using BANK_SEL register, address 0x02. To read registers in ADS93x4C Common register bank, write 0x0001, to the BANK_SEL register. Similarly, write 0x0002 and 0x0004 to BANK_SEL register, to read registers in AIN1 - AIN8 Channel and AIN9 - AIN16 Channel banks respectively. As illustrated in Figure 7-41, 24-bit SPI frames are required to read registers.Figure 7-41 describes the sequence required to read a N number of registers in a register bank, and the steps required are described in Table 7-16.

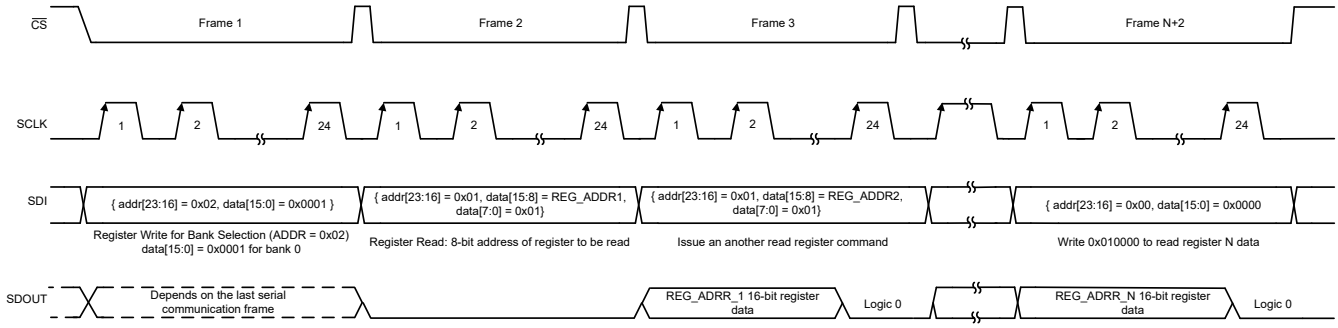

Figure 7-41. Register Read

Table 7-16. Register Read Sequence

FRAME NUMBER	24-bit SDI frame		SDOUT[23:0]	DESCRIPTION
	SDI[23:16]	SDI [15:0]		
1	0x02	0x0001 for register bank 0, 0x0002 for register bank 1, 0x0004 for register bank 2	X	Selects the register bank.
2	0x01	SDIN[15:8] = REG_ADDR1, SDIN[7:0] = 0x01	0x000000	Register read operation for register address REG_ADDR1. The register data, REG_ADDR1, is received in the next serial communication frame.
3	0x01	SDIN[15:8] = REG_ADDR1, SDIN[7:0] = 0x01	SDOUT[23:8] = REG_ADDR1 DATA, SDOUT[7:0]= 0x00	Register read operation for register address REG_ADDR2. The register data, REG_ADDR1, is received in this frame. The register data, REG_ADDR2, is received in the next serial communication frame.
N+2	0x00	0x0000	SDOUT[23:8]= REG_ADDRN DATA, SDOUT[7:0]= 0x00	Write 0x000000 to the SDIN to read register value, address REG_ADDR, selected in the previous serial communication frame.

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7.4.4.3 Initialization Example - DOUT Lane Configuration

By default, ADC output interface is configured in 8-lane mode with 16-bit ADC output size. Table 7-17 shows device initialization settings for 1-lane mode ADC data read using SDOUT.

Table 7-17. ADS9324C Initialization Sequence for 1-Lane Mode

STEP NUMBER	REGISTER		DESCRIPTION
	SDI[23:16] = REG_ADDR	SDI[15:0] = REG_ADDR DATA	
1	Wait 30ms		Power supply and voltage reference settling
2	0x01	0x0002	Software reset (optional)
3	Wait 1ms (optional)		Optional delay
4	0x02	0x0001	Select ADS93x4C Common regbank
5	0x0A	0x0032	User programs this register based on system requirements. 0x0032 selects ADC conversion data size of 16b, and 1-lane mode data output on SDOUT pin.

7.4.4.4 Initialization Example - Digital Filter

Table 7-18 shows device initialization example for block average filter with OSR of 2.

Table 7-18. ADS9324C Initialization Example for External Clock Oversampling

STEP NUMBER	REGISTER		DESCRIPTION
	SDI[23:16] = REG_ADDR	SDI[15:0] = REG_ADDR DATA	
1	Wait 30ms		Power supply and voltage reference settling
2	0x01	0x0002	Software reset (optional)
3	Wait 1ms (optional)		Optional delay
4	0x02	0x0001	Select ADS93x4C Common regbank
5	0x14	0x0010	User programs this based on oversampling requirements. 0x0010 selects block average filter with OSR factor of 2.
6	0x14	0x0011	Write 0b to 1b on the DIGITAL_FILT_SYSREF bit field in the DIGITAL_FILTER register.
7	Enable CONVST		Enable a free running CONVST clock or set the CONVST from HIGH to LOW, and LOW to HIGH.
8	$t_{wait} > t_{CONVST}$		Add a delay > t_{CONVST}.
9	0x14	0x0010	Set DIGITAL_FILT_SYSREF to 0b.

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7.4.4.5 Initialization Example - Common Mode Error Correction

Table 7-17 shows device initialization settings when using CMRR error correction feature.

Table 7-19. ADS9324C Initialization Example for Common Mode Error Correction

STEP NUMBER	REGISTER		DESCRIPTION
	SDI[23:16] = REG_ADDR	SDI[15:0] = REG_ADDR DATA	
1	Wait 30ms		Power supply and voltage reference settling
2	0x01	0x0002	Software reset (optional)
3	Wait 1ms (optional)		Optional delay
4	0x02	0x0002	Select AIN1 - AIN8 Channel regbank.
5	0x08	0x8080	Enable common mode error correction for AIN1 to AIN8.
6	0x09	0x8080	
7	0x0A	0x8080	
8	0x0B	0x8080	
9	0x02	0x0004	Select AIN9 - AIN16 Channel regbank.
10	0x08	0x8080	Enable common mode error correction for AIN9 to AIN16.
11	0x09	0x8080	
12	0x0A	0x8080	
13	0x0B	0x8080	
14	0x02	0x0001	Select ADS93x4C Common regbank.
15	0x14	0x0010	0x0010 selects block average filter with OSR factor of 2. When using moving average filter, set the length to at least 2. Or, use any FIR filters.
16	0x14	0x0011	Write 0b to 1b on the DIGITAL_FILT_SYSREF bit field in the DIGITAL_FILTER register.
17	Enable CONVST		Enable a free running CONVST clock or set the CONVST from HIGH to LOW, and LOW to HIGH.
18	$t_{wait} > t_{CONVST}$		Add a delay > t_{CONVST}.
19	0x14	0x0010	Set DIGITAL_FILT_SYSREF to 0b.

7.4.4.6 Initialization Example - ADC Calibration

Table 7-20 and Table 7-21 show ADC_CAL initialization example in single-shot and continuous CONVST modes.

Table 7-20. ADS9324C Initialization Example for ADC_CAL Module Single-shot

STEP NUMBER	REGISTER		DESCRIPTION
	SDI[23:16] = REG_ADDR	SDI[15:0] = REG_ADDR DATA	
1	Wait 30ms		Power supply and voltage reference settling
2	0x01	0x0002	Software reset (optional)
3	Wait 1ms (optional)		Optional delay
4	0x02	0x0001	Select ADS93x4C Common regbank
5	0x14	0x0002	Set the INT_TRIG_MODE to 1b
6	0x12	0x0003	Write ADC_CAL_MODE to 11b for offset and gain calibration. If the PGA inputs are configured in single-ended mode, set the SE_DIFF_M ODE_AINn to 1b by writing 0x12 to 0x3003.
7	0x12	0x0103	Write 0b to 1b for a rising edge transition on the ADC_CAL_TRIG bit. If the PGA inputs are configured in single-ended mode, set the 0x12 to 0x3103.
8	CONVST falling edge		Set the CONVST from HIGH to LOW. At least one falling edge of CONVST must be provided. End state of the CONVST must be high.
9	Wait 10µs		Add a 10µs delay.
10	0x12	0x0003	rite 0b to the ADC_CAL_TRIG bit. If the PGA inputs are configured in single-ended mode, set the 0x12 to 0x3003.
11	Wait 125ms		Wait for 125ms or poll CALIB_BUSY flag to determine when calibration is complete. User can now operate the ADC in normal operation.

Table 7-21. ADS9324C Initialization Example for ADC_CAL Module With Continuous CONVST

STEP NUMBER	REGISTER		DESCRIPTION
	SDI[23:16] = REG_ADDR	SDI[15:0] = REG_ADDR DATA	
1	Wait 30ms		Power supply and voltage reference settling
2	0x01	0x0002	Software reset (optional)
3	Wait 1ms (optional)		Optional delay
	Enable CONVST signal		A free running CONVST clock is provided to the ADC.
4	0x02	0x0001	Select ADS93x4C Common regbank
5	0x14	0x0002	Set the INT_TRIG_MODE to 1b
6	0x12	0x0003	Write ADC_CAL_MODE to 11b for offset and gain calibration. If the PGA inputs are configured in single-ended mode, set the SE_DIFF_M ODE_AINn to 1b by writing 0x12 to 0x3003.
7	0x12	0x0103	Write 0b to 1b for a rising edge transition on the ADC_CAL_TRIG bit. If the PGA inputs are configured in single-ended mode, set the 0x12 to 0x3103.
8	Wait t_{CONVST}		At least one falling edge of CONVST must be provided.
10	0x12	0x0003	Write 0b to the ADC_CAL_TRIG bit. If the PGA inputs are configured in single-ended mode, set the 0x12 to 0x3003.

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Table 7-21. ADS9324C Initialization Example for ADC_CAL Module With Continuous CONVST (continued)

STEP NUMBER	REGISTER		DESCRIPTION
	SDI[23:16] = REG_ADDR	SDI[15:0] = REG_ADDR DATA	
11	Wait 100,000 t_{CONVST}		Wait for 100,000 CONVST clock cycles or poll CALIB_BUSY flag to determine when calibration is complete. User can now operate the ADC in normal operation.

7.4.4.7 Initialization Example - Test Pattern Mode

Table 7-22 shows device initialization settings for constant test pattern output on AIN1.

Table 7-22. ADS9324C Initialization Example for Test Pattern Mode

STEP NUMBER	REGISTER		DESCRIPTION
	SDI[23:16] = REG_ADDR	SDI[15:0] = REG_ADDR DATA	
1	Wait 30ms		Power supply and voltage reference settling
2	0x01	0x0002	Software reset (optional)
3	Wait 1ms (optional)		Optional delay
4	0x02	0x0002	Select AIN1 - AIN8 Channel regbank
5	0x2F	0xAAAA	Program AIN1 constant test pattern to 0xAAAA.
6	0x2E	0x0001	Enables constant test pattern output for AIN1 to AIN8. By default, AIN2 to AIN8 test pattern is 0. User reads 0xAAAA data for AIN1, and 0x0000 for AIN2 to AIN8.

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8 Register Maps

8.1 ADS93xx Common Registers

Table 8-1 lists the memory-mapped registers for the ADS93xx Common registers. All register offset addresses not listed in Table 8-1 should be considered as reserved locations and the register contents should not be modified.

Table 8-1. ADS93xx_Common

Address	Acronym	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x01	GEN_CFG1	REG_RD_ADD[7:0]							
		RESERVED						SW_RST	REG_RD_EN
0x02	BANK_SEL	RESERVED							
		RESERVED					BANK_SEL[2:0]		
0x07	DIAG_CTRL	RESERVED							RESET_DETECT_FLAG
		RESERVED							
0x08	PDN_CTL	RESERVED							
		RESERVED							DEVICE_PDN
0x09	GEN_CFG2	RESERVED				DAISY_CHN_LOC[3:0]			
		DAISY_CHN_NUM_DEV[3:0]				RESERVED			DAISY_CHN_EN
0x0A	GEN_CFG3	RESERVED			EN_OFS_BINARY	RESERVED		EN_XOR_PATT	EN_DIAG_FLAG
		RESERVED		DOUT_LANE_SEL[1:0]		DOUT_LENGTH[1:0]		ADC_DATA_SDOUT_EN	RESERVED
0x0B	XOR_BITS_CTL	RESERVED							
		XOR_MODE[1:0]		NUM_XOR_BITS[1:0]		RESERVED			XOR_BIT_SEL
0x0C	DRDY_ALARM_SEL	ALRM_MASK[7:0]							
		RESERVED		ALRM_TYPE	ALRM_POL	DRDY_ALRM_SEL[3:0]			
0x0D	GEN_CFG4	RESERVED							
		RESERVED		ALRM_DIS	RESERVED	DIG_DELAY_EN	RESERVED	DRIVE_STRENGTH[1:0]	
0x0E	DIG_DELAY_CFG1	RESERVED	DIG_DELAY_SDOUT[2:0]			DIG_DELAY_D3[2:0]			DIG_DELAY_D2[2:0]
		DIG_DELAY_D2[2:0]		DIG_DELAY_D1[2:0]			DIG_DELAY_D0[2:0]		
0x0F	DIG_DELAY_CFG2	RESERVED				DIG_DELAY_D7[2:0]			DIG_DELAY_D6[2:0]
		DIG_DELAY_D6[2:0]		DIG_DELAY_D5[2:0]			DIG_DELAY_D4[2:0]		
0x10	ANA_CFG1	RESERVED							
		RESERVED						REFSEL_CTRL_DIS	EXT_REF_EN
0x11	ANA_CFG2	CH_XTALK_LOW_SPEED	RESERVED						
		RESERVED	ADC_CH_SEL[2:0]			ADC_NUM_SEL[1:0]		RESERVED	
0x12	ADC_CAL	RESERVED		SE_DIFF_MODE_AIN1_8	SE_DIFF_MODE_AIN9_16	RESERVED			ADC_CAL_TRIG
		RESERVED						ADC_CAL_MODE[1:0]	
0x14	DIG_FILTER	PHASE_DELAY_EN	FIR_FILT_SEL[2:0]			MVG_AVG_LEN[3:0]			
		BLK_AVG_OSR[3:0]				RESERVED		INT_TRIG_MODE	DIG_FILT_SYSREF
0x15	GEN_CFG5	RESERVED							
		RESERVED				T_MODE_OVR_EN	T_MODE	AVG_MODE_OVR_EN	AVG_MODE
0x1E	DEVICE_STATUS	RESERVED							
		RESERVED			CALIB_BUSY_FLAG	RESERVED			

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Table 8-1. ADS93xx_Common (continued)

Address	Acronym	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x21	DEVICE_ID	RESERVED							
		DEVICE_ID[7:0]							

Complex bit access types are encoded to fit into small table cells. Table 8-2 shows the codes that are used for access types in this section.

Table 8-2. ADS93xx Common Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.1.1 GEN_CFG1 Register (Address = 0x01) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-1. GEN_CFG1 Register

15	14	13	12	11	10	9	8
REG_RD_ADD[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
RESERVED						SW_RST	REG_RD_EN
R/W-000000b						R/W-0b	R/W-0b

Table 8-3. GEN_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	REG_RD_ADD[7:0]	R/W	00000000b	Register read address
7:2	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
1	SW_RST	R/W	0b	Writing 1b to this bit reset the device.
0	REG_RD_EN	R/W	0b	Register read enable. This bit must be 1b for every register read SPI frame.

8.1.2 BANK_SEL Register (Address = 0x02) [Reset = 0x0001]

Return to the Summary Table.

Figure 8-2. BANK_SEL Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0000000000000b							
7	6	5	4	3	2	1	0
RESERVED						BANK_SEL[2:0]	
R/W-0000000000000b						R/W-001b	

Table 8-4. BANK_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:3	RESERVED	R/W	0000000000000b	Reserved. Do not change from the default reset value.

Table 8-4. BANK_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	BANK_SEL[2:0]	R/W	001b	Register bank selection. 001b = Common Registers 010b = Channel Registers AIN1 - AIN8 100b = Channel Registers AIN9 - AIN16

8.1.3 DIAG_CTRL Register (Address = 0x07) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-3. DIAG_CTRL Register

15	14	13	12	11	10	9	8
RESERVED							RESET_DETECT_FLAG
R-0000000b							R/W-0b
7	6	5	4	3	2	1	0
RESERVED							
R-00000000b							

Table 8-5. DIAG_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	RESERVED	R	0000000b	
8	RESET_DETECT_FLAG	R/W	0b	Indicates reset of the device, User writes this bit to 0b. If the ADC undergoes reset, the bit is set to 1b. This bit can be read on the SDOUT status bits.
7:0	RESERVED	R	00000000b	

8.1.4 PDN_CTL Register (Address = 0x08) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-4. PDN_CTL Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
RESERVED							DEVICE_PDN
R/W-0000000000000000b							R/W-0b

Table 8-6. PDN_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	RESERVED	R/W	0000000000000 00b	Reserved. Do not change from the default reset value.
0	DEVICE_PDN	R/W	0b	Device power down control. 0b = Normal operation 1b = Device is powered down.

8.1.5 GEN_CFG2 Register (Address = 0x09) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-5. GEN_CFG2 Register

15	14	13	12	11	10	9	8
RESERVED				DAISY_CHN_LOC[3:0]			
R/W-0000b				R/W-0000b			
7	6	5	4	3	2	1	0
DAISY_CHN_NUM_DEV[3:0]				RESERVED			DAISY_CHN_EN
R/W-0000b				R/W-000b			R/W-0b

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Figure 8-5. GEN_CFG2 Register (continued)

Table 8-7. GEN_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0000b	Reserved. Do not change from the default reset value.
11:8	DAISY_CHN_LOC[3:0]	R/W	0000b	Location of the device in the daisy chain configuration.
7:4	DAISY_CHN_NUM_DEV[3:0]	R/W	0000b	Total number of devices in the daisy chain configuration.
3:1	RESERVED	R/W	000b	Reserved. Do not change from the default reset value.
0	DAISY_CHN_EN	R/W	0b	Daisy chain configuration enable. 0b = Daisy chain configuration disabled 1b = Daisy chain configuration enabled

8.1.6 GEN_CFG3 Register (Address = 0x0A) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-6. GEN_CFG3 Register

15	14	13	12	11	10	9	8
RESERVED			EN_OFS_BINARY	RESERVED		EN_XOR_PATT	EN_DIAG_FLAG
R/W-000b			R/W-0b	R/W-00b		R/W-0b	R/W-0b
7	6	5	4	3	2	1	0
RESERVED		DOUT_LANE_SEL[1:0]		DOUT_LENGTH[1:0]		ADC_DATA_SDOUT_EN	RESERVED
R/W-00b		R/W-00b		R/W-00b		R/W-0b	R/W-0b

Table 8-8. GEN_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R/W	000b	Reserved. Do not change from the default reset value.
12	EN_OFS_BINARY	R/W	0b	ADC conversion data output format selection. 0b = Two's complement 1b = Offset binary
11:10	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
9	EN_XOR_PATT	R/W	0b	Enables XOR operation on the ADC conversion result.
8	EN_DIAG_FLAG	R/W	0b	Status bits after the ADC conversion data output enable. 0b = XOR operation is disabled 1b = Bit-wise XOR operation on ADC conversion result is enabled
7:6	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
5:4	DOUT_LANE_SEL[1:0]	R/W	00b	Data lane selection. 00b = 8 lanes 01b = 4 lanes 10b = 2 lanes 11b = 1 lane
3:2	DOUT_LENGTH[1:0]	R/W	00b	ADC data size selection 00b = 16-bit 01b = Reserved 10b = 24-bit
1	ADC_DATA_SDOUT_EN	R/W	0b	ADC data output on SDOUT pin enable in single lane mode. 0b = ADC data output on D7 1b = ADC data output on SDOUT pin
0	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.

8.1.7 XOR_BITS_CTL Register (Address = 0x0B) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-7. XOR_BITS_CTL Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-00000000b							
7	6	5	4	3	2	1	0
XOR_MODE[1:0]		NUM_XOR_BITS[1:0]		RESERVED			XOR_BIT_SEL

Figure 8-7. XOR_BITS_CTL Register (continued)

R/W-00b	R/W-00b	R/W-000b	R/W-0b

Table 8-9. XOR_BITS_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED	R/W	00000000b	Reserved. Do not change from the default reset value.
7:6	XOR_MODE[1:0]	R/W	00b	Set the XOR_MODE to 3.
5:4	NUM_XOR_BITS[1:0]	R/W	00b	Select the number of XOR bits for ADC output randomizer. Set this bit field to 3.
3:1	RESERVED	R/W	000b	Reserved. Do not change from the default reset value.
0	XOR_BIT_SEL	R/W	0b	Set this bit 1b for PRBS bits.

8.1.8 DRDY_ALARM_SEL Register (Address = 0x0C) [Reset = 0x0000]

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Figure 8-8. DRDY_ALARM_SEL Register

15	14	13	12	11	10	9	8
ALRM_MASK[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
RESERVED		ALRM_TYPE	ALRM_POL	DRDY_ALRM_SEL[3:0]			
R/W-00b		R/W-0b	R/W-0b	R/W-0000b			

Table 8-10. DRDY_ALARM_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	ALRM_MASK[7:0]	R/W	00000000b	Alarm mask selection. Each bit controls mask for every alarm modes when ORed output of each alarm is selected on ALARM pin.
7:6	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
5	ALRM_TYPE	R/W	0b	Alarm type selection. Applicable only for DWC. 0b = Level based 1b = Pulse based
4	ALRM_POL	R/W	0b	DRDY/ALARM polarity selection. 0b = Active high 1b = Active low
3:0	DRDY_ALRM_SEL[3:0]	R/W	0000b	DRDY/ALARM selection. 0000b = ADC data ready flag (DRDY) 0001b = DWC output 0010b = Reserved 0011b = Reserved 0100b = Reserved 0101b = Reserved 0110b = ADC_CAL done flag (ADC_CAL_DONE) 0111b = Reserved 1000b = ORed of all above flags with individual mask before ORing

8.1.9 GEN_CFG4 Register (Address = 0x0D) [Reset = 0x0000]

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Figure 8-9. GEN_CFG4 Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0000000000b							
7	6	5	4	3	2	1	0
RESERVED		ALRM_DIS	RESERVED	DIG_DELAY_EN	RESERVED	DRIVE_STRENGTH[1:0]	
R/W-0000000000b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-00b	

Table 8-11. GEN_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:6	RESERVED	R/W	0000000000b	Reserved. Do not change from the default reset value.

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Table 8-11. GEN_CFG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	ALRM_DIS	R/W	0b	Alarm function disable. 0b = Enabled 1b = Disabled
4	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
3	DIG_DELAY_EN	R/W	0b	Control for digital delay on the output buffer path. 0b = Normal device operation. 1b = Digital delay on the output buffer path is enabled. The magnitude is controlled by DIG_DELAY_CFG1 and DIG_DELAY_CFG2.
2	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
1:0	DRIVE_STRENGTH[1:0]	R/W	00b	Control to configure the drive strength of the digital output buffer.. 00b = Normal device operation 01b = 0.5x drive strength 10b = 2x drive strength 11b = 1.5x drive strength

8.1.10 DIG_DELAY_CFG1 Register (Address = 0x0E) [Reset = 0x0000]

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Figure 8-10. DIG_DELAY_CFG1 Register

15	14	13	12	11	10	9	8
RESERVED	DIG_DELAY_SDOUT[2:0]			DIG_DELAY_D3[2:0]			DIG_DELAY_D2[2:0]
R/W-0b	R/W-000b			R/W-000b			R/W-000b
7	6	5	4	3	2	1	0
DIG_DELAY_D2[2:0]			DIG_DELAY_D1[2:0]			DIG_DELAY_D0[2:0]	
R/W-000b			R/W-000b			R/W-000b	

Table 8-12. DIG_DELAY_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
14:12	DIG_DELAY_SDOUT[2:0]	R/W	000b	Programmable digital delay on SDOUT. 000b = 0ns delay 001b = 1ns delay 010b = 2ns delay 011b = 3ns delay 100b = 4ns delay 101b = 5ns delay
11:9	DIG_DELAY_D3[2:0]	R/W	000b	Programmable digital delay on D3. 000b = 0ns delay 001b = 1ns delay 010b = 2ns delay 011b = 3ns delay 100b = 4ns delay 101b = 5ns delay
8:6	DIG_DELAY_D2[2:0]	R/W	000b	Programmable digital delay on D2. 000b = 0ns delay 001b = 1ns delay 010b = 2ns delay 011b = 3ns delay 100b = 4ns delay 101b = 5ns delay
5:3	DIG_DELAY_D1[2:0]	R/W	000b	Programmable digital delay on D1. 000b = 0ns delay 001b = 1ns delay 010b = 2ns delay 011b = 3ns delay 100b = 4ns delay 101b = 5ns delay
2:0	DIG_DELAY_D0[2:0]	R/W	000b	Programmable digital delay on D0. 000b = 0ns delay 001b = 1ns delay 010b = 2ns delay 011b = 3ns delay 100b = 4ns delay 101b = 5ns delay

8.1.11 DIG_DELAY_CFG2 Register (Address = 0x0F) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-11. DIG_DELAY_CFG2 Register

15	14	13	12	11	10	9	8
RESERVED				DIG_DELAY_D7[2:0]			DIG_DELAY_D6[2:0]
R/W-0000b				R/W-000b			R/W-000b
7	6	5	4	3	2	1	0
DIG_DELAY_D6[2:0]			DIG_DELAY_D5[2:0]			DIG_DELAY_D4[2:0]	
R/W-000b			R/W-000b			R/W-000b	

Table 8-13. DIG_DELAY_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0000b	Reserved. Do not change from the default reset value.
11:9	DIG_DELAY_D7[2:0]	R/W	000b	Programmable digital delay on D7. 000b = 0ns delay 001b = 1ns delay 010b = 2ns delay 011b = 3ns delay 100b = 4ns delay 101b = 5ns delay
8:6	DIG_DELAY_D6[2:0]	R/W	000b	Programmable digital delay on D6. 000b = 0ns delay 001b = 1ns delay 010b = 2ns delay 011b = 3ns delay 100b = 4ns delay 101b = 5ns delay
5:3	DIG_DELAY_D5[2:0]	R/W	000b	Programmable digital delay on D5. 000b = 0ns delay 001b = 1ns delay 010b = 2ns delay 011b = 3ns delay 100b = 4ns delay 101b = 5ns delay
2:0	DIG_DELAY_D4[2:0]	R/W	000b	Programmable digital delay on D4. 000b = 0ns delay 001b = 1ns delay 010b = 2ns delay 011b = 3ns delay 100b = 4ns delay 101b = 5ns delay

8.1.12 ANA_CFG1 Register (Address = 0x10) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-12. ANA_CFG1 Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-00000000000000b							
7	6	5	4	3	2	1	0
RESERVED						REFSEL_CTRL_DIS	EXT_REF_EN
R/W-00000000000000b						R/W-0b	R/W-0b

Table 8-14. ANA_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:2	RESERVED	R/W	00000000000000b	Reserved. Do not change from the default reset value.
1	REFSEL_CTRL_DIS	R/W	0b	RESEL pin control disable. 0b = Enabled 1b = Disabled
0	EXT_REF_EN	R/W	0b	ADC reference select. 0b = Internal reference 1b = External reference

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8.1.13 ANA_CFG2 Register (Address = 0x11) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-13. ANA_CFG2 Register

15	14	13	12	11	10	9	8
CH_XTALK_LOW_SPEED	RESERVED						
R/W-0b	R/W-00000000b						
7	6	5	4	3	2	1	0
RESERVED	ADC_CH_SEL[2:0]			ADC_NUM_SEL[1:0]		RESERVED	
R/W-00000000b	R/W-000b			R/W-00b		R/W-00b	

Table 8-15. ANA_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CH_XTALK_LOW_SPEED	R/W	0b	Set this bit to 1'b when the ADC sample rate is less than 100kSPS/ch
14:7	RESERVED	R/W	00000000b	Reserved. Do not change from the default reset value.
6:4	ADC_CH_SEL[2:0]	R/W	000b	Select the ADC channels corresponding to ADC_NUM_SEL. These configurations work when ADC_NUM_SEL is not 00'b.
3:2	ADC_NUM_SEL[1:0]	R/W	00b	Select the number of ADCs that are undergoing conversion. When ADC_NUM_SEL is 00'b, ADC_CH_SEL is don't care. 00b = 16 Channels (Default) 01b = 8 Channels 10b = 4 Channels 11b = 2 Channels
1:0	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.

8.1.14 ADC_CAL Register (Address = 0x12) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-14. ADC_CAL Register

15	14	13	12	11	10	9	8
RESERVED		SE_DIFF_MODE_AIN1_8	SE_DIFF_MODE_AIN9_16	RESERVED			ADC_CAL_TRIG
R/W-00b		R/W-0b	R/W-0b	R/W-000b			R/W-0b
7	6	5	4	3	2	1	0
RESERVED						ADC_CAL_MODE[1:0]	
R/W-000000b						R/W-00b	

Table 8-16. ADC_CAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13	SE_DIFF_MODE_AIN1_8	R/W	0b	Analog input signal type. User updates this bit before the start of ADC_CAL module. 0b = Differential input signals on AIN1 to AIN8 1b = Single ended input signals on AIN1 to AIN8
12	SE_DIFF_MODE_AIN9_16	R/W	0b	Analog input signal type. User updates this bit before the start of ADC_CAL module. 0b = Differential input signals on AIN9 to AIN16 1b = Single ended input signals on AIN9 to AIN16
11:9	RESERVED	R/W	000b	Reserved. Do not change from the default reset value.
8	ADC_CAL_TRIG	R/W	0b	ADC CAL module trigger signal. Write 1'b to trigger the ADC_CAL module.
7:2	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
1:0	ADC_CAL_MODE[1:0]	R/W	00b	ADC_CAL mode selection. 00b = Calibration is disabled 01b = Offset error calibration 10b = Gain error calibration 11b = Offset and gain error calibration

8.1.15 DIG_FILTER Register (Address = 0x14) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-15. DIG_FILTER Register

15	14	13	12	11	10	9	8
PHASE_DELAY_EN	FIR_FILT_SEL[2:0]			MVG_AVG_LEN[3:0]			
R/W-0b	R/W-000b			R/W-0000b			
7	6	5	4	3	2	1	0
BLK_AVG_OSR[3:0]				RESERVED		INT_TRIG_MODE	DIG_FILT_SYSREF
R/W-0000b				R/W-00b		R/W-0b	R/W-0b

Table 8-17. DIG_FILTER Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PHASE_DELAY_EN	R/W	0b	Phase delay enable. Used to adjust phase between analog input channels. 0b = Disabled 1b = Enabled
14:12	FIR_FILT_SEL[2:0]	R/W	000b	FIR filter selection. 000b = Disabled 001b = FIR1 010b = FIR2 011b = FIR3 100b = FIR4 101b = Reserved 110b = FIR6 111b = FIR7
11:8	MVG_AVG_LEN[3:0]	R/W	0000b	Moving average filter length selection. 0000b = No averaging 0001b = 2 samples averaged 0010b = 4 samples averaged 0011b = 6 samples averaged 0100b = 8 samples averaged 0101b = 10 samples averaged 0110b = 12 samples averaged 0111b = 16 samples averaged 1000b = 20 samples averaged 1001b = 32 samples averaged 1010b = 64 samples averaged 1011b = 128 samples averaged
7:4	BLK_AVG_OSR[3:0]	R/W	0000b	Oversampling ratio (OSR) configuration for block average filter. 0000b = No averaging 0001b = 2 samples averaged 0010b = 4 samples averaged 0011b = 6 samples averaged 0100b = 8 samples averaged 0101b = 10 samples averaged 0110b = 12 samples averaged 0111b = 16 samples averaged 1000b = 20 samples averaged 1001b = 32 samples averaged 1010b = 64 samples averaged 1011b = 128 samples averaged
3:2	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
1	INT_TRIG_MODE	R/W	0b	Auto trigger the sample and hold circuit during oversampling. 0b = Disabled 1b = Enabled
0	DIG_FILT_SYSREF	R/W	0b	Write 1'b to reset the digital filter accumulator.

8.1.16 GEN_CFG5 Register (Address = 0x15) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-16. GEN_CFG5 Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-000000000000b							
7	6	5	4	3	2	1	0
RESERVED				T_MODE_OVR_EN	T_MODE	AVG_MODE_OVR_EN	AVG_MODE
R/W-000000000000b				R/W-0b	R/W-0b	R/W-0b	R/W-0b

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Table 8-18. GEN_CFG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	RESERVED	R/W	000000000000b	Reserved. Do not change from the default reset value.
3	T_MODE_OVR_EN	R/W	0b	This bit enables T_MODE (truncate mode feature). Set this bit to 1b before configure T_MODE field.
2	T_MODE	R/W	0b	This bit allows user to truncate the ADC output to 16b when using test pattern of this device.
1	AVG_MODE_OVR_EN	R/W	0b	This bits enables AVG_MODE. Set this bit to 1b before configuring AVG_MODE to 1b.
0	AVG_MODE	R/W	0b	Set this 1b when oversampling to maximize the noise performance.

8.1.17 DEVICE_STATUS Register (Address = 0x1E) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-17. DEVICE_STATUS Register

15	14	13	12	11	10	9	8
RESERVED							
R-00000000000b							
7	6	5	4	3	2	1	0
RESERVED			CALIB_BUSY_FLAG	RESERVED			
R-00000000000b			R-0b	R-0000b			

Table 8-19. DEVICE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:5	RESERVED	R	00000000000b	Reserved. Do not change from the default reset value.
4	CALIB_BUSY_FLAG	R	0b	Indicates ADC_CAL is running. 0b = ADC_CAL module is idle 1b = ADC_CAL module is running.
3:0	RESERVED	R	0000b	Reserved. Do not change from the default reset value.

8.1.18 DEVICE_ID Register (Address = 0x21) [Reset = 0x0004]

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Figure 8-18. DEVICE_ID Register

15	14	13	12	11	10	9	8
RESERVED							
R-00000000b							
7	6	5	4	3	2	1	0
DEVICE_ID[7:0]							
R-00000100b							

Table 8-20. DEVICE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	RESERVED	R	00000000b	Reserved. Do not change from the default reset value.
7:0	DEVICE_ID[7:0]	R	00000100b	Device ID.

8.2 AIN1 - AIN8 Channel Registers

Table 8-21 lists the memory-mapped registers for the AIN1 - AIN8 Channel registers. All register offset addresses not listed in Table 8-21 should be considered as reserved locations and the register contents should not be modified.

Table 8-21. AIN1 - AIN8 Channel

Address	Acronym	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x08	PGA_CONFIG_AIN1_2	CME_CORR_EN_AIN2	CM_RANGE_AIN2[2:0]			RESERVED	INPUT_RANGE_AIN2[2:0]		
		CME_CORR_EN_AIN1	CM_RANGE_AIN1[2:0]			RESERVED	INPUT_RANGE_AIN1[2:0]		
0x09	PGA_CONFIG_AIN3_4	CME_CORR_EN_AIN4	CM_RANGE_AIN4[2:0]			RESERVED	INPUT_RANGE_AIN4[2:0]		
		CME_CORR_EN_AIN3	CM_RANGE_AIN3[2:0]			RESERVED	INPUT_RANGE_AIN3[2:0]		
0x0A	PGA_CONFIG_AIN5_6	CME_CORR_EN_AIN6	CM_RANGE_AIN6[2:0]			RESERVED	INPUT_RANGE_AIN6[2:0]		
		CME_CORR_EN_AIN5	CM_RANGE_AIN5[2:0]			RESERVED	INPUT_RANGE_AIN5[2:0]		
0x0B	PGA_CONFIG_AIN7_8	CME_CORR_EN_AIN8	CM_RANGE_AIN8[2:0]			RESERVED	INPUT_RANGE_AIN8[2:0]		
		CME_CORR_EN_AIN7	CM_RANGE_AIN7[2:0]			RESERVED	INPUT_RANGE_AIN7[2:0]		
0x0C	PGA_BW_SEL_AIN1_8	PGA_BW_SEL_AIN8[1:0]		PGA_BW_SEL_AIN7[1:0]		PGA_BW_SEL_AIN6[1:0]		PGA_BW_SEL_AIN5[1:0]	
		PGA_BW_SEL_AIN4[1:0]		PGA_BW_SEL_AIN3[1:0]		PGA_BW_SEL_AIN2[1:0]		PGA_BW_SEL_AIN1[1:0]	
0x0D	PHASE_DELAY_AIN1_2	PHASE_DELAY_AIN2[7:0]							
		PHASE_DELAY_AIN1[7:0]							
0x0E	PHASE_DELAY_AIN3_4	PHASE_DELAY_AIN4[7:0]							
		PHASE_DELAY_AIN3[7:0]							
0x0F	PHASE_DELAY_AIN5_6	PHASE_DELAY_AIN6[7:0]							
		PHASE_DELAY_AIN5[7:0]							
0x10	PHASE_DELAY_AIN7_8	PHASE_DELAY_AIN8[7:0]							
		PHASE_DELAY_AIN7[7:0]							
0x11	OFS_AIN1	RESERVED						OFS_AIN1[9:0]	
		OFS_AIN1[9:0]							
0x12	OFS_AIN2	RESERVED						OFS_AIN2[9:0]	
		OFS_AIN2[9:0]							
0x13	OFS_AIN3	RESERVED						OFS_AIN3[9:0]	
		OFS_AIN3[9:0]							
0x14	OFS_AIN4	RESERVED						OFS_AIN4[9:0]	
		OFS_AIN4[9:0]							
0x15	OFS_AIN5	RESERVED						OFS_AIN5[9:0]	
		OFS_AIN5[9:0]							
0x16	OFS_AIN6	RESERVED						OFS_AIN6[9:0]	
		OFS_AIN6[9:0]							
0x17	OFS_AIN7	RESERVED						OFS_AIN7[9:0]	
		OFS_AIN7[9:0]							
0x18	OFS_AIN8	RESERVED						OFS_AIN8[9:0]	
		OFS_AIN8[9:0]							
0x19	GAN_AIN1	RESERVED		GAN_AIN1[13:0]					
		GAN_AIN1[13:0]							
0x1A	GAN_AIN2	RESERVED		GAN_AIN2[13:0]					
		GAN_AIN2[13:0]							
0x1B	GAN_AIN3	RESERVED		GAN_AIN3[13:0]					
		GAN_AIN3[13:0]							
0x1C	GAN_AIN4	RESERVED		GAN_AIN4[13:0]					
		GAN_AIN4[13:0]							

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Table 8-21. AIN1 - AIN8 Channel (continued)

Address	Acronym	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1D	GAN_AIN5	RESERVED		GAN_AIN5[13:0]					
		GAN_AIN5[13:0]							
0x1E	GAN_AIN6	RESERVED		GAN_AIN6[13:0]					
		GAN_AIN6[13:0]							
0x1F	GAN_AIN7	RESERVED		GAN_AIN7[13:0]					
		GAN_AIN7[13:0]							
0x20	GAN_AIN8	RESERVED		GAN_AIN8[13:0]					
		GAN_AIN8[13:0]							
0x21	DWC_CFG	DWC_STAT_RST	RESERVED			DWC_GLITCH_FILT[3:0]			
		DWC_EN_AIN8	DWC_EN_AIN7	DWC_EN_AIN6	DWC_EN_AIN5	DWC_EN_AIN4	DWC_EN_AIN3	DWC_EN_AIN2	DWC_EN_AIN1
0x22	DWC_TH_AIN1	HIGH_TH_AIN1[7:0]							
		LOW_TH_AIN1[7:0]							
0x23	DWC_TH_AIN2	HIGH_TH_AIN2[7:0]							
		LOW_TH_AIN2[7:0]							
0x24	DWC_TH_AIN3	HIGH_TH_AIN3[7:0]							
		LOW_TH_AIN3[7:0]							
0x25	DWC_TH_AIN4	HIGH_TH_AIN4[7:0]							
		LOW_TH_AIN4[7:0]							
0x26	DWC_TH_AIN5	HIGH_TH_AIN5[7:0]							
		LOW_TH_AIN5[7:0]							
0x27	DWC_TH_AIN6	HIGH_TH_AIN6[7:0]							
		LOW_TH_AIN6[7:0]							
0x28	DWC_TH_AIN7	HIGH_TH_AIN7[7:0]							
		LOW_TH_AIN7[7:0]							
0x29	DWC_TH_AIN8	HIGH_TH_AIN8[7:0]							
		LOW_TH_AIN8[7:0]							
0x2A	DWC_HYS_AIN1_2	HYS_AIN2[7:0]							
		HYS_AIN1[7:0]							
0x2B	DWC_HYS_AIN3_4	HYS_AIN4[7:0]							
		HYS_AIN3[7:0]							
0x2C	DWC_HYS_AIN5_6	HYS_AIN6[7:0]							
		HYS_AIN5[7:0]							
0x2D	DWC_HYS_AIN7_8	HYS_AIN8[7:0]							
		HYS_AIN7[7:0]							
0x2E	TP_CFG	RESERVED							
		RESERVED	TP_MODE[2:0]			RESERVED	TP_DIS_IDX	TP_UPD_MODE	TP_EN
0x2F	TP_AIN1	TP_AIN1[15:0]							
		TP_AIN1[15:0]							
0x30	TP_AIN2	TP_AIN2[15:0]							
		TP_AIN2[15:0]							
0x31	TP_AIN3	TP_AIN3[15:0]							
		TP_AIN3[15:0]							
0x32	TP_AIN4	TP_AIN4[15:0]							
		TP_AIN4[15:0]							
0x33	TP_AIN5	TP_AIN5[15:0]							
		TP_AIN5[15:0]							
0x34	TP_AIN6	TP_AIN6[15:0]							
		TP_AIN6[15:0]							
0x35	TP_AIN7	TP_AIN7[15:0]							
		TP_AIN7[15:0]							
0x36	TP_AIN8	TP_AIN8[15:0]							
		TP_AIN8[15:0]							

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Table 8-21. AIN1 - AIN8 Channel (continued)

Address	Acronym	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x37	GEN_CFG5	RESERVED							
		RESERVED						OFS_CORR_DIS	GAN_CORR_DIS
0x3B	CH_XTALK_AIN1_8	RESERVED				CH_XTALK_AIN1_8	RESERVED		
		RESERVED							
0x3E	DWC_FLAG_AIN1_8	HIGH_FLAG_AIN8	HIGH_FLAG_AIN7	HIGH_FLAG_AIN6	HIGH_FLAG_AIN5	HIGH_FLAG_AIN4	HIGH_FLAG_AIN3	HIGH_FLAG_AIN2	HIGH_FLAG_AIN1
		LOW_FLAG_AIN8	LOW_FLAG_AIN7	LOW_FLAG_AIN6	LOW_FLAG_AIN5	LOW_FLAG_AIN4	LOW_FLAG_AIN3	LOW_FLAG_AIN2	LOW_FLAG_AIN1

Complex bit access types are encoded to fit into small table cells. Table 8-22 shows the codes that are used for access types in this section.

Table 8-22. AIN1 - AIN8 Channel Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.2.1 PGA_CONFIG_AIN1_2 Register (Address = 0x08) [Reset = 0x0000]

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Figure 8-19. PGA_CONFIG_AIN1_2 Register

15	14	13	12	11	10	9	8
CME_CORR_EN_AIN2	CM_RANGE_AIN2[2:0]			RESERVED	INPUT_RANGE_AIN2[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		
7	6	5	4	3	2	1	0
CME_CORR_EN_AIN1	CM_RANGE_AIN1[2:0]			RESERVED	INPUT_RANGE_AIN1[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		

Table 8-23. PGA_CONFIG_AIN1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CME_CORR_EN_AIN2	R/W	0b	Common mode error correction enable. 0b = Disabled 1b = Enabled
14:12	CM_RANGE_AIN2[2:0]	R/W	000b	Select input signal type. 000b = Differential 101b = Single ended 110b = Single ended open wire safe
11	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
10:8	INPUT_RANGE_AIN2[2:0]	R/W	000b	AIN2 analog input range selection. 000b = ±5V 001b = ±25V 010b = ±2.5V 011b = ±6.25V 100b = ±10V 101b = ±12.5V 110b = ±50V 111b = Reserved
7	CME_CORR_EN_AIN1	R/W	0b	Common mode error correction enable. 0b = Disabled 1b = Enabled

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Table 8-23. PGA_CONFIG_AIN1_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	CM_RANGE_AIN1[2:0]	R/W	000b	Select input signal type. 000b = Differential 101b = Single ended 110b = Single ended open wire safe
3	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
2:0	INPUT_RANGE_AIN1[2:0]	R/W	000b	AIN1 analog input range selection. 000b = ±5V 001b = ±25V 010b = ±2.5V 011b = ±6.25V 100b = ±10V 101b = ±12.5V 110b = ±50V 111b = Reserved

8.2.2 PGA_CONFIG_AIN3_4 Register (Address = 0x09) [Reset = 0x0000]

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Figure 8-20. PGA_CONFIG_AIN3_4 Register

15	14	13	12	11	10	9	8
CME_CORR_EN_AIN4	CM_RANGE_AIN4[2:0]			RESERVED	INPUT_RANGE_AIN4[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		
7	6	5	4	3	2	1	0
CME_CORR_EN_AIN3	CM_RANGE_AIN3[2:0]			RESERVED	INPUT_RANGE_AIN3[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		

Table 8-24. PGA_CONFIG_AIN3_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CME_CORR_EN_AIN4	R/W	0b	Common mode error correction enable. 0b = Disabled 1b = Enabled
14:12	CM_RANGE_AIN4[2:0]	R/W	000b	Select input signal type. 000b = Differential 101b = Single ended 110b = Single ended open wire safe
11	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
10:8	INPUT_RANGE_AIN4[2:0]	R/W	000b	AIN4 analog input range selection. 000b = ±5V 001b = ±25V 010b = ±2.5V 011b = ±6.25V 100b = ±10V 101b = ±12.5V 110b = ±50V 111b = Reserved
7	CME_CORR_EN_AIN3	R/W	0b	Common mode error correction enable. 0b = Disabled 1b = Enabled
6:4	CM_RANGE_AIN3[2:0]	R/W	000b	Select input signal type. 000b = Differential 101b = Single ended 110b = Single ended open wire safe
3	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
2:0	INPUT_RANGE_AIN3[2:0]	R/W	000b	AIN3 analog input range selection. 000b = ±5V 001b = ±25V 010b = ±2.5V 011b = ±6.25V 100b = ±10V 101b = ±12.5V 110b = ±50V 111b = Reserved

8.2.3 PGA_CONFIG_AIN5_6 Register (Address = 0x0A) [Reset = 0x0000]

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Figure 8-21. PGA_CONFIG_AIN5_6 Register

15	14	13	12	11	10	9	8
CME_CORR_EN_AIN6	CM_RANGE_AIN6[2:0]			RESERVED	INPUT_RANGE_AIN6[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		
7	6	5	4	3	2	1	0
CME_CORR_EN_AIN5	CM_RANGE_AIN5[2:0]			RESERVED	INPUT_RANGE_AIN5[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		

Table 8-25. PGA_CONFIG_AIN5_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CME_CORR_EN_AIN6	R/W	0b	Common mode error correction enable. 0b = Disabled 1b = Enabled
14:12	CM_RANGE_AIN6[2:0]	R/W	000b	Select input signal type. 000b = Differential 101b = Single ended 110b = Single ended open wire safe
11	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
10:8	INPUT_RANGE_AIN6[2:0]	R/W	000b	AIN6 analog input range selection. 000b = ±5V 001b = ±25V 010b = ±2.5V 011b = ±6.25V 100b = ±10V 101b = ±12.5V 110b = ±50V 111b = Reserved
7	CME_CORR_EN_AIN5	R/W	0b	Common mode error correction enable. 0b = Disabled 1b = Enabled
6:4	CM_RANGE_AIN5[2:0]	R/W	000b	Select input signal type. 000b = Differential 101b = Single ended 110b = Single ended open wire safe
3	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
2:0	INPUT_RANGE_AIN5[2:0]	R/W	000b	AIN5 analog input range selection. 000b = ±5V 001b = ±25V 010b = ±2.5V 011b = ±6.25V 100b = ±10V 101b = ±12.5V 110b = ±50V 111b = Reserved

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8.2.4 PGA_CONFIG_AIN7_8 Register (Address = 0x0B) [Reset = 0x0000]

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Figure 8-22. PGA_CONFIG_AIN7_8 Register

15	14	13	12	11	10	9	8
CME_CORR_EN_AIN8	CM_RANGE_AIN8[2:0]			RESERVED	INPUT_RANGE_AIN8[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		
7	6	5	4	3	2	1	0
CME_CORR_EN_AIN7	CM_RANGE_AIN7[2:0]			RESERVED	INPUT_RANGE_AIN7[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		

Table 8-26. PGA_CONFIG_AIN7_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CME_CORR_EN_AIN8	R/W	0b	Common mode error correction enable. 0b = Disabled 1b = Enabled
14:12	CM_RANGE_AIN8[2:0]	R/W	000b	Select input signal type. 000b = Differential 101b = Single ended 110b = Single ended open wire safe
11	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
10:8	INPUT_RANGE_AIN8[2:0]	R/W	000b	AIN8 analog input range selection. 000b = ±5V 001b = ±25V 010b = ±2.5V 011b = ±6.25V 100b = ±10V 101b = ±12.5V 110b = ±50V 111b = Reserved
7	CME_CORR_EN_AIN7	R/W	0b	Common mode error correction enable. 0b = Disabled 1b = Enabled
6:4	CM_RANGE_AIN7[2:0]	R/W	000b	Select input signal type. 000b = Differential 101b = Single ended 110b = Single ended open wire safe
3	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
2:0	INPUT_RANGE_AIN7[2:0]	R/W	000b	AIN7 analog input range selection. 000b = ±5V 001b = ±25V 010b = ±2.5V 011b = ±6.25V 100b = ±10V 101b = ±12.5V 110b = ±50V 111b = Reserved

8.2.5 PGA_BW_SEL_AIN1_8 Register (Address = 0x0C) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-23. PGA_BW_SEL_AIN1_8 Register

15	14	13	12	11	10	9	8
PGA_BW_SEL_AIN8[1:0]		PGA_BW_SEL_AIN7[1:0]		PGA_BW_SEL_AIN6[1:0]		PGA_BW_SEL_AIN5[1:0]	
R/W-00b		R/W-00b		R/W-00b		R/W-00b	
7	6	5	4	3	2	1	0
PGA_BW_SEL_AIN4[1:0]		PGA_BW_SEL_AIN3[1:0]		PGA_BW_SEL_AIN2[1:0]		PGA_BW_SEL_AIN1[1:0]	
R/W-00b		R/W-00b		R/W-00b		R/W-00b	

Table 8-27. PGA_BW_SEL_AIN1_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	PGA_BW_SEL_AIN8[1:0]	R/W	00b	AIN8 analog low pass filter configuration control. 00b = Low-bandwidth 01b = Wide-bandwidth 10b = Reserved 11b = Reserved
13:12	PGA_BW_SEL_AIN7[1:0]	R/W	00b	AIN7 analog low pass filter configuration control. 00b = Low-bandwidth 01b = Wide-bandwidth 10b = Reserved 11b = Reserved
11:10	PGA_BW_SEL_AIN6[1:0]	R/W	00b	AIN6 analog low pass filter configuration control. 00b = Low-bandwidth 01b = Wide-bandwidth 10b = Reserved 11b = Reserved
9:8	PGA_BW_SEL_AIN5[1:0]	R/W	00b	AIN5 analog low pass filter configuration control. 00b = Low-bandwidth 01b = Wide-bandwidth 10b = Reserved 11b = Reserved

Table 8-27. PGA_BW_SEL_AIN1_8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:6	PGA_BW_SEL_AIN4[1:0]	R/W	00b	AIN4 analog low pass filter configuration control. 00b = Low-bandwidth 01b = Wide-bandwidth 10b = Reserved 11b = Reserved
5:4	PGA_BW_SEL_AIN3[1:0]	R/W	00b	AIN3 analog low pass filter configuration control. 00b = Low-bandwidth 01b = Wide-bandwidth 10b = Reserved 11b = Reserved
3:2	PGA_BW_SEL_AIN2[1:0]	R/W	00b	AIN2 analog low pass filter configuration control. 00b = Low-bandwidth 01b = Wide-bandwidth 10b = Reserved 11b = Reserved
1:0	PGA_BW_SEL_AIN1[1:0]	R/W	00b	AIN1 analog low pass filter configuration control. 00b = Low-bandwidth 01b = Wide-bandwidth 10b = Reserved 11b = Reserved

8.2.6 PHASE_DELAY_AIN1_2 Register (Address = 0x0D) [Reset = 0x0000]

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Figure 8-24. PHASE_DELAY_AIN1_2 Register

15	14	13	12	11	10	9	8
PHASE_DELAY_AIN2[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
PHASE_DELAY_AIN1[7:0]							
R/W-00000000b							

Table 8-28. PHASE_DELAY_AIN1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	PHASE_DELAY_AIN2[7:0]	R/W	00000000b	Phase delay = n* ADC CONVST CLK, where n is 0 to 255.
7:0	PHASE_DELAY_AIN1[7:0]	R/W	00000000b	Phase delay = n* ADC CONVST CLK, where n is 0 to 255.

8.2.7 PHASE_DELAY_AIN3_4 Register (Address = 0x0E) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-25. PHASE_DELAY_AIN3_4 Register

15	14	13	12	11	10	9	8
PHASE_DELAY_AIN4[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
PHASE_DELAY_AIN3[7:0]							
R/W-00000000b							

Table 8-29. PHASE_DELAY_AIN3_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	PHASE_DELAY_AIN4[7:0]	R/W	00000000b	Phase delay = n* CONVST_CLK, where n is 0 to 255.
7:0	PHASE_DELAY_AIN3[7:0]	R/W	00000000b	Phase delay = n* CONVST_CLK, where n is 0 to 255.

8.2.8 PHASE_DELAY_AIN5_6 Register (Address = 0x0F) [Reset = 0x0000]

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Figure 8-26. PHASE_DELAY_AIN5_6 Register

15	14	13	12	11	10	9	8
PHASE_DELAY_AIN6[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
PHASE_DELAY_AIN5[7:0]							
R/W-00000000b							

Table 8-30. PHASE_DELAY_AIN5_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	PHASE_DELAY_AIN6[7:0]	R/W	00000000b	Phase delay = n* CONVST_CLK, where n is 0 to 255.
7:0	PHASE_DELAY_AIN5[7:0]	R/W	00000000b	Phase delay = n* CONVST_CLK, where n is 0 to 255.

8.2.9 PHASE_DELAY_AIN7_8 Register (Address = 0x10) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-27. PHASE_DELAY_AIN7_8 Register

15	14	13	12	11	10	9	8
PHASE_DELAY_AIN8[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
PHASE_DELAY_AIN7[7:0]							
R/W-00000000b							

Table 8-31. PHASE_DELAY_AIN7_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	PHASE_DELAY_AIN8[7:0]	R/W	00000000b	Phase delay = n* CONVST_CLK, where n is 0 to 255.
7:0	PHASE_DELAY_AIN7[7:0]	R/W	00000000b	Phase delay = n* CONVST_CLK, where n is 0 to 255.

8.2.10 OFS_AIN1 Register (Address = 0x11) [Reset = 0x0000]

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Figure 8-28. OFS_AIN1 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_AIN1[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_AIN1[9:0]							
R/W-0000000000b							

Table 8-32. OFS_AIN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_AIN1[9:0]	R/W	0000000000b	Offset correction register for AIN1. The offset value is in two's complement representation. The offset operation precedes the gain operation.

8.2.11 OFS_AIN2 Register (Address = 0x12) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-29. OFS_AIN2 Register

15	14	13	12	11	10	9	8

Figure 8-29. OFS_AIN2 Register (continued)

RESERVED						OFS_AIN2[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_AIN2[9:0]							
R/W-0000000000b							

Table 8-33. OFS_AIN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_AIN2[9:0]	R/W	0000000000b	Offset correction register for AIN2. The offset value is in two's complement representation. The offset operation precedes the gain operation.

8.2.12 OFS_AIN3 Register (Address = 0x13) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-30. OFS_AIN3 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_AIN3[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_AIN3[9:0]							
R/W-0000000000b							

Table 8-34. OFS_AIN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_AIN3[9:0]	R/W	0000000000b	Offset correction register for AIN3. The offset value is in two's complement representation. The offset operation precedes the gain operation.

8.2.13 OFS_AIN4 Register (Address = 0x14) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-31. OFS_AIN4 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_AIN4[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_AIN4[9:0]							
R/W-0000000000b							

Table 8-35. OFS_AIN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_AIN4[9:0]	R/W	0000000000b	Offset correction register for AIN4. The offset value is in two's complement representation. The offset operation precedes the gain operation.

8.2.14 OFS_AIN5 Register (Address = 0x15) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-32. OFS_AIN5 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_AIN5[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_AIN5[9:0]							
R/W-0000000000b							

Table 8-36. OFS_AIN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_AIN5[9:0]	R/W	0000000000b	Offset correction register for AIN5. The offset value is in two's complement representation. The offset operation precedes the gain operation.

8.2.15 OFS_AIN6 Register (Address = 0x16) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-33. OFS_AIN6 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_AIN6[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_AIN6[9:0]							
R/W-0000000000b							

Table 8-37. OFS_AIN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_AIN6[9:0]	R/W	0000000000b	Offset correction register for AIN6. The offset value is in two's complement representation. The offset operation precedes the gain operation.

8.2.16 OFS_AIN7 Register (Address = 0x17) [Reset = 0x0000]

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Figure 8-34. OFS_AIN7 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_AIN7[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_AIN7[9:0]							
R/W-0000000000b							

Table 8-38. OFS_AIN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_AIN7[9:0]	R/W	0000000000b	Offset correction register for AIN7. The offset value is in two's complement representation and is subtracted from the conversion result. The offset operation precedes the gain operation. Four LSB bits reserved for 12-bit ADS93xx device family variant.

8.2.17 OFS_AIN8 Register (Address = 0x18) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-35. OFS_AIN8 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_AIN8[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_AIN8[9:0]							
R/W-0000000000b							

Table 8-39. OFS_AIN8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_AIN8[9:0]	R/W	0000000000b	Offset correction register for AIN8. The offset value is in two's complement representation. The offset operation precedes the gain operation.

8.2.18 GAN_AIN1 Register (Address = 0x19) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-36. GAN_AIN1 Register

15	14	13	12	11	10	9	8
RESERVED		GAN_AIN1[13:0]					
R/W-00b		R/W-00000000000000b					
7	6	5	4	3	2	1	0
GAN_AIN1[13:0]							
R/W-00000000000000b							

Table 8-40. GAN_AIN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13:0	GAN_AIN1[13:0]	R/W	00000000000000b	Gain correction register for AIN1. The gain correction value is in two's complement representation, and is done after offset operation. During gain operating, the conversion data are multiplied by (1 + GAN_AINn[13:0] / 10000h).

8.2.19 GAN_AIN2 Register (Address = 0x1A) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-37. GAN_AIN2 Register

15	14	13	12	11	10	9	8
RESERVED		GAN_AIN2[13:0]					
R/W-00b		R/W-00000000000000b					
7	6	5	4	3	2	1	0
GAN_AIN2[13:0]							
R/W-00000000000000b							

Table 8-41. GAN_AIN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13:0	GAN_AIN2[13:0]	R/W	00000000000000b	Gain correction register for AIN2. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_AINn[13:0] / 10000h).

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8.2.20 GAN_AIN3 Register (Address = 0x1B) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-38. GAN_AIN3 Register

15	14	13	12	11	10	9	8
RESERVED		GAN_AIN3[13:0]					
R/W-00b		R/W-00000000000000b					
7	6	5	4	3	2	1	0
GAN_AIN3[13:0]							
R/W-00000000000000b							

Table 8-42. GAN_AIN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13:0	GAN_AIN3[13:0]	R/W	00000000000000b	Gain correction register for AIN3. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_AINn[13:0] / 10000h).

8.2.21 GAN_AIN4 Register (Address = 0x1C) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-39. GAN_AIN4 Register

15	14	13	12	11	10	9	8
RESERVED		GAN_AIN4[13:0]					
R/W-00b		R/W-00000000000000b					
7	6	5	4	3	2	1	0
GAN_AIN4[13:0]							
R/W-00000000000000b							

Table 8-43. GAN_AIN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13:0	GAN_AIN4[13:0]	R/W	00000000000000b	Gain correction register for AIN4. The gain correction value is in two's complement representation, and is done after offset operation. During gain operating, the conversion data are multiplied by (1 + GAN_AINn[13:0] / 10000h).

8.2.22 GAN_AIN5 Register (Address = 0x1D) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-40. GAN_AIN5 Register

15	14	13	12	11	10	9	8
RESERVED		GAN_AIN5[13:0]					
R/W-00b		R/W-00000000000000b					
7	6	5	4	3	2	1	0
GAN_AIN5[13:0]							
R/W-00000000000000b							

Table 8-44. GAN_AIN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.

Table 8-44. GAN_AIN5 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:0	GAN_AIN5[13:0]	R/W	0000000000000b	Gain correction register for AIN5. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_AINn[13:0] / 10000h).

8.2.23 GAN_AIN6 Register (Address = 0x1E) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-41. GAN_AIN6 Register

15	14	13	12	11	10	9	8
RESERVED		GAN_AIN6[13:0]					
R/W-00b		R/W-00000000000000b					
7	6	5	4	3	2	1	0
GAN_AIN6[13:0]							
R/W-00000000000000b							

Table 8-45. GAN_AIN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13:0	GAN_AIN6[13:0]	R/W	0000000000000b	Gain correction register for AIN6. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_AINn[13:0] / 10000h).

8.2.24 GAN_AIN7 Register (Address = 0x1F) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-42. GAN_AIN7 Register

15	14	13	12	11	10	9	8
RESERVED		GAN_AIN7[13:0]					
R/W-00b		R/W-00000000000000b					
7	6	5	4	3	2	1	0
GAN_AIN7[13:0]							
R/W-00000000000000b							

Table 8-46. GAN_AIN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13:0	GAN_AIN7[13:0]	R/W	0000000000000b	Gain correction register for AIN7. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_AINn[13:0] / 10000h).

8.2.25 GAN_AIN8 Register (Address = 0x20) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-43. GAN_AIN8 Register

15	14	13	12	11	10	9	8
RESERVED		GAN_AIN8[13:0]					
R/W-00b		R/W-00000000000000b					
7	6	5	4	3	2	1	0
GAN_AIN8[13:0]							
R/W-00000000000000b							

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Figure 8-43. GAN_AIN8 Register (continued)

Table 8-47. GAN_AIN8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13:0	GAN_AIN8[13:0]	R/W	0000000000000b	Gain correction register for AIN8. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_AINn[13:0] / 10000h).

8.2.26 DWC_CFG Register (Address = 0x21) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-44. DWC_CFG Register

15	14	13	12	11	10	9	8
DWC_STAT_RST	RESERVED			DWC_GLITCH_FILT[3:0]			
R/W-0b	R/W-000b			R/W-0000b			
7	6	5	4	3	2	1	0
DWC_EN_AIN8	DWC_EN_AIN7	DWC_EN_AIN6	DWC_EN_AIN5	DWC_EN_AIN4	DWC_EN_AIN3	DWC_EN_AIN2	DWC_EN_AIN1
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-48. DWC_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DWC_STAT_RST	R/W	0b	Digital window comparator reset control. Write 1'b to reset the DWC status flags.
14:12	RESERVED	R/W	000b	Reserved. Do not change from the default reset value.
11:8	DWC_GLITCH_FILT[3:0]	R/W	0000b	Digital window comparator glitch rejection filter control. Comparator flag is set only when ADC data exceeds the threshold for consecutive number of DWC_GLITCH_FILT[3:0] cycles.
7	DWC_EN_AIN8	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled
6	DWC_EN_AIN7	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled
5	DWC_EN_AIN6	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled
4	DWC_EN_AIN5	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled
3	DWC_EN_AIN4	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled
2	DWC_EN_AIN3	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled
1	DWC_EN_AIN2	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled
0	DWC_EN_AIN1	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled

8.2.27 DWC_TH_AIN1 Register (Address = 0x22) [Reset = 0xFF00]

Return to the Summary Table.

Figure 8-45. DWC_TH_AIN1 Register

15	14	13	12	11	10	9	8
HIGH_TH_AIN1[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0

Figure 8-45. DWC_TH_AIN1 Register (continued)

LOW_TH_AIN1[7:0]
R/W-00000000b

Table 8-49. DWC_TH_AIN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_AIN1[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_AIN1[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.2.28 DWC_TH_AIN2 Register (Address = 0x23) [Reset = 0xFF00]

Return to the Summary Table.

Figure 8-46. DWC_TH_AIN2 Register

15	14	13	12	11	10	9	8
HIGH_TH_AIN2[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
LOW_TH_AIN2[7:0]							
R/W-00000000b							

Table 8-50. DWC_TH_AIN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_AIN2[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_AIN2[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.2.29 DWC_TH_AIN3 Register (Address = 0x24) [Reset = 0xFF00]

Return to the Summary Table.

Figure 8-47. DWC_TH_AIN3 Register

15	14	13	12	11	10	9	8
HIGH_TH_AIN3[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
LOW_TH_AIN3[7:0]							
R/W-00000000b							

Table 8-51. DWC_TH_AIN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_AIN3[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_AIN3[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.2.30 DWC_TH_AIN4 Register (Address = 0x25) [Reset = 0xFF00]

Return to the Summary Table.

Figure 8-48. DWC_TH_AIN4 Register

15	14	13	12	11	10	9	8
HIGH_TH_AIN4[7:0]							
R/W-11111111b							

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Figure 8-48. DWC_TH_AIN4 Register (continued)

7	6	5	4	3	2	1	0
LOW_TH_AIN4[7:0]							
R/W-00000000b							

Table 8-52. DWC_TH_AIN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_AIN4[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_AIN4[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.2.31 DWC_TH_AIN5 Register (Address = 0x26) [Reset = 0xFF00]

Return to the Summary Table.

Figure 8-49. DWC_TH_AIN5 Register

15	14	13	12	11	10	9	8
HIGH_TH_AIN5[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
LOW_TH_AIN5[7:0]							
R/W-00000000b							

Table 8-53. DWC_TH_AIN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_AIN5[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_AIN5[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.2.32 DWC_TH_AIN6 Register (Address = 0x27) [Reset = 0xFF00]

Return to the Summary Table.

Figure 8-50. DWC_TH_AIN6 Register

15	14	13	12	11	10	9	8
HIGH_TH_AIN6[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
LOW_TH_AIN6[7:0]							
R/W-00000000b							

Table 8-54. DWC_TH_AIN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_AIN6[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_AIN6[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.2.33 DWC_TH_AIN7 Register (Address = 0x28) [Reset = 0xFF00]

Return to the Summary Table.

Figure 8-51. DWC_TH_AIN7 Register

15	14	13	12	11	10	9	8
HIGH_TH_AIN7[7:0]							

Figure 8-51. DWC_TH_AIN7 Register (continued)

R/W-11111111b							
7	6	5	4	3	2	1	0
LOW_TH_AIN7[7:0]							
R/W-00000000b							

Table 8-55. DWC_TH_AIN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_AIN7[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_AIN7[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.2.34 DWC_TH_AIN8 Register (Address = 0x29) [Reset = 0xFF00]

Return to the Summary Table.

Figure 8-52. DWC_TH_AIN8 Register

15	14	13	12	11	10	9	8
HIGH_TH_AIN8[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
LOW_TH_AIN8[7:0]							
R/W-00000000b							

Table 8-56. DWC_TH_AIN8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_AIN8[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_AIN8[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.2.35 DWC_HYS_AIN1_2 Register (Address = 0x2A) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-53. DWC_HYS_AIN1_2 Register

15	14	13	12	11	10	9	8
HYS_AIN2[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
HYS_AIN1[7:0]							
R/W-00000000b							

Table 8-57. DWC_HYS_AIN1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HYS_AIN2[7:0]	R/W	00000000b	8-bit hysteresis for high and low thresholds.
7:0	HYS_AIN1[7:0]	R/W	00000000b	8-bit hysteresis for high and low thresholds

8.2.36 DWC_HYS_AIN3_4 Register (Address = 0x2B) [Reset = 0xFF00]

Return to the Summary Table.

Figure 8-54. DWC_HYS_AIN3_4 Register

15	14	13	12	11	10	9	8
HYS_AIN4[7:0]							

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Figure 8-54. DWC_HYS_AIN3_4 Register (continued)

R/W-11111111b							
7	6	5	4	3	2	1	0
HYS_AIN3[7:0]							
R/W-00000000b							

Table 8-58. DWC_HYS_AIN3_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HYS_AIN4[7:0]	R/W	11111111b	8-bit hysteresis for high and low thresholds
7:0	HYS_AIN3[7:0]	R/W	00000000b	8-bit hysteresis for high and low thresholds

8.2.37 DWC_HYS_AIN5_6 Register (Address = 0x2C) [Reset = 0xFF00]

Return to the Summary Table.

Figure 8-55. DWC_HYS_AIN5_6 Register

15	14	13	12	11	10	9	8
HYS_AIN6[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
HYS_AIN5[7:0]							
R/W-00000000b							

Table 8-59. DWC_HYS_AIN5_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HYS_AIN6[7:0]	R/W	11111111b	8-bit hysteresis for high and low thresholds
7:0	HYS_AIN5[7:0]	R/W	00000000b	8-bit hysteresis for high and low thresholds

8.2.38 DWC_HYS_AIN7_8 Register (Address = 0x2D) [Reset = 0xFF00]

Return to the Summary Table.

Figure 8-56. DWC_HYS_AIN7_8 Register

15	14	13	12	11	10	9	8
HYS_AIN8[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
HYS_AIN7[7:0]							
R/W-00000000b							

Table 8-60. DWC_HYS_AIN7_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HYS_AIN8[7:0]	R/W	11111111b	8-bit hysteresis for high and low thresholds
7:0	HYS_AIN7[7:0]	R/W	00000000b	8-bit hysteresis for high and low thresholds

8.2.39 TP_CFG Register (Address = 0x2E) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-57. TP_CFG Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-000000000b							
7	6	5	4	3	2	1	0

Figure 8-57. TP_CFG Register (continued)

RESERVED	TP_MODE[2:0]	RESERVED	TP_DIS_IDX	TP_UPD_MODE	TP_EN
R/W-000000000b	R/W-000b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-61. TP_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:7	RESERVED	R/W	000000000b	Reserved. Do not change from the default reset value.
6:4	TP_MODE[2:0]	R/W	000b	Test pattern mode selection. 000b = Constant pattern 001b = Reserved 010b = Ramp pattern 011b = Reserved 100b = Reserved 101b = Reserved
3	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
2	TP_DIS_IDX	R/W	0b	When 1'b channel index insertion in test pattern is disabled.
1	TP_UPD_MODE	R/W	0b	Test pattern increment mode. 0b = Increment happens at channel frame boundary. 1b = Increment happens at every CONVST.
0	TP_EN	R/W	0b	Test pattern enable for AIN1 to AIN8. 0b = ADC conversion result is launched on the data interface 1b = Digital test pattern is launched on the data interface

8.2.40 TP_AIN1 Register (Address = 0x2F) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-58. TP_AIN1 Register

15	14	13	12	11	10	9	8
TP_AIN1[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_AIN1[15:0]							
R/W-0000000000000000b							

Table 8-62. TP_AIN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_AIN1[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for AIN1. In the ramp pattern mode, TP_AIN1 controls step size for AIN1 to AIN8.

8.2.41 TP_AIN2 Register (Address = 0x30) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-59. TP_AIN2 Register

15	14	13	12	11	10	9	8
TP_AIN2[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_AIN2[15:0]							
R/W-0000000000000000b							

Table 8-63. TP_AIN2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_AIN2[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for AIN2.

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8.2.42 TP_AIN3 Register (Address = 0x31) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-60. TP_AIN3 Register

15	14	13	12	11	10	9	8
TP_AIN3[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_AIN3[15:0]							
R/W-0000000000000000b							

Table 8-64. TP_AIN3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_AIN3[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for AIN3.

8.2.43 TP_AIN4 Register (Address = 0x32) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-61. TP_AIN4 Register

15	14	13	12	11	10	9	8
TP_AIN4[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_AIN4[15:0]							
R/W-0000000000000000b							

Table 8-65. TP_AIN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_AIN4[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for AIN4.

8.2.44 TP_AIN5 Register (Address = 0x33) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-62. TP_AIN5 Register

15	14	13	12	11	10	9	8
TP_AIN5[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_AIN5[15:0]							
R/W-0000000000000000b							

Table 8-66. TP_AIN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_AIN5[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for AIN5.

8.2.45 TP_AIN6 Register (Address = 0x34) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-63. TP_AIN6 Register

15	14	13	12	11	10	9	8

Figure 8-63. TP_AIN6 Register (continued)

TP_AIN6[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_AIN6[15:0]							
R/W-0000000000000000b							

Table 8-67. TP_AIN6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_AIN6[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for AIN6.

8.2.46 TP_AIN7 Register (Address = 0x35) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-64. TP_AIN7 Register

15	14	13	12	11	10	9	8
TP_AIN7[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_AIN7[15:0]							
R/W-0000000000000000b							

Table 8-68. TP_AIN7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_AIN7[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for AIN7.

8.2.47 TP_AIN8 Register (Address = 0x36) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-65. TP_AIN8 Register

15	14	13	12	11	10	9	8
TP_AIN8[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_AIN8[15:0]							
R/W-0000000000000000b							

Table 8-69. TP_AIN8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_AIN8[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for AIN8.

8.2.48 GEN_CFG5 Register (Address = 0x37) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-66. GEN_CFG5 Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-00000000000b							
7	6	5	4	3	2	1	0

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Figure 8-66. GEN_CFG5 Register (continued)

RESERVED	RESERVED	RESERVED	OFS_CORR_DIS	GAN_CORR_DIS
R/W-00000000000b	R/W-0b	R/W-00b	R/W-0b	R/W-0b

Table 8-70. GEN_CFG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:5	RESERVED	R/W	00000000000b	Reserved. Do not change from the default reset value.
4	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
3:2	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
1	OFS_CORR_DIS	R/W	0b	System offset correction disable for AIN1 to AIN8. 0b = Enabled 1b = Disabled
0	GAN_CORR_DIS	R/W	0b	System gain correction disable for AIN1 to AIN8. 0b = Enabled 1b = Disabled

8.2.49 CH_XTALK_AIN1_8 Register (Address = 0x3B) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-67. CH_XTALK_AIN1_8 Register

15	14	13	12	11	10	9	8
RESERVED				CH_XTALK_AIN1_8	RESERVED		
R/W-0000b				R/W-0b	R/W-0000000000b		
7	6	5	4	3	2	1	0
RESERVED							RESERVED
R/W-0000000000b							R-0b

Table 8-71. CH_XTALK_AIN1_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0000b	Reserved. Do not change from the default reset value.
11	CH_XTALK_AIN1_8	R/W	0b	Set this bit to 1b when CH_XTALK_LOW_SPEED is 1b. 0b = Disabled 1b = Enabled
10:1	RESERVED	R/W	0000000000b	Reserved. Do not change from the default reset value.
0	RESERVED	R	0b	

8.2.50 DWC_FLAG_AIN1_8 Register (Address = 0x3E) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-68. DWC_FLAG_AIN1_8 Register

15	14	13	12	11	10	9	8
HIGH_FLAG_AIN8	HIGH_FLAG_AIN7	HIGH_FLAG_AIN6	HIGH_FLAG_AIN5	HIGH_FLAG_AIN4	HIGH_FLAG_AIN3	HIGH_FLAG_AIN2	HIGH_FLAG_AIN1
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b
7	6	5	4	3	2	1	0
LOW_FLAG_AIN8	LOW_FLAG_AIN7	LOW_FLAG_AIN6	LOW_FLAG_AIN5	LOW_FLAG_AIN4	LOW_FLAG_AIN3	LOW_FLAG_AIN2	LOW_FLAG_AIN1
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-72. DWC_FLAG_AIN1_8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	HIGH_FLAG_AIN8	R	0b	Digital window comparator high flag for AIN8.
14	HIGH_FLAG_AIN7	R	0b	Digital window comparator high flag for AIN7.
13	HIGH_FLAG_AIN6	R	0b	Digital window comparator high flag for AIN6.
12	HIGH_FLAG_AIN5	R	0b	Digital window comparator high flag for AIN5.
11	HIGH_FLAG_AIN4	R	0b	Digital window comparator high flag for AIN4.
10	HIGH_FLAG_AIN3	R	0b	Digital window comparator high flag for AIN3.

Table 8-72. DWC_FLAG_AIN1_8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	HIGH_FLAG_AIN2	R	0b	Digital window comparator high flag for AIN2.
8	HIGH_FLAG_AIN1	R	0b	Digital window comparator high flag for AIN1.
7	LOW_FLAG_AIN8	R	0b	Digital window comparator low flag for AIN8.
6	LOW_FLAG_AIN7	R	0b	Digital window comparator low flag for AIN7.
5	LOW_FLAG_AIN6	R	0b	Digital window comparator low flag for AIN6.
4	LOW_FLAG_AIN5	R	0b	Digital window comparator low flag for AIN5.
3	LOW_FLAG_AIN4	R	0b	Digital window comparator low flag for AIN4.
2	LOW_FLAG_AIN3	R	0b	Digital window comparator low flag for AIN3.
1	LOW_FLAG_AIN2	R	0b	Digital window comparator low flag for AIN2.
0	LOW_FLAG_AIN1	R	0b	Digital window comparator low flag for AIN1.

8.3 AIN9 - AIN16 Channel Registers

Table 8-73 lists the memory-mapped registers for the AIN9 - AIN16 Channel registers. All register offset addresses not listed in Table 8-73 should be considered as reserved locations and the register contents should not be modified.

Table 8-73. AIN9 - AIN16 Channel

Address	Acronym	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x08	PGA_CONFIG_AIN15_16	CME_CORR_EN_AIN15	CM_RANGE_AIN15[2:0]			RESERVED	INPUT_RANGE_AIN15[2:0]		
		CME_CORR_EN_AIN16	CM_RANGE_AIN16[2:0]			RESERVED	INPUT_RANGE_AIN16[2:0]		
0x09	PGA_CONFIG_AIN13_14	CME_CORR_EN_AIN13	CM_RANGE_AIN13[2:0]			RESERVED	INPUT_RANGE_AIN13[2:0]		
		CME_CORR_EN_AIN14	CM_RANGE_AIN14[2:0]			RESERVED	INPUT_RANGE_AIN14[2:0]		
0x0A	PGA_CONFIG_AIN11_12	CME_CORR_EN_AIN11	CM_RANGE_AIN11[2:0]			RESERVED	INPUT_RANGE_AIN11[2:0]		
		CME_CORR_EN_AIN12	CM_RANGE_AIN12[2:0]			RESERVED	INPUT_RANGE_AIN12[2:0]		
0x0B	PGA_CONFIG_AIN9_10	CME_CORR_EN_AIN9	CM_RANGE_AIN9[2:0]			RESERVED	INPUT_RANGE_AIN9[2:0]		
		CME_CORR_EN_AIN10	CM_RANGE_AIN10[2:0]			RESERVED	INPUT_RANGE_AIN10[2:0]		
0x0C	PGA_BW_SEL_AIN9_16	PGA_BW_SEL_AIN9[1:0]		PGA_BW_SEL_AIN10[1:0]		PGA_BW_SEL_AIN11[1:0]		PGA_BW_SEL_AIN12[1:0]	
		PGA_BW_SEL_AIN13[1:0]		PGA_BW_SEL_AIN14[1:0]		PGA_BW_SEL_AIN15[1:0]		PGA_BW_SEL_AIN16[1:0]	
0x0D	PHASE_DELAY_AIN15_16	PHASE_DELAY_AIN15[7:0]							
		PHASE_DELAY_AIN16[7:0]							
0x0E	PHASE_DELAY_AIN13_14	PHASE_DELAY_AIN13[7:0]							
		PHASE_DELAY_AIN14[7:0]							
0x0F	PHASE_DELAY_AIN11_12	PHASE_DELAY_AIN11[7:0]							
		PHASE_DELAY_AIN12[7:0]							
0x10	PHASE_DELAY_AIN9_10	PHASE_DELAY_AIN9[7:0]							
		PHASE_DELAY_AIN10[7:0]							
0x11	OFS_AIN16	RESERVED						OFS_AIN16[9:0]	
		OFS_AIN16[9:0]							
0x12	OFS_AIN15	RESERVED						OFS_AIN15[9:0]	
		OFS_AIN15[9:0]							
0x13	OFS_AIN14	RESERVED						OFS_AIN14[9:0]	
		OFS_AIN14[9:0]							
0x14	OFS_AIN13	RESERVED						OFS_AIN13[9:0]	
		OFS_AIN13[9:0]							
0x15	OFS_AIN12	RESERVED						OFS_AIN12[9:0]	
		OFS_AIN12[9:0]							
0x16	OFS_AIN11	RESERVED						OFS_AIN11[9:0]	
		OFS_AIN11[9:0]							
0x17	OFS_AIN10	RESERVED						OFS_AIN10[9:0]	
		OFS_AIN10[9:0]							
0x18	OFS_AIN9	RESERVED						OFS_AIN9[9:0]	
		OFS_AIN9[9:0]							
0x19	GAN_AIN16	RESERVED		GAN_AIN16[13:0]					
		GAN_AIN16[13:0]							
0x1A	GAN_AIN15	RESERVED		GAN_AIN15[13:0]					
		GAN_AIN15[13:0]							
0x1B	GAN_AIN14	RESERVED		GAN_AIN14[13:0]					
		GAN_AIN14[13:0]							
0x1C	GAN_AIN13	RESERVED		GAN_AIN13[13:0]					
		GAN_AIN13[13:0]							

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Table 8-73. AIN9 - AIN16 Channel (continued)

Address	Acronym	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1D	GAN_AIN12	RESERVED		GAN_AIN12[13:0]					
		GAN_AIN12[13:0]							
0x1E	GAN_AIN11	RESERVED		GAN_AIN11[13:0]					
		GAN_AIN11[13:0]							
0x1F	GAN_AIN10	RESERVED		GAN_AIN10[13:0]					
		GAN_AIN10[13:0]							
0x20	GAN_AIN9	RESERVED		GAN_AIN9[13:0]					
		GAN_AIN9[13:0]							
0x21	DWC_CFG	DWC_STAT_RST	RESERVED			DWC_GLITCH_FILT[3:0]			
		DWC_EN_AIN9	DWC_EN_AIN10	DWC_EN_AIN11	DWC_EN_AIN12	DWC_EN_AIN13	DWC_EN_AIN14	DWC_EN_AIN15	DWC_EN_AIN16
0x22	DWC_TH_AIN16	HIGH_TH_AIN16[7:0]							
		LOW_TH_AIN16[7:0]							
0x23	DWC_TH_AIN15	HIGH_TH_AIN15[7:0]							
		LOW_TH_AIN15[7:0]							
0x24	DWC_TH_AIN14	HIGH_TH_AIN14[7:0]							
		LOW_TH_AIN14[7:0]							
0x25	DWC_TH_AIN13	HIGH_TH_AIN13[7:0]							
		LOW_TH_AIN13[7:0]							
0x26	DWC_TH_AIN12	HIGH_TH_AIN12[7:0]							
		LOW_TH_AIN12[7:0]							
0x27	DWC_TH_AIN11	HIGH_TH_AIN11[7:0]							
		LOW_TH_AIN11[7:0]							
0x28	DWC_TH_AIN10	HIGH_TH_AIN10[7:0]							
		LOW_TH_AIN10[7:0]							
0x29	DWC_TH_AIN9	HIGH_TH_AIN9[7:0]							
		LOW_TH_AIN9[7:0]							
0x2A	DWC_HYS_AIN15_16	HYS_AIN15[7:0]							
		HYS_AIN16[7:0]							
0x2B	DWC_HYS_AIN13_14	HYS_AIN13[7:0]							
		HYS_AIN14[7:0]							
0x2C	DWC_HYS_AIN11_12	HYS_AIN11[7:0]							
		HYS_AIN12[7:0]							
0x2D	DWC_HYS_AIN9_10	HYS_AIN9[7:0]							
		HYS_AIN10[7:0]							
0x2E	TP_CFG	RESERVED							
		RESERVED	TP_MODE[2:0]			RESERVED	TP_DIS_IDX	TP_UPD_MODE	TP_EN
0x2F	TP_AIN16	TP_AIN16[15:0]							
		TP_AIN16[15:0]							
0x30	TP_AIN15	TP_AIN15[15:0]							
		TP_AIN15[15:0]							
0x31	TP_AIN14	TP_AIN14[15:0]							
		TP_AIN14[15:0]							
0x32	TP_AIN13	TP_AIN13[15:0]							
		TP_AIN13[15:0]							
0x33	TP_AIN12	TP_AIN12[15:0]							
		TP_AIN12[15:0]							
0x34	TP_AIN11	TP_AIN11[15:0]							
		TP_AIN11[15:0]							
0x35	TP_AIN10	TP_AIN10[15:0]							
		TP_AIN10[15:0]							
0x36	TP_AIN9	TP_AIN9[15:0]							
		TP_AIN9[15:0]							

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Table 8-73. AIN9 - AIN16 Channel (continued)

Address	Acronym	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x37	GEN_CFG5	RESERVED							
		RESERVED						OFS_CORR_DIS	GAN_CORR_DIS
0x3B	CH_XTALK_AIN9_16	RESERVED				CH_XTALK_AIN9_16	RESERVED		
		RESERVED							
0x3E	DWC_FLAG_AIN9_16	HIGH_FLAG_AIN9	HIGH_FLAG_AIN10	HIGH_FLAG_AIN11	HIGH_FLAG_AIN12	HIGH_FLAG_AIN13	HIGH_FLAG_AIN14	HIGH_FLAG_AIN15	HIGH_FLAG_AIN16
		LOW_FLAG_AIN9	LOW_FLAG_AIN10	LOW_FLAG_AIN11	LOW_FLAG_AIN12	LOW_FLAG_AIN13	LOW_FLAG_AIN14	LOW_FLAG_AIN15	LOW_FLAG_AIN16

Complex bit access types are encoded to fit into small table cells. Table 8-74 shows the codes that are used for access types in this section.

Table 8-74. AIN9 - AIN16 Channel Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.3.1 PGA_CONFIG_AIN15_16 Register (Address = 0x08) [Reset = 0x0000]

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Figure 8-69. PGA_CONFIG_AIN15_16 Register

15	14	13	12	11	10	9	8
CME_CORR_EN_AIN15	CM_RANGE_AIN15[2:0]			RESERVED	INPUT_RANGE_AIN15[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		
7	6	5	4	3	2	1	0
CME_CORR_EN_AIN16	CM_RANGE_AIN16[2:0]			RESERVED	INPUT_RANGE_AIN16[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		

Table 8-75. PGA_CONFIG_AIN15_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CME_CORR_EN_AIN15	R/W	0b	Common mode error correction enable. 0b = Disabled 1b = Enabled
14:12	CM_RANGE_AIN15[2:0]	R/W	000b	Select input signal type. 000b = Differential 101b = Single ended 110b = Single ended open wire safe
11	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
10:8	INPUT_RANGE_AIN15[2:0]	R/W	000b	AIN15 analog input range selection. 000b = ±5V 001b = ±25V 010b = ±2.5V 011b = ±6.25V 100b = ±10V 101b = ±12.5V 110b = ±50V 111b = Reserved

Table 8-75. PGA_CONFIG_AIN15_16 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CME_CORR_EN_AIN16	R/W	0b	Common mode error correction enable. 0b = Disabled 1b = Enabled
6:4	CM_RANGE_AIN16[2:0]	R/W	000b	Select input signal type. 000b = Differential 101b = Single ended 110b = Single ended open wire safe
3	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
2:0	INPUT_RANGE_AIN16[2:0]	R/W	000b	AIN16 analog input range selection. 000b = ±5V 001b = ±25V 010b = ±2.5V 011b = ±6.25V 100b = ±10V 101b = ±12.5V 110b = ±50V 111b = Reserved

8.3.2 PGA_CONFIG_AIN13_14 Register (Address = 0x09) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-70. PGA_CONFIG_AIN13_14 Register

15	14	13	12	11	10	9	8
CME_CORR_EN_AIN13	CM_RANGE_AIN13[2:0]			RESERVED	INPUT_RANGE_AIN13[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		
7	6	5	4	3	2	1	0
CME_CORR_EN_AIN14	CM_RANGE_AIN14[2:0]			RESERVED	INPUT_RANGE_AIN14[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		

Table 8-76. PGA_CONFIG_AIN13_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CME_CORR_EN_AIN13	R/W	0b	Common mode error correction enable. 0b = Disabled 1b = Enabled
14:12	CM_RANGE_AIN13[2:0]	R/W	000b	Select input signal type. 000b = Differential 101b = Single ended 110b = Single ended open wire safe
11	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
10:8	INPUT_RANGE_AIN13[2:0]	R/W	000b	AIN13 analog input range selection. 000b = ±5V 001b = ±25V 010b = ±2.5V 011b = ±6.25V 100b = ±10V 101b = ±12.5V 110b = ±50V 111b = Reserved
7	CME_CORR_EN_AIN14	R/W	0b	Common mode error correction enable. 0b = Disabled 1b = Enabled
6:4	CM_RANGE_AIN14[2:0]	R/W	000b	Select input signal type. 000b = Differential 101b = Single ended 110b = Single ended open wire safe
3	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
2:0	INPUT_RANGE_AIN14[2:0]	R/W	000b	AIN14 analog input range selection. 000b = ±5V 001b = ±25V 010b = ±2.5V 011b = ±6.25V 100b = ±10V 101b = ±12.5V 110b = ±50V 111b = Reserved

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8.3.3 PGA_CONFIG_AIN11_12 Register (Address = 0x0A) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-71. PGA_CONFIG_AIN11_12 Register

15	14	13	12	11	10	9	8
CME_CORR_EN_AIN11	CM_RANGE_AIN11[2:0]			RESERVED	INPUT_RANGE_AIN11[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		
7	6	5	4	3	2	1	0
CME_CORR_EN_AIN12	CM_RANGE_AIN12[2:0]			RESERVED	INPUT_RANGE_AIN12[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		

Table 8-77. PGA_CONFIG_AIN11_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CME_CORR_EN_AIN11	R/W	0b	Common mode error correction enable. 0b = Disabled 1b = Enabled
14:12	CM_RANGE_AIN11[2:0]	R/W	000b	Select input signal type. 000b = Differential 101b = Single ended 110b = Single ended open wire safe
11	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
10:8	INPUT_RANGE_AIN11[2:0]	R/W	000b	AIN11 analog input range selection. 000b = ±5V 001b = ±25V 010b = ±2.5V 011b = ±6.25V 100b = ±10V 101b = ±12.5V 110b = ±50V 111b = Reserved
7	CME_CORR_EN_AIN12	R/W	0b	Common mode error correction enable. 0b = Disabled 1b = Enabled
6:4	CM_RANGE_AIN12[2:0]	R/W	000b	Select input signal type. 000b = Fully Differential 101b = Single ended 110b = Single ended open wire safe
3	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
2:0	INPUT_RANGE_AIN12[2:0]	R/W	000b	AIN12 analog input range selection. 000b = ±5V 001b = ±25V 010b = ±2.5V 011b = ±6.25V 100b = ±10V 101b = ±12.5V 110b = ±50V 111b = Reserved

8.3.4 PGA_CONFIG_AIN9_10 Register (Address = 0x0B) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-72. PGA_CONFIG_AIN9_10 Register

15	14	13	12	11	10	9	8
CME_CORR_EN_AIN9	CM_RANGE_AIN9[2:0]			RESERVED	INPUT_RANGE_AIN9[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		
7	6	5	4	3	2	1	0
CME_CORR_EN_AIN10	CM_RANGE_AIN10[2:0]			RESERVED	INPUT_RANGE_AIN10[2:0]		
R/W-0b	R/W-000b			R/W-0b	R/W-000b		

Table 8-78. PGA_CONFIG_AIN9_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CME_CORR_EN_AIN9	R/W	0b	Common mode error correction enable. 0b = Disabled 1b = Enabled
14:12	CM_RANGE_AIN9[2:0]	R/W	000b	Select input signal type. 000b = Differential 101b = Single ended 110b = Single ended open wire safe
11	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
10:8	INPUT_RANGE_AIN9[2:0]	R/W	000b	AIN9 analog input range selection. 000b = ±5V 001b = ±25V 010b = ±2.5V 011b = ±6.25V 100b = ±10V 101b = ±12.5V 110b = ±50V 111b = Reserved
7	CME_CORR_EN_AIN10	R/W	0b	Common mode error correction enable. 0b = Disabled 1b = Enabled
6:4	CM_RANGE_AIN10[2:0]	R/W	000b	Select input signal type. 000b = Differential 101b = Single ended 110b = Single ended open wire safe
3	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
2:0	INPUT_RANGE_AIN10[2:0]	R/W	000b	AIN10 analog input range selection. 000b = ±5V 001b = ±25V 010b = ±2.5V 011b = ±6.25V 100b = ±10V 101b = ±12.5V 110b = ±50V 111b = Reserved

8.3.5 PGA_BW_SEL_AIN9_16 Register (Address = 0x0C) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-73. PGA_BW_SEL_AIN9_16 Register

15	14	13	12	11	10	9	8
PGA_BW_SEL_AIN9[1:0]		PGA_BW_SEL_AIN10[1:0]		PGA_BW_SEL_AIN11[1:0]		PGA_BW_SEL_AIN12[1:0]	
R/W-00b		R/W-00b		R/W-00b		R/W-00b	
7	6	5	4	3	2	1	0
PGA_BW_SEL_AIN13[1:0]		PGA_BW_SEL_AIN14[1:0]		PGA_BW_SEL_AIN15[1:0]		PGA_BW_SEL_AIN16[1:0]	
R/W-00b		R/W-00b		R/W-00b		R/W-00b	

Table 8-79. PGA_BW_SEL_AIN9_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	PGA_BW_SEL_AIN9[1:0]	R/W	00b	AIN9 analog low pass filter configuration control. 00b = Low-bandwidth 01b = Wide-bandwidth 10b = Reserved 11b = Reserved
13:12	PGA_BW_SEL_AIN10[1:0]	R/W	00b	AIN10 analog low pass filter configuration control. 00b = Low-bandwidth 01b = Wide-bandwidth 10b = Reserved 11b = Reserved
11:10	PGA_BW_SEL_AIN11[1:0]	R/W	00b	AIN11 analog low pass filter configuration control. 00b = Low-bandwidth 01b = Wide-bandwidth 10b = Reserved 11b = Reserved
9:8	PGA_BW_SEL_AIN12[1:0]	R/W	00b	AIN12 analog low pass filter configuration control. 00b = Low-bandwidth 01b = Wide-bandwidth 10b = Reserved 11b = Reserved

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Table 8-79. PGA_BW_SEL_AIN9_16 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:6	PGA_BW_SEL_AIN13[1:0]	R/W	00b	AIN13 analog low pass filter configuration control. 00b = Low-bandwidth 01b = Wide-bandwidth 10b = Reserved 11b = Reserved
5:4	PGA_BW_SEL_AIN14[1:0]	R/W	00b	AIN14analog low pass filter configuration control. 00b = Low-bandwidth 01b = Wide-bandwidth 10b = Reserved 11b = Reserved
3:2	PGA_BW_SEL_AIN15[1:0]	R/W	00b	AIN15 analog low pass filter configuration control. 00b = Low-bandwidth 01b = Wide-bandwidth 10b = Reserved 11b = Reserved
1:0	PGA_BW_SEL_AIN16[1:0]	R/W	00b	AIN16 analog low pass filter configuration control. 00b = Low-bandwidth 01b = Wide-bandwidth 10b = Reserved 11b = Reserved

8.3.6 PHASE_DELAY_AIN15_16 Register (Address = 0x0D) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-74. PHASE_DELAY_AIN15_16 Register

15	14	13	12	11	10	9	8
PHASE_DELAY_AIN15[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
PHASE_DELAY_AIN16[7:0]							
R/W-00000000b							

Table 8-80. PHASE_DELAY_AIN15_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	PHASE_DELAY_AIN15[7:0]	R/W	00000000b	Phase delay = n* ADC CONVST CLK, where n is 0 to 255.
7:0	PHASE_DELAY_AIN16[7:0]	R/W	00000000b	Phase delay = n* ADC CONVST CLK, where n is 0 to 255.

8.3.7 PHASE_DELAY_AIN13_14 Register (Address = 0x0E) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-75. PHASE_DELAY_AIN13_14 Register

15	14	13	12	11	10	9	8
PHASE_DELAY_AIN13[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
PHASE_DELAY_AIN14[7:0]							
R/W-00000000b							

Table 8-81. PHASE_DELAY_AIN13_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	PHASE_DELAY_AIN13[7:0]	R/W	00000000b	Phase delay = n* CONVST_CLK, where n is 0 to 255.
7:0	PHASE_DELAY_AIN14[7:0]	R/W	00000000b	Phase delay = n* CONVST_CLK, where n is 0 to 255.

8.3.8 PHASE_DELAY_AIN11_12 Register (Address = 0x0F) [Reset = 0x0000]

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Figure 8-76. PHASE_DELAY_AIN11_12 Register

15	14	13	12	11	10	9	8
PHASE_DELAY_AIN11[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
PHASE_DELAY_AIN12[7:0]							
R/W-00000000b							

Table 8-82. PHASE_DELAY_AIN11_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	PHASE_DELAY_AIN11[7:0]	R/W	00000000b	Phase delay = n* CONVST_CLK, where n is 0 to 255.
7:0	PHASE_DELAY_AIN12[7:0]	R/W	00000000b	Phase delay = n* CONVST_CLK, where n is 0 to 255.

8.3.9 PHASE_DELAY_AIN9_10 Register (Address = 0x10) [Reset = 0x0000]

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Figure 8-77. PHASE_DELAY_AIN9_10 Register

15	14	13	12	11	10	9	8
PHASE_DELAY_AIN9[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
PHASE_DELAY_AIN10[7:0]							
R/W-00000000b							

Table 8-83. PHASE_DELAY_AIN9_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	PHASE_DELAY_AIN9[7:0]	R/W	00000000b	Phase delay = n* CONVST_CLK, where n is 0 to 255.
7:0	PHASE_DELAY_AIN10[7:0]	R/W	00000000b	Phase delay = n* CONVST_CLK, where n is 0 to 255.

8.3.10 OFS_AIN16 Register (Address = 0x11) [Reset = 0x0000]

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Figure 8-78. OFS_AIN16 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_AIN16[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_AIN16[9:0]							
R/W-0000000000b							

Table 8-84. OFS_AIN16 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_AIN16[9:0]	R/W	0000000000b	Offset correction register for AIN16. The offset value is in two's complement representation. The offset operation precedes the gain operation.

8.3.11 OFS_AIN15 Register (Address = 0x12) [Reset = 0x0000]

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Figure 8-79. OFS_AIN15 Register

15	14	13	12	11	10	9	8

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Figure 8-79. OFS_AIN15 Register (continued)

RESERVED						OFS_AIN15[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_AIN15[9:0]							
R/W-0000000000b							

Table 8-85. OFS_AIN15 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_AIN15[9:0]	R/W	0000000000b	Offset correction register for AIN15. The offset value is in two's complement representation. The offset operation precedes the gain operation.

8.3.12 OFS_AIN14 Register (Address = 0x13) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-80. OFS_AIN14 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_AIN14[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_AIN14[9:0]							
R/W-0000000000b							

Table 8-86. OFS_AIN14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_AIN14[9:0]	R/W	0000000000b	Offset correction register for AIN14. The offset value is in two's complement representation. The offset operation precedes the gain operation.

8.3.13 OFS_AIN13 Register (Address = 0x14) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-81. OFS_AIN13 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_AIN13[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_AIN13[9:0]							
R/W-0000000000b							

Table 8-87. OFS_AIN13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_AIN13[9:0]	R/W	0000000000b	Offset correction register for AIN13. The offset value is in two's complement representation. The offset operation precedes the gain operation.

8.3.14 OFS_AIN12 Register (Address = 0x15) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-82. OFS_AIN12 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_AIN12[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_AIN12[9:0]							
R/W-0000000000b							

Table 8-88. OFS_AIN12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_AIN12[9:0]	R/W	0000000000b	Offset correction register for AIN12. The offset value is in two's complement representation. The offset operation precedes the gain operation.

8.3.15 OFS_AIN11 Register (Address = 0x16) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-83. OFS_AIN11 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_AIN11[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_AIN11[9:0]							
R/W-0000000000b							

Table 8-89. OFS_AIN11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_AIN11[9:0]	R/W	0000000000b	Offset correction register for AIN11. The offset value is in two's complement representation. The offset operation precedes the gain operation.

8.3.16 OFS_AIN10 Register (Address = 0x17) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-84. OFS_AIN10 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_AIN10[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_AIN10[9:0]							
R/W-0000000000b							

Table 8-90. OFS_AIN10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_AIN10[9:0]	R/W	0000000000b	Offset correction register for AIN10. The offset value is in two's complement representation. The offset operation precedes the gain operation.

8.3.17 OFS_AIN9 Register (Address = 0x18) [Reset = 0x0000]

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Figure 8-85. OFS_AIN9 Register

15	14	13	12	11	10	9	8
RESERVED						OFS_AIN9[9:0]	
R/W-000000b						R/W-0000000000b	
7	6	5	4	3	2	1	0
OFS_AIN9[9:0]							
R/W-0000000000b							

Table 8-91. OFS_AIN9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R/W	000000b	Reserved. Do not change from the default reset value.
9:0	OFS_AIN9[9:0]	R/W	0000000000b	Offset correction register for AIN9. The offset value is in two's complement representation. The offset operation precedes the gain operation.

8.3.18 GAN_AIN16 Register (Address = 0x19) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-86. GAN_AIN16 Register

15	14	13	12	11	10	9	8
RESERVED		GAN_AIN16[13:0]					
R/W-00b		R/W-00000000000000b					
7	6	5	4	3	2	1	0
GAN_AIN16[13:0]							
R/W-00000000000000b							

Table 8-92. GAN_AIN16 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13:0	GAN_AIN16[13:0]	R/W	00000000000000b	Gain correction register for AIN16. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_AINn[13:0] / 10000h).

8.3.19 GAN_AIN15 Register (Address = 0x1A) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-87. GAN_AIN15 Register

15	14	13	12	11	10	9	8
RESERVED		GAN_AIN15[13:0]					
R/W-00b		R/W-00000000000000b					
7	6	5	4	3	2	1	0
GAN_AIN15[13:0]							
R/W-00000000000000b							

Table 8-93. GAN_AIN15 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13:0	GAN_AIN15[13:0]	R/W	00000000000000b	Gain correction register for AIN15. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_AINn[13:0] / 10000h).

8.3.20 GAN_AIN14 Register (Address = 0x1B) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-88. GAN_AIN14 Register

15	14	13	12	11	10	9	8
RESERVED		GAN_AIN14[13:0]					
R/W-00b		R/W-00000000000000b					
7	6	5	4	3	2	1	0
GAN_AIN14[13:0]							
R/W-00000000000000b							

Table 8-94. GAN_AIN14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13:0	GAN_AIN14[13:0]	R/W	00000000000000b	Gain correction register for AIN14. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_AINn[13:0] / 10000h).

8.3.21 GAN_AIN13 Register (Address = 0x1C) [Reset = 0x0000]

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Figure 8-89. GAN_AIN13 Register

15	14	13	12	11	10	9	8
RESERVED		GAN_AIN13[13:0]					
R/W-00b		R/W-00000000000000b					
7	6	5	4	3	2	1	0
GAN_AIN13[13:0]							
R/W-00000000000000b							

Table 8-95. GAN_AIN13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13:0	GAN_AIN13[13:0]	R/W	00000000000000b	Gain correction register for AIN13. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_AINn[13:0] / 10000h).

8.3.22 GAN_AIN12 Register (Address = 0x1D) [Reset = 0x0000]

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Figure 8-90. GAN_AIN12 Register

15	14	13	12	11	10	9	8
RESERVED		GAN_AIN12[13:0]					
R/W-00b		R/W-00000000000000b					
7	6	5	4	3	2	1	0
GAN_AIN12[13:0]							
R/W-00000000000000b							

Table 8-96. GAN_AIN12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.

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Table 8-96. GAN_AIN12 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:0	GAN_AIN12[13:0]	R/W	0000000000000b	Gain correction register for AIN12. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_AINn[13:0] / 10000h).

8.3.23 GAN_AIN11 Register (Address = 0x1E) [Reset = 0x0000]

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Figure 8-91. GAN_AIN11 Register

15	14	13	12	11	10	9	8
RESERVED		GAN_AIN11[13:0]					
R/W-00b		R/W-00000000000000b					
7	6	5	4	3	2	1	0
GAN_AIN11[13:0]							
R/W-00000000000000b							

Table 8-97. GAN_AIN11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13:0	GAN_AIN11[13:0]	R/W	0000000000000b	Gain correction register for AIN11. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_AINn[13:0] / 10000h).

8.3.24 GAN_AIN10 Register (Address = 0x1F) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-92. GAN_AIN10 Register

15	14	13	12	11	10	9	8
RESERVED		GAN_AIN10[13:0]					
R/W-00b		R/W-00000000000000b					
7	6	5	4	3	2	1	0
GAN_AIN10[13:0]							
R/W-00000000000000b							

Table 8-98. GAN_AIN10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13:0	GAN_AIN10[13:0]	R/W	0000000000000b	Gain correction register for AIN10. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_AINn[13:0] / 10000h).

8.3.25 GAN_AIN9 Register (Address = 0x20) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-93. GAN_AIN9 Register

15	14	13	12	11	10	9	8
RESERVED		GAN_AIN9[13:0]					
R/W-00b		R/W-00000000000000b					
7	6	5	4	3	2	1	0
GAN_AIN9[13:0]							
R/W-00000000000000b							

Figure 8-93. GAN_AIN9 Register (continued)

Table 8-99. GAN_AIN9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
13:0	GAN_AIN9[13:0]	R/W	00000000000000b	Gain correction register for AIN9. The gain correction value is in two's complement representation, and is done after offset operation. During gain operation, the conversion data are multiplied by (1 + GAN_AINn[13:0] / 10000h).

8.3.26 DWC_CFG Register (Address = 0x21) [Reset = 0x0000]

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Figure 8-94. DWC_CFG Register

15	14	13	12	11	10	9	8
DWC_STAT_RST	RESERVED			DWC_GLITCH_FILT[3:0]			
R/W-0b	R/W-000b			R/W-0000b			
7	6	5	4	3	2	1	0
DWC_EN_AIN9	DWC_EN_AIN10	DWC_EN_AIN11	DWC_EN_AIN12	DWC_EN_AIN13	DWC_EN_AIN14	DWC_EN_AIN15	DWC_EN_AIN16
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-100. DWC_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DWC_STAT_RST	R/W	0b	Digital window comparator reset control. Write 1'b to reset the DWC status flags.
14:12	RESERVED	R/W	000b	Reserved. Do not change from the default reset value.
11:8	DWC_GLITCH_FILT[3:0]	R/W	0000b	Digital window comparator glitch rejection filter control. Comparator flag is set only when ADC data exceeds the threshold for consecutive number of DWC_GLITCH_FILT[3:0] cycles.
7	DWC_EN_AIN9	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled
6	DWC_EN_AIN10	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled
5	DWC_EN_AIN11	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled
4	DWC_EN_AIN12	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled
3	DWC_EN_AIN13	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled
2	DWC_EN_AIN14	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled
1	DWC_EN_AIN15	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled
0	DWC_EN_AIN16	R/W	0b	Digital window comparator enable. 0b = Disabled 1b = Enabled

8.3.27 DWC_TH_AIN16 Register (Address = 0x22) [Reset = 0xFF00]

Return to the Summary Table.

Figure 8-95. DWC_TH_AIN16 Register

15	14	13	12	11	10	9	8
HIGH_TH_AIN16[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0

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Figure 8-95. DWC_TH_AIN16 Register (continued)

LOW_TH_AIN16[7:0]
R/W-00000000b

Table 8-101. DWC_TH_AIN16 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_AIN16[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_AIN16[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.3.28 DWC_TH_AIN15 Register (Address = 0x23) [Reset = 0xFF00]

Return to the Summary Table.

Figure 8-96. DWC_TH_AIN15 Register

15	14	13	12	11	10	9	8
HIGH_TH_AIN15[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
LOW_TH_AIN15[7:0]							
R/W-00000000b							

Table 8-102. DWC_TH_AIN15 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_AIN15[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_AIN15[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.3.29 DWC_TH_AIN14 Register (Address = 0x24) [Reset = 0xFF00]

Return to the Summary Table.

Figure 8-97. DWC_TH_AIN14 Register

15	14	13	12	11	10	9	8
HIGH_TH_AIN14[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
LOW_TH_AIN14[7:0]							
R/W-00000000b							

Table 8-103. DWC_TH_AIN14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_AIN14[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_AIN14[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.3.30 DWC_TH_AIN13 Register (Address = 0x25) [Reset = 0xFF00]

Return to the Summary Table.

Figure 8-98. DWC_TH_AIN13 Register

15	14	13	12	11	10	9	8
HIGH_TH_AIN13[7:0]							
R/W-11111111b							

Figure 8-98. DWC_TH_AIN13 Register (continued)

7	6	5	4	3	2	1	0
LOW_TH_AIN13[7:0]							
R/W-00000000b							

Table 8-104. DWC_TH_AIN13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_AIN13[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_AIN13[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.3.31 DWC_TH_AIN12 Register (Address = 0x26) [Reset = 0xFF00]

Return to the Summary Table.

Figure 8-99. DWC_TH_AIN12 Register

15	14	13	12	11	10	9	8
HIGH_TH_AIN12[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
LOW_TH_AIN12[7:0]							
R/W-00000000b							

Table 8-105. DWC_TH_AIN12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_AIN12[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_AIN12[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.3.32 DWC_TH_AIN11 Register (Address = 0x27) [Reset = 0xFF00]

Return to the Summary Table.

Figure 8-100. DWC_TH_AIN11 Register

15	14	13	12	11	10	9	8
HIGH_TH_AIN11[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
LOW_TH_AIN11[7:0]							
R/W-00000000b							

Table 8-106. DWC_TH_AIN11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_AIN11[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_AIN11[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.3.33 DWC_TH_AIN10 Register (Address = 0x28) [Reset = 0xFF00]

Return to the Summary Table.

Figure 8-101. DWC_TH_AIN10 Register

15	14	13	12	11	10	9	8
HIGH_TH_AIN10[7:0]							

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Figure 8-101. DWC_TH_AIN10 Register (continued)

R/W-11111111b							
7	6	5	4	3	2	1	0
LOW_TH_AIN10[7:0]							
R/W-00000000b							

Table 8-107. DWC_TH_AIN10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_AIN10[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_AIN10[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.3.34 DWC_TH_AIN9 Register (Address = 0x29) [Reset = 0xFF00]

Return to the Summary Table.

Figure 8-102. DWC_TH_AIN9 Register

15	14	13	12	11	10	9	8
HIGH_TH_AIN9[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
LOW_TH_AIN9[7:0]							
R/W-00000000b							

Table 8-108. DWC_TH_AIN9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HIGH_TH_AIN9[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.
7:0	LOW_TH_AIN9[7:0]	R/W	00000000b	MSB aligned low threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.3.35 DWC_HYS_AIN15_16 Register (Address = 0x2A) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-103. DWC_HYS_AIN15_16 Register

15	14	13	12	11	10	9	8
HYS_AIN15[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
HYS_AIN16[7:0]							
R/W-00000000b							

Table 8-109. DWC_HYS_AIN15_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HYS_AIN15[7:0]	R/W	00000000b	8-bit hysteresis for high and low thresholds.
7:0	HYS_AIN16[7:0]	R/W	00000000b	8-bit hysteresis for high and low thresholds.

8.3.36 DWC_HYS_AIN13_14 Register (Address = 0x2B) [Reset = 0xFF00]

Return to the Summary Table.

Figure 8-104. DWC_HYS_AIN13_14 Register

15	14	13	12	11	10	9	8
HYS_AIN13[7:0]							

Figure 8-104. DWC_HYS_AIN13_14 Register (continued)

R/W-11111111b							
7	6	5	4	3	2	1	0
HYS_AIN14[7:0]							
R/W-00000000b							

Table 8-110. DWC_HYS_AIN13_14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HYS_AIN13[7:0]	R/W	11111111b	8-bit hysteresis for high and low thresholds.
7:0	HYS_AIN14[7:0]	R/W	00000000b	8-bit hysteresis for high and low thresholds.

8.3.37 DWC_HYS_AIN11_12 Register (Address = 0x2C) [Reset = 0xFF00]

Return to the Summary Table.

Figure 8-105. DWC_HYS_AIN11_12 Register

15	14	13	12	11	10	9	8
HYS_AIN11[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
HYS_AIN12[7:0]							
R/W-00000000b							

Table 8-111. DWC_HYS_AIN11_12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HYS_AIN11[7:0]	R/W	11111111b	8-bit hysteresis for high and low thresholds.
7:0	HYS_AIN12[7:0]	R/W	00000000b	8-bit hysteresis for high and low thresholds.

8.3.38 DWC_HYS_AIN9_10 Register (Address = 0x2D) [Reset = 0xFF00]

Return to the Summary Table.

Figure 8-106. DWC_HYS_AIN9_10 Register

15	14	13	12	11	10	9	8
HYS_AIN9[7:0]							
R/W-11111111b							
7	6	5	4	3	2	1	0
HYS_AIN10[7:0]							
R/W-00000000b							

Table 8-112. DWC_HYS_AIN9_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	HYS_AIN9[7:0]	R/W	11111111b	8-bit hysteresis for high and low thresholds.
7:0	HYS_AIN10[7:0]	R/W	00000000b	8-bit hysteresis for high and low thresholds.

8.3.39 TP_CFG Register (Address = 0x2E) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-107. TP_CFG Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-000000000b							
7	6	5	4	3	2	1	0

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Figure 8-107. TP_CFG Register (continued)

RESERVED	TP_MODE[2:0]	RESERVED	TP_DIS_IDX	TP_UPD_MODE	TP_EN
R/W-000000000b	R/W-000b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-113. TP_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:7	RESERVED	R/W	000000000b	Reserved. Do not change from the default reset value.
6:4	TP_MODE[2:0]	R/W	000b	Test pattern mode selection. 000b = Constant pattern 001b = Reserved 010b = Ramp pattern 011b = Reserved 100b = Reserved 101b = Reserved
3	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
2	TP_DIS_IDX	R/W	0b	When 1'b channel index insertion in test pattern is disabled.
1	TP_UPD_MODE	R/W	0b	Test pattern increment mode. 0b = Increment happens at channel frame boundary. 1b = Increment happens at every CONVST.
0	TP_EN	R/W	0b	Test pattern enable for AIN9 to AIN16. 0b = ADC conversion result is launched on the data interface 1b = Digital test pattern is launched on the data interface

8.3.40 TP_AIN16 Register (Address = 0x2F) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-108. TP_AIN16 Register

15	14	13	12	11	10	9	8
TP_AIN16[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_AIN16[15:0]							
R/W-0000000000000000b							

Table 8-114. TP_AIN16 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_AIN16[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for AIN16. In the ramp pattern mode, TP_AIN16 controls step size for AIN9 to AIN16.

8.3.41 TP_AIN15 Register (Address = 0x30) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-109. TP_AIN15 Register

15	14	13	12	11	10	9	8
TP_AIN15[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_AIN15[15:0]							
R/W-0000000000000000b							

Table 8-115. TP_AIN15 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_AIN15[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for AIN15.

8.3.42 TP_AIN14 Register (Address = 0x31) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-110. TP_AIN14 Register

15	14	13	12	11	10	9	8
TP_AIN14[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_AIN14[15:0]							
R/W-0000000000000000b							

Table 8-116. TP_AIN14 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_AIN14[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for AIN14.

8.3.43 TP_AIN13 Register (Address = 0x32) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-111. TP_AIN13 Register

15	14	13	12	11	10	9	8
TP_AIN13[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_AIN13[15:0]							
R/W-0000000000000000b							

Table 8-117. TP_AIN13 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_AIN13[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for AIN13.

8.3.44 TP_AIN12 Register (Address = 0x33) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-112. TP_AIN12 Register

15	14	13	12	11	10	9	8
TP_AIN12[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_AIN12[15:0]							
R/W-0000000000000000b							

Table 8-118. TP_AIN12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_AIN12[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for AIN12.

8.3.45 TP_AIN11 Register (Address = 0x34) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-113. TP_AIN11 Register

15	14	13	12	11	10	9	8

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Figure 8-113. TP_AIN11 Register (continued)

TP_AIN11[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_AIN11[15:0]							
R/W-0000000000000000b							

Table 8-119. TP_AIN11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_AIN11[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for AIN11.

8.3.46 TP_AIN10 Register (Address = 0x35) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-114. TP_AIN10 Register

15	14	13	12	11	10	9	8
TP_AIN10[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_AIN10[15:0]							
R/W-0000000000000000b							

Table 8-120. TP_AIN10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_AIN10[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for AIN10.

8.3.47 TP_AIN9 Register (Address = 0x36) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-115. TP_AIN9 Register

15	14	13	12	11	10	9	8
TP_AIN9[15:0]							
R/W-0000000000000000b							
7	6	5	4	3	2	1	0
TP_AIN9[15:0]							
R/W-0000000000000000b							

Table 8-121. TP_AIN9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	TP_AIN9[15:0]	R/W	0000000000000000b	Fixed 16 bit pattern for AIN9.

8.3.48 GEN_CFG5 Register (Address = 0x37) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-116. GEN_CFG5 Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-00000000000b							
7	6	5	4	3	2	1	0

Figure 8-116. GEN_CFG5 Register (continued)

RESERVED	RESERVED	RESERVED	OFS_CORR_DIS	GAN_CORR_DIS
R/W-00000000000b	R/W-0b	R/W-00b	R/W-0b	R/W-0b

Table 8-122. GEN_CFG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:5	RESERVED	R/W	00000000000b	Reserved. Do not change from the default reset value.
4	RESERVED	R/W	0b	Reserved. Do not change from the default reset value.
3:2	RESERVED	R/W	00b	Reserved. Do not change from the default reset value.
1	OFS_CORR_DIS	R/W	0b	System offset correction disable for AIN9 to AIN16. 0b = Enabled 1b = Disabled
0	GAN_CORR_DIS	R/W	0b	System gain correction disable for AIN9 to AIN16. 0b = Enabled 1b = Disabled

8.3.49 CH_XTALK_AIN9_16 Register (Address = 0x3B) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-117. CH_XTALK_AIN9_16 Register

15	14	13	12	11	10	9	8
RESERVED				CH_XTALK_AIN9_16	RESERVED		
R/W-0000b				R/W-0b	R/W-0000000000b		
7	6	5	4	3	2	1	0
RESERVED							RESERVED
R/W-0000000000b							R-0b

Table 8-123. CH_XTALK_AIN9_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0000b	Reserved. Do not change from the default reset value.
11	CH_XTALK_AIN9_16	R/W	0b	Set this bit to 1b when CH_XTALK_LOW_SPEED is 1b. 0b = Disabled 1b = Enabled
10:1	RESERVED	R/W	0000000000b	Reserved. Do not change from the default reset value.
0	RESERVED	R	0b	

8.3.50 DWC_FLAG_AIN9_16 Register (Address = 0x3E) [Reset = 0x0000]

Return to the Summary Table.

Figure 8-118. DWC_FLAG_AIN9_16 Register

15	14	13	12	11	10	9	8
HIGH_FLAG_AIN9	HIGH_FLAG_AIN10	HIGH_FLAG_AIN11	HIGH_FLAG_AIN12	HIGH_FLAG_AIN13	HIGH_FLAG_AIN14	HIGH_FLAG_AIN15	HIGH_FLAG_AIN16
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b
7	6	5	4	3	2	1	0
LOW_FLAG_AIN9	LOW_FLAG_AIN10	LOW_FLAG_AIN11	LOW_FLAG_AIN12	LOW_FLAG_AIN13	LOW_FLAG_AIN14	LOW_FLAG_AIN15	LOW_FLAG_AIN16
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 8-124. DWC_FLAG_AIN9_16 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	HIGH_FLAG_AIN9	R	0b	Digital window comparator high flag for AIN9.
14	HIGH_FLAG_AIN10	R	0b	Digital window comparator high flag for AIN10.
13	HIGH_FLAG_AIN11	R	0b	Digital window comparator high flag for AIN11.
12	HIGH_FLAG_AIN12	R	0b	Digital window comparator high flag for AIN12.
11	HIGH_FLAG_AIN13	R	0b	Digital window comparator high flag for AIN13.
10	HIGH_FLAG_AIN14	R	0b	Digital window comparator high flag for AIN14.

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Table 8-124. DWC_FLAG_AIN9_16 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	HIGH_FLAG_AIN15	R	0b	Digital window comparator high flag for AIN15.
8	HIGH_FLAG_AIN16	R	0b	Digital window comparator high flag for AIN16.
7	LOW_FLAG_AIN9	R	0b	Digital window comparator low flag for AIN9.
6	LOW_FLAG_AIN10	R	0b	Digital window comparator low flag for AIN10.
5	LOW_FLAG_AIN11	R	0b	Digital window comparator low flag for AIN11.
4	LOW_FLAG_AIN12	R	0b	Digital window comparator low flag for AIN12.
3	LOW_FLAG_AIN13	R	0b	Digital window comparator low flag for AIN13.
2	LOW_FLAG_AIN14	R	0b	Digital window comparator low flag for AIN14.
1	LOW_FLAG_AIN15	R	0b	Digital window comparator low flag for AIN15.
0	LOW_FLAG_AIN16	R	0b	Digital window comparator low flag for AIN16.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Typical Application

9.1.1 16S Battery Cell Voltage Monitoring

The ADS93x4C is a 16-channel, simultaneous-sampling ADC providing excellent common-mode reject ratio (105dB) for accurate cell voltage monitoring in series-stacked lithium-ion battery packs. In these applications, each cell voltage must be monitored precisely to detect overcharge, overdischarge, and cell imbalance conditions during charging and discharging cycles. The device integrates 16 independent sample-and-hold circuits that capture all input channels simultaneously, providing an accurate snapshot of the battery pack state.

The ADS93x4C differential input programmable gain amplifier (PGA) offers 1MΩ input impedance on both AINnP and AINnM pins, allowing direct connection to each cell. The typical approach requires accurate differential voltage measurements across each cell while managing high common-mode voltages that increase with each cell position in the stack. The ADC inputs can support up to ±40V common-mode voltage, hence, eliminates the need for external amplifiers or attenuation stage. The Figure 9-1 shows application schematic. The device interfaces to a microcontroller via a standard SPI (CS, SCLK, SDI, SDOUT). The ADS93x4C also offers an 8-bit parallel interface that can used in high throughput application (>200KSPS per channel).

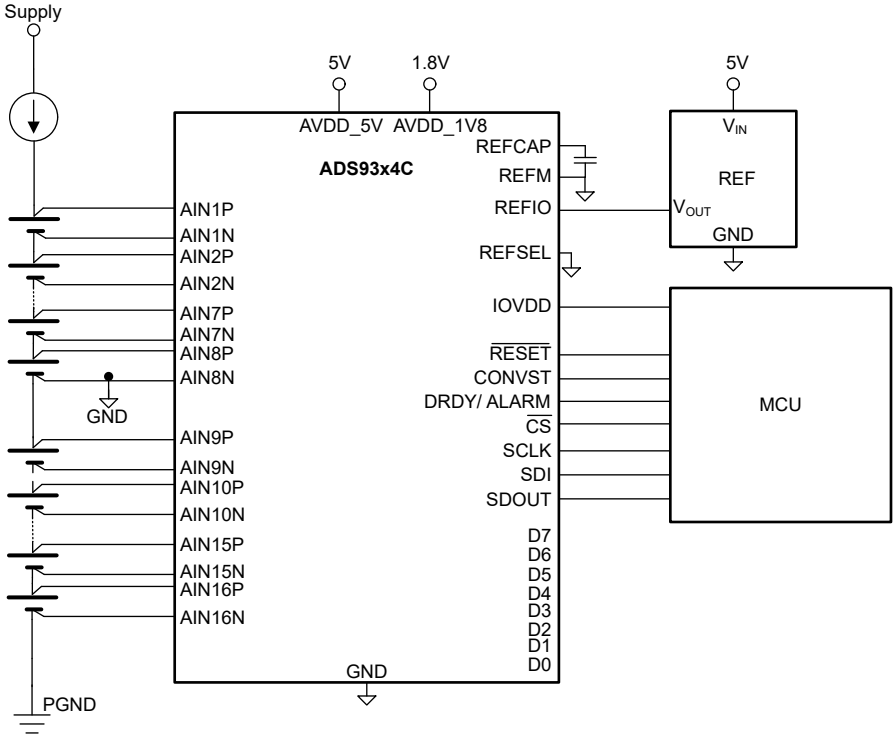

Figure 9-1. 16S Battery Cell Voltage Monitoring Using the ADS9324C

Figure 9-2 shows ADC output error with change input common mode voltage. The ADC excellent common-mode noise rejection results in less than 0.25mV error for ±40V input common mode swing, helping in maintaining the cell voltage measuring accuracy during battery charge and discharge cycles.

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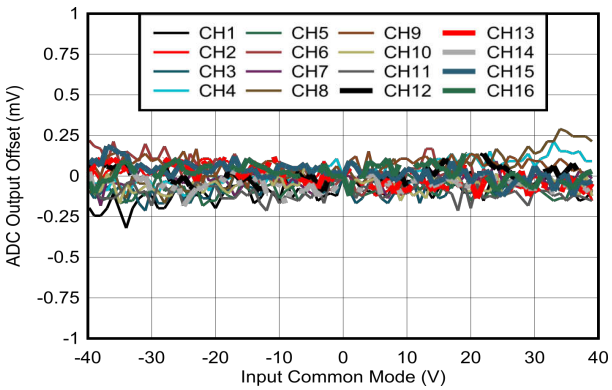

Figure 9-2. ADC Output vs Input Common-Mode

ADVANCE INFORMATION

9.2 Power Supply Recommendations

The ADS93x4C has three separate power supplies: AVDD_5V, AVDD_1V8, and IOVDD. There is no requirement for a specific power-up sequence. IOVDD powers the digital IOVDD. When using a 1.8V rail for IOVDD, AVDD_1V8 can be shorted with IOVDD with a 100Ω ferrite bead. Figure 9-3 illustrates the decoupling capacitor connections for the respective power supplies. Make sure each power-supply pin has separate 0.1µF decoupling capacitors.

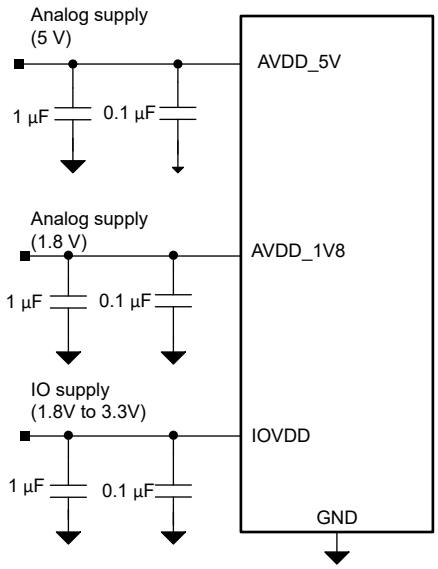

Figure 9-3. Power-Supply Decoupling

9.3 Layout

9.3.1 Layout Guidelines

Figure 9-4 illustrates a board layout example for the ADS9324C. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference signals away from noise sources.

For best performance, filter the internal reference noise by connecting a 4.7µF ceramic bypass capacitor to the REFIO pin, and connect 1µF ceramic capacitors directly between REFCAPA and REFM pins, and between the REFCAPB and REFM pins. Place 1µF reference decoupling capacitors close to the device REFCAP and REFM pins. Avoid placing vias between the REFIO pin and the bypass capacitors. Connect the GND and REFM pins to a ground plane using short, low-impedance paths.

Use 0.1µF ceramic bypass capacitors in close proximity to the AVDD_5V, AVDD_1V8, and IOVDD power-supply pins. Avoid placing vias between the power-supply pins and the bypass capacitors.

ADVANCE INFORMATION

9.3.1.1 Layout Example

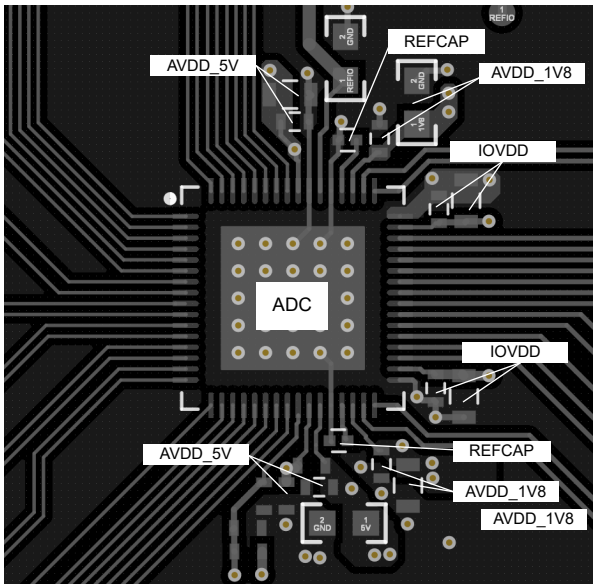

Figure 9-4. Example Layout

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference* data sheet
- Texas Instruments, *AN-2029 Handling & Process Recommendations* application note

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2026	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGE OPTION ADDENDUM

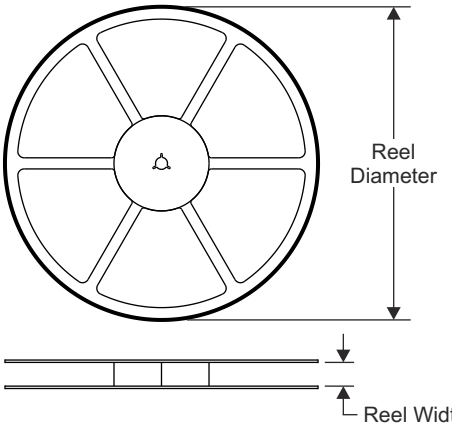
PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/Ball material (4)	MSL rating/Peak reflow (5)	Op temp (°C)	Part marking (6)
PADS9324CRSKR	Active	Preproduction	VQFN (RSK) | 64	3500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	PADS93XXV

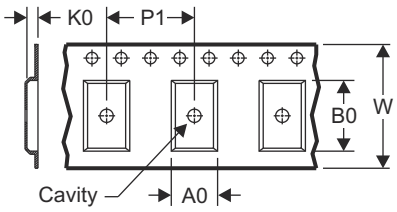
(1) **Status:** For more details on status, see our product life cycle.
(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

12.1 Tape and Reel Information

REEL DIMENSIONS

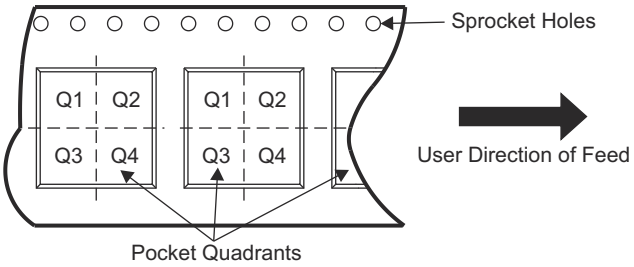


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

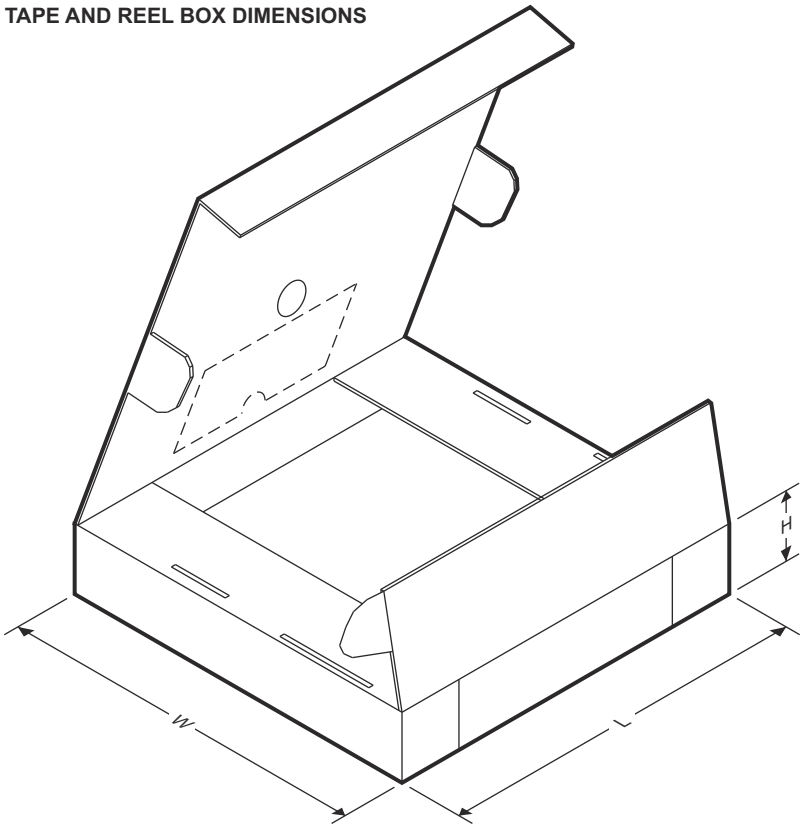
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PADS9324CRSKR	VQFN	RSK	64	3500	330.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PADS9324CRSKR	VQFN	RSK	64	3500	360.0	360.0	36.0

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Last updated 10/2025