

AFE7954 Quad RF Sampling 12 GSPS Digital-to-Analog Converter (DAC)

1 Features

- [Request full data sheet](#)
- Quad RF sampling 12-GSPS DACs
- Maximum RF signal bandwidth:
 - 4TX: 1200 MHz or
 - 2TX: 2400 MHz
- RF frequency range: 600 MHz - 12 GHz
- Digital step attenuators (DSA):
 - TX: 40 dB range, 0.125-dB steps
- Single or dual-band DUCs
- 16x NCOs per TX
- Optional Internal PLL/VCO for DAC or external clock at DAC sample rate
- SerDes data interface:
 - JESD204B and JESD204C compatible
 - 8 SerDes receivers up to 29.5 Gbps
 - Subclass 1 multi-device synchronization
- Package: 17-mm × 17-mm FCBGA, 0.8-mm pitch

2 Applications

- [Radar](#)
- [Seeker front end](#)
- [Defense radio](#)
- Tactical communications infrastructure
- [Wireless communications test](#)

3 Description

The AFE7954 is a high performance, wide bandwidth quad channel RF sampling DAC. With operation up to 12 GHz, this device enables direct RF sampling in the L, S, C and X-band frequency ranges without the need for additional frequency conversions stages. This improvement in density and flexibility enables high-channel-count, multi-mission systems.

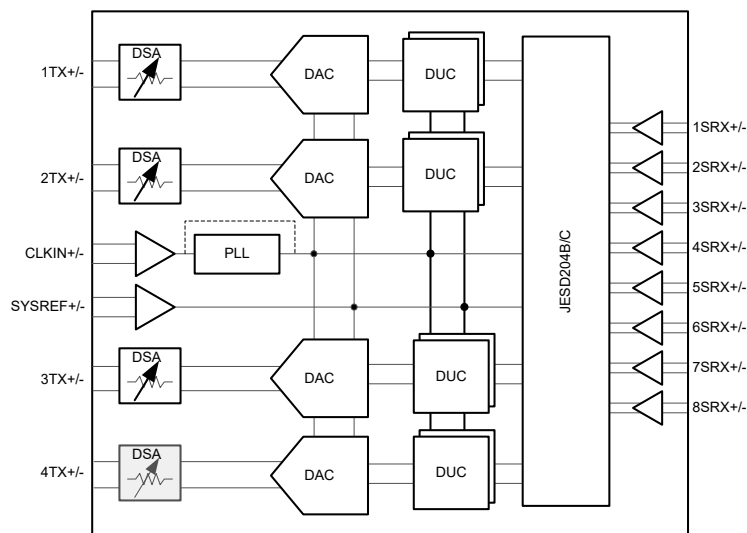
The signal paths support interpolation and digital up conversion options that deliver up to 1200 MHz of signal bandwidth for four DACs (TX) or 2400 MHz for two DACs. The output of the DUCs drives a 12-GSPS DAC (digital to analog converter) with a mixed mode output option to enhance 2nd Nyquist operation. The DAC output includes a variable gain amplifier (TX DSA) with 40-dB range and 1-dB analog and 0.125-dB digital steps.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
AFE7954	FC-BGA	17 mm × 17 mm

(1) For more information, see *Mechanical, Packaging, and Orderable Information*.

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Functional Block Diagram



Table of Contents

1 Features	1	6.7 Digital Electrical Characteristics.....	15
2 Applications	1	6.8 Power Supply Electrical Characteristics.....	17
3 Description	1	6.9 Timing Requirements.....	19
4 Description (continued)	3	6.10 Switching Characteristics.....	20
5 Revision History	3	7 Device and Documentation Support	21
6 Specifications	4	7.1 Receiving Notification of Documentation Updates....	21
6.1 Absolute Maximum Ratings.....	4	7.2 Support Resources.....	21
6.2 ESD Ratings.....	4	7.3 Trademarks.....	21
6.3 Recommended Operating Conditions.....	5	7.4 Electrostatic Discharge Caution.....	21
6.4 Thermal Information AFE79xx.....	5	7.5 Glossary.....	21
6.5 Transmitter Electrical Characteristics.....	6	8 Mechanical, Packaging, and Orderable Information..	21
6.6 PLL/VCO/Clock Electrical Characteristics.....	13		

4 Description (continued)

Each receiver chain includes a 25-dB range DSA (Digital Step Attenuator), followed by a 3-GSPS ADC (analog-to-digital converter). Each receiver channel has an analog peak power detector and various digital power detectors to assist an external or internal autonomous automatic gain controller, and RF overload detectors for device reliability protection. Flexible decimation options provide optimization of data bandwidth up to 1200 MHz for four RX without FB paths or 600 MHz with two FB paths (1200 MHz BW each).

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2023	*	Initial Release

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply Voltage Range	DVDD0P9, VDDT0P9	−0.3	1.2	V
	VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2PLL, VDD1P2PLLCLKREF, VDD1P2FB, VDD1P2FBCML, VDD1P2RXCML	−0.3	1.4	V
	VDD1P8RX, VDD1P8RXCLK, VDD1P8TX, VDD1P8TXDAC, VDD1P8TXENC, VDD1P8PLL, VDD1P8PLLVC0, VDD1P8FB, VDD1P8FBCML, VDD1P8GPIO, VDDA1P8	−0.5	2.1	V
Pin Volatge Range	{1/2/3/4}TXOUT+/-	−0.5	VDDTX1P8+0.3	V
	REFCLK+/-, SYSREF+/-	−0.3	1.4	V
	{1:8}SRX+/-	−0.3	1.4	V
	GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1	−0.5	VDD1P8GPIO + 0.3	V
	IFORCE, VSENSE	−0.3	VDDCLK1P8 + 0.3	V
	SRDAMUX1, SRDAMUX2	−0.3	VDDA1P8+0.3	V
Peak Input Current	any input		20	mA
T _J	Junction temperature		150	°C
T _{stg}	Storage temperature	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾	1000	V
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002, all pins	150	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
DVDD0P9, VDDT0P9	Supply voltage 0.9V	0.9	0.925	0.95	V
VDD1P2{RX/TXCLK/TXENC/FB/PLL/ PLLCLKREF/FBCML/RXCML}	Supply voltage 1.2V	1.15	1.2	1.25	V
VDD1P8{RX/RXCLK/TX/TXDAC/ TXENC/PLL/PLLVCO/FB/FBCLK/ GPIO}, VDDA1P8	Supply voltage 1.8V	1.75	1.8	1.85	V
T _A	Ambient temperature	–40		85	°C
T _J	Operating Junction Temperature			110 ⁽¹⁾	°C
	Maximum Operating Junction Temperature	125			°C

- (1) Prolonged use at or above this junction temperature can increase the device failure-in-time (FIT) rate. Refer to [SBAA403 application note](#) for additional details

6.4 Thermal Information AFE79xx

THERMAL METRIC ⁽¹⁾		17mmx17mm FC-BGA	UNIT
		400 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	16.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	0.42	°C/W
R _{θJB}	Junction-to-board thermal resistance	4.85	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	0.12	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	4.6	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Transmitter Electrical Characteristics

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC _{RES}	DAC resolution			14		bits
f _{RFout}	RF output frequency range	f _{DAC} = 12 GSPS, 1 st Nyquist	600		6000	MHz
		f _{DAC} = 12 GSPS, 2 nd Nyquist	6000		12000	
		f _{DAC} = 9 GSPS, 1 st Nyquist	600		4500	
		f _{DAC} = 9 GSPS, 2 nd Nyquist	4500		9000	
		f _{DAC} = 6 GSPS, 1 st Nyquist	600		3000	
		f _{DAC} = 6 GSPS, 2 nd Nyquist	3000		6000	
P _{max_FS}	Max Full Scale Output Power, max gain 1 tone, at device pins	f _{out} = 850 MHz, f _{DAC} = 5898.24 MSPS, -0.5dBFS		4.2		dBm
		f _{out} = 1800 MHz, f _{DAC} = 5898.24 MSPS, -0.5dBFS		4.6		dBm
		f _{out} = 2600 MHz, f _{DAC} = 8847.36 MSPS, -0.5dBFS		4.0		dBm
		f _{out} = 3500 MHz, -0.5dBFS		3.9		dBm
		f _{out} = 4900 MHz, -0.5dBFS		3.1		dBm
		f _{out} = 3500 MHz, f _{DAC} = 5898.24 MSPS, -0.5dBFS, straight mode		1.0		dBm
		f _{out} = 4900 MHz, f _{DAC} = 5898.24 MSPS, -0.5dBFS, straight mode		0.1		dBm
		f _{out} = 4900 MHz, f _{DAC} = 8847.36 MSPS, -0.5dBFS, straight mode		-0.7		dBm
		f _{out} = 8100 MHz, -0.1dBFS, mixed mode		-2.8		dBm
		f _{out} = 9600 MHz, -0.1dBFS, mixed mode		-4.3		dBm
R _{TERM}	Output termination resistor	Default setting		50		Ω
ATT _{range}	DSA Attenuation range			40		dB
ATT _{step}	DSA Analog Attenuation step			1.0		dB
	DSA Attenuation step accuracy (DNL)	0 < Atten < 40dB, before calibration		±0.2		dB
	DSA Attenuation step accuracy (DNL)	0 < Atten < 40dB, after calibration		±0.1		dB
ATT _{phase-err}	DSA Gain Steps Phase accuracy, any 8dB range	f _{out} = 850MHz ⁽²⁾		±1		deg
		f _{out} = 1800MHz ⁽²⁾		±1		deg
		f _{out} = 2600MHz ⁽²⁾		±1		deg
		f _{out} = 3500MHz ⁽²⁾		±1		deg
		f _{out} = 4900MHz ⁽²⁾		±1		deg
		f _{out} = 8100MHz ⁽²⁾		±2		deg
G _{flat}	Gain flatness	any 20MHz		0.1		dB
		600MHz BW, F _{out} < 4.9G		1.2		

6.5 Transmitter Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{A,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IMD3	3rd Order Intermodulation distortion, 2 tones at $f_{\text{IF}} \pm 10\text{ MHz}$	$f_{\text{out}} = 850\text{MHz}$, -7dBFS each tone		-66		dBc
		$f_{\text{out}} = 1800\text{MHz}$, -7dBFS each tone		-63		dBc
		$f_{\text{out}} = 2600\text{MHz}$, -7dBFS each tone		-62		dBc
		$f_{\text{out}} = 3500\text{MHz}$, -7dBFS each tone		-61		dBc
		$f_{\text{out}} = 4900\text{MHz}$, -7dBFS each tone		-57		dBc
		$f_{\text{out}} = 8100\text{MHz}$, -7dBFS each tone		-55		dBc
		$f_{\text{out}} = 9600\text{MHz}$, -7dBFS each tone		-52		dBc
		$f_{\text{out}} = 850\text{MHz}$, -13dBFS each tone		-74.4		dBc
		$f_{\text{out}} = 1800\text{MHz}$, -13dBFS each tone		-71.1		dBc
		$f_{\text{out}} = 2600\text{MHz}$, -13dBFS each tone		-73		dBc
		$f_{\text{out}} = 3500\text{MHz}$, -13dBFS each tone		-72		dBc
		$f_{\text{out}} = 4900\text{MHz}$, -13dBFS each tone		-67.8		dBc
		$f_{\text{out}} = 8100\text{MHz}$, -13dBFS each tone		-64		dBc
		$f_{\text{out}} = 9600\text{MHz}$, -13dBFS each tone		-68		dBc
SFDR	Spurious Free Dynamic Range (within Nyquist zone)	$f_{\text{out}} = 850\text{ MHz}$		50.8		dBc
		$f_{\text{out}} = 1800\text{ MHz}$		51.9		dBc
		$f_{\text{out}} = 2600\text{ MHz}$		42		dBc
		$f_{\text{out}} = 3500\text{ MHz}$		44		dBc
		$f_{\text{out}} = 4900\text{ MHz}$		46.1		dBc
$f_{\text{S}}/2 - f_{\text{OUT}}$	Interleaving Image	$f_{\text{DAC}} = 5898.24\text{MSPS}$, interleave mode		-51.9		dBc
		$f_{\text{DAC}} = 8847.36\text{ MSPS}$, interleave mode		-46.0		dBc
		$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode		-41		dBc
HD2	2nd Harmonic Distortion (within Nyquist zone)	$f_{\text{out}} = 850\text{ MHz}$		-49		dBc
		$f_{\text{out}} = 1800\text{ MHz}$		-53		dBc
		$f_{\text{out}} = 2600\text{ MHz}$		-50		dBc
		$f_{\text{out}} = 3500\text{ MHz}$		-48		dBc
		$f_{\text{out}} = 4900\text{ MHz}$		-47		dBc
		$f_{\text{out}} = 8100\text{ MHz}$		-50		dBc
		$f_{\text{out}} = 9600\text{ MHz}$		-53		dBc
		$f_{\text{out}} = 850\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-60		dBc
		$f_{\text{out}} = 1800\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-64		dBc
		$f_{\text{out}} = 2600\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-45		dBc
		$f_{\text{out}} = 3500\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-57		dBc
		$f_{\text{out}} = 4900\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-58		dBc
		$f_{\text{out}} = 8100\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-60		dBc
		$f_{\text{out}} = 9600\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-62		dBc

6.5 Transmitter Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD3	3rd Harmonic Distortion (within Nyquist zone)	$f_{\text{out}} = 850\text{ MHz}$		-62		dBc
		$f_{\text{out}} = 1800\text{ MHz}$		-55		dBc
		$f_{\text{out}} = 2600\text{ MHz}$		-57		dBc
		$f_{\text{out}} = 3500\text{ MHz}$		-60		dBc
		$f_{\text{out}} = 4900\text{ MHz}$		-54		dBc
		$f_{\text{out}} = 8100\text{ MHz}$		-54		dBc
		$f_{\text{out}} = 9600\text{ MHz}$		-56		dBc
		$f_{\text{out}} = 850\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-80		dBc
		$f_{\text{out}} = 1800\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-79		dBc
		$f_{\text{out}} = 2600\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-77		dBc
		$f_{\text{out}} = 3500\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-77		dBc
		$f_{\text{out}} = 4900\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-78		dBc
		$f_{\text{out}} = 8100\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-82		dBc
		$f_{\text{out}} = 9600\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-80		dBc
HDn, n >= 4	Harmonic Distortion n >= 4 (within Nyquist zone)	$f_{\text{out}} = 850\text{ MHz}$		-81		dBc
		$f_{\text{out}} = 1800\text{ MHz}$		-88		dBc
		$f_{\text{out}} = 2600\text{ MHz}$		-86		dBc
		$f_{\text{out}} = 3500\text{ MHz}$		-79		dBc
		$f_{\text{out}} = 4900\text{ MHz}$		-86		dBc
		$f_{\text{out}} = 8100\text{ MHz}$		-87		dBc
		$f_{\text{out}} = 9600\text{ MHz}$		-85		dBc
		$f_{\text{out}} = 850\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-93		dBc
		$f_{\text{out}} = 1800\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-98		dBc
		$f_{\text{out}} = 2600\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-84		dBc
		$f_{\text{out}} = 3500\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
		$f_{\text{out}} = 4900\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
		$f_{\text{out}} = 8100\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
		$f_{\text{out}} = 9600\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
SFDR +/- 250 MHz	Spurious Free Dynamic Range within +/- 250 MHz	$f_{\text{out}} = 850\text{ MHz}$		68.5		dBc
		$f_{\text{out}} = 1800\text{ MHz}$		79.4		dBc
		$f_{\text{out}} = 2600\text{ MHz}$		77		dBc
		$f_{\text{out}} = 3500\text{ MHz}$		75		dBc
		$f_{\text{out}} = 4900\text{ MHz}$		76		dBc
		$f_{\text{out}} = 8100\text{ MHz}$		61		dBc
		$f_{\text{out}} = 9600\text{ MHz}$		64		dBc
$f_s/4$	Fixed Spur	$f_{\text{DAC}} = 5898.24\text{MSPS}$		-64		dBFS
		$f_{\text{DAC}} = 8847.36\text{MSPS}$		-75		dBFS
		$f_{\text{DAC}} = 11796.48\text{MSPS}$		-67		dBFS
$f_s/2$	Fixed Spur	$f_{\text{DAC}} = 5898.24\text{MSPS}$		-49		dBFS
		$f_{\text{DAC}} = 8847.36\text{MSPS}$		-48		dBFS
		$f_{\text{DAC}} = 11796.48\text{MSPS}$		-48		dBFS

6.5 Transmitter Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{A,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
3*f _S /4	Fixed Spur	2nd Nyquist, f _{DAC} = 5898.24MSPS		-76		dBFS
		2nd Nyquist, f _{DAC} = 8847.36MSPS		-89		dBFS
		2nd Nyquist, f _{DAC} = 11796.48MSPS		-63		dBFS
ACPR _{1xcarr}	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f _{out} = 0.85 GHz	Atten=0dB, Pout=-13dBFS		-68.5		dBc
		Atten=20dB, Pout=-13dBFS		-67.2		dBc
		Atten=28dB, Pout=-13dBFS		-64.5		dBc
		Atten=39dB, Pout=-13dBFS		-53.9		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f _{out} = 1.8425 GHz	Atten=0dB, Pout=-13dBFS		-70.7		dBc
		Atten=20dB, Pout=-13dBFS		-68.3		dBc
		Atten=28dB, Pout=-13dBFS		-62.9		dBc
		Atten=39dB, Pout=-13dBFS		-52.0		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f _{out} = 2.6 GHz	Atten=0dB, Pout=-13dBFS		-71		dBc
		Atten=20dB, Pout=-13dBFS		-68		dBc
		Atten=28dB, Pout=-13dBFS		-62		dBc
		Atten=39dB, Pout=-13dBFS		-51.3		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f _{out} = 3.5 GHz	Atten=0dB, Pout=-13dBFS		-70		dBc
		Atten=20dB, Pout=-13dBFS		-67		dBc
		Atten=28dB, Pout=-13dBFS		-60		dBc
		Atten=39dB, Pout=-13dBFS		-49.8		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f _{out} = 4.9 GHz	Atten=0dB, Pout=-13dBFS		-68.8		dBc
		Atten=20dB, Pout=-13dBFS		-65.9		dBc
		Atten=28dB, Pout=-13dBFS		-60.6		dBc
		Atten=39dB, Pout=-13dBFS		-49.5		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f _{out} = 2.6 GHz	Atten=0dB, Pout=-13dBFS		-65		dBc
		Atten=20dB, Pout=-13dBFS		-62		dBc
		Atten=20dB, Pout=-13dBFS		-55		dBc
		Atten=39dB, Pout=-13dBFS		-44.3		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f _{out} = 3.5 GHz	Atten=0dB, Pout=-13dBFS		-64		dBc
		Atten=20dB, Pout=-13dBFS		-59		dBc
		Atten=28dB, Pout=-13dBFS		-52		dBc
		Atten=39dB, Pout=-13dBFS		-41.1		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f _{out} = 4.9 GHz	Atten=0dB, Pout=-13dBFS		-64.1		dBc
		Atten=20dB, Pout=-13dBFS		-60.4		dBc
		Atten=28dB, Pout=-13dBFS		-53.5		dBc
		Atten=39dB, Pout=-13dBFS		-42.5		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f _{out} = 8.1 GHz	Atten=0dB, Pout=-13dBFS		-58		dBc
		Atten=20dB, Pout=-13dBFS		-53		dBc
		Atten=28dB, Pout=-13dBFS		-46		dBc
		Atten=39dB, Pout=-13dBFS		-36		dBc

6.5 Transmitter Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{A,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ACPR _{1xcarr}	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier $f_{\text{out}} = 9.6\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-57		dBc
		Atten=20dB, Pout=-13dBFS		-50		dBc
		Atten=28dB, Pout=-13dBFS		-42		dBc
		Atten=39dB, Pout=-13dBFS		-31		dBc
EVM	Error Vector Magnitude, 1x 20MHz E-TM3.1/3.1a, no ref. clock noise	$F_{\text{out}} = 0.85\text{ GHz}$, $P_{\text{OUT}} = -13\text{ dBFS}$		0.2		%
		$F_{\text{out}} = 1.8425\text{ GHz}$, $P_{\text{OUT}} = -13\text{ dBFS}$		0.3		%
		$F_{\text{out}} = 2.6\text{ GHz}$, $P_{\text{OUT}} = -13\text{ dBFS}$		0.28		%
		$F_{\text{out}} = 3.5\text{ GHz}$, $P_{\text{OUT}} = -13\text{ dBFS}$		0.38		%
		$F_{\text{out}} = 4.9\text{ GHz}$, $P_{\text{OUT}} = -13\text{ dBFS}$		0.4		%
NSD _{dBFS}	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 0.85\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-157.6		dBFS/Hz
		Atten=20dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-153.3		dBFS/Hz
		Atten=28dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-147.9		dBFS/Hz
		Atten=39dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-136.9		dBFS/Hz
NSD _{dBFS}	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 1.8\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-158.4		dBFS/Hz
		Atten=20dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-152.2		dBFS/Hz
		Atten=28dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-145.6		dBFS/Hz
		Atten=39dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-134.6		dBFS/Hz
NSD _{dBFS}	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 2.6\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$, Pout=-13dBFS		-157		dBFS/Hz
		Atten=20dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$, Pout=-13dBFS		-151		dBFS/Hz
		Atten=28dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$, Pout=-13dBFS		-144		dBFS/Hz
		Atten=39dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$, Pout=-13dBFS		-133.0		dBFS/Hz
NSD _{dBFS}	Noise Spectral Density 20MHz offset $F_{\text{out}} = 3.5\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-158		dBFS/Hz
		Atten=20dB, Pout=-13dBFS		-150		dBFS/Hz
		Atten=28dB, Pout=-13dBFS		-143		dBFS/Hz
		Atten=39dB, Pout=-13dBFS		-131.8		dBFS/Hz

6.5 Transmitter Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD _{dBFS}	Noise Spectral Density 20MHz offset $F_{\text{out}} = 4.9\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-155.5		dBFS/ Hz
		Atten=20dB, Pout=-13dBFS		-147.8		dBFS/ Hz
		Atten=28dB, Pout=-13dBFS		-140.8		dBFS/ Hz
		Atten=39dB, Pout=-13dBFS		-129.6		dBFS/ Hz
NSD _{dBFS}	Noise Spectral Density 50MHz offset $F_{\text{out}} = 8.1\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-153		dBFS/ Hz
		Atten=20dB, Pout=-13dBFS		-147		dBFS/ Hz
		Atten=28dB, Pout=-13dBFS		-140		dBFS/ Hz
		Atten=39dB, Pout=-13dBFS		-129		dBFS/ Hz
NSD _{dBFS}	Noise Spectral Density 50MHz offset $F_{\text{out}} = 9.6\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-152		dBFS/ Hz
		Atten=20dB, Pout=-13dBFS		-147		dBFS/ Hz
		Atten=28dB, Pout=-13dBFS		-140		dBFS/ Hz
		Atten=39dB, Pout=-13dBFS		-129		dBFS/ Hz
S22	Output Return Loss, <6GHz, +/- fc * 10%	with matching		-17		dB
	Output Return Loss, >8GHz, +/- fc * 10%	with matching		-10		dB
Isolation	Near Channel: 1TXOUT to 2TXOUT or 3TXOUT to 4TXOUT ⁽¹⁾	$f_{\text{out}} = 900\text{ MHz}$, $f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode		-49		dB
		$f_{\text{out}} = 1850\text{ MHz}$, $f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode		-59		dB
		$f_{\text{out}} = 2600\text{ MHz}$, $f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode		-65		dB
		$f_{\text{out}} = 3500\text{ MHz}$, $f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode		-66		dB
		$f_{\text{out}} = 4900\text{ MHz}$, $f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode		-60		dB
		$f_{\text{out}} = 900\text{ MHz}$, $f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode		-90		dB
		$f_{\text{out}} = 1850\text{ MHz}$, $f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode		-91		dB
		$f_{\text{out}} = 2600\text{ MHz}$, $f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode		-93		dB
		$f_{\text{out}} = 3500\text{ MHz}$, $f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode		-94		dB
		$f_{\text{out}} = 4900\text{ MHz}$, $f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode		-83		dB

6.5 Transmitter Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS below 6GHz and 1474.56MSPS above 6GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PN _{TXADD}	Additive Phase Noise External Clock Mode ⁽³⁾	$f_{\text{out}} = 9.6\text{GHz}$, $f_{\text{OFFSET}} = 100\text{Hz}$		-88		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$, $f_{\text{OFFSET}} = 1\text{kHz}$		-102		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$, $f_{\text{OFFSET}} = 10\text{kHz}$		-110		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$, $f_{\text{OFFSET}} = 100\text{kHz}$		-123		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$, $f_{\text{OFFSET}} = 1\text{MHz}$		-136		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$, $f_{\text{OFFSET}} = 10\text{MHz}$		-143		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$, $f_{\text{OFFSET}} = 100\text{MHz}$		-146		dBc/Hz

- (1) Measured with differential 50 ohm across TxP/M. The DC bias to 1.8V to each TxP/M at each pin remains and is not removed. Other external components on the TX paths are disconnected.
- (2) After DSA calibration procedure
- (3) Single side band, input clock phase noise subtracted.

6.6 PLL/VCO/Clock Electrical Characteristics

Typical values at TA = +25°C, full temperature range is T_{A,MIN} = -40°C to T_{J,MAX} = +110°C; Reference clock input frequency 491.52MHz (unless otherwise noted), f_{DAC} = f_{VCO}, f_{OUT} = f_{DAC}/4, normalized to f_{VCO}.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{VCO1}	VCO1 min frequency				7.2	GHz
	VCO1 max frequency		7.68			GHz
f _{VCO2}	VCO2 min frequency				8.8	GHz
	VCO2 max frequency		9.1			GHz
f _{VCO3}	VCO3 min frequency				9.7	GHz
	VCO3 max frequency		10.24			GHz
f _{VCO4}	VCO4 min frequency				11.6	GHz
	VCO4 max frequency		12.08			GHz
DIV _{DAC}	DAC sample rate divider			1, 2 or 3		
DIV _{FBAD} C	ADC sample rate divider from DAC sample rate			1, 2, 3, 4, 6 or 8		
DIV _{RXAD} C	ADC sample rate divider			1, 2, 3, 4, 6 or 8		
PN _{VCO}	Closed Loop Phase Noise F _{PLL} = 11.79848 GHz F _{REF} =491.52MHz	600kHz		-113		dBc/Hz
		800kHz		-116		dBc/Hz
		1MHz		-119		dBc/Hz
		1.8MHz		-125		dBc/Hz
		5MHz		-133		dBc/Hz
		50MHz		-141		dBc/Hz
	Closed Loop Phase Noise F _{PLL} =8.84736 GHz F _{REF} =491.52MHz	600kHz		-114		dBc/Hz
		800kHz		-118		dBc/Hz
		1MHz		-120		dBc/Hz
		1.8MHz		-127		dBc/Hz
		5MHz		-135		dBc/Hz
		50MHz		-142		dBc/Hz
	Closed Loop Phase Noise F _{PLL} = 9.8403 GHz F _{REF} =491.52MHz	600kHz		-113		dBc/Hz
		800kHz		-116		dBc/Hz
		1MHz		-119		dBc/Hz
		1.8MHz		-125		dBc/Hz
		5MHz		-134		dBc/Hz
		50MHz		-140		dBc/Hz
	Closed Loop Phase Noise F _{PLL} = 7.86432GHz F _{REF} =491.52MHz	600kHz		-116		dBc/Hz
		800kHz		-119		dBc/Hz
		1MHz		-122		dBc/Hz
		1.8MHz		-127		dBc/Hz
		5MHz		-136		dBc/Hz
		50MHz		-143		dBc/Hz
F _{rms}	Clock PLL integrated phase error ⁽¹⁾	f _{PLL} =11.79848 GHz, [1KHz, 100MHz]		-43.4		dBc/Hz
		f _{PLL} =8.8536 GHz, [1KHz, 100MHz]		-47.6		dBc/Hz
		f _{PLL} =9.8304 GHz, [1KHz, 100MHz]		-46.2		dBc/Hz
f _{PFD}	PFD frequency		100		500	MHz
PN _{pll_flat}	Normalized PLL flat Noise	f _{VCO} = 11796.48MHz		-226.5		dBc/Hz
F _{REF}	Input Clock frequency		0.1		12	GHz
V _{SS}	Input Clock level		0.6		1.8	Vppdiff

6.6 PLL/VCO/Clock Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; Reference clock input frequency 491.52MHz (unless otherwise noted), $f_{\text{DAC}} = f_{\text{VCO}}$, $f_{\text{OUT}} = f_{\text{DAC}}/4$, normalized to f_{VCO} .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Coupling				AC Coupling Only		
	REFCLK input impedance ⁽²⁾	Parallel resistance		100		Ω
		Parallel capacitance		0.5		pF

(1) Single Sideband, not including the reference clock contribution

(2) Refer to S11 data available from TI for impedance vs frequency

6.7 Digital Electrical Characteristics

Typical values at TA = +25°C, full temperature range is T_{A,MIN} = -40°C to T_{J,MAX} = +110°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CML SerDes Inputs [8:1]SRX+/-						
V _{SRDIFF}	SerDes Receiver Input Amplitude	differential	100		1200	mVpp
V _{SRCOM}	SerDes Input Common Mode		0.4	0.5	0.6	V
Z _{SRdiff}	SerDes Internal Differential Termination ⁽¹⁾			100		Ω
F _{SerDes}	SerDes Bit Rate	Full rate mode	19		29.5	Gbps
		Half rate mode	9.5		16.25	Gbps
		Quarter rate mode	4.75		8.125	Gbps
	Insertion Loss Tolerance ⁽²⁾	Serdes supply = 1.8V		25		dB
TJ	Total Jitter Tolerance				0.42	UI
CMOS I/O: GPIO{B/C/D/E}x, SPICLK, SPIDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1						
V _{IH}	High-Level Input Voltage		0.6×VDD1 P8GPIO			V
V _{IL}	Low-Level Input Voltage		0.4×VDD1 P8GPIO			V
I _{IH}	High-Level Input Current		-250		250	μA
I _{IL}	Low-Level Input Current		-250		250	μA
C _L	CMOS input capacitance			2		pF
V _{OH}	High-Level Output Voltage		VDD1P8G PIO-0.2			V
V _{OL}	Low-Level Output Voltage				0.2	V
Differential Inputs: SYSREF+/- Mode A						
Clock _{MODE}				PLL Clock Mode Only		
F _{SYSREFMAX}	SYSREF Input Frequency Maximum			40		MHz
V _{SWINGSRMAX}	SYSREF Input Swing Maximum			1.8		Vppdiff ⁽³⁾
V _{SWINGSRMIN}	SYSREF Input Swing Minimum	f _{REF} < 500MHz		0.3		Vppdiff ⁽³⁾
V _{SWINGSRMIN}	SYSREF Input Swing Minimum	f _{REF} > 500MHz		0.6		Vppdiff ⁽³⁾
V _{COMSRMAX}	SYSREF Input Common Mode Voltage Maximum			0.8		V
V _{COMSRMIN}	SYSREF Input Common Mode Voltage Minimum			0.6		V
Z _T	Input termination	differential		100 ⁽¹⁾		Ω
C _L	Input capacitance	Each pin to GND		0.5		pF
LVDS Inputs: 0SYNCIN+/- and 1SYNCIN+/-						
V _{ICOM}	Input Common Voltage			1.2		V
V _{ID}	Differential Input Voltage swing			450		Vppdiff ⁽³⁾
Z _T	Input termination	differential		100		Ω
LVDS Outputs: 0SYNCOUT+/- and 1SYNCOUT+/-						
V _{OCOM}	Output Common Voltage			1.2		V
V _{OD}	Differential Output Voltage swing			500		Vppdiff ⁽³⁾
Z _T	Internal Termination			100		Ω

(1) SYSREF termination is programmable between 100Ω, 150Ω and 300Ω

(2) Loss tolerance is bump to bump from STX to SRX

- (3) V_{ppdiff} is the difference between the maximum differential voltage (positive value) and minimum differential voltage (negative value).

6.8 Power Supply Electrical Characteristics

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 500MSPS, RX Output Rate = 500MSPS, $f_{\text{DAC}} = 9000\text{MSPS}$ interleave mode; $f_{\text{ADC}} = 3000\text{MSPS}$; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 20Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 1: 4TX TX Dual Band: 96x Int, TX Rate 125 MSPS $f_{\text{DAC}} = 12\text{ GSPS}$, $f_{\text{TX}} = 1.85 + 2.15\text{ GHz}$ JESD: 8/10 coding, 20Gbps TX: 2-16-16-1		564		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8			274		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLCO			71		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			953		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1747		mA
P_{diss}	Power Dissipation			4396		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 2: 4TX TX Single Band: 24x Int, TX Rate 500 MSPS $f_{\text{DAC}} = 12\text{ GSPS}$, $f_{\text{TX}} = 2.75\text{ GHz}$ JESD: 8/10 coding, 20Gbps TX: 4-8-4-1		570		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8			382		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLCO			72		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			967		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2172		mA
P_{diss}	Power Dissipation			5011		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 3: 4TX TX Single Band: 12x Int, TX Rate 1 GSPS $f_{\text{DAC}} = 12\text{ GSPS}$, $f_{\text{TX}} = 2.75\text{ GHz}$ JESD: 8/10 coding, 20Gbps TX: 8-8-2-1		571		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8			495		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLCO			72		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			969		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2465		mA
P_{diss}	Power Dissipation			5490		mW

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 500MSPS, RX Output Rate = 500MSPS, $f_{\text{DAC}} = 9000\text{MSPS}$ interleave mode; $f_{\text{ADC}} = 3000\text{MSPS}$; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 20Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 4: 4TX TX Single Band: 8x Int, TX Rate 1500 MSPS $f_{\text{DAC}} = 12\text{ GSPS}$, $f_{\text{TX}} = 2.75\text{ GHz}$ JESD: 64/66 coding, 24.75Gbps TX: 8-8-2-1		569		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8			521		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			73		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			981		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2719		mA
P_{diss}	Power Dissipation			5786		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 5: 2TX TX Single Band: 4x Int, TX Rate 3000 MSPS $f_{\text{DAC}} = 12\text{ GSPS}$, $f_{\text{TX}} = 2.75\text{ GHz}$ JESD: 64/66 coding, 24.75Gbps TX: 8-4-1-1		297		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8			446		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			72		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			544		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			1575		mA
P_{diss}	Power Dissipation			3577		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 6: Same as Mode 5 in Sleep mode with Sleep pin pulled high.		96		mA
I_{VDD1P8}	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8			330		mA
I_{VDD1P8}	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			16		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			48		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			302		mA
P_{diss}	Power Dissipation			1132		mW

6.9 Timing Requirements

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS, $f_{\text{DAC}} = 8847.36\text{MSPS}$; $f_{\text{ADC}} = 2949.12\text{MSPS}$; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

		MIN	NOM	MAX	UNIT
Timing: SYSREF+/-					
$t_s(\text{SYSREF})$	Setup Time, SYSREF+/- Valid to Rising Edge of CLK+/-		50		ps
$t_h(\text{SYSREF})$	Hold Time, SYSREF+/- Valid after Rising Edge of CLK+/-		50		ps
Timing: Serial ports					
$t_s(\text{SENB})$	Setup Time, SENB to Rising Edge of SCLK			15	ns
$t_h(\text{SENB})$	Hold Time, SENB after last Rising Edge of SCLK ⁽¹⁾		$5 + t_{\text{SCLK}}$		ns
$t_s(\text{SDIO})$	Setup Time, SDIO valid to Rising Edge of SCLK			15	ns
$t_h(\text{SDIO})$	Hold Time, SDIO valid after Rising Edge of SCLK			5	ns
$t_{\text{SCLK_W}}$	Minimum SCLK period: registers write			25	ns
$t_{\text{SCLK_R}}$	Minimum SCLK period: registers read			50	ns
$t_{\text{d}(\text{data_out})}$	Minimum Data Output delay after Falling Edge of SCLK			0	ns
	Maximum Data Output delay after Falling Edge of SCLK			15	ns
t_{RESET}	Minimum RESETZ Pulse Width		1		ms

(1) SDEN\ need to be held one more extra clock cycle with the last SCLK edge

6.10 Switching Characteristics

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS, $f_{\text{DAC}} = 8847.36\text{MSPS}$; $f_{\text{ADC}} = 2949.12\text{MSPS}$; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TX Channel Latency						
	SerDes Receiver Analog Delay	Full rate		2.8		ns
$t_{\text{JESD TX}}$	JESD to TX output Latency	LMFSHd=2-8-8-1, 368.64 MSPS input rate, 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		152		interface clock cycles ⁽¹⁾
		LMFSHd=8-16-4-1, 491.52 MSPS 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		176		
		LMFSHd=4-16-8-1, 245.76 MSPS 48x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		124		
		LMFSHd=2-16-16-1, 122.88 MSPS 96x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		97		

(1) Interface clock cycles is the period of the digital interface sample rate, e.g. 1GSPS = 1ns.

7 Device and Documentation Support

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

7.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

7.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AFE7954IABJ	Active	Production	FCBGA (ABJ) 400	90 JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE7954I
AFE7954IALK	Active	Production	FCBGA (ALK) 400	90 JEDEC TRAY (5+1)	No	SNPB	Level-3-220C-168 HR	-40 to 85	AFE7954 SNPB

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

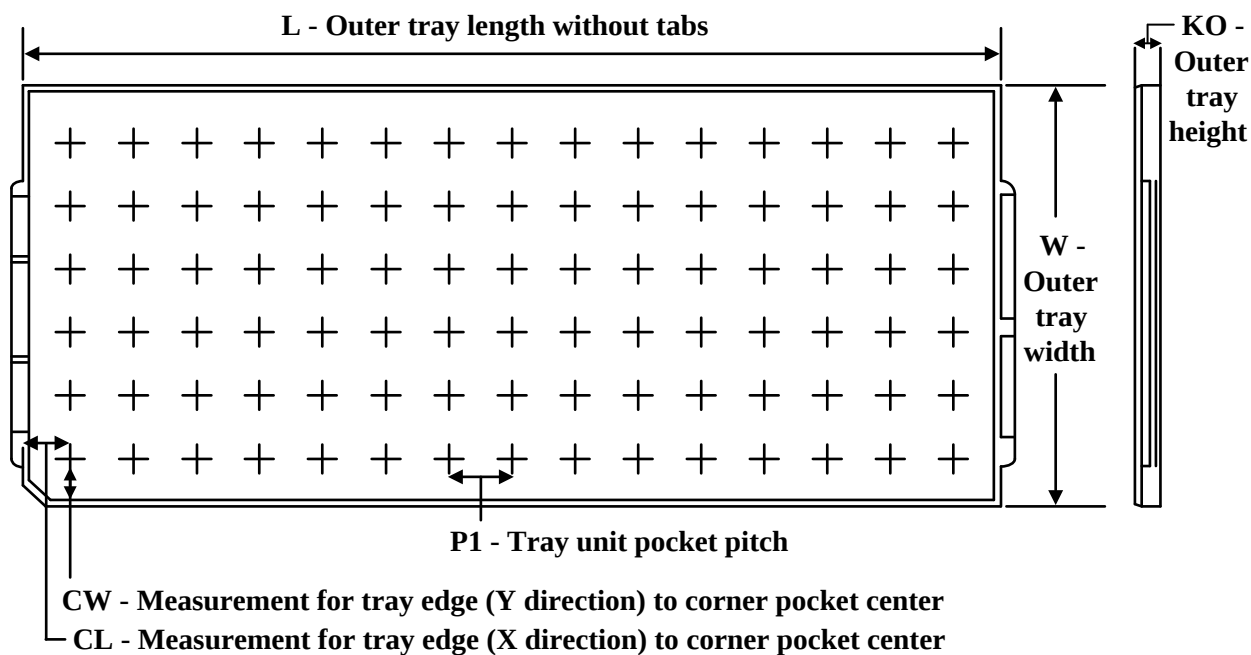
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (μm)	P1 (mm)	CL (mm)	CW (mm)
AFE7954IABJ	ABJ	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7954IABJ	ABJ	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7954IALK	ALK	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7954IALK	ALK	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2

FCBGA - 2.65 mm max height

Top View: Shows a square package with overall dimensions of 17.2 mm by 17.2 mm and a core area of 16.8 mm by 16.8 mm. A corner is identified as "BALL A1 CORNER". A dashed square indicates the internal core area.

Side View: Shows the package profile with a maximum height of 2.65 mm and a base height of 2.29 mm. The ball pitch is 0.5 mm. The top surface has a flatness of 0.2 mm. The bottom surface has a flatness of 0.12 mm. The seating plane is indicated by a triangle and labeled "SEATING PLANE NOTE 4".

Bottom View: Shows the ball grid array layout. The ball pitch is 0.5 mm. The grid is 20 balls by 20 balls. The overall dimensions are 15.2 mm by 15.2 mm. The grid is symmetrical (SYMM) about both the horizontal and vertical centerlines. The ball diameter is 0.45 mm. The grid is labeled with letters A through W and numbers 1 through 20.

Callouts:

- 0.8 TYP:** Dimension for the ball pitch.
- 15.2 TYP:** Dimension for the overall package width and height.
- 0.5 TYP:** Dimension for the ball pitch.
- 0.2 C:** Dimension for the top surface flatness.
- 0.12 C:** Dimension for the bottom surface flatness.
- SEATING PLANE NOTE 4:** Indicated by a triangle.
- SYMM:** Symmetrical about the centerline.
- 400X Ø 0.55 0.45:** Dimension for the ball diameter.
- NOTE 3:** Reference to a note on the drawing.

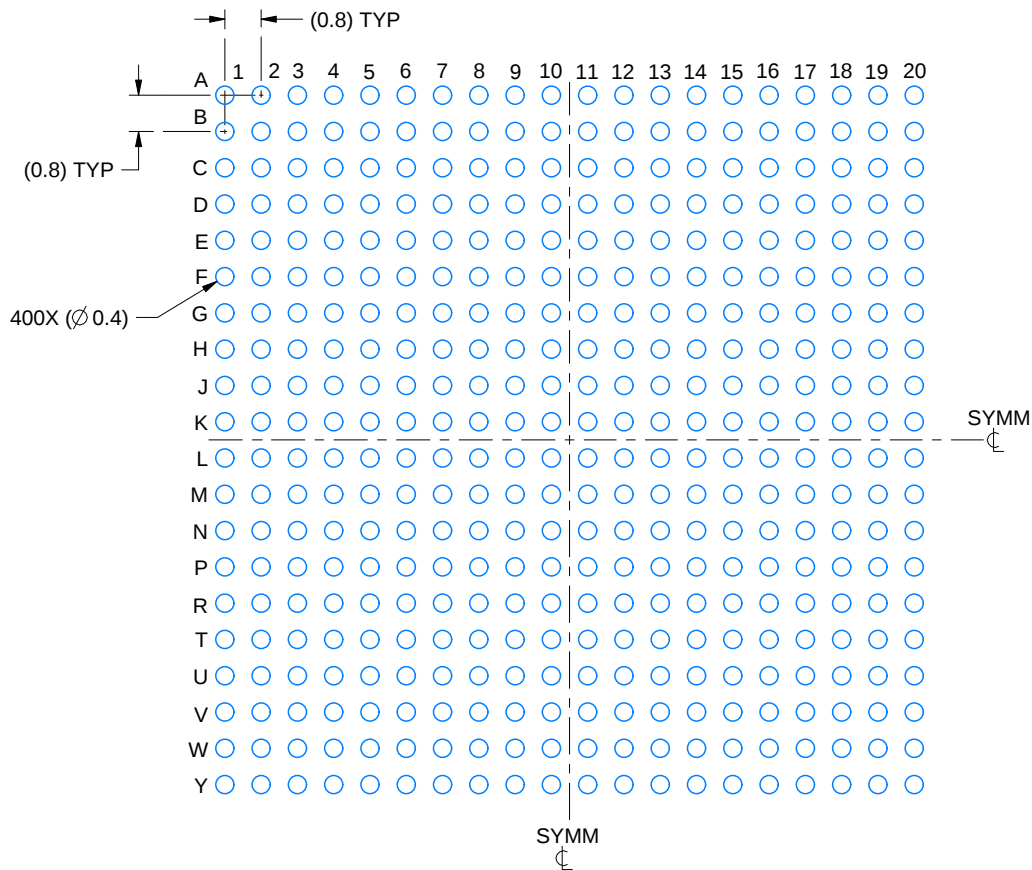
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. The lids are electrically floating (e.g. not tied to GND).

EXAMPLE BOARD LAYOUT

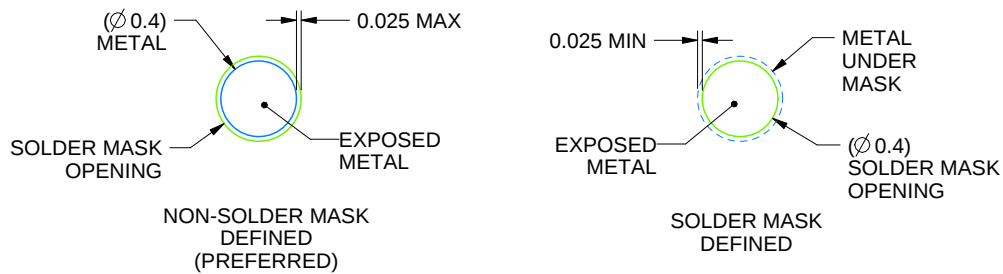
ABJ0400A

FCBGA - 2.65 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

4221311/D 03/2023

NOTES: (continued)

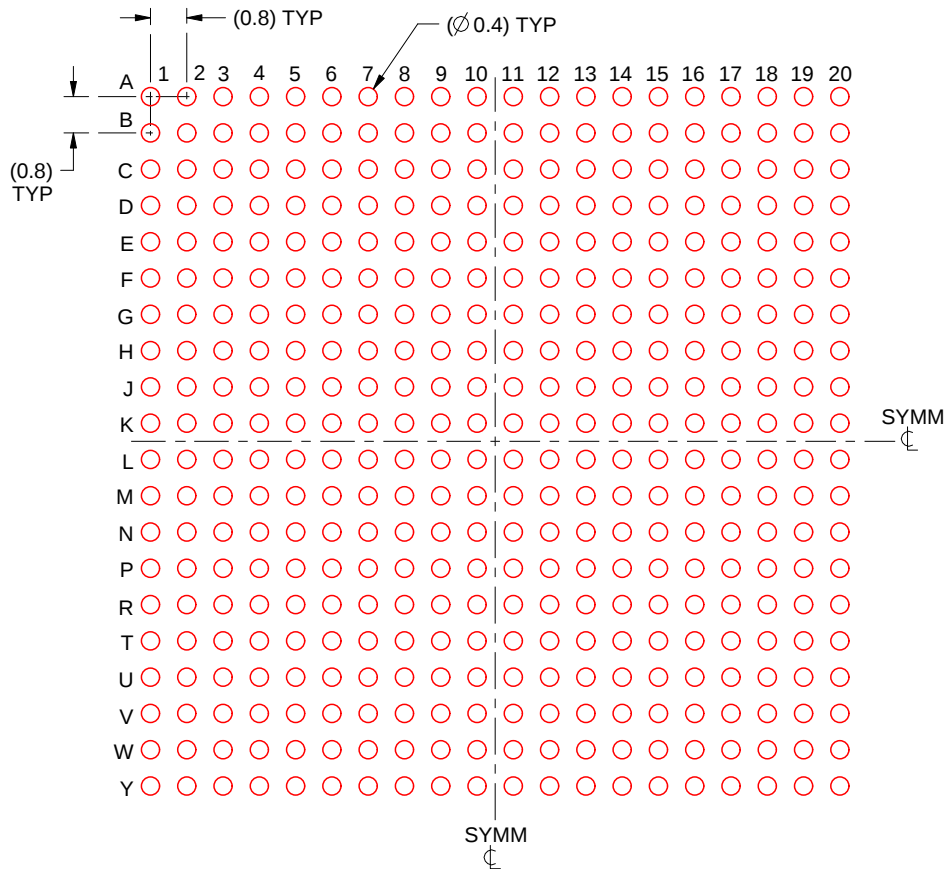
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).

EXAMPLE STENCIL DESIGN

ABJ0400A

FCBGA - 2.65 mm max height

BALL GRID ARRAY



SOLDER PASTE EXAMPLE
 BASED ON 0.15 mm THICK STENCIL
 SCALE:6X

4221311/D 03/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

FCBGA - 2.65 mm max height

[illegible]

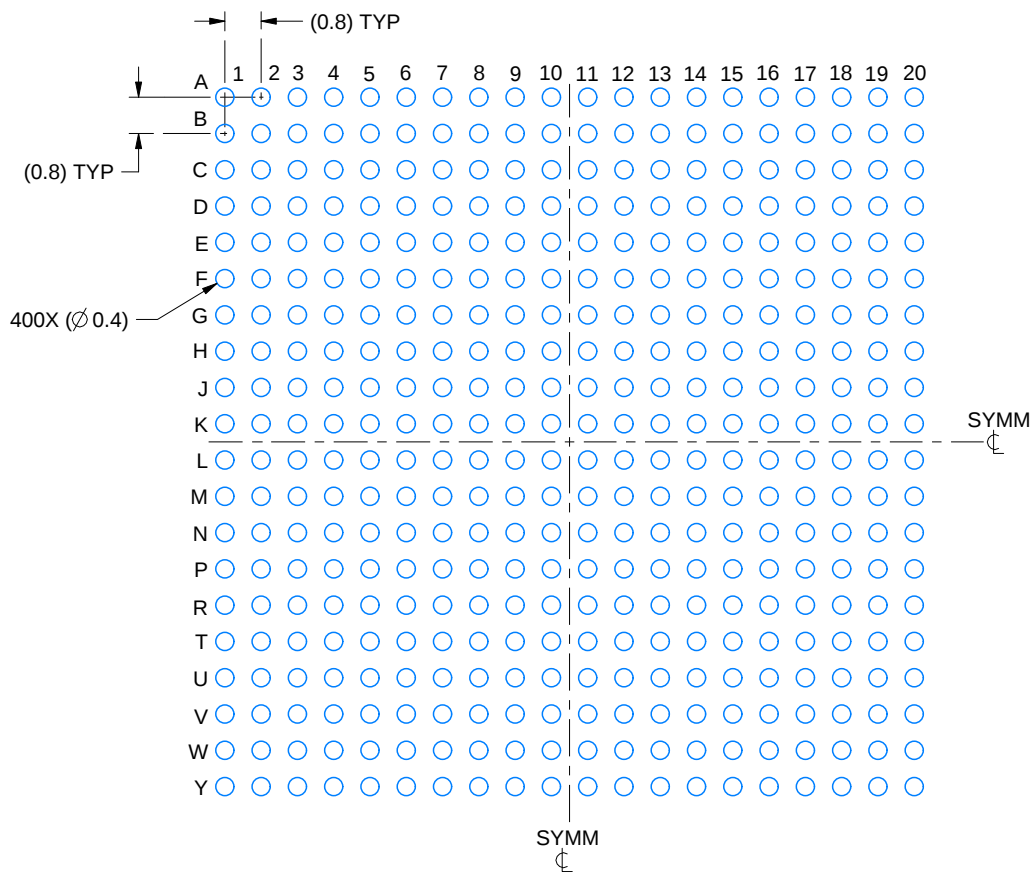
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. Pb-Free die bump and SnPb solder ball.
6. The lids are electrically floating (e.g. not tied to GND).

EXAMPLE BOARD LAYOUT

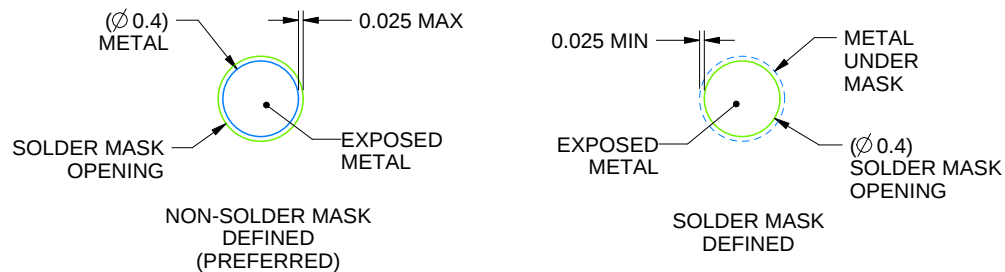
ALK0400A

FCBGA - 2.65 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

4225930/C 03/2023

NOTES: (continued)

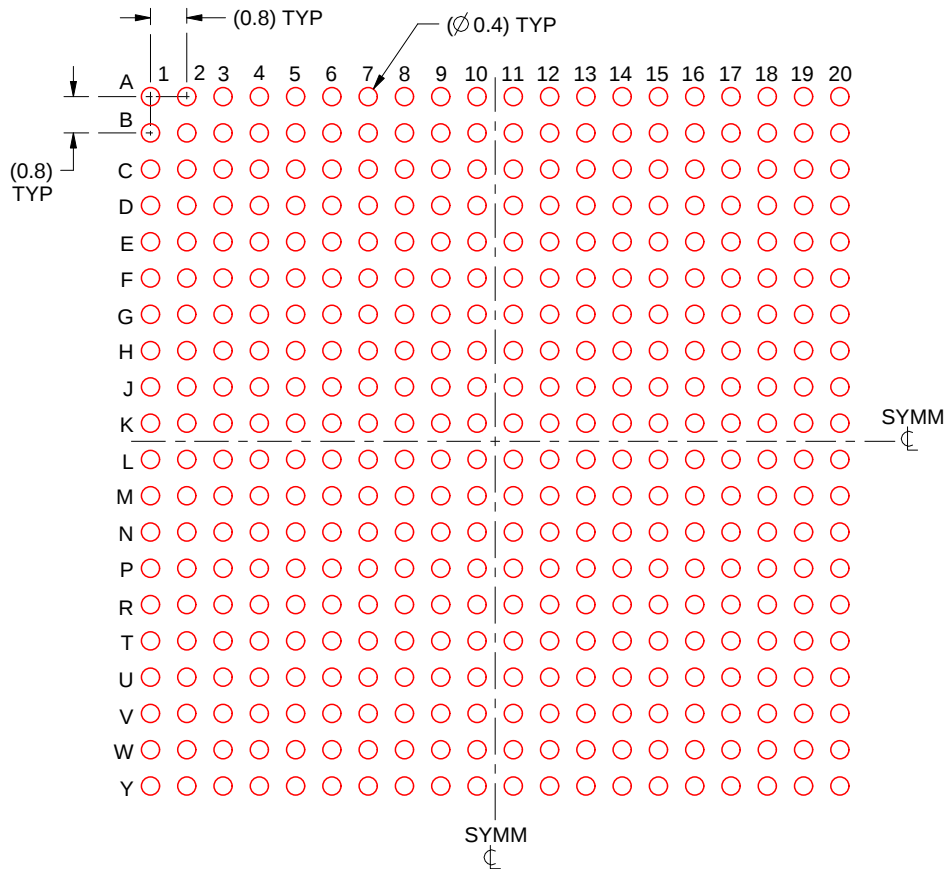
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).

EXAMPLE STENCIL DESIGN

ALK0400A

FCBGA - 2.65 mm max height

BALL GRID ARRAY



SOLDER PASTE EXAMPLE
 BASED ON 0.15 mm THICK STENCIL
 SCALE:6X

4225930/C 03/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025