



## Multi-Channel LCD Gamma Correction Buffer

 Check for Samples: [BUF07703](#), [BUF06703](#), [BUF05703](#)

### FEATURES

- Gamma Correction Channels: 6, 4
- Integrated  $V_{COM}$  Buffer
- Excellent Output Current Drive:
  - Gamma Channels: > 10mA
  - $V_{COM}$ : > 100mA typ
- Large Capacitive Load Drive Capability
- Rail-to-Rail Output
- PowerPAD™ Package: BUF07703
- Low-Power/Channel: < 250 $\mu$ A
- Wide Supply Range: 4.5V to 16V
- Specified for –40°C to 85°C
- High ESD Rating: 4kV HBM, 1.5kV CDM

### APPLICATIONS

- LCD Flat Panel Displays
- LCD Television Displays

#### DEVICE COMPARISON

MODEL	GAMMA CHANNELS	$V_{COM}$ CHANNELS
<a href="#">BUF07703</a>	6	1
<a href="#">BUF06703</a>	6	0
<a href="#">BUF05703</a>	4	1

### DESCRIPTION

The BUFxx703 are a series of multi-channel buffers targeted towards gamma correction in high-resolution liquid crystal display (LCD) panels. The number of gamma correction channels required depends on a variety of factors and differs greatly from design to design. Therefore, various channel options are offered. For additional space and cost savings, a  $V_{COM}$  channel with higher current drive capability is integrated in the BUF07703 and BUF05703.

A flow-through pinout has been adopted to allow simple printed circuit board (PCB) routing and maintain the cost-effectiveness of this solution. All inputs and outputs of the BUFxx703 incorporate internal ESD protection circuits that prevent functional failures at voltages up to 4kV HBM and 1.5kV CDM.

The various buffers within the BUFxx703 are carefully matched to the voltage I/O requirements for the gamma correction application. Each buffer is capable of driving heavy capacitive loads and offers fast load current switching. The  $V_{COM}$  channel has increased output drive of > 100mA and can handle even larger capacitive loads.

The BUF07703 is available in the HTSSOP PowerPAD™ package for dramatically increased power dissipation capability. The BUF06703 and BUF05703 are available in standard TSSOP-16 and TSSOP-14 packages.

#### RELATED PRODUCTS

DEVICE	GAMMA CHANNELS	$V_{COM}$ CHANNELS
<a href="#">BUF11702</a>	10	1
<a href="#">BUF04701</a>	4	—
<a href="#">TLV2374</a>	4	—



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### PACKAGE INFORMATION<sup>(1)</sup>

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
BUF07703	HTSSOP-20	PWP	BUF07703
BUF06703	TSSOP-16	PW	BUF06703
BUF05703	TSSOP-14	PW	BUF05703

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over operating free-air temperature range (unless otherwise noted).

	BUFxx703	UNIT
Supply, $V_{DD}$ <sup>(2)</sup>	16.5	16.5
Input Voltage Range, $V_I$	$V_{DD}$	V
Continuous Total Power Dissipation	See <a href="#">Dissipation Ratings Table</a>	
Operating Free-Air Temperature Range, $T_A$	-40 to +85	°C
Maximum Junction Temperature, $T_J$	+150	°C
Storage Temperature Range, $T_{STG}$	-65 to +150	°C

- (1) Stresses above these ratings may cause permanent damage. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.

### DISSIPATION RATINGS

PACKAGE TYPE	PACKAGE DESIGNATOR	$\theta_{JC}$ (°C/W)	$\theta_{JA}$ (°C/W)	$T_A \leq +25^\circ\text{C}$ POWER RATING
TSSOP-20 PowerPAD	PWP (20)	1.40 <sup>(1)</sup>	32.63 <sup>(1)</sup>	3.83W <sup>(1)</sup>
TSSOP-16	PW (16)	—	108	1.15W
TSSOP-14	PW (14)	—	112	1.11W

(1) Thermal specifications assume 2oz. trace and copper pad with solder.

### RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
Supply Voltage, $V_{DD}$		4.5		16	V
Operating Free-Air Temperature, $T_A$		-40		+85	°C
Junction Temperature	TSSOP-20 PowerPAD			+125	°C
	TSSOP-16, 14			+150	°C

## ELECTRICAL CHARACTERISTICS

Over operating free-air temperature range,  $V_{DD} = 4.5V$  to  $16V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

PARAMETER		CONDITIONS	$T_A$ <sup>(1)</sup>	BUF07703, BUF06703, BUF05703			UNIT
				MIN	TYP	MAX	
$V_{IO}$	Input offset voltage	$V_I = V_{DD}/2$ , $R_S = 50\Omega$	+25°C	1.5	1.2		mV
			Full range			15	mV
$I_{IB}$	Input bias current	$V_I = V_{DD}/2$	+25°C	1			pA
			Full range	200			pA
$k_{SVR}$	Supply voltage rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 4.5V$ to $16V$	+25°C	62	80		dB
			Full range	60			dB
Buffer gain		$V_I = 5V$	+25°C	0.9995			V/V
BW_3dB	3dB bandwidth	Gamma buffers	$C_L = 100pF$ , $R_L = 2k\Omega$	+25°C	0.8		MHz
		$V_{COM}$ buffer	$C_L = 100pF$ , $R_L = 2k\Omega$	+25°C	0.7		MHz
SR	Slew rate	Gamma buffers	$C_L = 100pF$ , $R_L = 2k\Omega$ $V_{IN} = 2V$ to $8V$	+25°C	1		V/ $\mu s$
		$V_{COM}$ buffer	$C_L = 100pF$ , $R_L = 2k\Omega$ $V_{IN} = 2V$ to $8V$	+25°C	0.7		V/ $\mu s$
Transient load regulation		$I_O = 0$ to $\pm 5mA$ , $V_O = 5V$ $C_L = 100pF$ , $t_T = 0.1\mu s$	+25°C	900			mV
Transient load response		See <a href="#">Figure 3</a>	+25°C	160			mV
$t_{S, (I-sink)}$	Settling time–current	$I_O = 0$ to $-5mA$ , $V_O = 5V$ $C_L = 100pF$ , $R_L = 2k\Omega$	Full range	1			$\mu s$
$t_{S, (I-src)}$	Settling time–current	$I_O = 0$ to $+5mA$ , $V_O = 5V$ $C_L = 100pF$ , $R_L = 2k\Omega$	Full range	2			$\mu s$
$t_S$	Settling time–voltage	Gamma buffers	$V_I = 4.5V$ to $5.5V$ , 0.1%	+25°C	6		$\mu s$
			$V_I = 5.5V$ to $4.5V$ , 0.1%	+25°C	4.6		$\mu s$
		$V_{COM}$ buffer	$V_I = 4.5V$ to $5.5V$ , 0.1%	+25°C	5.8		$\mu s$
			$V_I = 5.5V$ to $4.5V$ , 0.1%	+25°C	5.6		$\mu s$
$V_n$	Noise voltage	Gamma buffers	$V_I = 5V$ , $f = 1kHz$	+25°C	45		$nV/\sqrt{Hz}$
		$V_{COM}$ buffer	$V_I = 5V$ , $f = 1kHz$	+25°C	40		$nV/\sqrt{Hz}$
Crosstalk		$V_{IPP} = 6V$ , $f = 1kHz$	+25°C	85			dB

(1) Full range is  $-40^\circ C$  to  $+85^\circ C$ .

**ELECTRICAL CHARACTERISTICS: BUF07703**

Over operating free-air temperature range,  $V_{DD} = 4.5V$  to  $16V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

PARAMETER		CONDITIONS	$T_A$ (1)	BUF07703			UNIT
				MIN	TYP	MAX	
$I_{DD}$	Supply current	All	$V_O = V_{DD}/2$ , $V_I = V_{DD}/2$ , $V_{DD} = 10V$	+25°C	1.7	2	mA
				Full range		3	
	Common-mode input range	Buffers 1–3		+25°C	1	$V_{DD}$	V
		Buffers 4–6		+25°C	0	$V_{DD} - 1$	V
		$V_{COM}$ buffer		+25°C	1	$V_{DD}$	V
	Load regulation	$V_{COM}$ buffer sinking	$V_{DD} = 10V$ , $I_O = 1mA$ to $30mA$	+25°C	1		mV/mA
		$V_{COM}$ buffer sourcing	$V_{DD} = 10V$ , $I_O = -1mA$ to $-30mA$	+25°C	1		mV/mA
		Buffers 1–6 sinking	$V_{DD} = 10V$ , $I_O = 1mA$ to $10mA$	+25°C	0.85		mV/mA
		Buffers 1–6 sourcing	$V_{DD} = 10V$ , $I_O = -1mA$ to $-10mA$	+25°C	0.85		mV/mA
$V_{OSH1}$	High-level saturated output voltage	Buffer 1	$V_{DD} = 16V$ , $V_{IO} = -5mA$ , $V_I = 16V$	+25°C	15.85	15.9	V
				Full range	15.8		V
$V_{OSL6}$	Low-level saturated output voltage	Buffer 6	$V_{DD} = 16V$ , $V_{IO} = 5mA$ , $V_I = 0V$	+25°C	0.1	0.15	V
				Full range		0.2	V
$V_{OH1}$	High-level output voltage	Buffer 1	$V_{DD} = 10V$ , $V_{IO} = -10mA$ , $V_I = 9.8V$	+25°C	9.75	9.8	V
				Full range	9.7		V
$V_{OH2/3}$	High-level output voltage	Buffer 2/3	$V_{DD} = 10V$ , $V_{IO} = -10mA$ , $V_I = 9.5V$	+25°C	9.45	9.5	V
				Full range	9.4		V
$V_{OH4/5}$	High-level output voltage	Buffer 4/5	$V_{DD} = 10V$ , $V_{IO} = -10mA$ , $V_I = 8V$	+25°C	7.95	8	V
				Full range	7.9		V
$V_{OH6}$	High-level output voltage	Buffer 6	$V_{DD} = 10V$ , $V_{IO} = -10mA$ , $V_I = 8V$	+25°C	7.95	8	V
				Full range	7.9		V
$V_{OHCOM}$	High-level output voltage	$V_{COM}$ buffer	$V_{DD} = 10V$ , $V_{IO} = -30mA$ , $V_I = 8V$	+25°C	7.95	8	V
				Full range	7.9		V
$V_{OL1}$	Low-level output voltage	Buffer 1	$V_{DD} = 10V$ , $I_O = 10mA$ , $V_I = 2V$	+25°C	2	2.05	V
				Full range		2.1	V
$V_{OL2/3}$	Low-level output voltage	Buffer 2/3	$V_{DD} = 10V$ , $I_O = 10mA$ , $V_I = 2V$	+25°C	2	2.05	V
				Full range		2.1	V
$V_{OL4/5}$	Low-level output voltage	Buffer 4/5	$V_{DD} = 10V$ , $I_O = 10mA$ , $V_I = 0.5V$	+25°C	0.5	0.55	V
				Full range		0.6	V
$V_{OL6}$	Low-level output voltage	Buffer 6	$V_{DD} = 10V$ , $I_O = 10mA$ , $V_I = 0.2V$	+25°C	0.2	0.25	V
				Full range		0.3	V
$V_{OLCOM}$	Low-level output voltage	$V_{COM}$ buffer	$V_{DD} = 10V$ , $I_O = 30mA$ , $V_I = 2V$	+25°C	2	2.05	V
				Full range		2.1	V

(1) Full range is  $-40^\circ C$  to  $+85^\circ C$ .

**ELECTRICAL CHARACTERISTICS: BUF06703**

 Over operating free-air temperature range,  $V_{DD} = 4.5V$  to  $16V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

PARAMETER		CONDITIONS	$T_A$ <sup>(1)</sup>	BUF06703			UNIT	
				MIN	TYP	MAX		
$I_{DD}$	Supply current	All	$V_O = V_{DD}/2$ , $V_I = V_{DD}/2$ , $V_{DD} = 10V$	+25°C	1.7	2	mA	
				Full range		3	mA	
	Common-mode input range	Buffers 1–3		+25°C	1	$V_{DD}$	V	
		Buffers 4–6		+25°C	0	$V_{DD} - 1$	V	
	Load regulation	Buffers 1–6 sinking	$V_{DD} = 10V$ , $I_O = 1mA$ to $10mA$	+25°C	0.85		mV/mA	
		Buffers 1–6 sourcing	$V_{DD} = 10V$ , $I_O = -1mA$ to $-10mA$	+25°C	0.85		mV/mA	
$V_{OSH1}$	High-level saturated output voltage	Buffer 1	$V_{DD} = 16V$ , $V_{IO} = -5mA$ , $V_I = 16V$	+25°C	15.85	15.9	V	
				Full range	15.8		V	
$V_{OSL6}$	Low-level saturated output voltage	Buffer 6	$V_{DD} = 16V$ , $V_{IO} = 5mA$ , $V_I = 0V$	+25°C		0.1	0.15	V
				Full range			0.2	V
$V_{OH1}$	High-level output voltage	Buffer 1	$V_{DD} = 10V$ , $V_{IO} = -10mA$ , $V_I = 9.8V$	+25°C	9.75	9.8	V	
				Full range	9.7		V	
$V_{OH2/3}$	High-level output voltage	Buffer 2/3	$V_{DD} = 10V$ , $V_{IO} = -10mA$ , $V_I = 9.5V$	+25°C	9.45	9.5	V	
				Full range	9.4		V	
$V_{OH4/5}$	High-level output voltage	Buffer 4/5	$V_{DD} = 10V$ , $V_{IO} = -10mA$ , $V_I = 8V$	+25°C	7.95	8	V	
				Full range	7.9		V	
$V_{OH6}$	High-level output voltage	Buffer 6	$V_{DD} = 10V$ , $V_{IO} = -10mA$ , $V_I = 8V$	+25°C	7.95	8	V	
				Full range	7.9		V	
$V_{OL1}$	Low-level output voltage	Buffer 1	$V_{DD} = 10V$ , $I_O = 10mA$ , $V_I = 2V$	+25°C		2	2.05	V
				Full range			2.1	V
$V_{OL2/3}$	Low-level output voltage	Buffer 2/3	$V_{DD} = 10V$ , $I_O = 10mA$ , $V_I = 2V$	+25°C		2	2.05	V
				Full range			2.1	V
$V_{OL4/5}$	Low-level output voltage	Buffer 4/5	$V_{DD} = 10V$ , $I_O = 10mA$ , $V_I = 0.5V$	+25°C		0.5	0.55	V
				Full range			0.6	V
$V_{OL6}$	Low-level output voltage	Buffer 6	$V_{DD} = 10V$ , $I_O = 10mA$ , $V_I = 0.2V$	+25°C		0.2	0.25	V
				Full range			0.3	V

 (1) Full range is  $-40^\circ C$  to  $+85^\circ C$ .

**ELECTRICAL CHARACTERISTICS: BUF05703**

Over operating free-air temperature range,  $V_{DD} = 4.5V$  to  $16V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

PARAMETER		CONDITIONS	$T_A$ (1)	BUF05703			UNIT
				MIN	TYP	MAX	
$I_{DD}$	Supply current	All	$V_O = V_{DD}/2$ , $V_I = V_{DD}/2$ , $V_{DD} = 10V$	+25°C	1.7	2	mA
				Full range		3	mA
Common-mode input range	Buffers 1–2		+25°C	1	$V_{DD}$	V	
	Buffers 3–4		+25°C	0	$V_{DD} - 1$	V	
	$V_{COM}$ buffer		+25°C	1	$V_{DD}$	V	
Load regulation	$V_{COM}$ buffer sinking	$V_{DD} = 10V$ , $I_O = 1mA$ to $30mA$	+25°C	1		mV/mA	
	$V_{COM}$ buffer sourcing	$V_{DD} = 10V$ , $I_O = -1mA$ to $-30mA$	+25°C	1		mV/mA	
	Buffers 1–4 sinking	$V_{DD} = 10V$ , $I_O = 1mA$ to $10mA$	+25°C	0.85		mV/mA	
	Buffers 1–4 sourcing	$V_{DD} = 10V$ , $I_O = -1mA$ to $-10mA$	+25°C	0.85		mV/mA	
$V_{OSH1}$	High-level saturated output voltage	Buffer 1	$V_{DD} = 16V$ , $V_{IO} = -5mA$ , $V_I = 16V$	+25°C	15.85	15.9	V
				Full range	15.8		V
$V_{OSL4}$	Low-level saturated output voltage	Buffer 4	$V_{DD} = 16V$ , $V_{IO} = 5mA$ , $V_I = 0V$	+25°C	0.1	0.15	V
				Full range		0.2	V
$V_{OH1}$	High-level output voltage	Buffer 1	$V_{DD} = 10V$ , $V_{IO} = -10mA$ , $V_I = 9.8V$	+25°C	9.75	9.8	V
				Full range	9.7		V
$V_{OH2}$	High-level output voltage	Buffer 2	$V_{DD} = 10V$ , $V_{IO} = -10mA$ , $V_I = 9.5V$	+25°C	9.45	9.5	V
				Full range	9.4		V
$V_{OH3}$	High-level output voltage	Buffer 3	$V_{DD} = 10V$ , $V_{IO} = -10mA$ , $V_I = 8V$	+25°C	7.95	8	V
				Full range	7.9		V
$V_{OH4}$	High-level output voltage	Buffer 4	$V_{DD} = 10V$ , $V_{IO} = -10mA$ , $V_I = 8V$	+25°C	7.95	8	V
				Full range	7.9		V
$V_{OHCOM}$	High-level output voltage	$V_{COM}$ buffer	$V_{DD} = 10V$ , $V_{IO} = -30mA$ , $V_I = 8V$	+25°C	7.95	8	V
				Full range	7.9		V
$V_{OL1}$	Low-level output voltage	Buffer 1	$V_{DD} = 10V$ , $I_O = 10mA$ , $V_I = 2V$	+25°C	2	2.05	V
				Full range		2.1	V
$V_{OL2}$	Low-level output voltage	Buffer 2	$V_{DD} = 10V$ , $I_O = 10mA$ , $V_I = 2V$	+25°C	2	2.05	V
				Full range		2.1	V
$V_{OL3}$	Low-level output voltage	Buffer 3	$V_{DD} = 10V$ , $I_O = 10mA$ , $V_I = 0.5V$	+25°C	0.5	0.55	V
				Full range		0.6	V
$V_{OL4}$	Low-level output voltage	Buffer 4	$V_{DD} = 10V$ , $I_O = 10mA$ , $V_I = 0.2V$	+25°C	0.2	0.25	V
				Full range		0.3	V
$V_{OLCOM}$	Low-level output voltage	$V_{COM}$ buffer	$V_{DD} = 10V$ , $I_O = 30mA$ , $V_I = 2V$	+25°C	2	2.05	V
				Full range		2.1	V

(1) Full range is  $-40^\circ C$  to  $+85^\circ C$ .

### PIN CONFIGURATIONS

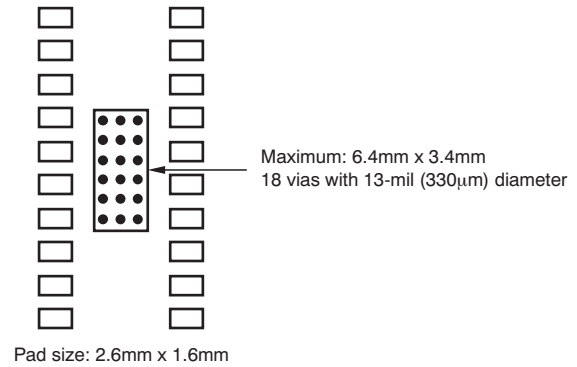
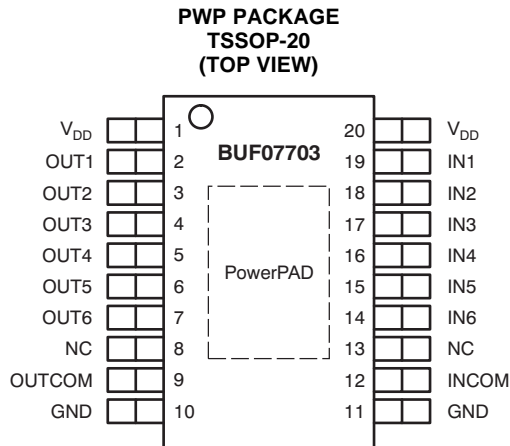
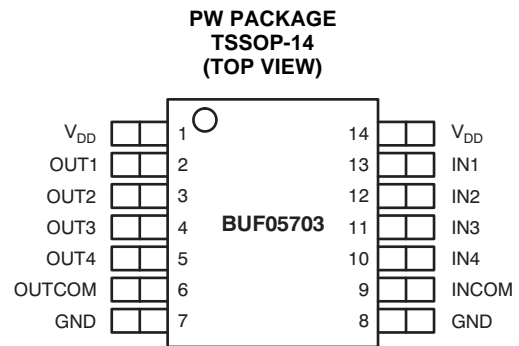
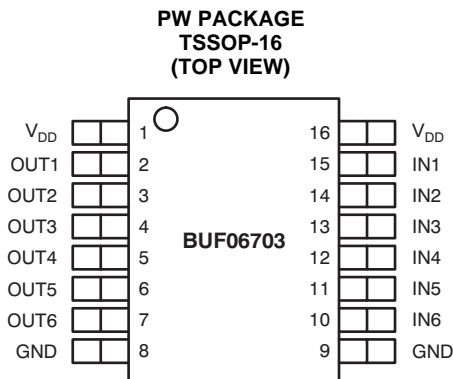


Figure 1. Land Pattern



### Equivalent Schematics of Inputs and Outputs

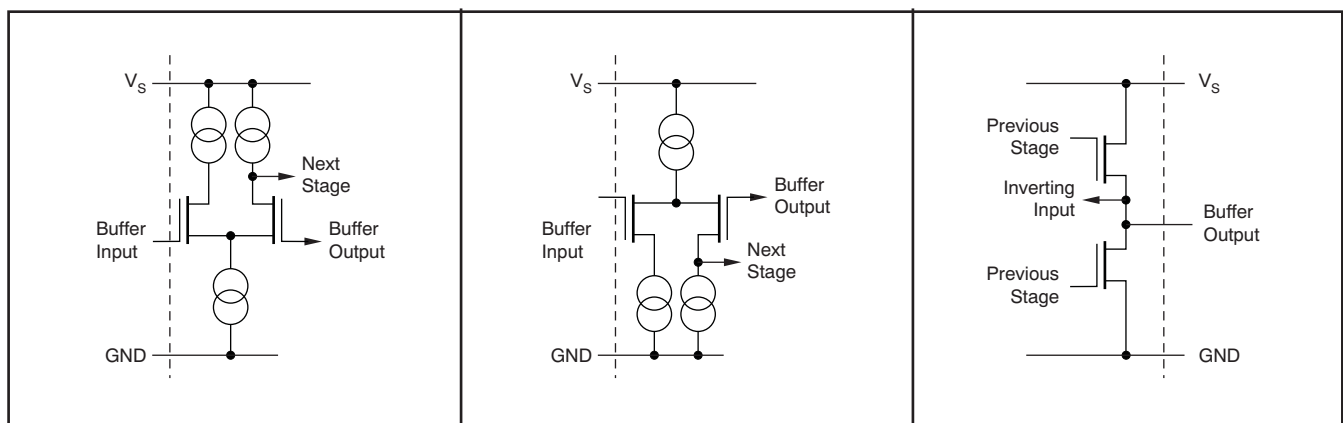
**INPUT STAGE OF BUFFERS**

BUF07703: 1 to 3 and  $V_{COM}$   
BUF06703: 1 to 3  
BUF05703: 1 to 2 and  $V_{COM}$

**INPUT STAGE OF BUFFERS**

BUF07703: 4 to 6  
BUF06703: 4 to 6  
BUF05703: 3 to 4

**OUTPUT STAGE OF ALL BUFFERS**



PARAMETER MEASUREMENT INFORMATION

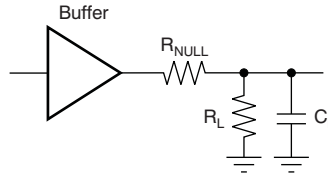
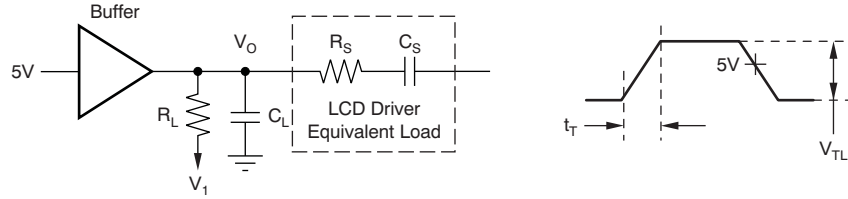


Figure 2. Bandwidth and Phase Shift Test Circuit



Test		V <sub>1</sub>	V <sub>TL</sub>	t <sub>T</sub>	C <sub>S</sub>	R <sub>S</sub>	C <sub>L</sub>	R <sub>L</sub>
Source	Gamma Channels	0V	2V	0.1 μs	100pF	100Ω	100pF	1kΩ
Sink	Gamma Channels	10V	2V	0.1 μs	100pF	100Ω	100pF	1kΩ

Figure 3. Transient Load Response Test Circuit

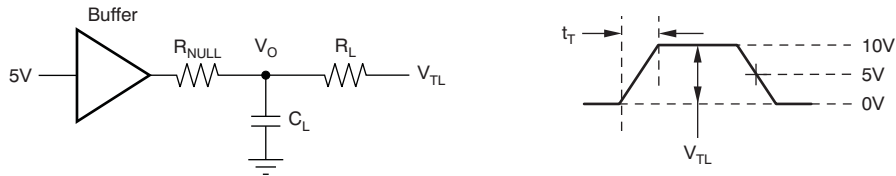


Figure 4. Transient Load Regulation Test Circuit



### TYPICAL CHARACTERISTICS

At  $V_{DD} = 10V$ , unless otherwise noted.

#### DC CURVES

INPUT OFFSET VOLTAGE vs INPUT VOLTAGE

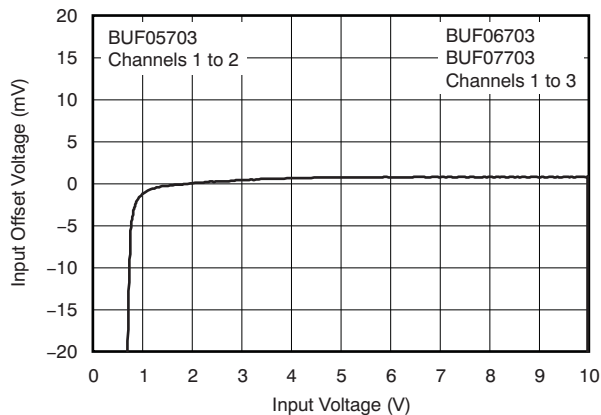


Figure 5.

INPUT OFFSET VOLTAGE vs INPUT VOLTAGE

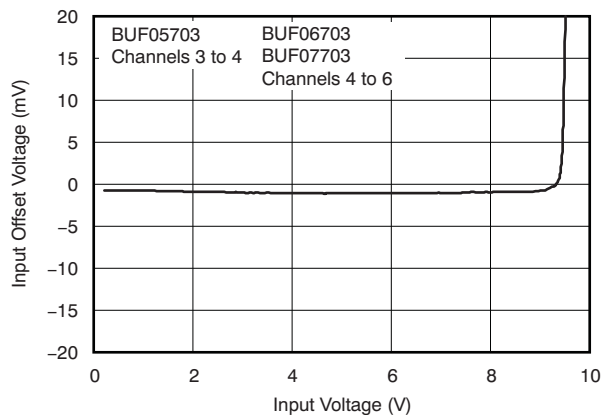


Figure 6.

INPUT OFFSET VOLTAGE vs INPUT VOLTAGE

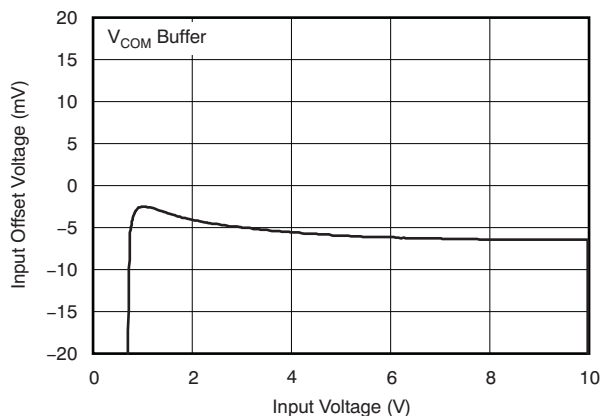


Figure 7.

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

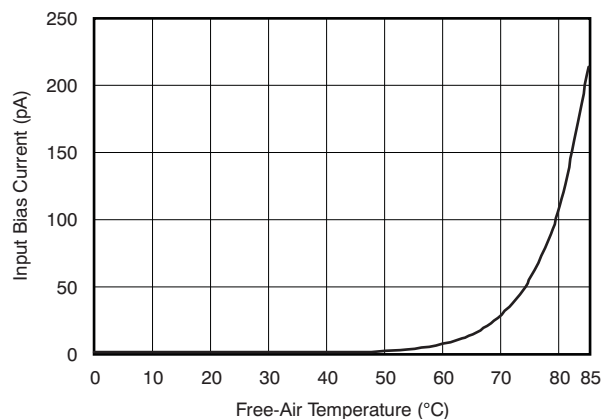


Figure 8.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

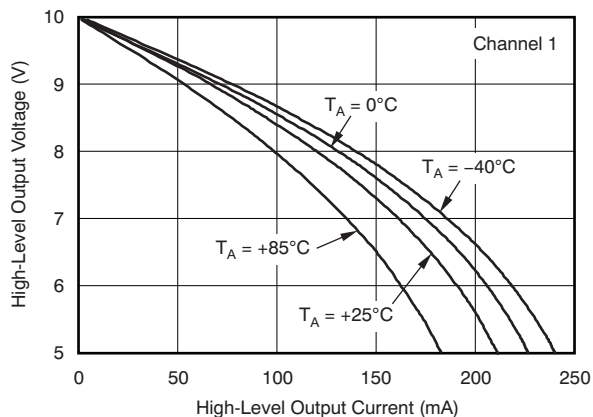


Figure 9.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

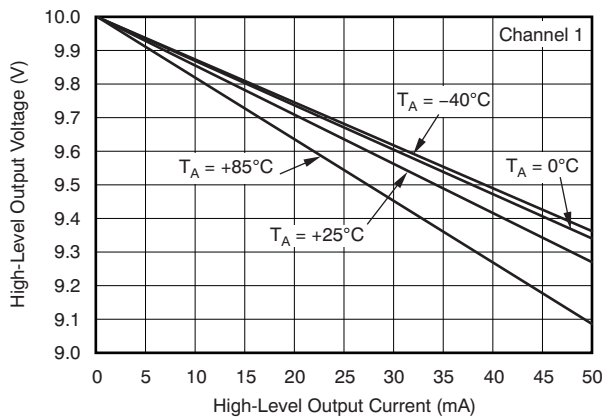


Figure 10.

TYPICAL CHARACTERISTICS (continued)

At  $V_{DD} = 10V$ , unless otherwise noted.

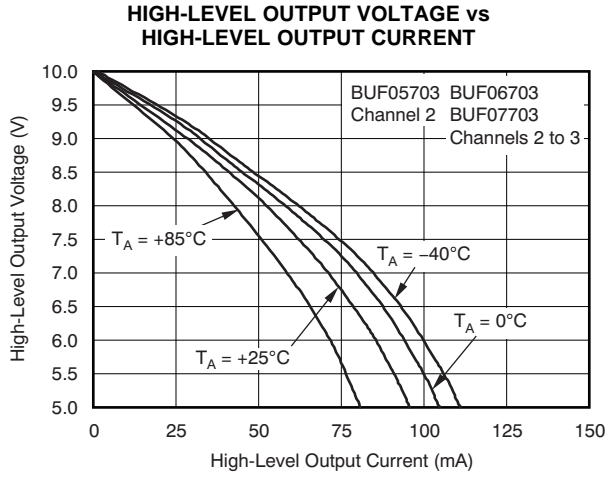


Figure 11.

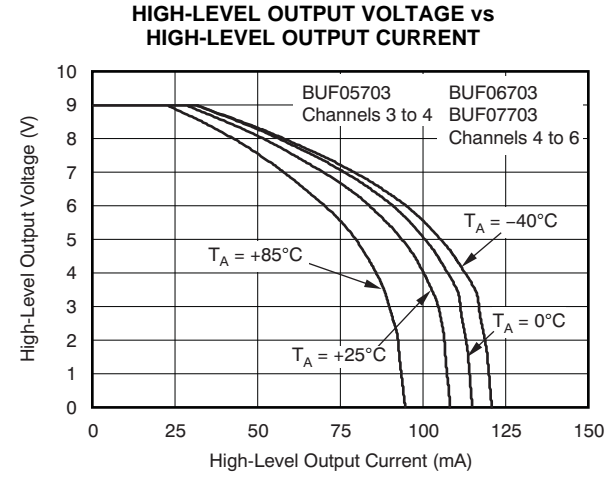


Figure 12.

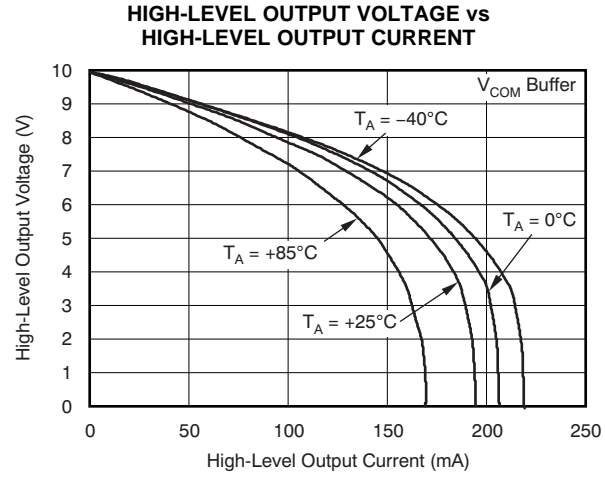


Figure 13.

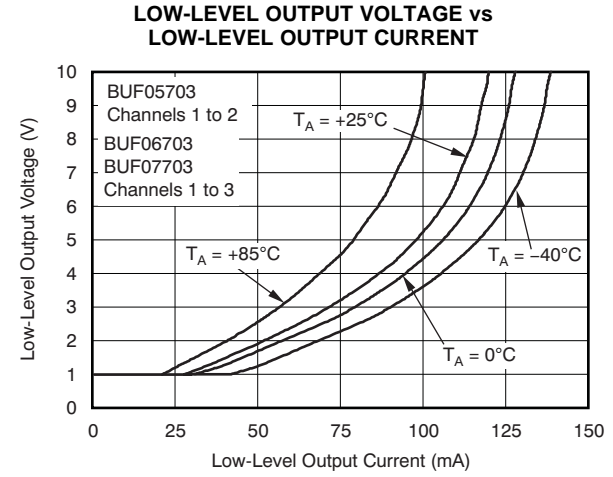


Figure 14.

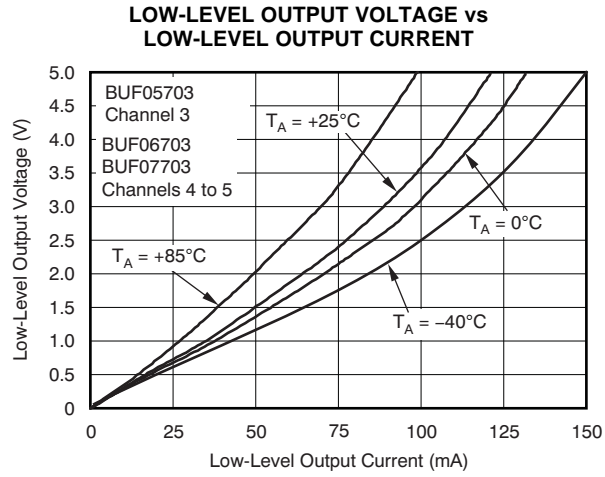


Figure 15.

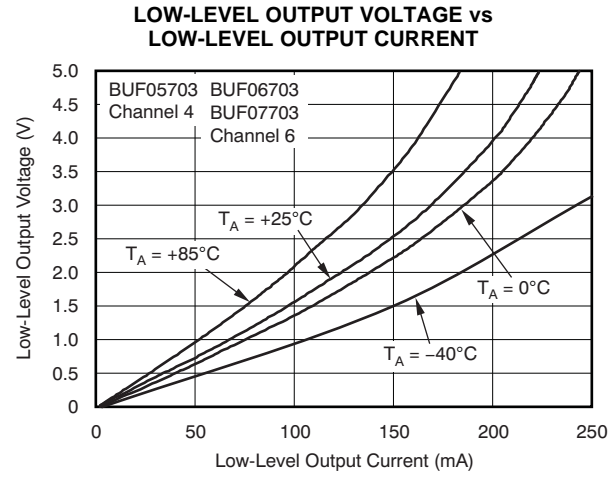


Figure 16.

TYPICAL CHARACTERISTICS (continued)

At  $V_{DD} = 10V$ , unless otherwise noted.

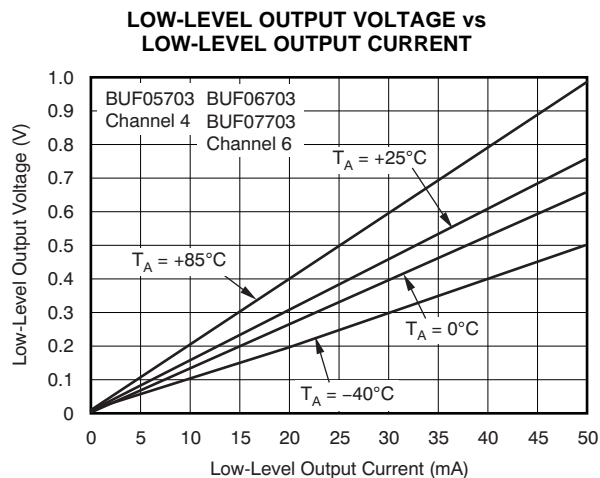


Figure 17.

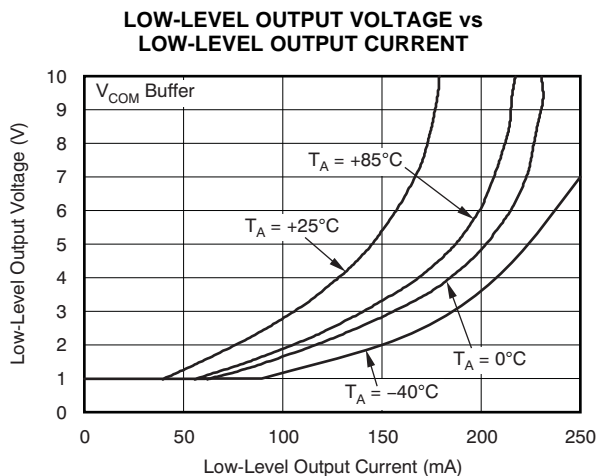


Figure 18.

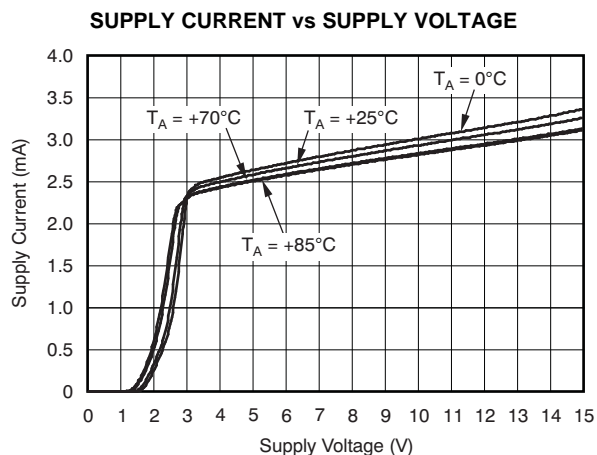


Figure 19.

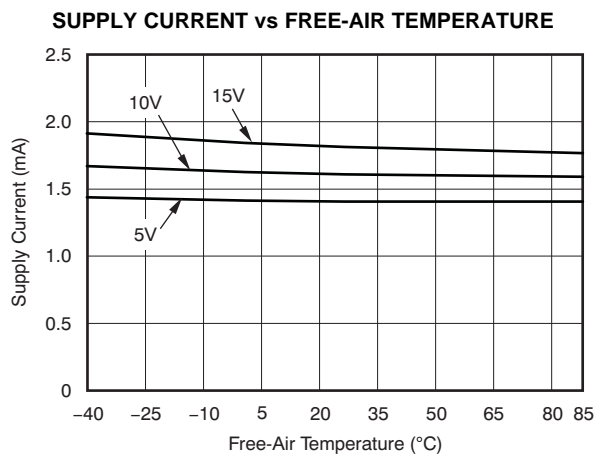


Figure 20.

AC CURVES

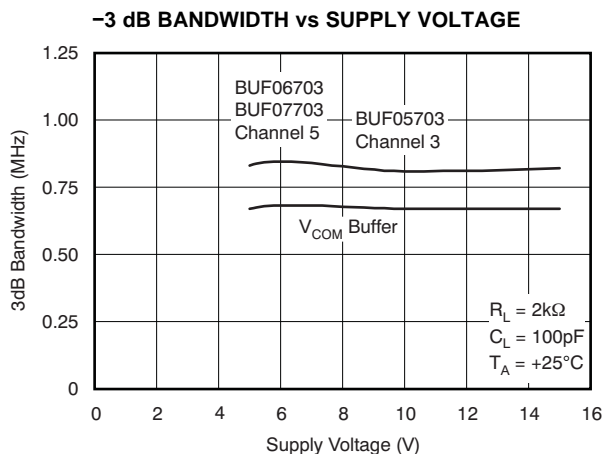


Figure 21.

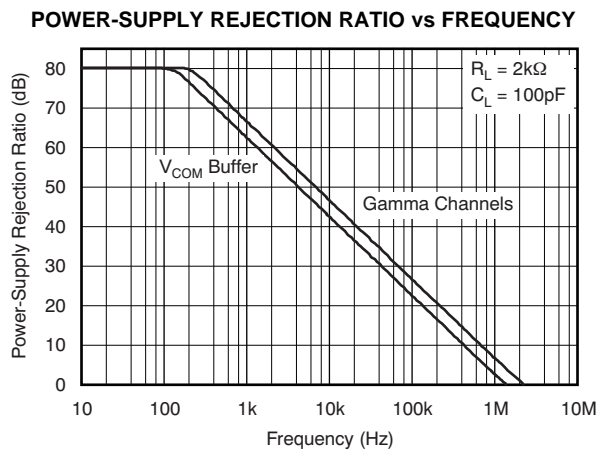


Figure 22.

TYPICAL CHARACTERISTICS (continued)

At  $V_{DD} = 10V$ , unless otherwise noted.

TRANSIENT CURVES

SUPPLY VOLTAGE, OUTPUT VOLTAGE,  
 AND SUPPLY CURRENT

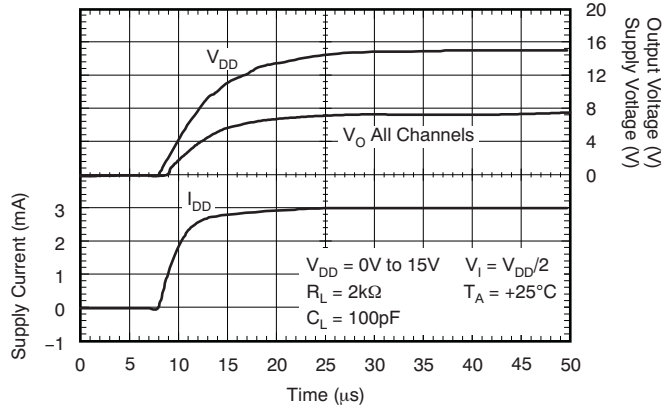


Figure 23.

LARGE-SIGNAL VOLTAGE FOLLOWER

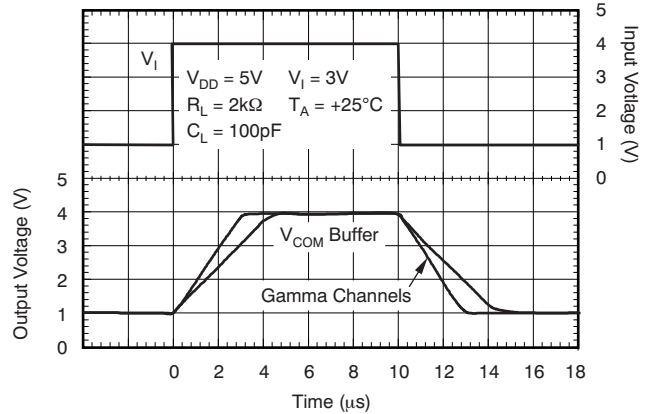


Figure 24.

LARGE-SIGNAL VOLTAGE FOLLOWER

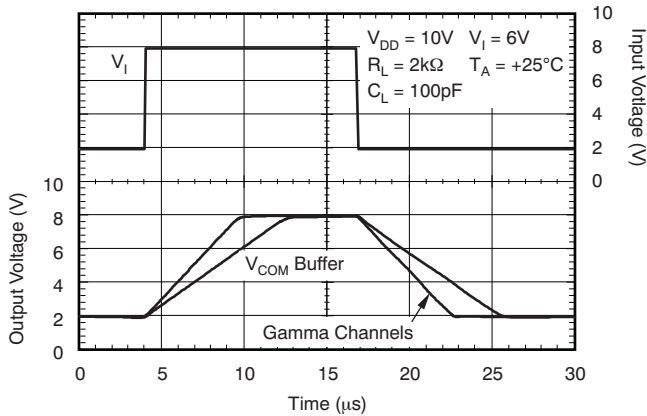


Figure 25.

LARGE-SIGNAL VOLTAGE FOLLOWER

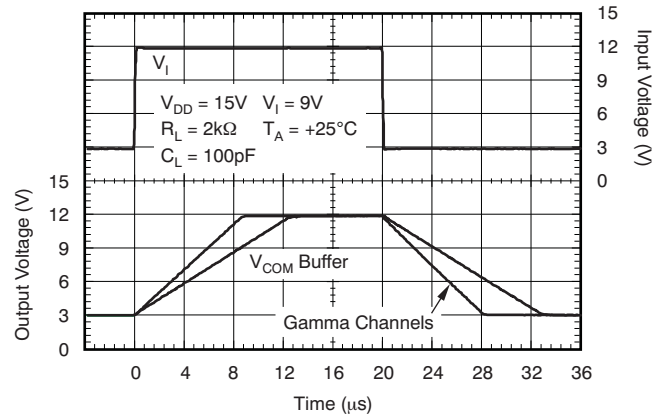


Figure 26.

SMALL-SIGNAL VOLTAGE FOLLOWER

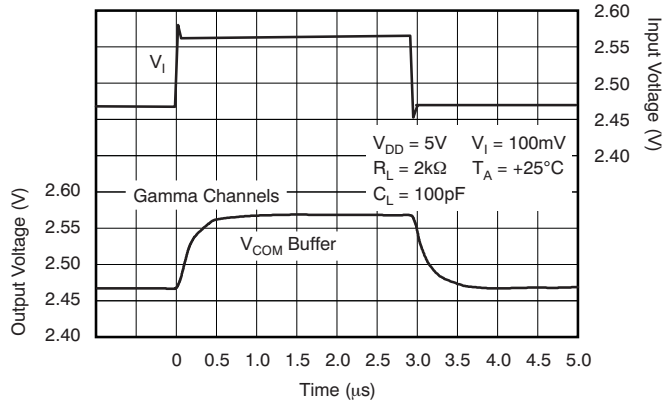


Figure 27.

SMALL-SIGNAL VOLTAGE FOLLOWER

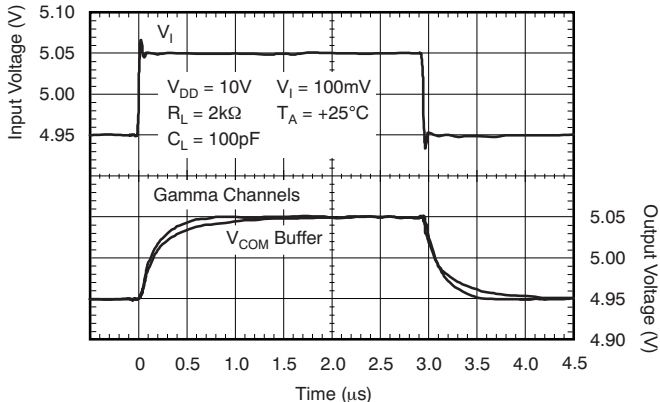


Figure 28.

TYPICAL CHARACTERISTICS (continued)

At  $V_{DD} = 10V$ , unless otherwise noted.

SMALL-SIGNAL VOLTAGE FOLLOWER

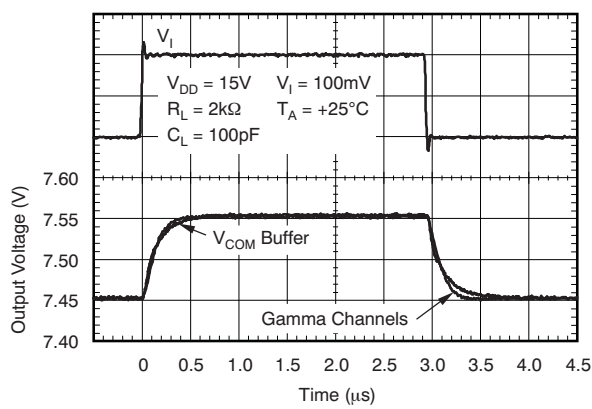


Figure 29.

TRANSIENT LOAD RESPONSE: SOURCING

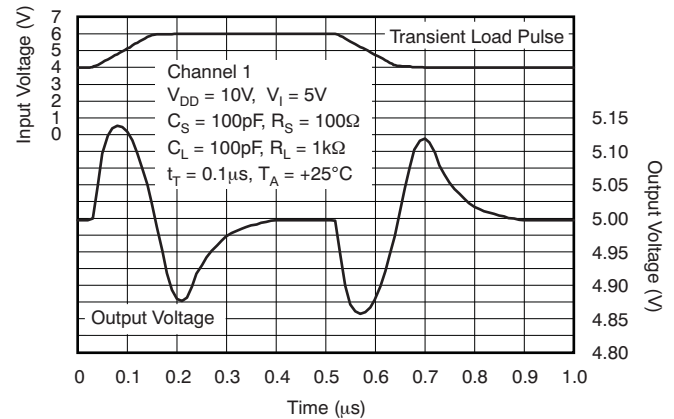


Figure 30.

TRANSIENT LOAD RESPONSE: SINKING

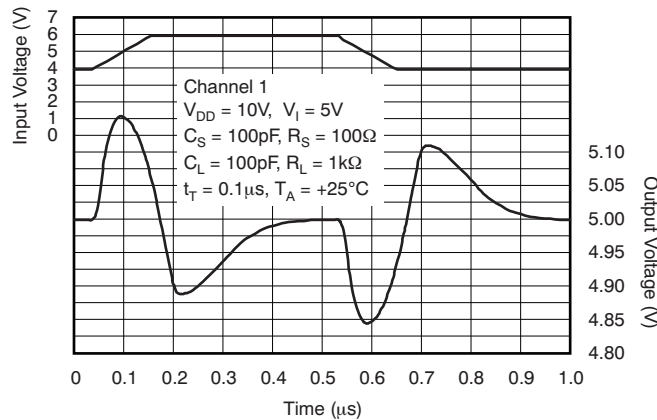


Figure 31.

TRANSIENT LOAD REGULATION: SINKING

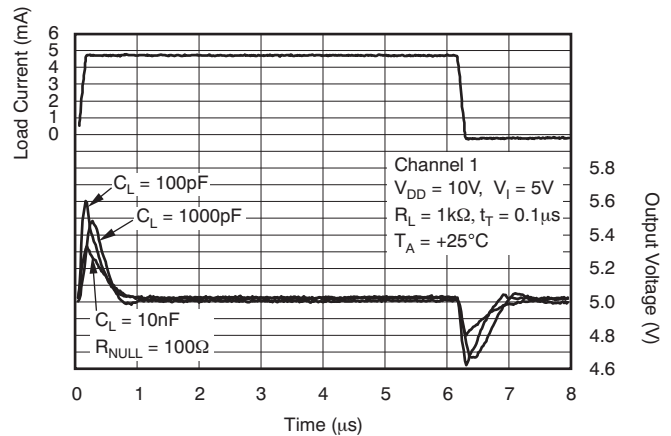


Figure 32.

TRANSIENT LOAD REGULATION: SOURCING

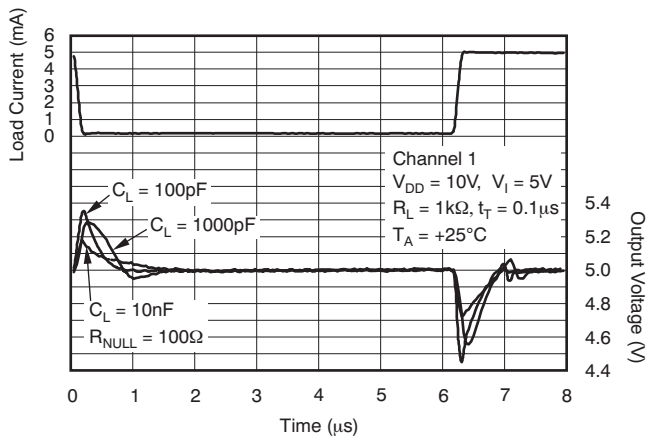


Figure 33.

TRANSIENT LOAD REGULATION: VCOM BUFFER

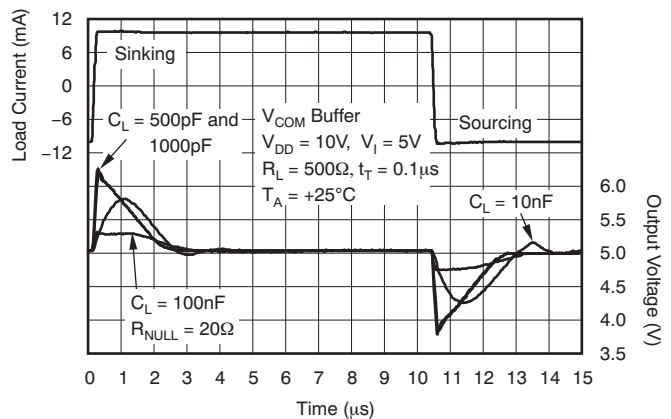


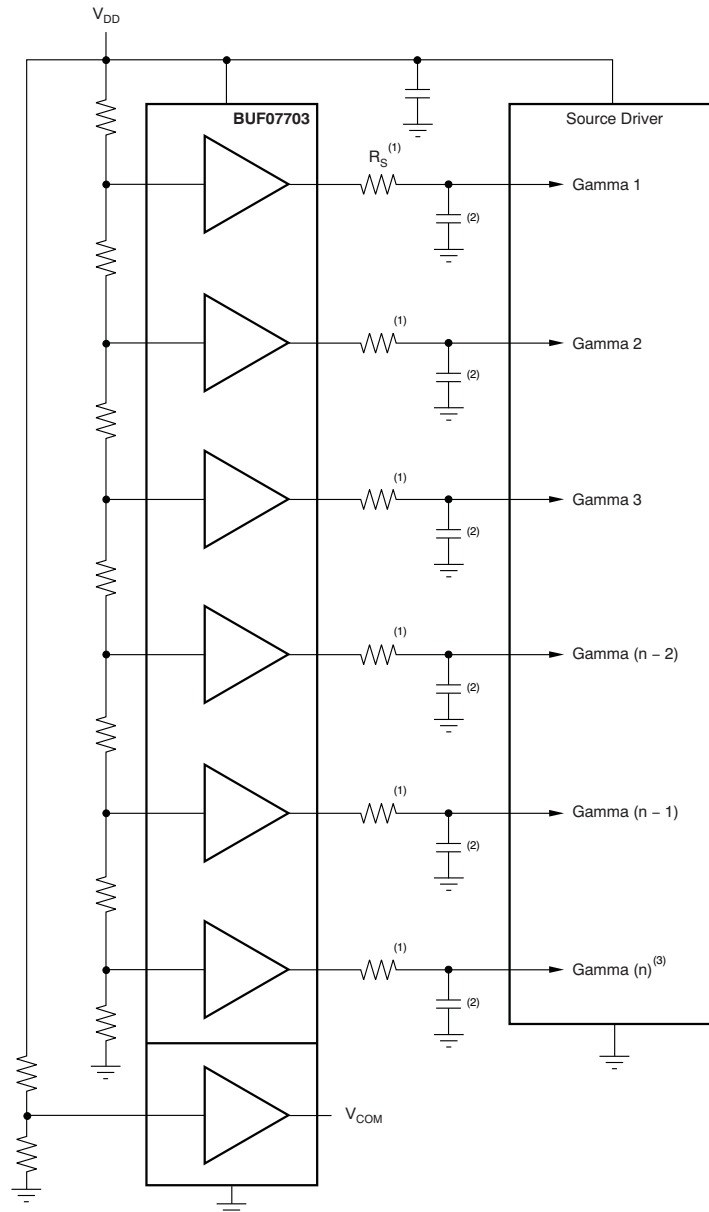
Figure 34.

### APPLICATION INFORMATION

The requirements on the number of gamma correction channels vary greatly from panel to panel. Therefore, the BUFxx703 series of gamma correction buffers offers different channel combinations. The  $V_{COM}$  channel can be used to drive the  $V_{COM}$  node on the LCD panel.

Gamma correction voltages are often generated using a simple resistor ladder, as shown in Figure 35.

The BUFxx703 buffers the various nodes on the gamma correction resistor ladder. The low output impedance of the BUFxx703 forces the external gamma correction voltage on the respective reference node of the LCD source driver. Figure 35 shows an example of the BUFxx703 in a typical block diagram driving an LCD source driver with 6-channel gamma correction reference inputs.



- (1) Optional; increases stability.
- (2) Stable without  $R_S$  up to  $30\mu F$ .
- (3)  $n$  = maximum number of gamma channels on respective BUFxx7703 devices.

Figure 35. LCD Source Driver Typical Block Diagram

## INPUT VOLTAGE RANGE GAMMA BUFFERS

Figure 36 shows a typical gamma correction curve with 10 gamma correction reference points (GMA1 through GMA10). As can be seen from this curve, the voltage requirements for each buffer varies greatly. The swing capability of the input stages of the various buffers in the BUFxx703 is carefully matched to the application. Using the example of the BUF07703 with six gamma correction channels, buffers 1 to 3 have input stages that include  $V_{DD}$ , but will only swing within 1V to GND. Buffers 1 through 5 have only a single NMOS input stage. Buffers 4 through 6 have only a single PMOS input stage. The input range of the PMOS input stage includes GND.

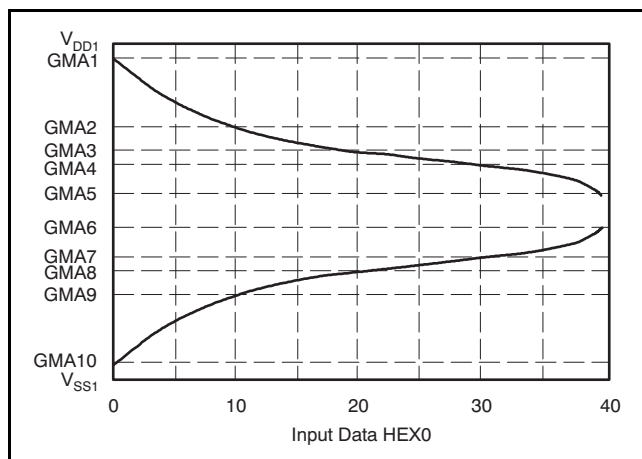


Figure 36. Gamma Correction Curve

## OUTPUT VOLTAGE SWING GAMMA BUFFERS

The output stages have been designed to match the characteristic of the input stage. Once again using the example of the BUF07703 means that the output stage of buffer 1 swings very close to  $V_{DD}$ , typically  $V_{CC} - 100\text{mV}$  at 5mA; its ability to swing to GND is limited. Buffers 2 and 3 have smaller output stages with slightly larger output resistances, as they will not have to swing as close to the positive rail as buffer 1. Buffers 4 through 6 swing closer to GND than  $V_{DD}$ . Buffer 6 is designed to swing very close to GND, typically  $\text{GND} + 100\text{mV}$  at a 5mA load current. See the [Typical Characteristics](#) for more details. This approach significantly reduces the silicon area and cost of the whole solution. However, due to this architecture, the correct buffer needs to be connected to the correct gamma correction voltage.

Connect buffer 1 to the gamma voltage closest to  $V_{DD}$ , and buffers 2 and 3 to the sequential voltages. Buffer 6 should be connected to the gamma correction voltage closest to GND (or the negative rail), buffers 4 and 5 to the sequential higher voltages.

## COMMON BUFFER ( $V_{COM}$ )

The common buffer output of the BUF07703 and BUF05703 has a greater output drive capability than the gamma correction buffers, to meet the heavier current demands of driving the common node of the LCD panel. It was also designed to drive heavier capacitive loads and still remain stable, as shown in Figure 37.

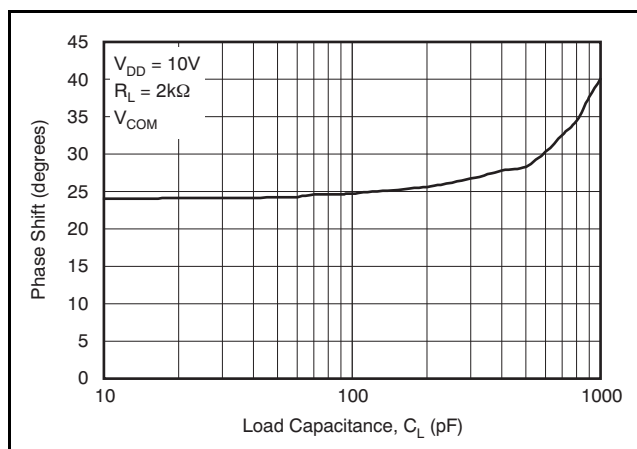


Figure 37. Phase Shift vs Load Capacitance

## CAPACITIVE LOAD DRIVE

The BUFxx703 has been designed to be able to sink/source DC currents in excess of 10mA. Its output stage has been designed to deliver output current transients with little disturbance of the output voltage. However, there are times when very fast current pulses are required. Therefore, in LCD source-driver buffer applications, it is quite normal for capacitors to be placed at the outputs of the reference buffers. These are to improve the transient load regulation. These will typically vary from 100pF and more. The BUFxx703 gamma buffers were designed to drive capacitances in excess of 100pF and retain effective phase margins above  $50^\circ$ , as shown in Figure 38.

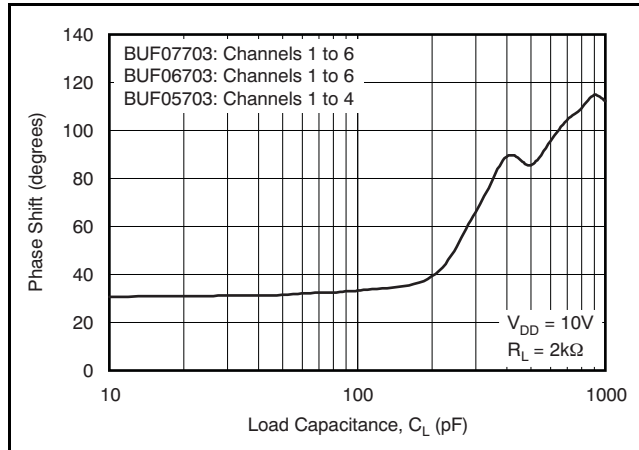


Figure 38. Phase Shift Between Output and Input vs Load Capacitance for the Gamma Buffers

### APPLICATIONS WITH >10 GAMMA CHANNELS

When a greater number of gamma correction channels are required, two or more BUFxx703 devices can be used in parallel, as shown in Figure 39. This provides a cost-effective way of creating more reference voltages over the use of quad-channel op amps or buffers. The suggested configuration in Figure 39 simplifies layout. The various different channel versions provide a high degree of flexibility and also minimize total cost and space. Table 1 lists a variety of gamma combinations for applications with more than 10 channels.

Table 1. > 10 Channel Gamma Combinations

	BUF11702	BUF07703	BUF06703	BUF05703
12ch	—	—	2	—
12ch + V <sub>COM</sub>	—	1	1	—
14ch + V <sub>COM</sub>	1	—	—	1
16ch + V <sub>COM</sub>	1	—	1	—
18ch + V <sub>COM</sub>	2	—	—	—
20ch + V <sub>COM</sub>	2	—	—	—

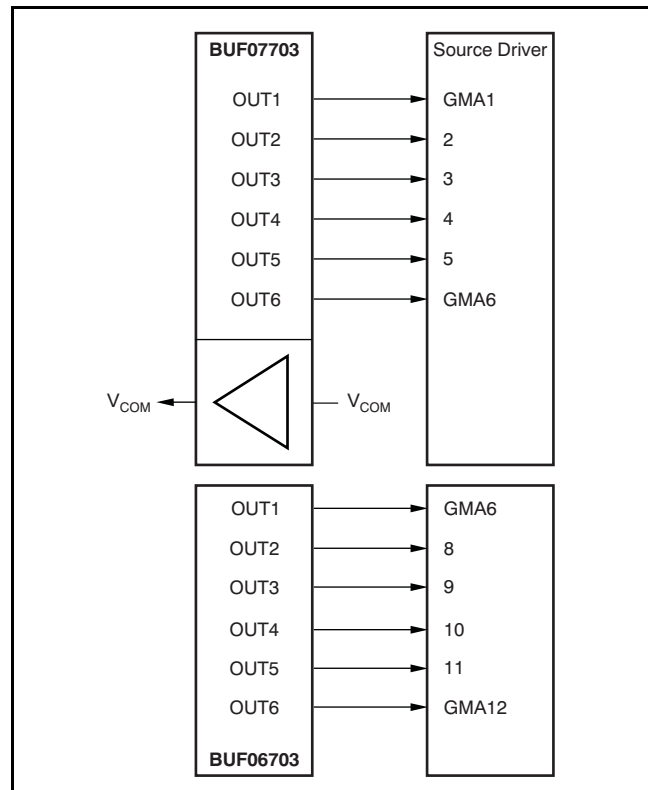


Figure 39. Creating > 10 Gamma Voltage Channels

### MULTIPLE V<sub>COM</sub> CHANNELS

In some LCD panels, more than one V<sub>COM</sub> driver is required for best panel performance. Figure 40 uses three BUF07703s to create a total of 18 gamma-correction and three V<sub>COM</sub> channels. This solution saves considerable space and cost over the more conventional approach of using five or six quad-channel buffers or op amps.



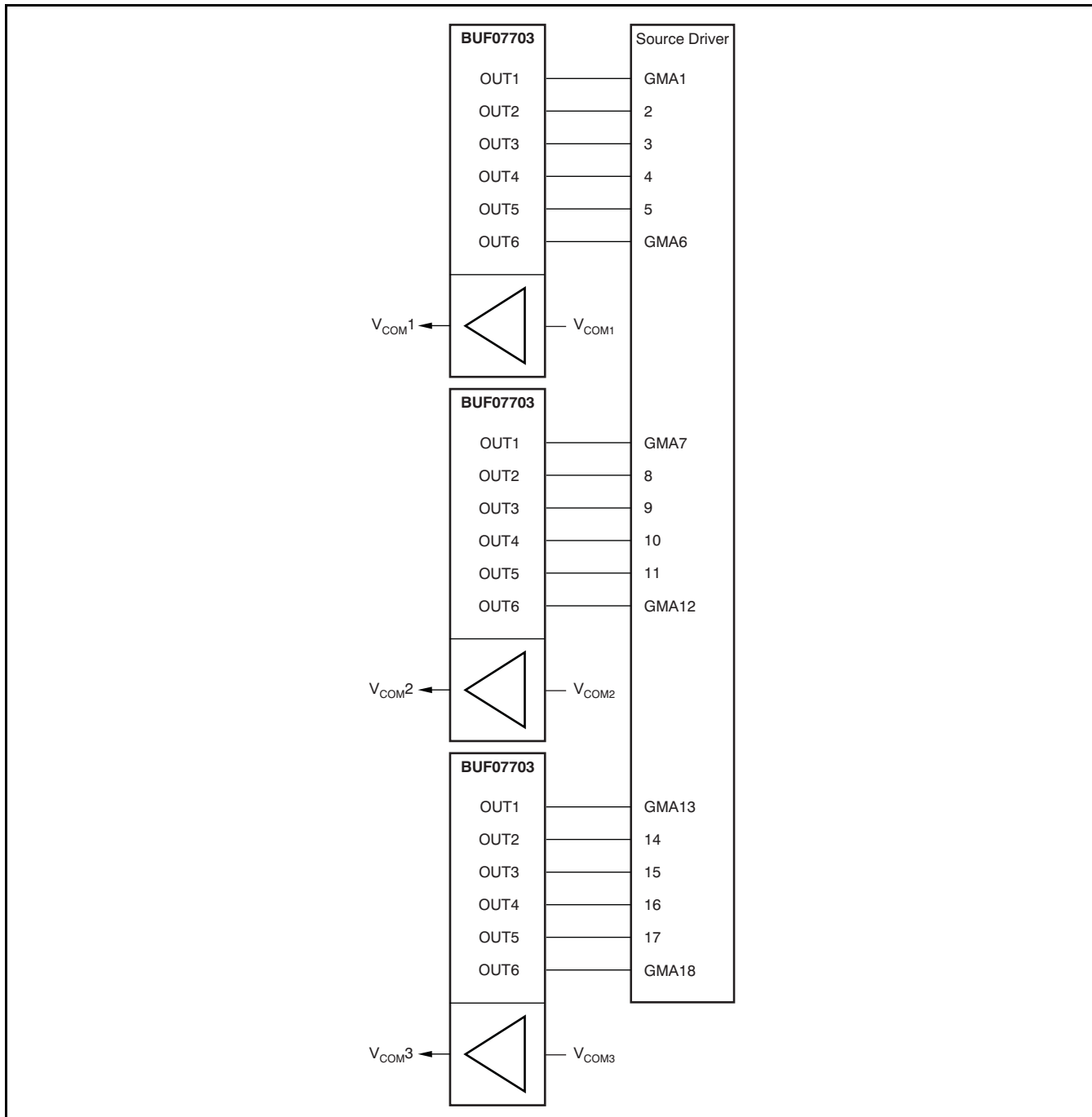


Figure 40. 18-Channel Application with Five Integrated  $V_{COM}$  Channels

## COMPLETE LCD SOLUTION FROM TI

Besides the BUFxx703 line of gamma correction buffers, TI offers a complete set of ICs for the LCD panel market: source and gate drivers, various power-supply solutions, as well as audio power solutions. Figure 41 shows the total IC solution from TI.

### Audio Power Amplifier for TV Speakers

The TPA3002D2 is a 7W (per channel) stereo audio amplifier specifically targeted towards LCD monitors and TVs. It offers highly efficient, filter-free Class-D operation for driving bridged tied stereo speakers. The TPA3002D2 is designed to drive stereo speakers as low as  $8\Omega$  without an output filter. The high efficiency of the TPA3002D2 eliminates the need for external heatsinks when playing music. Stereo speaker volume is controlled with a dc voltage applied to the volume control terminal offering a range of gain from  $-40\text{dB}$  to  $+36\text{dB}$ . Line outputs, for driving external headphone amplifier inputs, are also dc voltage controlled with a range of gain from  $-56\text{dB}$  to  $+20\text{dB}$ . An integrated  $+5\text{V}$  regulated supply is provided for powering an external headphone

amplifier. Texas Instruments offers a full line of linear and switch-mode audio power amplifiers. For excellent audio performance TI recommends the OPA364 or OPA353 as headphone drivers. For more information visit [www.ti.com](http://www.ti.com).

### Integrated DC/DC Converter for LCD Panels: TPS65100

The TPS65100 offers a very compact and small power supply solution to provide all three power-supply voltages required by TFT (thin film transistor) LCD displays. Additionally the device has an integrated  $V_{\text{COM}}$  buffer. The auxiliary linear regulator controller can be used to generate the  $3.3\text{V}$  logic power rail for systems powered by a  $5\text{V}$  supply rail only. The main output can power the LCD source drivers as well as the BUFxx703. An integrated adjustable charge pump doubler/tripler provides the positive LCD gate drive voltage. An externally adjustable negative charge pump provides the negative gate drive voltage. The TPS65100 has an integrated  $V_{\text{COM}}$  buffer to power the LCD backplane. A version of the BUFxx703 without the integrated  $V_{\text{COM}}$  buffer could be used for minimum redundancy and lowest cost. For LCD panels powered by  $5\text{V}$  only, the TPS65100 has a linear regulator controller that uses an external transistor to provide a regulated  $3.3\text{V}$  output for the digital circuits. Contact the local sales office for more information.

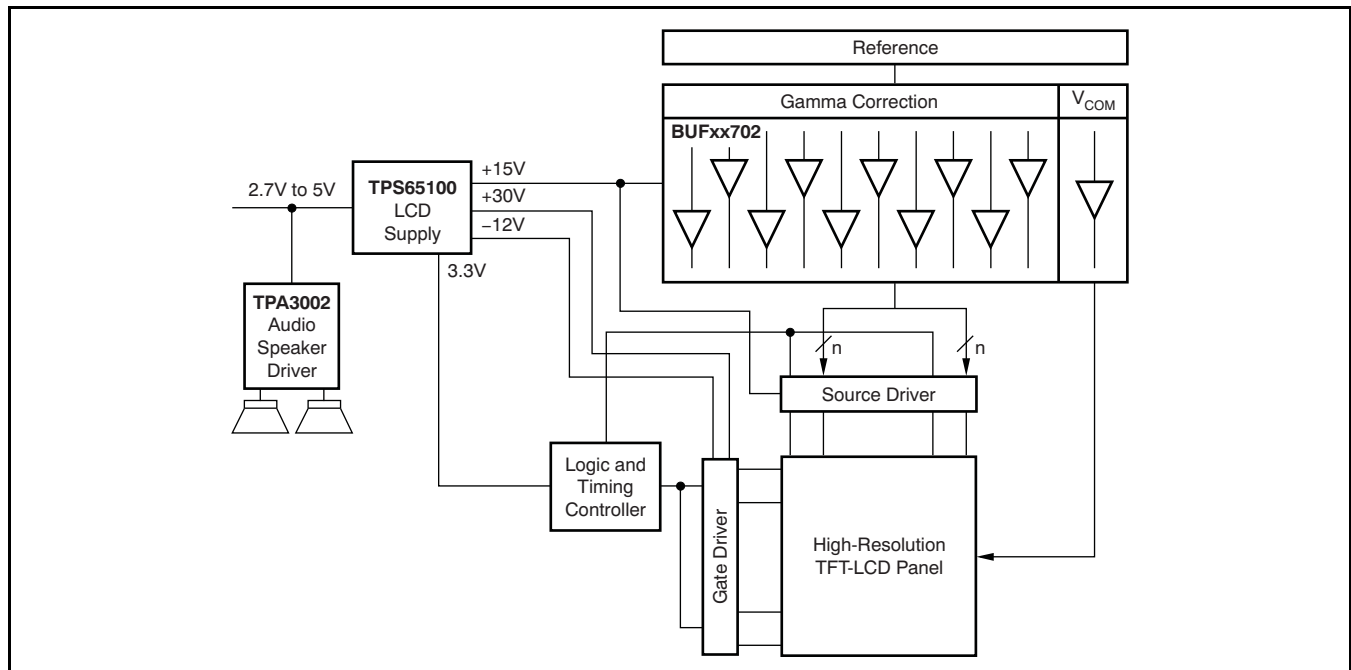


Figure 41. TI LCD Solution

## GENERAL PowerPAD DESIGN CONSIDERATIONS

The BUF07703 is available in the thermally enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted; see [Figure 42\(a\)](#) and [\(b\)](#). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package; see [Figure 42\(c\)](#). Due to this thermal pad having direct thermal contact with the die, excellent thermal performance is achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device. Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

1. Prepare the PCB with a top-side etch pattern, (see [Pin Configurations](#)). There must be etching for the leads as well as etch for the thermal pad.
2. Place 18 holes in the area of the thermal pad. These holes must be 13 mils in diameter. Keep them small, so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the BUF07703 IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered, so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during

soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the BUF07703 PowerPAD package must make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.

6. The top-side solder mask must leave the terminals of the package and the thermal pad area with its five holes (dual) or nine holes (quad) exposed. The bottom-side solder mask must cover the five or nine holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the BUF07703 IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

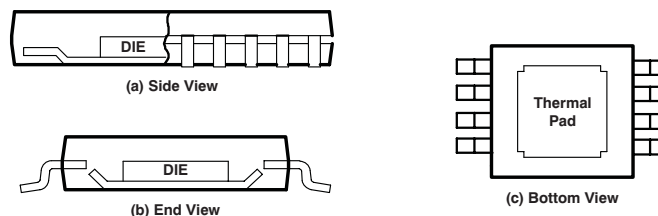
For a given  $\theta_{JA}$ , the maximum power dissipation is calculated by the following formula:

$$P_D = \left( \frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

- $P_D$  = maximum power dissipation (W)
- $T_{MAX}$  = absolute maximum junction temperature (+150°C)
- $T_A$  = free-ambient air temperature (°C)
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- $\theta_{JC}$  = thermal coefficient from junction to case (°C/W)
- $\theta_{CA}$  = thermal coefficient from case-to-ambient air (°C/W)

This lower thermal resistance enables the BUF07703 to deliver maximum output currents even at high ambient temperatures.



Note: The thermal pad is electrically isolated from all terminals in the package.

**Figure 42. Views of Thermally-Enhanced DGN Package**

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November, 2007) to Revision C	Page
• Updated document format to current standards .....	1
• Updated <i>Features</i> bullet: changed temperature specification lower limit from 0°C to –40°C .....	1
• Updated format of <i>Package Information</i> table .....	2
• Deleted lead temperature specification from, changed operating free-air temperature specification in <i>Absolute Maximum Ratings</i> .....	2
• Changed operating free-air temperature specification in <i>Recommended Operating Conditions</i> to –40°C .....	2
• Changed footnote to <i>Electrical Characteristics</i> table .....	3
• Changed footnote to <i>Electrical Characteristics: BUF07703</i> table .....	4
• Changed footnote to <i>Electrical Characteristics: BUF07703</i> table .....	5
• Changed footnote to <i>Electrical Characteristics: BUF07703</i> table .....	6
• Updated Typical Characteristics Figure 9 through Figure 18 .....	9
• Replaced Figure 20 .....	11
• Deleted previous Figure 21 (–3dB Bandwidth vs Free-Air Temperature graph) .....	11

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BUF05703PWR	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BUF05703
BUF05703PWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BUF05703
BUF06703PWR	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BF06703
BUF06703PWR.A	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BF06703

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BUF05703PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
BUF06703PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BUF05703PWR	TSSOP	PW	14	2000	350.0	350.0	43.0
BUF06703PWR	TSSOP	PW	16	2000	353.0	353.0	32.0



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

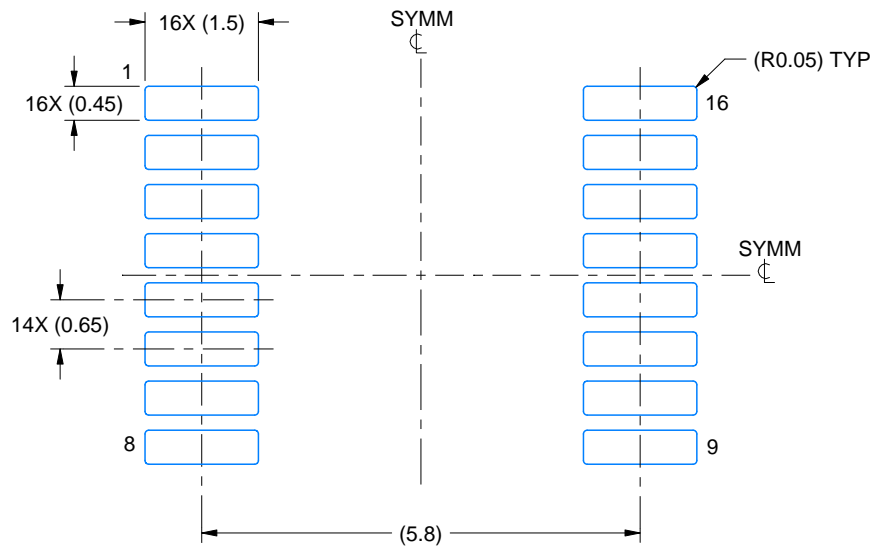


# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0014A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

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TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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