CC2340R5MODA SimpleLink™ 2.4GHz Wireless MCU Module with Integrated Antenna

1 Features

Certified wireless module

- Optimized 48MHz Arm® Cortex®-M0+ processor
- 512KB of in-system programmable flash
- 12KB of ROM for bootloader and drivers
- 64KB of ultra-low leakage SRAM. Full RAM retention in standby mode
- 2.4GHz RF transceiver compatible with Bluetooth® Low Energy
- Built on the CC2340R53 WCSP package
- Integrated antenna
- Optional external antenna
- Supports over-the-air upgrade (OTA)
- Serial wire debug (SWD)

Low power consumption

- MCU consumption:
  - 2.6mA active mode, CoreMark®
  - 53µA/MHz running CoreMark®
  - 710nA standby mode
  - 165nA shutdown mode, wake-up on pin
- Radio consumption:
  - 5.5mA RX
  - 5.1mA TX at 0dBm
  - < 11.0mA TX at +8dBm

Wireless protocol support

- Bluetooth® LE[1]
  - Features: LE 2M, LE Coded, Periodic Advertising, Extended Advertising, LE Secure Connections
  - Qualified against Bluetooth Core 5.4

High-performance radio

- -102dBm sensitivity for Bluetooth® Low Energy 125kbps
- -96.5dBm sensitivity for Bluetooth® Low Energy 1Mbps
- Output power up to +8dBm with temperature compensation

Regulatory compliance

- Designed for systems targeting compliance with these standards:
  - EN 300 328 (Europe)
  - FCC CFR47 Part 15
  - ARIB STD-T66 (Japan)
  - ISED (Canada)
  - NCC (Taiwan)
  - KCC (Korea)

[1] Module is pre-certified for Bluetooth LE only

MCU peripherals

- Up to 12 I/O pads
  - 2 IO pads SWD, muxed with GPIOs
  - 2 IO pads LFXT, muxed with GPIOs
  - Up to 12 DIOs (analog or digital IOs)
- 3 × 16-bit and 1× 24-bit general-purpose timers, quadrature decode mode support
- 12-bit ADC, 267ksps with internal reference, 4 external ADC inputs
- 1× low power comparator
- 1× UART
- 1× SPI
- 1× I^2C
- Real-time clock (RTC)
- Integrated temperature and battery monitor
- Watchdog timer

Security enablers

- AES 128-bit cryptographic accelerator
- Random number generator from on-chip analog noise

Development tools and software

- LP-EM-CC2340R53 LaunchPad Development Kit
- LP-EM-CC2340R5MODA Design Files
- SimpleLink™ Low Power F3 software development kit
- SmartRF™ Studio for simple radio configuration
- SysConfig system configuration tool

Operating range

- On-chip buck DC/DC converter
- 1.71V to 3.8V single supply voltage
- T_j: –40°C up to +85°C

RoHS-compliant package

- 7mm x 10mm 24 pin MHA Package

2 Applications

- Medical
  - Home healthcare – blood glucose monitors, blood pressure monitor, CPAP machine, electronic thermometer
  - Patient monitoring and diagnostics – medical sensor patches
  - Personal care and fitness – electric toothbrush, wearable fitness & activity monitor
- Building automation
  - Building security systems – motion detector, electronic smart lock, door and window sensor, garage door system, gateway
  - HVAC – thermostat, wireless environmental sensor
  - Fire safety system – smoke and heat detector
  - Video surveillance – IP network camera
- Lighting
  - LED luminaire
  - Lighting control – daylight sensor, lighting sensor, wireless control
- Factory automation and control
- Retail automation & payment – electronic point of sale
  - Electronic shelf label
- Grid infrastructure
  - Smart meters – water meter, gas meter, electricity meter, and heat cost allocators
  - Grid communications – wireless communications – Long-range sensor applications
  - Other alternative energy – energy harvesting
- Communication equipment
  - Wired networking
  - wireless LAN or Wi-Fi access points, edge router
- Personal electronics
  - Connected peripherals – consumer wireless module, pointing devices, keyboards and keypads
  - Gaming – electronic and robotic toys
  - Wearables (non-medical) – smart trackers, smart clothing

3 Description

The CC2340R5MODA SimpleLink™ of devices are 2.4GHz wireless microcontrollers (MCUs), targeting Bluetooth® Low Energy. These devices are optimized for low-power wireless communication with Over the Air Download (OAD) support in Building automation (wireless sensors, lighting control, beacons), asset tracking, medical, and Personal electronics (toys) markets. Highlighted features of this device include:

- The CC2340R5MODA is a 7mm x 10mm certified wireless module 2.4GHz with integrated antenna, DCDC components and high-frequency crystal oscillator.
- Support for Bluetooth 5 features: high-speed mode (2Mbps PHY), long-range (LE Coded 125kbps and 500kbps PHYs), privacy 1.2.1 and channel selection algorithm #2, as well as backward compatibility and support for key features from the Bluetooth 4.2 and earlier Low Energy specifications.
- Fully qualified Bluetooth software protocol stack included with the SimpleLink™ Low Power F3 software development kit (SDK)
- Ultra-low standby current less than 0.71µA with RTC operational and full RAM retention that enables significant battery life extension, especially for applications with longer sleep intervals.
- Excellent radio sensitivity and robustness (selectivity and blocking) performance for Bluetooth Low Energy (–102dBm for 125kbps LE Coded PHY)

The CC2340R5MODA family is part of the SimpleLink™ MCU platform, which consists of Wi-Fi®, Bluetooth Low Energy, Thread, Zigbee, Sub-1GHz MCUs, and host MCUs that all share a common, easy-to-use development environment with a single-core software development kit (SDK) and rich tool set. A one-time integration of the SimpleLink™ platform enables you to add any combination of the portfolio's devices into your design, allowing 100 percent code reuse when your design requirements change. For more information, visit the SimpleLink™ MCU platform.

Device Information

PART NUMBER(1)	FLASH	RAM	TEMPERATURE RANGE	PACKAGE	STATUS
CC2340R5MODAN0MHAR	512kB	64kB	–40°C–85°C	MHA24	Preview

(1) For more information, see Section 13.

4 Functional Block Diagram

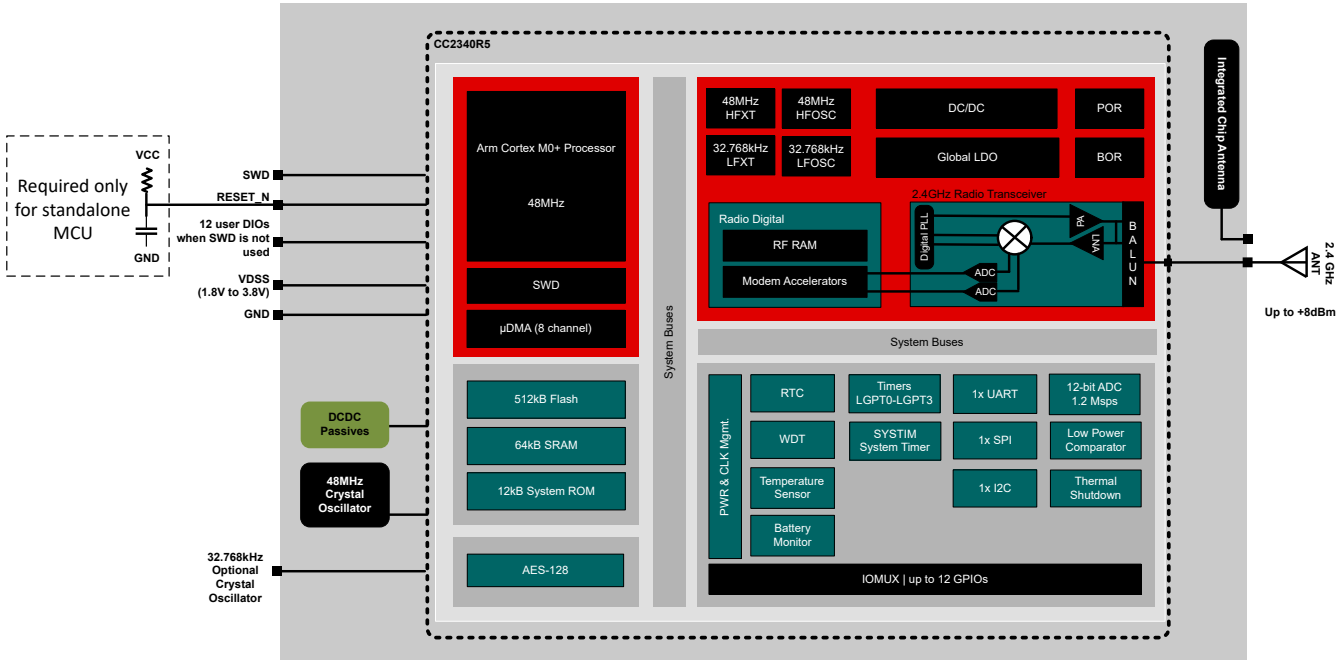

Figure 4-1. CC2340R5MODA Block Diagram

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5 Device Comparison

Module	ANTENNA		RADIO SUPPORT			CERTIFICATIONS						FLASH (KB)	RAM + Cache (KB)	GPIO	PACKAGE SIZE			
	External	Integrated	*Bluetooth*® LE	ZigBee	+10dBm PA	FCC/IC	CE	RER (UK)	Japan	Korea	Taiwan				7 x 7 QFM (73)	7 x 7 QFM (59)	16.9 x 11.0 QFM (29)	7 x 10 MHA (24)
CC2340R5MODA	X	X	X			X	X	X	X	X	X	512	64	12				X
CC2650MODA		X	X	X		X	X		X			128	20 + 8	15			X	
CC2651R3SIPA	X	X	X	X		X	X	X	X	X	X	352	32 + 8	32		X		
CC2652RSIP	X		X	X		X	X	X				352	80 + 8	32	X			
CC2652PSIP	X		X	X	X	X	X	X				352	80 + 8	30	X			

6 Pin Configurations and Functions

6.1 Pin Diagrams

6.1.1 Pin Diagram - MHA Package (Top View)

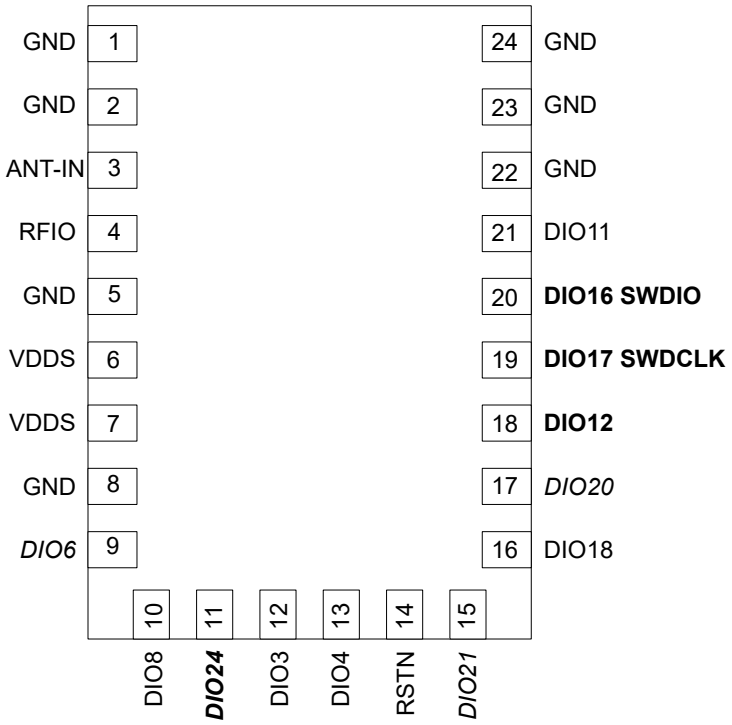


Figure 6-1. Pin Diagram - MHA Package (Top View)

The following I/O pins marked in Pin Diagram - MHA Package (Top View)in **bold** have high-drive capabilities:

- Pin 18, DIO12
- Pin 20, DIO16_SWDIO
- Pin 19, DIO17_SWDCK
- Pin 11, DIO24_A7

The following I/O pins marked in Pin Diagram - MHA Package (Top View) in *italics* have analog capabilities:

- Pin 17, DIO20_A11
- Pin 15, DIO21_A10
- Pin 11, DIO24_A7
- Pin 9, DIO6_A1

Table 6-1. Pin Attributes (MHA Package)

PIN NUMBER	SIGNAL NAME	PIN NAME	MUX ENCODING	SIGNAL TYPE
3	ANT-IN	ANT-IN		RF
10	DIO8	GPIO8	0	I/O
		SPI0SCLK	1	I/O
		UART0RTS	2	I/O
		T1C0N	3	I/O
		I2C0SDA	4	I/O
		T0C0N	5	I/O
		DTB3	7	I/O

Table 6-1. Pin Attributes (MHA Package) (continued)

PIN NUMBER	SIGNAL NAME	PIN NAME	MUX ENCODING	SIGNAL TYPE
21	DIO11	GPIO11	0	I/O
		SPI0CSN	1	I/O
		T1C2N	2	I/O
		T0C0	3	I/O
		LRFD0	4	I/O
		SPI0POCI	5	I/O
		DTB9	7	I/O
18	DIO12	GPIO12	0	I/O
		SPI0POCI	1	I/O
		SPI0PICO	2	I/O
		UART0RXD	3	I/O
		T1C1	4	I/O
		I2C0SDA	5	I/O
		DTB13	7	I/O
20	DIO16_SWDIO	GPIO16	0	I/O
		SPI0PICO	1	I/O
		UART0RXD	2	I/O
		I2C0SDA	3	I/O
		T1C2	4	I/O
		T1C0N	5	I/O
		DTB10	7	I/O
19	DIO17_SWDCK	GPIO17	0	I/O
		SPI0SCLK	1	I/O
		UART0TXD	2	I/O
		I2C0SCL	3	I/O
		T1C1N	4	I/O
		T0C2	5	I/O
		DTB11	7	I/O
16	DIO18	GPIO18	0	I/O
		T3C0	1	I/O
		LPCO	2	I/O
		UART0TXD	3	I/O
		SPI0SCLK	4	I/O
		DTB12	7	I/O
17	DIO20_A11	GPIO20	0	I/O
		LPCO	1	I/O
		UART0TXD	2	I/O
		UART0RXD	3	I/O
		T1C0	4	I/O
		SPI0POCI	5	I/O
		ANA11	6	ANALOG
		DTB14	7	I/O
15	DIO21_A10	GPIO21	0	I/O
		UART0CTS	1	I/O
		T1C1N	2	I/O
		T0C1	3	I/O
		SPI0POCI	4	I/O
		LRFD1	5	I/O
		ANA10	6	ANALOG
		DTB15	7	I/O

Table 6-1. Pin Attributes (MHA Package) (continued)

PIN NUMBER	SIGNAL NAME	PIN NAME	MUX ENCODING	SIGNAL TYPE
11	DIO24_A7	GPIO24	0	I/O
		SPI0SCLK	1	I/O
		T1C0	2	I/O
		T3C0	3	I/O
		T0PE	4	I/O
		I2C0SCL	5	I/O
		ANA7	6	ANALOG
		DTB5	7	I/O
12	DIO3_X32P	GPIO3	0	I/O
		LFCI	1	I/O
		T0C1N	2	I/O
		LRFD0	3	I/O
		T3C1	4	I/O
		T1C2	5	I/O
		LFXT_P	6	I/O
		DTB7	7	I/O
13	DIO4_X32N	GPIO4	0	I/O
		T0C2N	1	I/O
		UART0TXD	2	I/O
		LRFD1	3	I/O
		SPI0PICO	4	I/O
		T0C2	5	I/O
		LFXT_N	6	I/O
		DTB8	7	I/O
9	DIO6_A1	GPIO6	0	I/O
		SPI0CSN	1	I/O
		I2C0SCL	2	I/O
		T1C2	3	I/O
		LRFD2	4	I/O
		UART0TXD	5	I/O
		ANA1	6	ANALOG
		DTB6	7	I/O
1, 2, 22, 23, 24, 5, 8	GND	GND		GND
4	RFIO	RFIO		RF
14	RSTN	RSTN		I/O
6, 7	VDDS	VDDS		PWR

6.2 Signal Descriptions

Table 6-2. Analog Input Signal Descriptions

SIGNAL NAME	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION	MHA PIN
ANA1	ANALOG	I	ADC reference (positive terminal) or ADC channel 1 input	9
ANA7	ANALOG	I	Low power comparator input (positive or negative terminal) / ADC channel 7 input	11
ANA10	ANALOG	I	Low power comparator input (positive terminal) / ADC channel 10 input	15
ANA11	ANALOG	I	ADC channel 11 input	17

Table 6-3. Clock Signal Descriptions

SIGNAL NAME	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION	MHA PIN
LFCI	I/O	I	Low frequency clock input (LFXT bypass clock from pin)	12
LFXT_N	I/O	I	32kHz crystal oscillator pin 2	13

Table 6-3. Clock Signal Descriptions (continued)

SIGNAL NAME	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION	MHA PIN
LFXT_P	I/O	I	32kHz crystal oscillator pin 1	12

Table 6-4. DTB Signal Descriptions

SIGNAL NAME	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION	MHA PIN
DTB3	I/O	O	Digital test bus output 3	10
DTB5	I/O	O	Digital test bus output 5	11
DTB6	I/O	O	Digital test bus output6	9
DTB7	I/O	O	Digital test bus output 7	12
DTB8	I/O	O	Digital test bus output 8	13
DTB9	I/O	O	Digital test bus output 9	21
DTB10	I/O	O	Digital test bus output 10	20
DTB11	I/O	O	Digital test bus output 11	19
DTB12	I/O	O	Digital test bus output 12	16
DTB13	I/O	O	Digital test bus output 13	18
DTB14	I/O	O	Digital test bus output 14	17
DTB15	I/O	O	Digital test bus output 15	15

Table 6-5. GPIO Signal Descriptions

SIGNAL NAME	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION	MHA PIN
GPIO3	I/O	I/O	General-purpose input or output	12
GPIO4	I/O	I/O	General-purpose input or output	13
GPIO6	I/O	I/O	General-purpose input or output	9
GPIO8	I/O	I/O	General-purpose input or output	10
GPIO11	I/O	I/O	General-purpose input or output	21
GPIO12	I/O	I/O	General-purpose input or output	18
GPIO16	I/O	I/O	General-purpose input or output	20
GPIO17	I/O	I/O	General-purpose input or output	19
GPIO18	I/O	I/O	General-purpose input or output	16
GPIO20	I/O	I/O	General-purpose input or output	17
GPIO21	I/O	I/O	General-purpose input or output	15
GPIO24	I/O	I/O	General-purpose input or output	11

Table 6-6. Device Grounds

SIGNAL NAME	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION	MHA PIN
GND	GND	N/A	Ground	1, 2, 22, 23, 24, 5, 8

Table 6-7. I2C Signal Descriptions

SIGNAL NAME	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION	MHA PIN
I2C0SCL	I/O	I/O	I2C0 clock	11, 19, 9
I2C0SDA	I/O	I/O	I2C0 data	10, 18, 20

Table 6-8. Low Power Comparator Output Signal Descriptions

SIGNAL NAME	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION	MHA PIN
LPCO	I/O	O	Low power comparator output	16, 17

Table 6-9. Device Power

SIGNAL NAME	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION	MHA PIN
VDDS	PWR	N/A	1.71V to 3.8V supply	6, 7

Table 6-10. Reset Signal Descriptions

SIGNAL NAME	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION	MHA PIN
RSTN	I/O	I	Global main device reset (active low)	14

Table 6-11. Radio Digital Output Signal Descriptions

SIGNAL NAME	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION	MHA PIN
LRFD0	I/O	O	Radio Core Output 0	12, 21
LRFD1	I/O	O	Radio Core Output 1	13, 15
LRFD2	I/O	O	Radio Core Output 2	9

Table 6-12. RF Port

SIGNAL NAME	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION	MHA PIN
ANT-IN	RF	I/O	Connect for integrated antenna	3
RFIO	RF	I/O	50Ohm RF port	4

Table 6-13. SPI Signal Descriptions

SIGNAL NAME	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION	MHA PIN
SPI0CSN	I/O	I/O	SPI0 chip select	21, 9
SPI0PICO	I/O	I/O	SPI0 peripheral in controller out	13, 18, 20
SPI0POCI	I/O	I/O	SPI0 peripheral out controller in	15, 17, 18, 21
SPI0SCLK	I/O	I/O	SPI0 clock	10, 11, 16, 19

Table 6-14. Timers Capture or Compare Signal Descriptions

SIGNAL NAME	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION	MHA PIN
T0C0	I/O	I/O	Capture or compare 0 from timer 0	21
T0C1	I/O	I/O	Capture or compare 1 from timer 0	15
T0C2	I/O	I/O	Capture or compare 2 from timer 0	13, 19
T1C0	I/O	I/O	Capture or compare 0 from timer 1	11, 17
T1C1	I/O	I/O	Capture or compare 1 from timer 1	18
T1C2	I/O	I/O	Capture or compare 2 from timer 1	12, 20, 9
T3C0 (1)	I/O	I/O	Capture or compare 0 from timer 3	11, 16
T3C1	I/O	I/O	Capture or compare 1 from timer 3	12

(1) Timer 3 not available on CC2340R21.

Table 6-15. Timers Complementary Output Signal Descriptions

SIGNAL NAME	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION	MHA PIN
T0C0N	I/O	O	Complementary compare or PWM output 0 from timer 0	10
T0C1N	I/O	O	Complementary compare or PWM output 1 from timer 0	12
T0C2N	I/O	O	Complementary compare or PWM output 2 from timer 0	13
T1C0N	I/O	O	Complementary compare or PWM output 0 from timer 1	10, 20
T1C1N	I/O	O	Complementary compare or PWM output 1 from timer 1	15, 19
T1C2N	I/O	O	Complementary compare or PWM output 2 from timer 0	21

Table 6-16. Timers Prescaler Event Signal Descriptions

SIGNAL NAME	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION	MHA PIN
T0PE	I/O	O	Prescaler event output from timer 0	11

Table 6-17. UART Signal Descriptions

SIGNAL NAME	PIN TYPE	SIGNAL DIRECTION	DESCRIPTION	MHA PIN
UART0CTS	I/O	I	UART0 clear-to-send input (active low)	15
UART0RTS	I/O	O	UART0 request-to-send (active low)	10
UART0RXD	I/O	I	UART0 receive data	17, 18, 20
UART0TXD	I/O	O	UART0 transmit data	13, 16, 17, 19, 9

6.3 Connections for Unused Pins and Modules

Table 6-18. Connections for Unused Pins

FUNCTION	SIGNAL NAME	ACCEPTABLE PRACTICE(1)	PREFERRED PRACTICE(1)
GPIO (digital)	DIOn	NC, GND, or VDDS	NC
SWD	DIO16_SWDIO	NC, GND, or VDDS	NC or VDDS
	DIO17_SWDCK	NC, GND, or VDDS	NC or GND
GPIO (digital or analog)	DIOn_Am	NC, GND, or VDDS	NC
32.768-kHz crystal	DIO3_X32P	NC or GND	NC
	DIO4_X32N		

(1) NC = No connect

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
VDDS	Supply voltage	–0.3	4.1	V
	Voltage on any digital pin(3)	–0.3	VDDS + 0.3, max 4.1	V
	Voltage on crystal oscillator pins X48P and X48N	–0.3	1.24	V
V_{in_adc}	Voltage on ADC input	0	VDDS	V
	Input level, RF pins		5	dBm
T_{stg}	Storage temperature	–40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to ground, unless otherwise noted.
(3) Including analog capable DIOs.

7.2 ESD Ratings

				VALUE	UNIT
MHA package					
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) (3)	All pins	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process
(3) ESD Rating is based on CC2340R53E0YBGR

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating ambient temperature(1) (2)	–40	85	°C
Operating junction temperature(1) (2)	–40	85	°C
Operating supply voltage (VDDS)	1.71	3.8	V
Rising supply voltage slew rate	0	100	mV/µs
Falling supply voltage slew rate(3)	0	1	mV/µs

(1) Operation at or near maximum operating temperature for extended durations will result in a reduction in lifetime.
(2) For thermal resistance details, refer to *Thermal Resistance Characteristics* table in this document.
(3) For small coin-cell batteries, with high worst-case end-of-life equivalent source resistance, a 10-µF VDDS input capacitor must be used to make sure compliance with this slew rate.

7.4 DCDC

When measured on the LP-EM-CC2340R5MODA reference design with T_c = 25°C and DCDC enabled unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDDS supply voltage for DCDC operation (1) (2)		2.2	3.0	3.8	V

(1) When the supply voltage drops below the DCDC operation min voltage, the device automatically transitions to use GLDO regulator on-chip.
(2) A 10µH and 10µF load capacitor are required on the VDDR voltage rail. They should be placed close to the DCDC output pin.

7.5 Global LDO (GLDO)

When measured on the LP-EM-CC2340R5MODA reference design with T_c = 25°C.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDDS supply voltage for GLDO operation (1)		1.71	3.0	3.8	V

(1) A 10 µF capacitor is recommended at VDDR pin.

7.6 Power Supply and Modules

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDDS_BOD					
Brownout rising threshold (1)			1.68		V
Brownout falling threshold (1)			1.67		V
POR					
power-on reset power-up level			1.5		V
power-on reset power-down level			1.45		V

(1) Brown-out Detector is trimmed at initial boot, value is kept until device is reset by a POR reset or the RSTN pin.

7.7 Battery Monitor

Measured on the LP-EM-CC2340R5MODA reference design with T_c = 25°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			22		mV
Range		1.71		3.8	V
Accuracy	VDDS = 3.0V		30		mV

7.8 Temperature Sensor

Measured on the LP-EM-CC2340R5MODA reference design with T_c = 25°C, V_{DDS} = 3.0V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Accuracy	-40°C to 85°C		±10(1)		°C

(1) Raw output from register.

7.9 Power Consumption - Power Modes

When measured on the LP-EM-CC2340R5MODA reference design with T_c = 25°C, V_{DDS} = 3.0V, DCDC enabled, GLDO disabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Core Current Consumption with DCDC						
I_{core}	Active	MCU running CoreMark from Flash at 48MHz		2.6		mA
I_{core}	Active	MCU running CoreMark from Flash at 48MHz		53		µA / MHz
I_{core}	Idle	Supply Systems and RAM powered, flash disabled, DMA disabled		0.8		mA
I_{core}	Idle	Supply Systems and RAM powered, flash disabled, DMA enabled		0.8		mA
I_{core}	Idle	Supply Systems and RAM powered, flash enabled, DMA disabled		1.1		mA
I_{core}	Idle	Supply Systems and RAM powered, flash enabled, DMA enabled		1.2		mA
I_{core}	Standby	RTC running, full RAM retention LFOSC, DCDC recharge current setting (ipeak = 1)		0.71		µA
I_{core}	Standby	RTC running, full RAM retention LFXT, DCDC recharge current setting (ipeak = 1)		0.74		µA
Core Current consumption with GLDO						
I_{core}	Active	MCU running CoreMark from Flash at 48MHz		4.1		mA
I_{core}	Idle	Supply Systems and RAM powered, flash disabled, DMA disabled		1.2		mA
I_{core}	Idle	Supply Systems and RAM powered, flash disabled, DMA enabled		1.3		mA
I_{core}	Idle	Supply Systems and RAM powered, flash enabled, DMA disabled		1.5		mA
I_{core}	Idle	Supply Systems and RAM powered, flash enabled, DMA enabled		1.7		mA
I_{core}	Standby	RTC running, full RAM retention LFOSC, default GLDO recharge current setting		1.1		µA
I_{core}	Standby	RTC running, full RAM retention LFXT default GLDO recharge current setting		1.15		µA
Reset, Shutdown Current Consumption						
I_{core}	Reset	Reset. RSTN pin asserted or VDDS below power-on-reset threshold		165		nA
I_{core}	Shutdown	Shutdown measured in steady state. No clocks running, no retention, IO wakeup enabled		165		nA
Peripheral Current Consumption						
I_{peri}	RF	Delta current, clock enabled, RF subsystem idle		40		µA
I_{peri}	Timers	Delta current with clock enabled, module is idle, one LGPT timer		2.4		µA
I_{peri}	I2C	Delta current with clock enabled, module is idle		10.6		µA
I_{peri}	SPI	Delta current with clock enabled, module is idle		3.4		µA
I_{peri}	UART	Delta current with clock enabled, module is idle		24.5		µA
I_{peri}	CRYPTO (AES)	Delta current with clock enabled, module is idle		3.8		µA

7.10 Power Consumption - Radio Modes

When measured on the LP-EM-CC2340R5MODA reference design with T_c = 25°C, V_{DDS} = 3.0V with DCDC enabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{RX}	Radio receive current	2440MHz, 1Mbps, GFSK, system bus off (1)		5.5		mA
I_{RX}	Radio receive current	2440MHz, 1Mbps, GFSK, DCDC OFF, system bus off (1)		9		mA
I_{TX}	Radio transmit current	-8dBm output power setting 2440MHz system bus off (1)		4.5		mA
I_{TX}	Radio transmit current	0dBm output power setting 2440MHz system bus off (1)		5.1		mA
I_{TX}	Radio transmit current	0dBm output power setting 2440MHz DCDC OFF, system bus off (1)		9.0		mA
I_{TX}	Radio transmit current	+4dBm output power setting 2440MHz system bus off (1)		7.9		mA
I_{TX}	Radio transmit current	+6dBm output power setting 2440MHz system bus off (1)		8.9		mA
I_{TX}	Radio transmit current	+8dBm output power setting 2440MHz system bus off (1)		10.7		mA
I_{TX}	Radio transmit current	+8dBm output power setting 2440MHz DCDC OFF, system bus off (1)		19		mA

(1) System bus off refers to device idle mode, DMA disabled, flash disabled

7.11 Nonvolatile (Flash) Memory Characteristics

Over operating free-air temperature range and V_{DDS} = 3.0V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Flash sector size			2		KB
Supported flash erase cycles before failure, full bank(1) (2)		30			k Cycles
Supported flash erase cycles before failure, single sector(3)		60			k Cycles
Maximum number of write operations per row before sector erase(4)				83	Write Operations
Flash retention	85°C	11.4			Years
Flash sector erase current	Average delta current		1.2		mA
Flash sector erase time(5)	0 erase cycles		2.2		ms
Flash write current	Average delta current, full sector at a time		1.7		mA
Flash write time(5)	full sector (2kB) at a time, 0 erase cycles		8.3		ms

(1) A full bank erase is counted as a single erase cycle on each sector
(2) Aborting flash during erase or program modes is not a safe operation.
(3) Up to 16 customer-designated sectors can be individually erased an additional 30k times beyond the baseline bank limitation of 30k cycles
(4) Each wordline is 2048 bits (or 256 bytes) wide. This limitation corresponds to sequential memory writes of 4 (3.1) bytes minimum per write over a whole wordline. If additional writes to the same wordline are required, a sector erase is required once the maximum number of write operations per row is reached.
(5) This number is dependent on Flash aging and increases over time and erase cycles

7.12 Thermal Resistance Characteristics

THERMAL METRIC	THERMAL METRIC	PACKAGE	UNIT (1)
		MHA	
		26 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.7	°C/W

THERMAL METRIC	THERMAL METRIC	PACKAGE	UNIT (1)
		MHA	
		26 PINS	
ψ_{JB}	Junction-to-board characterization parameter	30.4	°C/W

(1) °C/W = degrees Celsius per watt.

7.13 RF Frequency Bands

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	MIN	TYP	MAX	UNIT
Frequency bands	2360		2510	MHz

7.14 Bluetooth Low Energy - Receive (RX)

When measured on the LP-EM-CC2340R5MODA reference design with T_c = 25°C, V_{DDS} = 3.0V, f_{RF} = 2440MHz with DCDC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
125kbps (LE Coded)					
Receiver sensitivity	BER = 10^{-3}		–102		dBm
Receiver saturation	BER = 10^{-3}		5		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–250/ 250) (1)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (–90 / 90) (1)		ppm
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (255-byte packets)		> (–90 / 90) (1)		ppm
Co-channel rejection(2)	Wanted signal at –79dBm, modulated interferer in channel, BER = 10^{-3}		–6		dB
Selectivity, ±1MHz(2)	Wanted signal at –79dBm, modulated interferer at ±1MHz, BER = 10^{-3}		9 / 5 (3)		dB
Selectivity, ±2MHz(2)	Wanted signal at –79dBm, modulated interferer at ±2MHz, BER = 10^{-3}		44 / 31 (3)		dB
Selectivity, ±3MHz(2)	Wanted signal at –79dBm, modulated interferer at ±3MHz, BER = 10^{-3}		47 / 42 (3)		dB
Selectivity, ±4MHz(2)	Wanted signal at –79dBm, modulated interferer at ±4MHz, BER = 10^{-3}		49 / 45 (3)		dB
Selectivity, ±6MHz(2)	Wanted signal at –79dBm, modulated interferer at ≥ ±6MHz, BER = 10^{-3}		52 / 48 (3)		dB
Selectivity, ±7MHz	Wanted signal at –79dBm, modulated interferer at ≥ ±7MHz, BER = 10^{-3}		54 / 49 (3)		dB
Selectivity, Image frequency(2)	Wanted signal at –79dBm, modulated interferer at image frequency, BER = 10^{-3}		31		dB
Selectivity, Image frequency ±1MHz(2)	Note that Image frequency +1MHz is the Co- channel – 1MHz. Wanted signal at –79dBm, modulated interferer at ±1MHz from image frequency, BER = 10^{-3}		5 / 42 (3)		dB
500kbps (LE Coded)					
Receiver sensitivity	BER = 10^{-3}		–99		dBm
Receiver saturation	BER = 10^{-3}		5		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–250 / 250) (1)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (–90/ 90) (1)		ppm
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (255-byte packets)		> (–90 / 90) (1)		ppm
Co-channel rejection(2)	Wanted signal at –72dBm, modulated interferer in channel, BER = 10^{-3}		–4.5		dB
Selectivity, ±1MHz(2)	Wanted signal at –72dBm, modulated interferer at ±1MHz, BER = 10^{-3}		9 / 5 (3)		dB
Selectivity, ±2MHz(2)	Wanted signal at –72dBm, modulated interferer at ±2MHz, BER = 10^{-3}		42 / 31 (3)		dB
Selectivity, ±3MHz(2)	Wanted signal at –72dBm, modulated interferer at ±3MHz, BER = 10^{-3}		45 / 41 (3)		dB
Selectivity, ±4MHz(2)	Wanted signal at –72dBm, modulated interferer at ±4MHz, BER = 10^{-3}		46 / 42 (3)		dB
Selectivity, ±6MHz(2)	Wanted signal at –72dBm, modulated interferer at ≥ ±6MHz, BER = 10^{-3}		50 / 45 (3)		dB
Selectivity, ±7MHz	Wanted signal at –72dBm, modulated interferer at ≥ ±7MHz, BER = 10^{-3}		51 / 46 (3)		dB
Selectivity, Image frequency(2)	Wanted signal at –72dBm, modulated interferer at image frequency, BER = 10^{-3}		31		dB

When measured on the LP-EM-CC2340R5MODA reference design with T_c = 25°C, V_{DDS} = 3.0V, f_{RF} = 2440MHz with DCDC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Selectivity, Image frequency ±1MHz(2)	Note that Image frequency +1MHz is the Co- channel – 1MHz. Wanted signal at –72dBm, modulated interferer at ±1MHz from image frequency, BER = 10^{-3}		5 / 41 (3)		dB
1Mbps (LE 1M)					
Receiver sensitivity	BER = 10^{-3}		–96.5		dBm
Receiver saturation	BER = 10^{-3}		5		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–250/250) (1)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (–90 / 90) (1)		ppm
Co-channel rejection(2)	Wanted signal at –67dBm, modulated interferer in channel, BER = 10^{-3}		–6		dB
Selectivity, ±1MHz(2)	Wanted signal at –67dBm, modulated interferer at ±1MHz, BER = 10^{-3}		7 / 5 (3)		dB
Selectivity, ±2MHz(2)	Wanted signal at –67dBm, modulated interferer at ±2MHz,BER = 10^{-3}		39 / 28 (3)		dB
Selectivity, ±3MHz(2)	Wanted signal at –67dBm, modulated interferer at ±3MHz, BER = 10^{-3}		38 / 38 (3)		dB
Selectivity, ±4MHz(2)	Wanted signal at –67dBm, modulated interferer at ±4MHz, BER = 10^{-3}		47 / 35 (3)		dB
Selectivity, ±5MHz or more(2)	Wanted signal at –67dBm, modulated interferer at ≥ ±5MHz, BER = 10^{-3}		40		dB
Selectivity, image frequency(2)	Wanted signal at –67dBm, modulated interferer at image frequency, BER = 10^{-3}		28		dB
Selectivity, image frequency ±1MHz(2)	Note that Image frequency +1MHz is the Co- channel – 1MHz. Wanted signal at –67dBm, modulated interferer at ±1MHz from image frequency, BER = 10^{-3}		5 / 38 (3)		dB
Out-of-band blocking(4)	30MHz to 2000MHz		–10		dBm
Out-of-band blocking	2003MHz to 2399MHz		–10		dBm
Out-of-band blocking	2484MHz to 2997MHz		–10		dBm
Out-of-band blocking	3000MHz to 12.75GHz (excluding VCO frequency)		–2		dBm
Intermodulation	Wanted signal at 2402MHz, –64dBm. Two interferers at 2405 and 2408MHz respectively, at the given power level		–37		dBm
Spurious emissions, 30 to 1000MHz(5)	Measurement in a 50-Ω single-ended load.		< –59		dBm
Spurious emissions, 1 to 12.75GHz(5)	Measurement in a 50-Ω single-ended load.		< –47		dBm
RSSI dynamic range (6)			70		dB
RSSI accuracy			±4		dB
RSSI resolution			1		dB
2Mbps (LE 2M)					
Receiver sensitivity	Measured at SMA connector, BER = 10^{-3}		–92		dBm
Receiver saturation	Measured at SMA connector, BER = 10^{-3}		2		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–250 / 250) (1)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (–90/ 90) (1)		ppm
Co-channel rejection(2)	Wanted signal at –67dBm, modulated interferer in channel,BER = 10^{-3}		–8		dB
Selectivity, ±2MHz(2)	Wanted signal at –67dBm, modulated interferer at ±2MHz, Image frequency is at –2MHz, BER = 10^{-3}		9 / 5 (3)		dB
Selectivity, ±4MHz(2)	Wanted signal at –67dBm, modulated interferer at ±4MHz, BER = 10^{-3}		40 / 32 (3)		dB
Selectivity, ±6MHz(2)	Wanted signal at –67dBm, modulated interferer at ±6MHz, BER = 10^{-3}		42 / 38 (3)		dB

When measured on the LP-EM-CC2340R5MODA reference design with T_c = 25°C, V_{DDS} = 3.0V, f_{RF} = 2440MHz with DCDC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Selectivity, image frequency(2)	Wanted signal at –67dBm, modulated interferer at image frequency, BER = 10^{-3}		5		dB
Selectivity, image frequency ±2MHz(2)	Note that Image frequency +2MHz is the Co-channel. Wanted signal at –67dBm, modulated interferer at ±2MHz from image frequency, BER = 10^{-3}		–8 / 32 (3)		dB
Out-of-band blocking(4)	30MHz to 2000MHz		–10		dBm
Out-of-band blocking	2003MHz to 2399MHz		–10		dBm
Out-of-band blocking	2484MHz to 2997MHz		–12		dBm
Out-of-band blocking	3000MHz to 12.75GHz (excluding VCO frequency)		–10		dBm
Intermodulation	Wanted signal at 2402MHz, –64dBm. Two interferers at 2408 and 2414MHz respectively, at the given power level		–38		dBm

(1) Actual performance exceeding Bluetooth specification
(2) Numbers given as I/C dB
(3) X / Y, where X is +N MHz and Y is –N MHz
(4) Excluding one exception at F_{wanted} / 2, per Bluetooth Specification
(5) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)
(6) The device will saturate at -30dB.

7.15 Bluetooth Low Energy - Transmit (TX)

When measured on the LP-EM-CC2340R5MODA reference design with T_c = 25°C, V_{DDS} = 3.0V, f_{RF} = 2440MHz with DCDC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General Parameters					
Max output power	Delivered to a single-ended 50-Ω load through integrated balun		8		dBm
Output power programmable range	Delivered to a single-ended 50-Ω load through integrated balun		28		dB

7.16 2.4GHz RX/TX CW

When measured on the LP-EM-CC2340R5MODA reference design with T_c = 25°C, V_{DDS} = 3.0V, f_{RF} = 2440MHz with DCDC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Spurious emissions and harmonics						
Spurious emissions(1)	f < 1GHz, outside restricted bands	+8dBm setting		< –36		dBm
	f < 1GHz, restricted bands ETSI			< –54		dBm
	f < 1GHz, restricted bands FCC			< –55		dBm
	f > 1GHz, including harmonics (ETSI)			< –30		dBm
Harmonics (1)	Second harmonic			< –42		dBm
	Third harmonic			< –42		dBm

(1) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

7.17 Timing and Switching Characteristics

7.17.1 Reset Timing

PARAMETER	MIN	TYP	MAX	UNIT
RSTN low duration	1			µs

7.17.2 Wakeup Timing

Measured over operating free-air temperature with V_{DDS} = 3.0V (unless otherwise noted). The times listed here do not include any software overhead (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MCU, Reset/Shutdown to Active(1)	GLDO default charge current setting, VDDR capacitor fully charged (2)		350-450		µs
MCU, Standby to Active	MCU, Standby to Active (ready to execute code from flash). DCDC ON, default recharge current configuration		33-43 (3)		µs
MCU, Standby to Active	MCU, Standby to Active (ready to execute code from flash). GLDO ON, default recharge current configuration		33-50 (3)		µs
MCU, Idle to Active	Flash enabled in idle mode		3		µs
MCU, Idle to Active	Flash disabled in idle mode		14		µs

(1) Wakeup time includes device ROM bootcode execution time. The wakeup time is dependent on remaining charge on VDDR capacitor when starting the device, and thus how long the device has been in Reset or Shutdown before starting up again.
(2) This is the best case reset/shutdown to active time (including ROM bootcode operation), for the specified GLDO charge current setting considering the VDDR capacitor is fully charged and is not discharged during the reset and shutdown events; that is, when the device is in reset / shutdown modes for only a very short period of time
(3) Depending on VDDR capacitor voltage level.

7.17.3 Clock Specifications

7.17.3.1 48MHz Crystal Oscillator (HFXT)

Measured on a Texas Instruments reference design with integrated 48MHz crystal including parameters based on external manufacturer's crystal specification at Tc = 25°C, VDDS = 3.0V at initial time, unless otherwise noted.

	PARAMETER	MIN	TYP	MAX	UNIT
	Crystal frequency		48		MHz
Start-up time	Until clock is qualified(1)		200		µs
	Crystal frequency tolerance(2)	-10		10	ppm
	Crystal aging(2)	-3		3	ppm/year

Measured on a Texas Instruments reference design with integrated 48MHz crystal including parameters based on external manufacturer's crystal specification at Tc = 25°C, VDDS = 3.0V at initial time, unless otherwise noted.

	PARAMETER	MIN	TYP	MAX	UNIT
	Software calibration value to tune internal capacitor		0x2A		hex value

(1) Start-up time using the TI-provided power driver. Start-up time may increase if driver is not used.
(2) External manufacturer's crystal specification

7.17.3.2 48MHz RC Oscillator (HFOSC)

Measured on the LP-EM-CC2340R5MODA reference design with T_c = 25°C, V_{DDS} = 3.0V, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Frequency		48		MHz
Uncalibrated frequency accuracy		±3		%
Calibrated frequency accuracy (1)		±0.25		%

(1) Accuracy relative to the calibration source (HFXT)

7.17.3.3 32kHz Crystal Oscillator (LFXT)

Measured on the LP-EM-CC2340R5MODA reference design with T_c = 25°C, V_{DDS} = 3.0V, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Crystal frequency		32.768		kHz
Supported crystal load capacitance	6		12	pF
ESR		30	100	kΩ

7.17.3.4 32kHz RC Oscillator (LFOSC)

Measured on the LP-EM-CC2340R5MODA reference design with T_c = 25°C, V_{DDS} = 3.0V, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Calibrated frequency		32.768 (1)		kHz

(1) When using LFOSC as source for the low frequency system clock (LFCLK), the accuracy of the LFCLK-derived Real Time Clock (RTC) can be improved by measuring LFOSC relative to HFXT and compensating for the RTC tick speed. This functionality is available through the TI-provided Power driver.

7.18 Peripheral Characteristics

7.18.1 UART

7.18.1.1 UART Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
UART rate			3	MBaud

7.18.2 SPI

7.18.2.1 SPI Characteristics

Using TI SPI driver, over operating free-air temperature range (unless otherwise noted).

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
fSCLK 1/tsclk	SPI clock frequency	Controller Mode and Peripheral Mode (1) 2.7V ≤ VDDS < 3.8V			12	MHz
		Controller Mode and Peripheral Mode (1) VDDS < 2.7V			8	MHz
DC_{SCK}	SCK Duty Cycle		45	50	55	%

(1) Assume interfacing with ideal SPI controller and SPI peripheral devices

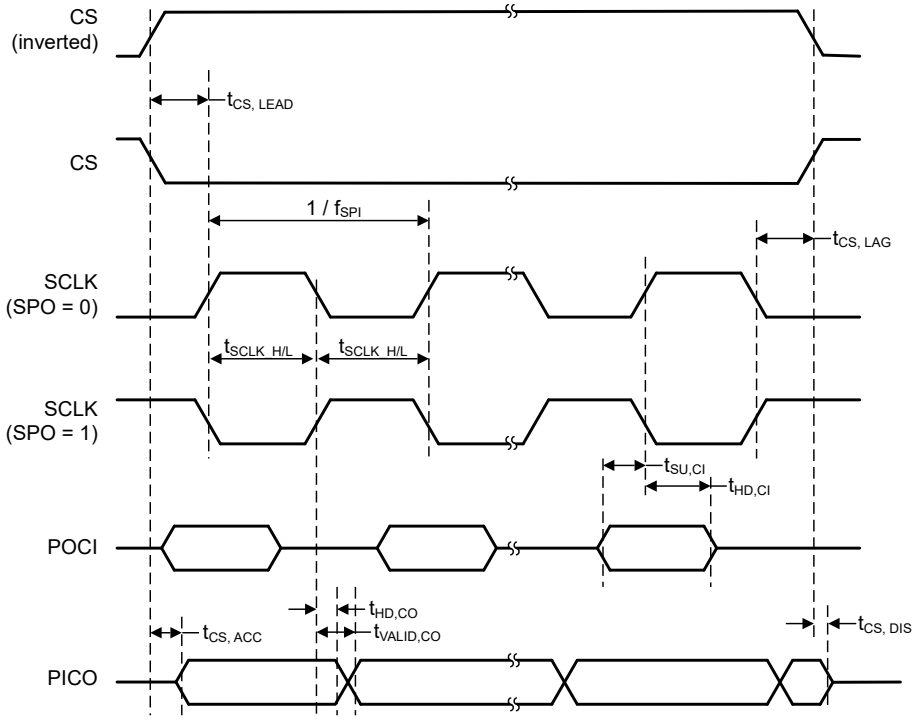
7.18.2.2 SPI Controller Mode

Using TI SPI driver, over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SCLK\_H/L}$	SCLK High or Low time		(t_{SPI}/2) - 1	t_{SPI}/2	(t_{SPI}/2) + 1	ns
$t_{CS.LEAD}$	CS lead-time, CS active to clock		1			SCLK
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive		1			SCLK
$t_{CS.ACC}$	CS access time, CS active to PICO data out				1	SCLK
$t_{CS.DIS}$	CS disable time, CS inactive to PICO high impedance				1	SCLK
$t_{VALID.CO}$	PICO output data valid time(1)	SCLK edge to PICO valid,C_L = 20pF			13	ns
$t_{HD.CO}$	PICO output data hold time(2)	C_L = 20pF	0			ns

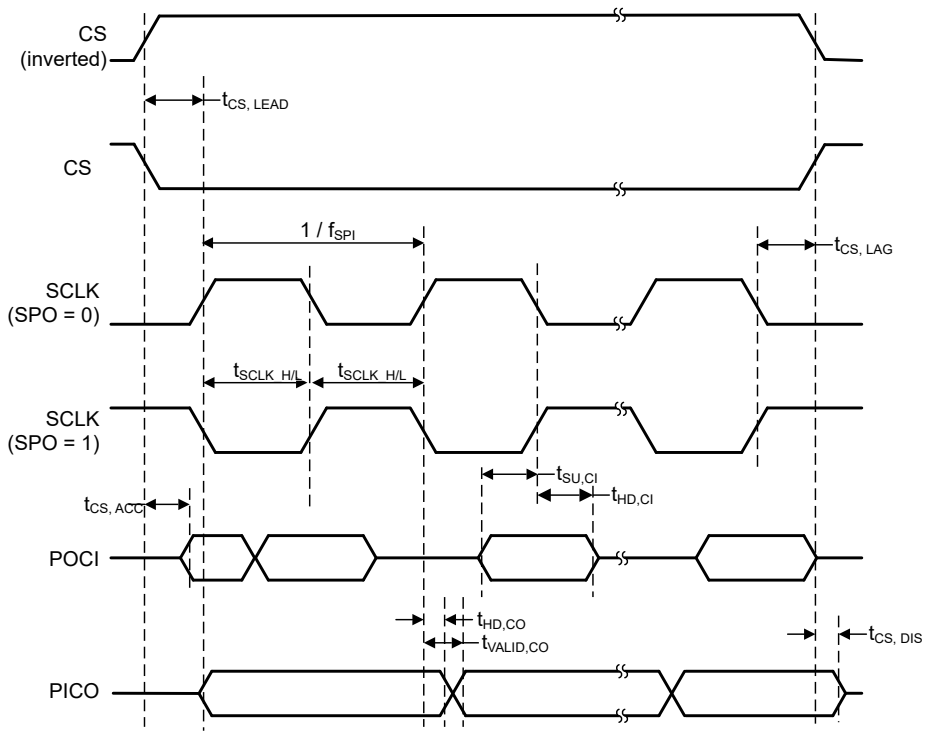
(1) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
(2) Specifies how long data on the output is valid after the output changing SCLK clock edge

7.18.2.3 SPI Timing Diagrams - Controller Mode



Controller Mode, SPH = 0

Figure 7-1. SPI Timing Diagram - Controller Mode, SPH = 0



Controller Mode, SPH = 1

Figure 7-2. SPI Timing Diagram - Controller Mode, SPH = 1

7.18.2.4 SPI Peripheral Mode

Using TI SPI driver, over operating free-air temperature range (unless otherwise noted),

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{CS.LEAD}$	CS lead-time, CS active to clock		1			SCLK
$t_{CS.LAG}$	CS lag time, Last clock to CS inactive		1			SCLK
$t_{CS.ACC}$	CS access time, CS active to POCI data out	VDDS = 3.3V			35	ns
$t_{CS.ACC}$	CS access time, CS active to POCI data out	VDDS = 1.8V			50	ns
$t_{CS.DIS}$	CS disable time, CS inactive to POCI high inpedance	VDDS = 3.3V			35	ns
$t_{CS.DIS}$	CS disable time, CS inactive to POCI high impedance	VDDS = 1.8V			50	ns
$t_{SU.PI}$	PICO input data setup time		13			ns
$t_{HD.PI}$	PICO input data hold time		0			ns
$t_{VALID.PO}$	POCI output data valid time(1)	SCLK edge to POCI valid,C_L = 20pF, 3.3V			35	ns
$t_{VALID.PO}$	POCI output data valid time(1)	SCLK edge to POCI valid,C_L = 20pF, 1.8V			50	ns
$t_{HD.PO}$	POCI output data hold time(2)	C_L = 20pF	0			ns

(1) Specifies the time to drive the next valid data to the output after the output changing SCLK clock edge
(2) Specifies how long data on the output is valid after the output changing SCLK clock edge

7.18.2.5 SPI Timing Diagrams - Peripheral Mode

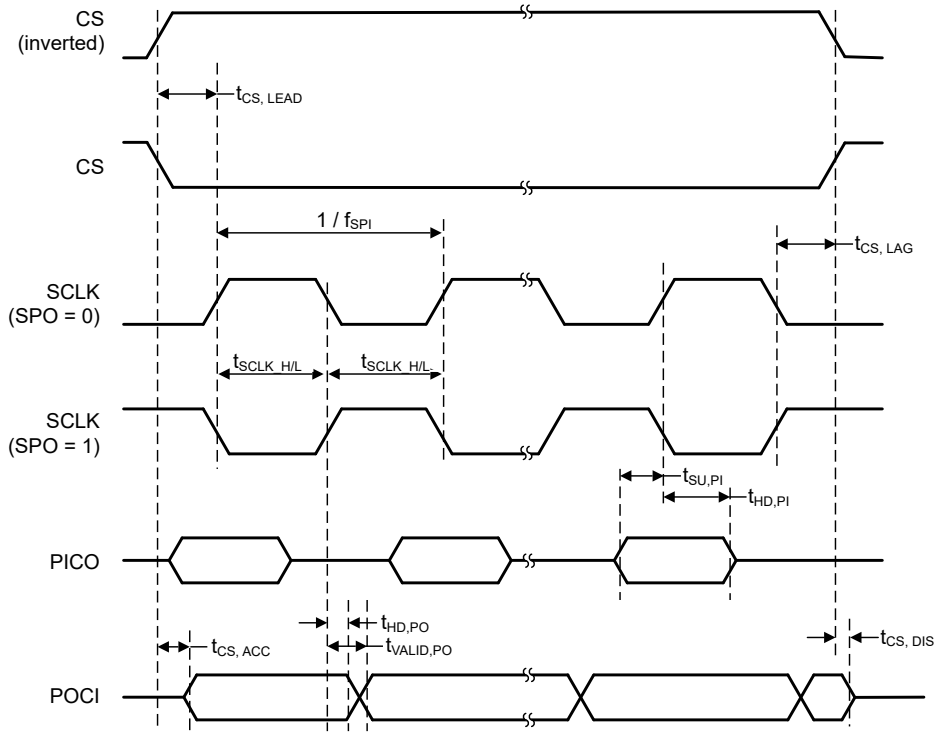


Figure 7-3. SPI Timing Diagram - Peripheral Mode, SPH = 0

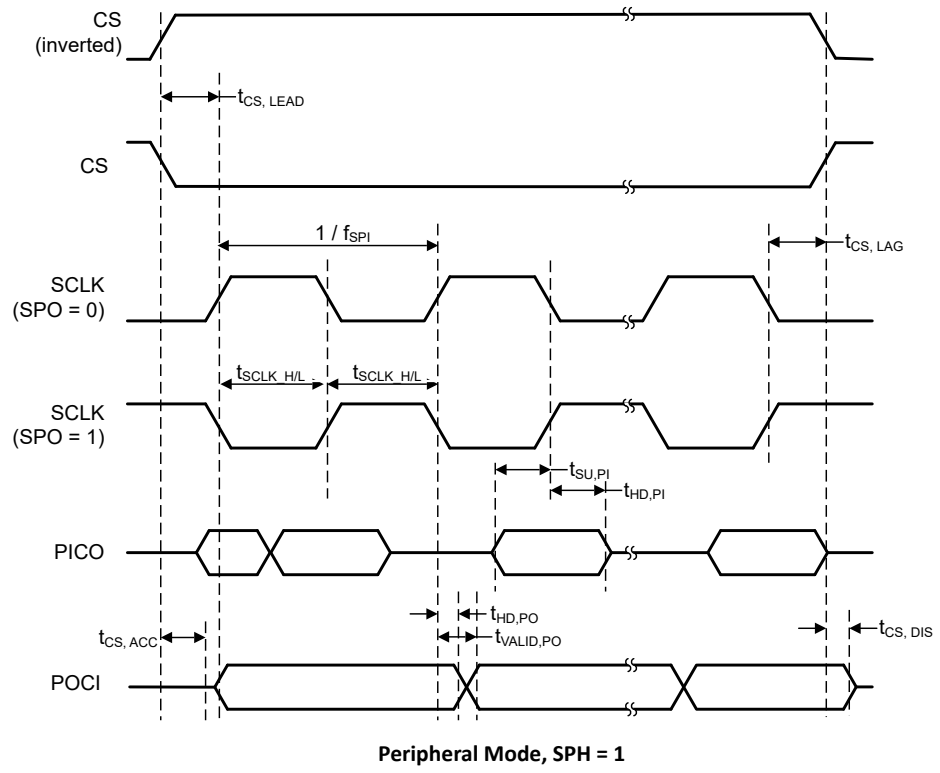


Figure 7-4. SPI Timing Diagram - Peripheral Mode, SPH = 1

7.18.3 I²C

7.18.3.1 I2C

Over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency		0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} = 100kHz	4.0			µs
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} > 100kHz	0.6			µs
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} = 100kHz	4.7			µs
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} > 100kHz	0.6			µs
$t_{HD,DAT}$	Data hold time		0			µs
$t_{SU,DAT}$	Data setup time	f_{SCL} = 100kHz	250			ns
$t_{SU,DAT}$	Data setup time	f_{SCL} > 100kHz	100			ns
$t_{SU,STO}$	Setup time for STOP	f_{SCL} = 100kHz	4.0			µs
$t_{SU,STO}$	Setup time for STOP	f_{SCL} > 100kHz	0.6			µs
t_{BUF}	Bus free time between STOP and START conditions	f_{SCL} = 100kHz	4.7			µs
t_{BUF}	Bus free time between STOP and START conditions	f_{SCL} > 100kHz	1.3			µs
t_{SP}	Pulse duration of spikes supressed by input deglitch filter		50			ns

7.18.3.2 I²C Timing Diagram

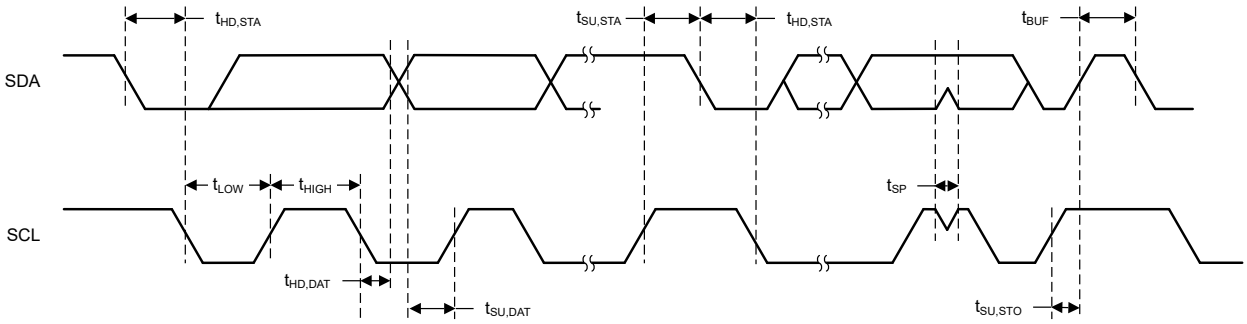


Figure 7-5. I²C Timing Diagram

7.18.4 GPIO

7.18.4.1 GPIO DC Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_A = 25°C, V_{DDS} = 1.8V					
GPIO pullup current	Input mode, pullup enabled, Vpad = 0V	39	66	109	µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS	10	21	40	µA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1	0.91	1.11	1.27	V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0	0.59	0.75	0.91	V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points	0.26	0.35	0.44	V
T_A = 25°C, V_{DDS} = 3.0V					
GPIO VOH at 10mA load	high-drive GPIOs only, max drive setting	2.47			V
GPIO VOL at 10mA load	high-drive GPIOs only, max drive setting			0.25	V
GPIO VOH at 2mA load	standard drive GPIOs	2.52			V
GPIO VOL at 2mA load	standard drive GPIOs			0.20	V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_A = 25°C, V_{DDS} = 3.8V					
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V	170	262	393	µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS	60	110	172	µA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1	1.76	1.98	2.27	V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0	1.26	1.52	1.79	V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points	0.40	0.47	0.54	V
T_A = 25°C					
VIH	Lowest GPIO input voltage reliably interpreted as a *High*	0.8*V_{DDS}			V
VIL	Highest GPIO input voltage reliably interpreted as a *Low*			0.2*V_{DDS}	V

7.18.5 ADC

7.18.5.1 Analog-to-Digital Converter (ADC) Characteristics

T_c = 25°C, V_{DDS} = 3.0V, unless otherwise noted.(1)
Performance numbers require use of offset and gain adjustements in software by TI-provided ADC drivers.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Power Supply and Input Range Conditions						
$V_{(Ax)}$	Analog input voltage range	All ADC analog input pins Ax	0		VDDS	V
$I_{(ADC)}$ single-ended mode	Operating supply current into VDDS terminal	RES = 0x0 (12Bit mode), Fs = 1.2MSPS, Internal reference OFF (ADCREF_EN = 0), VeREF+ = VDDS		480		µA
		RES = 0x0 (12Bit mode), Fs = 266ksps, Internal reference ON (ADCREF_EN = 0), ADCREF = 2.5V		365		
$C_{I\ GPIO}$	Input capacitance into a single terminal			5	7	pF
$R_{I\ GPIO}$	Input MUX ON-resistance			0.5	1	kΩ
ADC Switching Characteristics						
F_S ADC REF	ADC sampling frequency when using the internal ADC reference voltage	ADCREF_EN = 1, RES = 0x0 (12-bit), VDDS = 1.71V to VDDSmax			267 (2)	ksps
F_S ADC REF	ADC sampling frequency when using the internal ADC reference voltage	ADCREF_EN = 1, RES = 0x1 (10-bit), VDDS = 1.71V to VDDSmax			308 (2)	ksps
F_S ADC REF	ADC sampling frequency when using the internal ADC reference voltage	ADCREF_EN = 1, RES = 0x2 (8-bit), VDDS = 1.71V to VDDSmax			400 (2)	ksps
F_S EXTREF	ADC sampling frequency when using the external ADC reference voltage	ADCREF_EN = 0, VeREF+ = VDDS, RES = 0x0 (12-bit), VDDS = 1.71V to VDDSmax			1.2 (2)	Msps
F_S EXTREF	ADC sampling frequency when using the external ADC reference voltage	ADCREF_EN = 0, VeREF+ = VDDS, RES = 0x1 (10-bit), VDDS = 1.71V to VDDSmax			1.33 (2)	Msps
F_S EXTREF	ADC sampling frequency when using the external ADC reference voltage	ADCREF_EN = 0, VeREF+ = VDDS, RES = 0x2 (8-bit), VDDS = 1.71V to VDDSmax			1.6 (2)	Msps
$N_{CONVERT}$	Clock cycles for conversion	RES = 0x0 (12-bit)		14		cycles
$N_{CONVERT}$	Clock cycles for conversion	RES = 0x1 (10-bit)		12		cycles
$N_{CONVERT}$	Clock cycles for conversion	RES = 0x2 (8-bit)		9		cycles
t_{Sample}	Sampling time	RES = 0x0 (12-bit), R_S = 25 Ω, C_{pext} = 10 pF. +/- 0.5 LSB settling	250			ns
$t_{VSUPPLY/3(sample)}$	Sample time required when Vsupply/3 channel is selected		20			µs
ADC Linearity Parameters						
E_I	Integral linearity error (INL) for single-ended inputs	12-bit Mode, V_{R+} = VeREF+ = VDDS, VDDS=1.71-->3.8		+/- 2		LSB
E_D	Differential linearity error (DNL)	12-bit Mode, V_{R+} = VeREF+ = VDDS, VDDS=1.71-->3.8		+/- 1		LSB
E_O	Offset error	12-bit Mode, Internal reference, V_{R+} = ADCREF = 2.5V		1.02		LSB
E_G	Gain error	Internal reference, V_{R+} = ADCREF = 2.5V		+/- 40		LSB
ADC Dynamic Parameters						
ENOB	Effective number of bits	ADCREF_EN = 0, VeREF+ = VDDS =3.3V, VeREF-=0V, RES = 0x2 (8-bit)		8		bit
ENOB	Effective number of bits	ADCREF_EN = 0, VeREF+ = VDDS =3.3V, VeREF-=0V, RES = 0x1 (10-bit)		9.9		bit
ENOB	Effective number of bits	ADCREF_EN = 0, VeREF+ = VDDS =3.3V, VeREF-=0V, RES = 0x0 (12-bit)		11.2		bit
ENOB	Effective number of bits	ADCREF_EN = 1, ADCREF_VSEL = {2.5V, 1.4V}, RES = 0x2 (8-bit)		8		bit

T_c = 25°C, V_{DDS} = 3.0V, unless otherwise noted.(1)
Performance numbers require use of offset and gain adjustements in software by TI-provided ADC drivers.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENOB	Effective number of bits	ADCREF_EN = 1, ADCREF_VSEL = {2.5V, 1.4V} , RES = 0x1 (10-bit)		9.6		bit
ENOB	Effective number of bits	ADCREF_EN = 1, ADCREF_VSEL = {2.5V, 1.4V}, RES = 0x0 (12-bit)		10.4		bit
ENOB	Effective number of bits	VDDS reference, RES = 0x0 (12-bit)		11.2		bit
SINAD	Signal-to-noise and distortion ratio	ADCREF_EN = 0, VeREF+ = VDDS =3.3V, VeREF-=0V, RES = 0x0 (12-bit)		69.18		dB
SINAD	Signal-to-noise and distortion ratio	ADCREF_EN = 1, ADCREF_VSEL = {2.5V, 1.4V}, RES = 0x0 (12-bit)		64.37		dB
SINAD	Signal-to-noise and distortion ratio	VDDS reference, RES = 0x0 (12-bit)		69.18		dB
ADC Temperature Diode, Supply Monitor						
Temp_diode Accuracy	Temperature Error	ADC input channel: Temp diode voltage, Error calculated in temperature range: -30C to +40C, with single point calibration (1)		+/- 3		C
ADC Internal Input: V_{SUPPLY} / 3 Accuracy	V_{supply} voltage divider accuracy for supply monitoring	ADC input channel: Vsupply monitor		+/- 1		%
ADC Internal Input: $I_{Vsupply / 3}$	V_{supply} voltage divider current consumption	ADC input channel Vsupply monitor. V_{supply}=VDDS=3.3V		10		µA
ADC Internal and VDDS Reference						
VDDSREF	Positive ADC reference voltage	ADC reference sourced from VDDS		VDDS		V
ADCREF	Internal ADC Reference Voltage	ADCREF_EN = 1, ADCREF_VSEL = 0, VDDS = 1.71V - VDDSmax		1.4		V
		ADCREF_EN = 1, ADCREF_VSEL = 1, VDDS = 2.7V - VDDSmax		2.5		V
I_{ADCREF}	Operating supply current into VDDA terminal with internal reference ON	ADCREF_EN = 1, VDDA = 1.7V to VDDAmax, ADCREF_VSEL = {0,1}		80		µA
t_{ON}	Internal ADC Reference Voltage power on-time	ADCREF_EN = 1		2		µs

(1) Using IEEE Std 1241-2010 for terminology and test methods
(2) Measured with 48MHz HFOSC

7.18.6 Comparators

7.18.6.1 Ultra-low power comparator

T_c = 25°C, V_{DDS} = 3.0V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		0		V_{DDS}	V
Clock frequency			32		KHz
Voltage Divider Accuracy	Input voltage range is between VDDS/4 and VDDS		98		%
Offset	Measured at V_{DDS} / 2 (Errors seen when using two external inputs)		+/- 27.3		mV
Decision time	Step from –50mV to 50mV		1	3	Clock Cycle
Comparator enable time	COMP_LP disable → enable, VIN+, VIN- from pins, Overdrive ≥ 20mV		70		µs
Current consumption	Including using VDDS/2 as internal reference at VIN- comparator terminal		370		nA

7.19 Typical Characteristics

All measurements in this section are done with T_c = 25°C and V_{DDS} = 3.0V, unless otherwise noted. See *Recommended Operating Conditions* for device limits. Values exceeding these limits are for reference only.

7.19.1 MCU Current

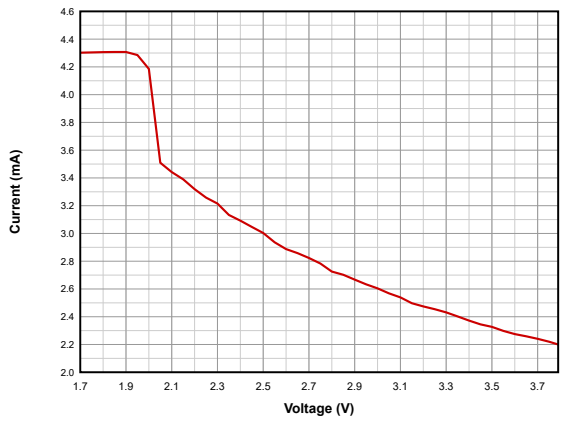


Figure 7-6. Active Mode (MCU) Current vs. Supply Voltage (VDDS) (Running CoreMark)

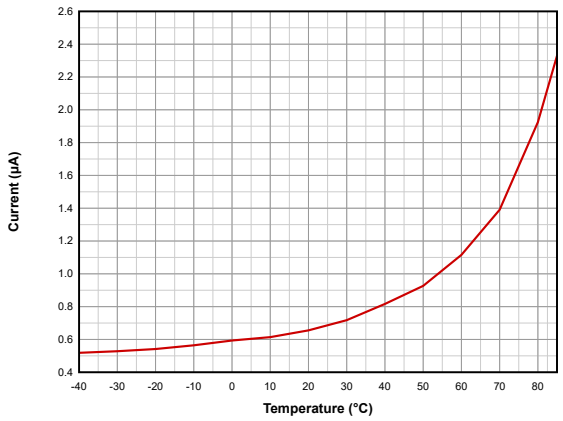


Figure 7-7. Standby Mode (MCU) Current vs. Temperature (RAM and partial register retention, RTC)

7.19.2 RX Current

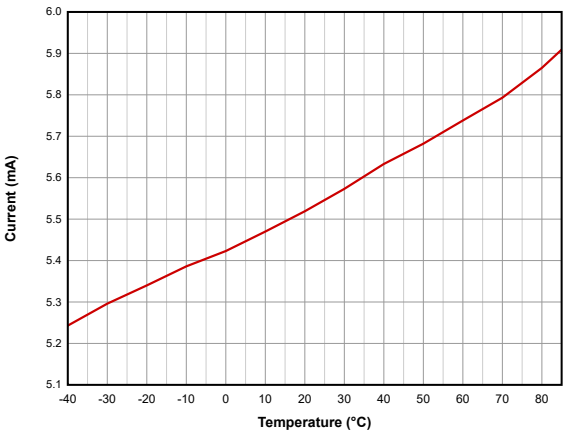


Figure 7-8. RX Current vs. Temperature (BLE 1Mbps, 2.44GHz)

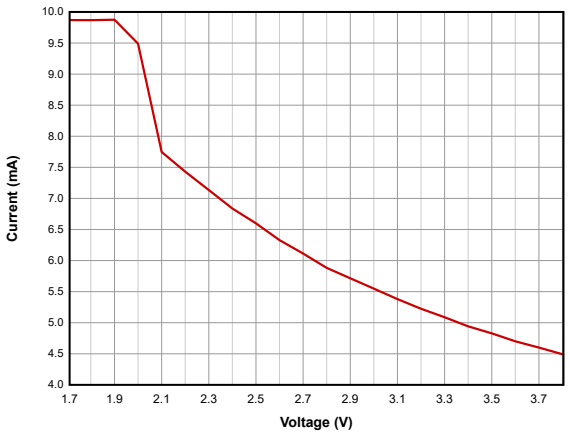


Figure 7-9. RX Current vs. Supply Voltage (VDDS) (BLE 1Mbps, 2.44GHz)

7.19.3 TX Current

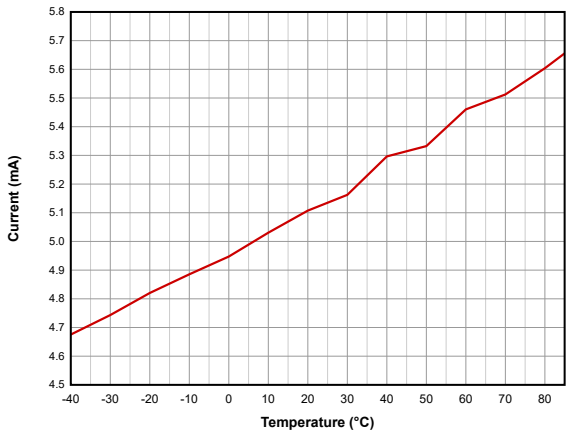


Figure 7-10. TX Current vs. Temperature (BLE 1Mbps, 2.44GHz, 0dBm)

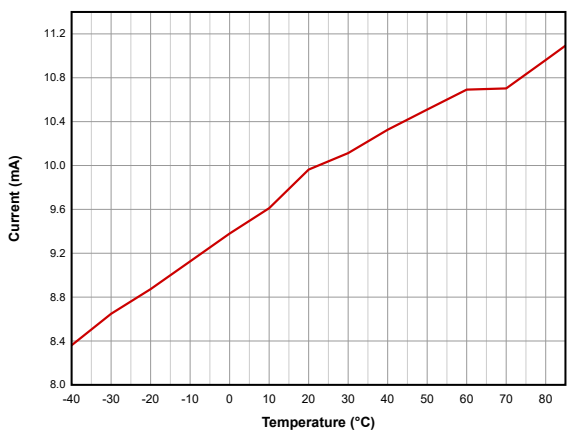


Figure 7-11. TX Current vs. Temperature (BLE 1Mbps, 2.44GHz, +8dBm)

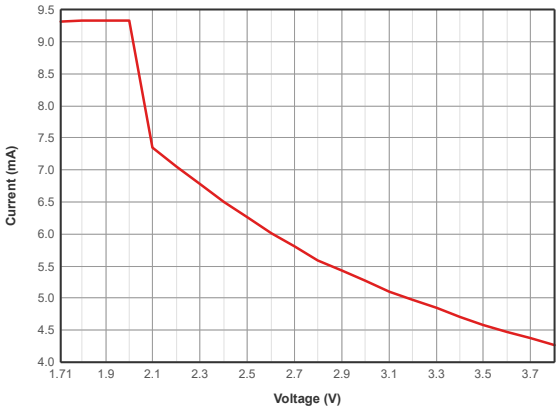


Figure 7-12. TX Current vs. Supply Voltage, VDDS (BLE 1Mbps, 2.44GHz, 0dBm)

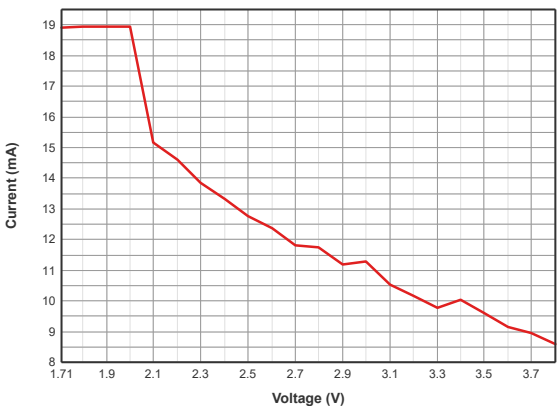


Figure 7-13. TX Current vs. Supply Voltage, VDDS (BLE 1Mbps, 2.44GHz, +8dBm)

Table 7-1 shows typical TX current and output power for different output power settings.

Table 7-1. Typical TX Current and Output Power

2.4GHz, VDDS = 3.0V, DCDC=On, Temperature = 25°C (Measured on LP-EM-CC2340R5MODA)			
txPowerTable Index	**TX Power Setting [dBm] (SmartRF Studio)**	**Typical Output Power [dBm]**	**Typical Current Consumption [mA]**
13	8	7.7	10.7
12	7	7.1	9.5
11	6	6.3	8.9
10	5	5.5	8.3
9	4	4.5	7.9
8	3	3.7	7.5
7	2	2.4	7.1
6	1	1.0	5.4
5	0	0.4	5.1
4	-4	-3.1	4.8
3	-8	-7.3	4.5
2	-12	-10.9	4.2
1	-16	-15.1	4.0
0	-20	-19.0	3.8

7.19.4 RX Performance

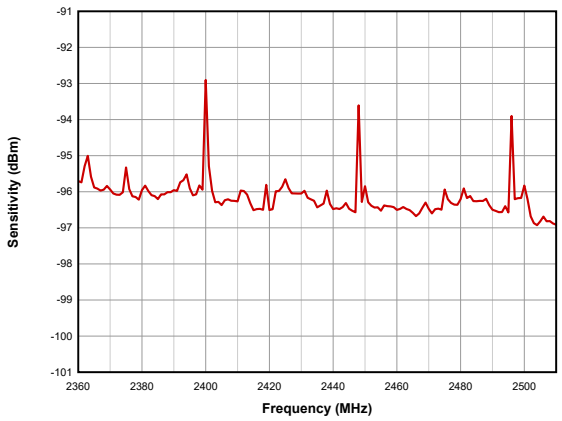


Figure 7-14. Sensitivity vs. Frequency (BLE 1Mbps)

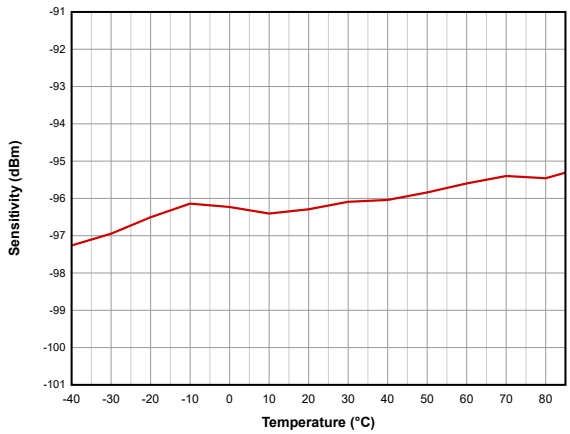


Figure 7-15. Sensitivity vs. Temperature (BLE 1Mbps, 2.44GHz)

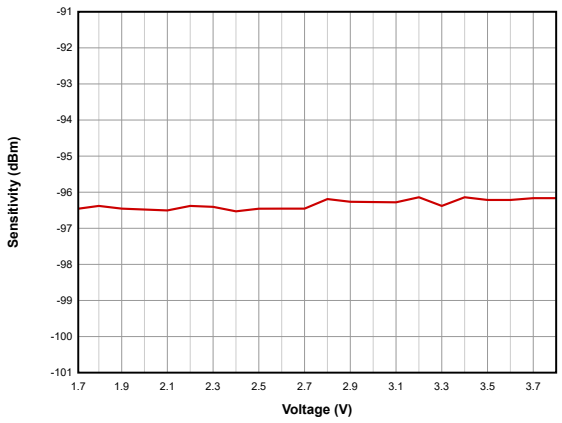


Figure 7-16. Sensitivity vs. Supply Voltage (VDDS) (BLE 1Mbps, 2.44GHz)

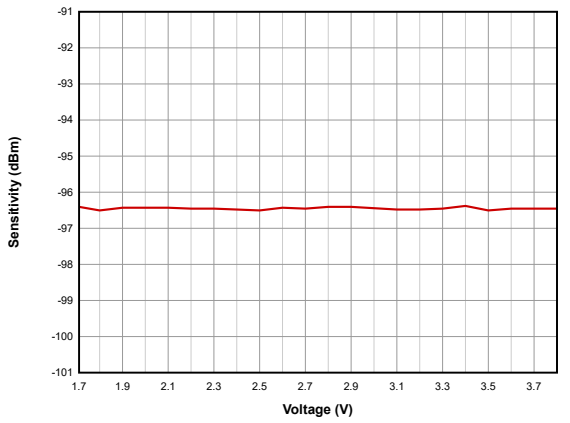


Figure 7-17. Sensitivity vs. Supply Voltage (VDDS) (BLE 1Mbps, 2.44GHz, DCDC Off)

7.19.5 TX Performance

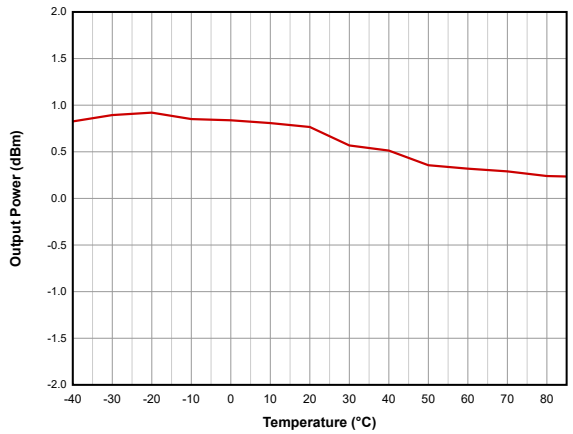


Figure 7-18. Output Power vs. Temperature (BLE 1Mbps, 2.44GHz, 0dBm)

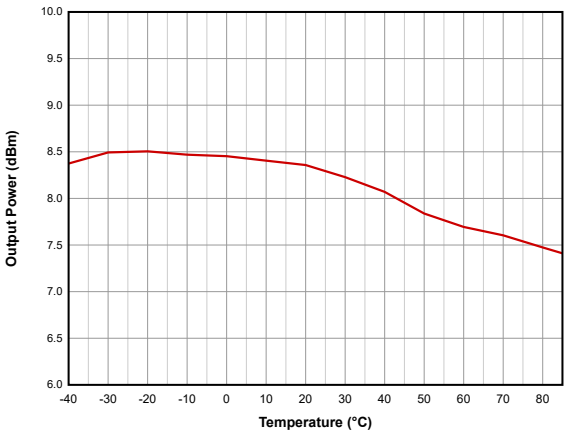


Figure 7-19. Output Power vs. Temperature (BLE 1Mbps, 2.44GHz, +8dBm)

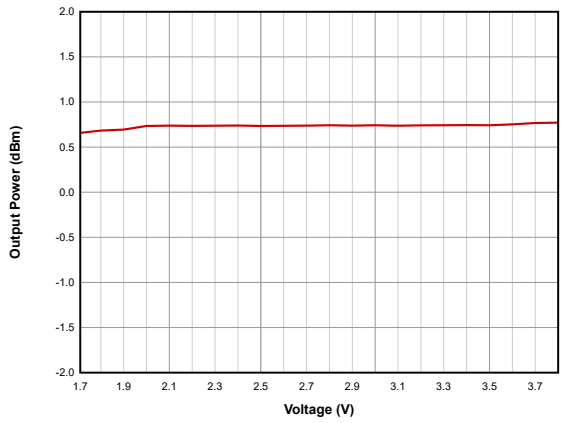


Figure 7-20. Output Power vs. Supply Voltage (VDDS) (BLE 1Mbps, 2.44GHz, 0dBm)

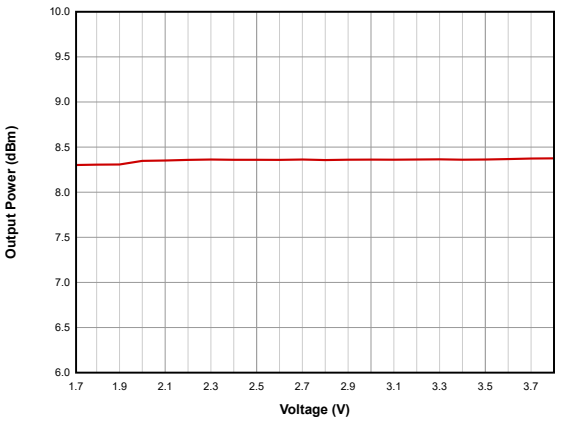


Figure 7-21. Output Power vs. Supply Voltage (VDDS) (BLE 1Mbps, 2.44GHz, +8dBm)

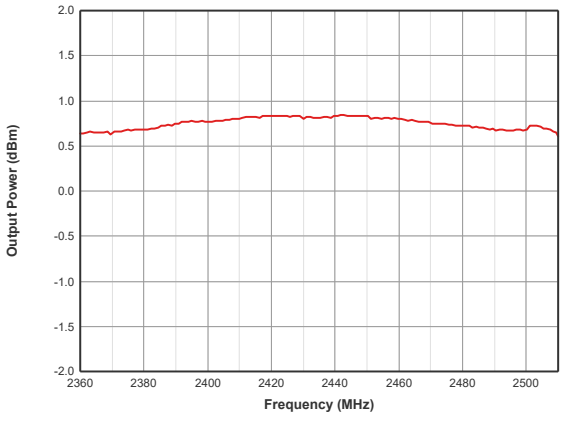


Figure 7-22. Output Power vs. Frequency (BLE 1Mbps, 0dBm)

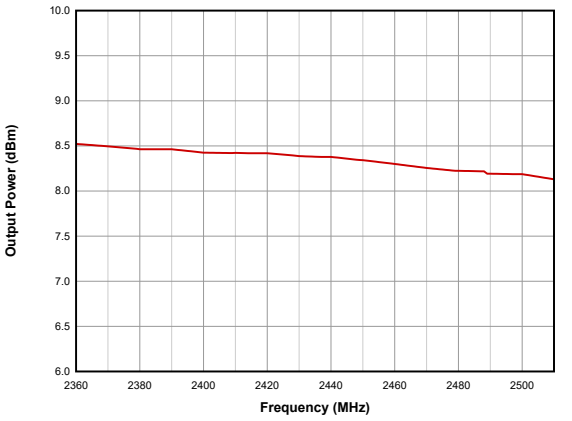


Figure 7-23. Output Power vs. Frequency (BLE 1Mbps, +8dBm)

7.19.6 ADC Performance

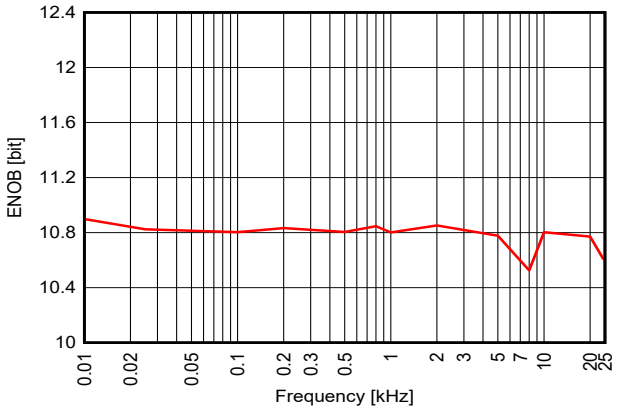


Figure 7-24. ENOB vs. Input Frequency (Internal Reference)

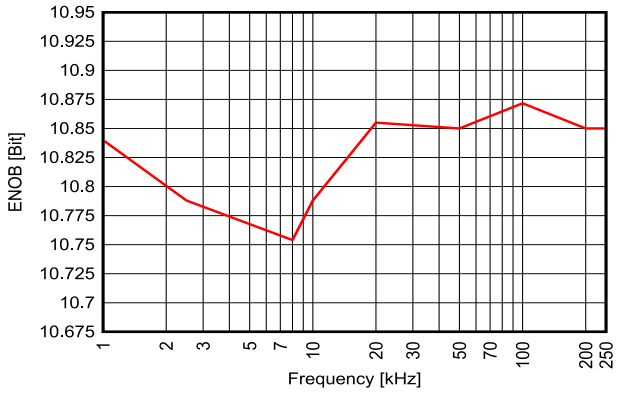


Figure 7-25. ENOB vs. Sampling Frequency (V_{in}= 3V Sine Wave, Internal Reference, F_{in}=F_s/10)

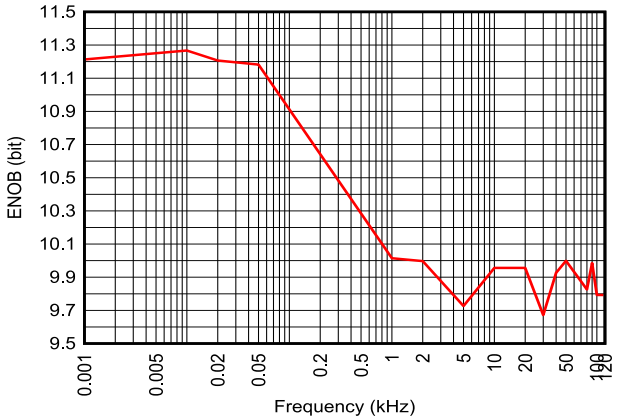


Figure 7-26. ENOB vs. Input Frequency (External Reference = 3.0V)

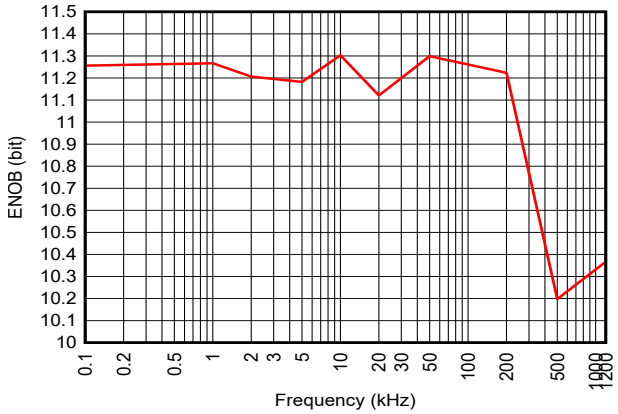


Figure 7-27. ENOB vs. Sampling Frequency (V_{in} = 3V Sine Wave, External Reference = 3.0V, F_{in}=F_s/10

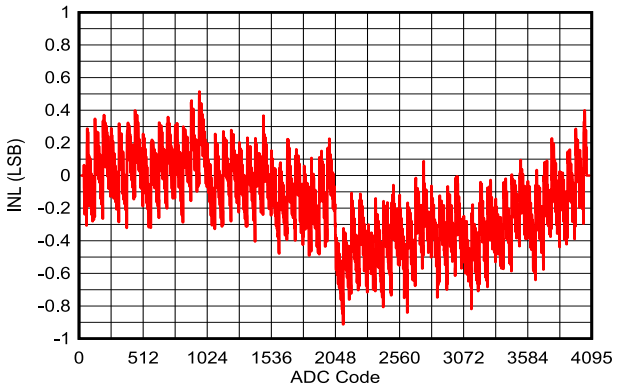


Figure 7-28. INL vs. ADC Code (V_{in}= 3V Sine Wave, Internal Reference, 200ksps)

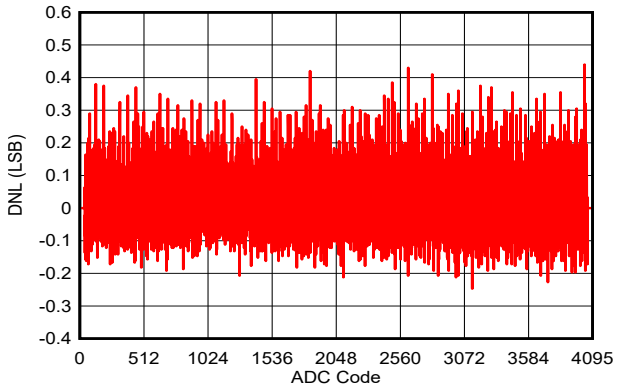


Figure 7-29. DNL vs. ADC Code (V_{in}= 3V Sine Wave, Internal Reference, 200ksps)

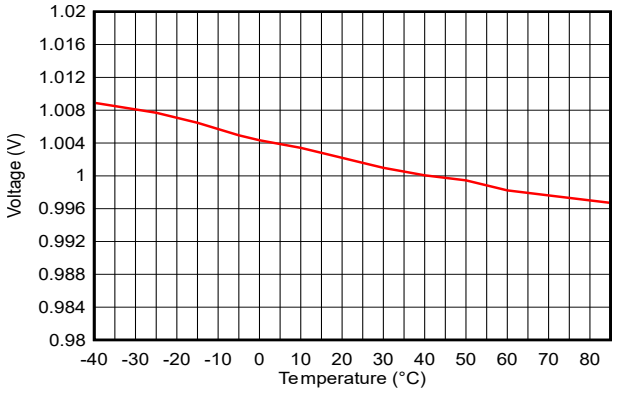


Figure 7-30. ADC Accuracy vs. Temperature (V_{in}= 1V, Internal Reference, 200ksps)

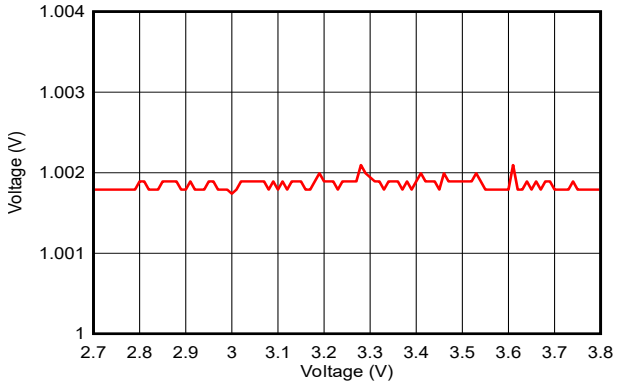


Figure 7-31. ADC Accuracy vs. Supply Voltage (V_{in}= 1V, Internal Reference, 200ksps)

8 Detailed Description

8.1 Overview

Section 4 shows the core modules of the CC2340R5MODA device.

8.2 System CPU

The CC2340R5MODA SimpleLink™ Wireless MCU contains an Arm® Cortex®-M0+ system CPU, which runs the application, the protocol stacks, and the radio. The Cortex-M0+ processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier. The Cortex-M0+ processor offers multiple benefits to developers including:

- Ultra-low power, energy efficient operation
- Deterministic, high-performance interrupt handling for time-critical applications
- Upward compatibility with the Cortex-M processors family

The Cortex-M0+ processor provides the excellent performance expected of a modern 32-bit architecture core, with higher code density than other 8-bit and 16-bit microcontrollers. Its features include the following:

- ARMv6-M architecture optimized for small-footprint embedded applications
- Subset of Arm Thumb/Thumb-2 mixed 16- and 32-bit instructions delivers the high performance expected of a 32-bit Arm
- Single-cycle multiply instruction
- VTOR supporting offset of the vector table base address
- Serial Wire debug with HW break-point comparators
- Ultra-low-power consumption with integrated sleep modes
- SysTick timer
- 48MHz operation
- 0.99DMIPS/MHz

Additionally, the CC2340R5MODA devices are compatible with all ARM tools and software.

8.3 Radio (RF Core)

The low-power RF Core (LRF) implements a high performance and highly flexible RF sub system containing RF and baseband circuitry in addition to a software defined digital radio (LRFD). LRFD provides a high-level, command-based API to the main CPU and handles all of the timing critical and low-level details of many different radio PHYs. Several signals are also available to control external circuitry such as RF switches or range extenders autonomously.

The software-defined modem is not programmable by customers but is instead loaded with precompiled images provided in the radio driver in the SimpleLink™ Low Power F3 software development kit (SDK) for the CC23xx devices. This mechanism allows the radio platform to be updated for support of future versions of standards with over-the-air (OTA) updates while still using the same silicon. LRFD stores the code images in the RF SRAM and does not make use of any ROM memory, thus image loading from NV memory only occurs once after boot and also, no patching is required when exiting power modes.

8.3.1 Bluetooth Low Energy

The RF Core offers full support for Bluetooth Low Energy, including the high-speed 2Mbps physical layer and the 500kbps and 125kbps long range PHYs (Coded PHY) through the TI provided Bluetooth stack or through a high-level Bluetooth API.

The new high-speed mode allows data transfers up to 2Mbps. In addition to faster speeds, this mode offers significant improvements in energy efficiency and wireless coexistence with reduced radio communication time.

Bluetooth LE also enables unparalleled flexibility for adjustment of speed and range based on application needs, which capitalizes on the high-speed or long-range modes respectively. Data transfers are now possible

at 2Mbps, enabling the development of applications using voice, audio, imaging, and data logging that were not previously an option using Bluetooth low energy. With high-speed mode, existing applications deliver faster responses, richer engagement, and longer battery life. Bluetooth LE enables fast, reliable firmware updates.

8.4 Memory

Up to 512KB nonvolatile (Flash) memory provides storage for code and data. The flash memory is in-system programmable and erasable. A special flash memory sector must contain a Customer Configuration section (CCFG) that is used by boot ROM and TI provided drivers to configure the device. This configuration is done through the ccfg.c source file that is included in all TI provided examples.

Up to 64KB ultra-low leakage system static RAM (SRAM) can be used for both storage of data and execution of code. Retention of SRAM contents in Standby power mode is enabled by default and included in Standby mode power consumption numbers. System SRAM is always initialized to zeroes upon code execution during boot.

The ROM includes device bootcode firmware handling initial device trimming operations, security configurations, and device lifecycle management. The ROM also contains a serial (SPI and UART) bootloader that can be used for the initial programming of the device.

8.5 Cryptography

The CC2340R5MODA device comes with AES-128 cryptography hardware accelerator, reducing code footprint and execution time for cryptographic operations. It also has the benefit of being lower power and improves availability and responsiveness of the system because the cryptography operations run in a background hardware thread. The AES hardware accelerators supports the following block cipher modes and message authentication codes:

- AES ECB encrypt
- AES CBC encrypt
- AES CTR encrypt/decrypt
- AES CBC-MAC
- AES GCM
- AEC CCM (uses a combination of CTR + CBC-MAC hardware via software drivers)

The AES hardware accelerator can be fed with plaintext/ciphertext from either CPU or using DMA. Sustained throughput of one 16 byte ECB block per 23 cycles is possible corresponding to > 30Mbps.

The CC2340R5MODA device supports Random Number Generation (RNG) using on-chip analog noise as the non-deterministic noise source for the purpose of generating a seed for a cryptographically secure counter deterministic random bit generator (CTR-DRBG) that in turn is used to generate random numbers for keys, initialization vectors (IVs), and other random number requirements. Hardware acceleration of AES CTR-DRBG is supported.

The CC2340R5MODA device includes a complete SHA 256 library in ROM, reducing the code footprint of the application. Uses cases may include generating digests for use in digital signature algorithms, data integrity checks, and password storage.

Together with a large selection of open-source cryptography libraries provided with the Software Development Kit (SDK), this allows for secure and future proof IoT applications to be easily built on top of the platform.

8.6 Timers

A large selection of timers are available as part of the CC2340R5MODA device. These timers are:

- **Real-Time Clock (RTC)**

  The RTC is a 67-bit, 2-channel timer running on the LFCLK system clock. The RTC is active in STANDBY and ACTIVE power states. When the device enters the RESET or SHUTDOWN state the RTC is reset.

  The RTC accumulates time elapsed since reset on each LFCLK. The RTC counter is incremented by LFINC at a rate of 32.768kHz. LFINC indicates the period of LFCLK in µs, with an additional granularity of 16 fractional bits.

  The counter can be read from two 32-bit registers. RTC.TIME8U has a range of approximately 9.5 hours with an LSB representing 8 microseconds. RTC.TIME524M has a range of approximately 71.4 years with an LSB representing 524 milliseconds.

  There is hardware synchronization between the system timer (SYSTIM) and the RTC so that the multichannel and higher resolution SYSTIM remains in synchronization with the RTC's time base.

  The RTC has two channels: one compare channel and one capture channel and is capable of waking the device out of the standby power state. The RTC compare channel is typically used only by system software and only during the standby power state.
- **System Timer (SYSTIM)**

  The SYSTIM is a 34-bit, 5-channel wrap-around timer with a per-channel selectable 32b slice with either a 1µs resolution and 1h11m35s range or 250ns resolution and 17m54s range. All channels support both capture and single-shot compare (posting an event) operation. One channel is reserved for system software, three channels are reserved for radio software and one channel is freely available to user applications.

For software convenience, a hardware synchronization mechanism automatically confirms that the RTC and SYSTIM share a common time base (albeit with different resolutions/spans). Another software convenience feature is that SYSTIM qualifies any submitted compare values so that the timer channel will immediately trigger if the submitted event is in the immediate past (4.294s with 1µs resolution and 1.049s with 250ns resolution).

- **General Purpose Timers (LGPT)**

  The CC2340R5MODA device provides up to four LGPTs with 3 × 16 bit timers and 1× 24 bit timer, all running up to 48MHz. The LGPTs support a wide range of features such as:

  – Three capture/compare channels
  – One-shot or periodic counting
  – Pulse width modulation (PWM)
  – Time counting between edges and edge counting
  – Input filter implemented on each of the channels for all timers
  – IR generation feature available on Timer-0 and Timer-1
  – Dead band feature available on Timer-1

  The timer capture/compare and PWM signals are connected to IOs through the IO controller module (IOC) and the internal timer event connections to CPU, DMA, and other peripherals are through the event fabric, which allows the timers to interact with signals such as GPIO inputs, other timers, DMA and ADC. Two LGPTs (2× 16-bit timers) support quadrature decoder mode to enable buffered decoding of quadrature-encoded sensor signals. The LGPTs are available in device Active and Idle power modes.

Table 8-1. Timer Comparison

Feature	Timer 0	Timer 1	Timer 2	Timer 3
Counter Width	16-bit	16-bit	16-bit	24-bit
Quadrature Decoder	Yes	No	Yes	No
Park Mode on Fault	No	Yes	No	No
Programmable Dead-Band Insertion	No	Yes	No	No

Table 8-2. Timer Availability

Part Number	Timer 0	Timer 1	Timer 2	Timer 3
CC2340R21	Yes	Yes	No	No
CC2340R22	Yes	Yes	Yes	Yes
CC2340R52	Yes	Yes	Yes	Yes
CC2340R53	Yes	Yes	Yes	Yes

- **Watchdog timer**

  The watchdog timer is used to regain control if the system operates incorrectly due to software errors. Upon counter expiry, the watchdog timer resets the device when periodic monitoring of the system components and tasks fails to verify proper functionality. The watchdog timer runs on a 32kHz clock rate and operates in device active, idle, and standby modes and cannot be stopped once enabled.

8.7 Serial Peripherals and I/O

The CC2340R5MODA device provides 1xUART, 1xSPI, and 1xI2C serial peripherals.

The SPI module supports both SPI controller and peripheral up to 12MHz with configurable phase and polarity.

The UART module implements universal asynchronous receiver and transmitter functions. They support flexible baud-rate generation up to a maximum of 3Mbps and IRDA SIR mode of operation.

The I²C module is used to communicate with devices compatible with the I²C standard. The I²C interface can handle 100kHz and 400kHz operation and can serve as both controller and target.

The I/O controller (IOC) controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a fixed manner over DIOs. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function, and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull, open-drain, or open-source. Some GPIOs have high-drive capabilities, which are marked in **bold** in *Pin Configurations and Functions*.

For more information, see the *CC23xx SimpleLink™ Wireless MCU Technical Reference Manual*.

8.8 Battery and Temperature Monitor

A combined temperature and battery voltage monitor is available in the CC2340R5MODA device. The battery and temperature monitor allows an application to continuously monitor on-chip temperature and supply voltage and respond to changes in environmental conditions as needed. The module contains window comparators to interrupt the system CPU when temperature or supply voltage go outside defined windows. These events can also be used to wake up the device from Standby mode through the Always-On (AON) event fabric.

8.9 µDMA

The device includes a direct memory access (µDMA) controller. The µDMA controller provides a way to offload data-transfer tasks from the system CPU, thus allowing for more efficient use of the processor and the available bus bandwidth. The µDMA controller can perform a transfer between memory and peripherals. The µDMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory when the peripheral is ready to transfer more data.

Some features of the µDMA controller include the following (this is not an exhaustive list):

- Channel operation of up to 8 channels, with 6 channels having dedicated peripheral interface and 2 channels having ability to be triggered via configurable events.
- Transfer modes: memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits
- Ping-pong mode for continuous streaming of data

8.10 Debug

On-chip debug is supported through the serial wire debug (SWD) interface, which is an ARM bi-directional 2-wire protocol that communicates with the JTAG Test Access Port (TAP) controller and allows for complete debug functionality. SWD is fully compatible with Texas Instruments' XDS family of debug probes.

8.11 Power Management

To minimize power consumption, the CC2340R5MODA supports a number of power modes and power management features (see Table 8-3).

Table 8-3. Power Modes

MODE	SOFTWARE CONFIGURABLE POWER MODES (1)				RESET PIN HELD
	ACTIVE	IDLE	STANDBY	SHUTDOWN	
CPU	Active	Off	Off	Off	Off
Flash	On	Available	Off	Off	Off
SRAM	On	On	Retention	Off	Off
Radio	Available	Available	Off	Off	Off
Supply System	On	On	Duty Cycled	Off	Off
CPU register retention	Full	Full	Full (2)	No	No
SRAM retention	Full	Full	Full	Off	Off
48MHz high-speed clock (HFCLK)	HFOSC (tracks HFXT)	HFOSC (tracks HFXT)	Off	Off	Off
32kHz low-speed clock (LFCLK)	LFXT or LFOSC	LFXT or LFOSC	LFXT or LFOSC	Off	Off
Peripherals	Available	Available	IOC, BATMON, RTC, LPCOMP	Off	Off
Wake-up on RTC	N/A	Available	Available	Off	Off
Wake-up on pin edge	N/A	Available	Available	Available	Off
Wake-up on reset pin	On	On	On	On	On
Brownout detector (BOD)	On	On	Duty Cycled	Off	Off
Power-on reset (POR)	On	On	On	On	On
Watchdog timer (WDT)	Available	Available	Available	Off	Off

(1) “Available” indicates that the specific IP or feature can be enabled by user application in the corresponding device operating modes. “On” indicates that the specific IP or feature is turned on irrespective of the user application configuration of the device in the corresponding device operating mode. “Off” indicates that the specific IP or feature is turned off and not available for the user application in the corresponding device operating mode.
(2) Software-based retention of CPU registers with context save and restore when entering and exiting standby power mode

In the **Active** mode, both of MCU and AON power domains are powered. Clock gating is used to minimize power consumption. Clock gating to peripherals/subsystems is controlled manually by the CPU.

In **Idle** mode the CPU is in sleep but selected peripherals and subsystems (such as the radio) can be active. Infrastructure (Flash, ROM, SRAM, bus) clock gating is possible depending on state of the DMA and debug subsystem.

In **Standby** mode, only the always-on (AON) domain is active. An external wake-up event, RTC event, or comparator event (LP-COMP) is required to bring the device back to active mode. Pin Reset will also drive the device from Standby to Active. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In **Shutdown** mode, the device is entirely turned off (including the AON domain), and the I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a *wake from shutdown pin* wakes up the device and functions as a reset trigger. The CPU can differentiate between reset in this way and reset-by-reset pin or power-on reset by reading the reset status register. The only state retained in this mode are the latched I/O state, 3V register bank, and the flash memory contents.

Note

The power, RF and clock management for the CC2340R5MODA device require specific configuration and handling by software for optimized performance. This configuration and handling is implemented in the TI-provided drivers that are part of the CC2340R5MODA software development kit (SDK). Therefore, TI highly recommends using this software framework for all application development on the device. The complete SDK with FreeRTOS, device drivers, and examples are offered free of charge in source code.

8.12 Clock Systems

The CC2340R5MODA device has the following internal system clocks.

The 48MHz HFCLK is used as the main system (MCU and peripherals) clock. This is driven by the internal 48MHz RC Oscillator (HFOSC), which can track its accuracy against an external 48MHz crystal (HFXT). Radio operation requires an external 48MHz crystal.

The 32.768kHz LFCLK is used as the internal low-frequency system clock. It is used for the RTC, the watchdog timer (if enabled in standby power mode), and to synchronize the radio timer before or after Standby power mode. LFCLK can be driven by the internal 32.8kHz RC Oscillator (LFOSC), a 32.768kHz watch-type crystal, or clock input in LFXT bypass mode. When using a crystal or the internal RC oscillator, the device can output the 32kHz LFCLK signal to other devices, thereby reducing the overall system cost.

8.13 Network Processor

Depending on the product configuration, the CC2340R5MODA device can function as a wireless network processor (WNP), a device running the wireless protocol stack with the application running on a separate host MCU, or as a system-on-chip (SoC), with the application and protocol stack running on the system CPU inside the device.

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

8.14 Device Certification and Qualification

The CC2340R5MODA module from TI is certified for FCC, IC/ISED, and ETSI/CE as listed in Table 8-4. Moreover, the module is a Bluetooth Qualified Design by the Bluetooth Special Interest Group (Bluetooth SIG). TI Customers that build products based on the TI CC2340R5MODA module can save in testing cost and time per product family.

Note

The FCC and IC IDs, as well as the CE markings, must be located in both the user manual and on the packaging. Due to the small size of the module (7mm x 10mm), placing the IDs and markings in a type size large enough to be legible without the aid of magnification is impractical.

Table 8-4. CC2340R5MODA List of Certifications

Regulatory Body	Specification	ID (IF APPLICABLE)
FCC (USA)	Part 15C + MPE FCC RF Exposure (Bluetooth)	ZAT-2340R5MODA
IC/ISED (Canada)	RSS-102 (MPE) and RSS-247 (Bluetooth)	451H-2340R5MODA
ETSI/CE (Europe)	EN 300328 v2.2.2 (2019-07) (Bluetooth)	—
ETSI/CE (Europe)	EN 62311:2020 and EN 50655:2017 (MPE)	—
ETSI/CE (Europe)	EN 301 489-1 v2.2.3 (2019-11)	—
ETSI/CE (Europe)	EN 301489-17 v3.3.1 (2024-09)	—
ETSI/CE (Europe)	EN 62368-1:2020/A11:2020	—
MIC (Japan)	ARIB STD-T66	Coming Soon
	JATE	Coming Soon
KCC (South Korea)	KCC	R-C-T3P-CC2340R5MODA
NCC (Taiwan)	NCC	Coming Soon

8.14.1 FCC Certification and Statement

CAUTION

FCC RF Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions for satisfying RF exposure limits. This transmitter must not be co-located or operating with any other antenna or transmitter.

The CC2340R5MODA module from TI is certified for FCC as a single-modular transmitter. The module is an FCC-certified radio module that carries a modular grant.

You are cautioned that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This device is planned to comply with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference.
- This device must accept any interference received, including interference that may cause undesired operation of the device.

8.14.2 IC/ISED Certification and Statement

CAUTION

IC RF Radiation Exposure Statement:

To comply with IC RF exposure requirements, this device and its antenna must not be co-located or operating in conjunction with any other antenna or transmitter.

Pour se conformer aux exigences de conformité RF canadienne l'exposition, cet appareil et son antenne ne doivent pas étre co-localisés ou fonctionnant en conjonction avec une autre antenne ou transmetteur.

The CC2340R5MODA module from TI is certified for IC as a single-modular transmitter. The CC2340R5MODA module from TI is meets IC modular approval and labeling requirements. The IC follows the same testing and rules as the FCC regarding certified modules in authorized equipment.

This device complies with Industry Canada licence-exempt RSS standards.

Operation is subject to the following two conditions:

- This device may not cause interference.
- This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence.

L'exploitation est autorisée aux deux conditions suivantes:

- L'appareil ne doit pas produire de brouillage
- L'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

8.14.3 ETSI/CE Certification

The CC2340R5MODA module from TI is CE certified with certifications to the appropriate EU radio and EMC directives summarized in the Declaration of Conformity and evidenced by the CE mark. The module is tested and certified against the Radio Equipment Directive (RED).

See the full text of the for the EU Declaration of Conformity for the CC2340R5MODA device.

8.15 Module Markings

Figure 8-1 shows the top-side marking for the CC2340R5MODA module.

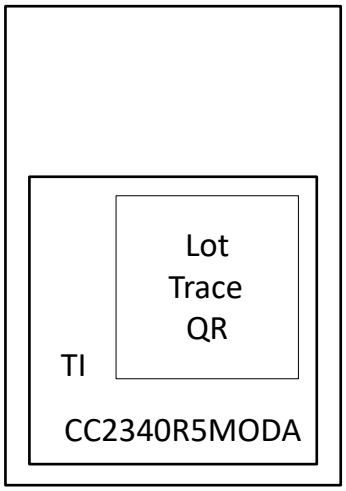


Figure 8-1. Top-Side Marking

Table 8-5 lists the CC2340R5MODA module markings.

Table 8-5. Module Descriptions

MARKING	DESCRIPTION
CC2340R5MODA	Generic Part Number
TI	Texas Instruments
QR Code	LTC (Lot Trace Code)

8.16 End Product Labeling

The CC2340R5MODA module complies with the FCC single modular FCC grant, FCC ID: **ZAT-2340R5MODA**. The host system using this module must display a visible label indicating the following text:

Contains FCC ID: **ZAT-2340R5MODA**

The CC2340R5MODA module complies with the IC single modular IC grant, IC: **451H-2340R5MODA**. The host system using this module must display a visible label indicating the following text:

Contains IC: **451H-2340R5MODA**

For more information on end product labeling and a sample label, please see section 4 of the OEM Integrators Guide

8.17 Manual Information to the End User

The OEM integrator must be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The end user manual must include all required regulatory information and warnings as shown in this manual.

9 Application, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Typical Application Circuit

Figure 9-1 shows the typical application schematic using the CC2340R5MODA module. RFIO (pin 4) is the conducted Tx and Rx RF port and ANT_IN (pin 3) is the connection to the integrated antenna. CA1 should be assembled when using the integrated antenna option within the module.

If using the external antenna option, CA2 should be assembled and CA1 should be removed. For the full reference schematic, download the LP-EM-CC2340R5MODA Design Files.

- If a Power-On-Reset is required then components R1 and C92 should be added. R1 should be 100 kΩ and C92 should be 100 nF.
- If a low-power oscillator is required for the application, then Y1 should be added with the load capacitors C81 and C91

Note

The following guidelines are recommended for implementation of the RF design when using an external antenna on the RFIO path, pin 4:

- Make sure the RF path is designed with an impedance of 50 Ω.
- Tuning of the antenna impedance π matching network is recommended after manufacturing of the PCB to account for PCB parasitics.

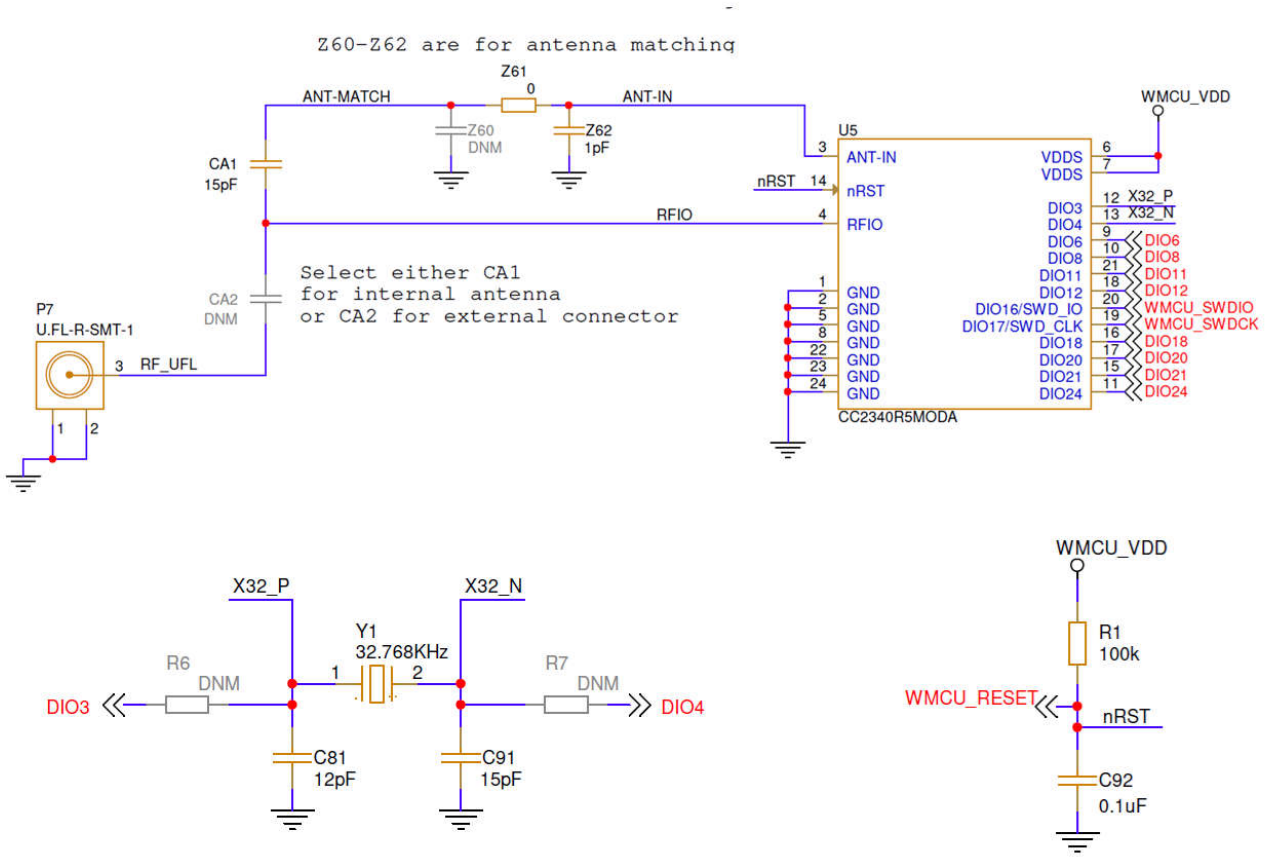


Figure 9-1. CC2340R5MODA Typical Application Schematic

Table 9-1 provides the bill of materials for a typical application using the CC2340R5MODA module with the internal antenna as shown in Figure 9-1.

For full operation reference design, see the LP-EM-CC2340R5MODA Design Files.

Table 9-1. Bill of Materials for Internal Antenna Configuration

PART REFERENCE	VALUE	MANUFACTURER	PART NUMBER	DESCRIPTION
CA1, CA2(1)	15 pF	Murata	GRM0335C1H150GA01D	Capacitor, ceramic, 15 pF, 50 V, ±2%, C0G/NP0, 0201
U5	CC2340R5MODA	Texas Instruments	CC2340R5MODAN0MHAR	SimpleLink™ multiprotocol 2.4-GHz wireless MCU with integrated power amplifier and Antenna
Y1	32.768kHz	TAI-SAW	TZ3359DAAO73	Crystal, resonator, 32.768kHz, -40°C / +125°C, SMD

(1) CA1 is placed when using the integrated antenna. CA2 is placed when using an external antenna

9.2 Device Connections

9.2.1 Unused Pins

All unused pins can be left unconnected without the concern of having leakage current.

9.3 PCB Layout Guidelines

This section details the PCB guidelines to speed up the PCB design using the CC2340R5MODA module. The integrator of the CC2340R5MODA modules must comply with the PCB layout recommendations described in the

following subsections to minimize the risk with regulatory certifications for the FCC, IC/ISED, ETSI/CE, and RAR (UK). Moreover, TI recommends customers to follow the guidelines described in this section to achieve similar performance to that obtained with the TI reference design.

9.3.1 General Layout Recommendations

Make sure that the following general layout recommendations are followed:

- Have a solid ground plane and ground vias under the module apart from underneath the antenna section for stable system and thermal dissipation. Underneath the antenna section, there should be no routing at all for all the main board layers. The route keep-out area should be 7.0 x 3.2mm on all layers; refer to Figure 9-2. If this route keep-out area is reduced or any components are placed within this area on the bottom layer, then the antenna efficiency is reduced.
- Do not run signal traces underneath the module on a layer where the module is mounted.

9.3.1.1 Typical RF Layout Recommendations with Integrated Antenna

It is critical that the RF section be laid out correctly to make sure optimal module performance. A poor layout can cause low-output power and sensitivity degradation. Figure 9-2 shows the RF placement and routing of the CC2340R5MODA module with the 2.4-GHz integrated antenna.

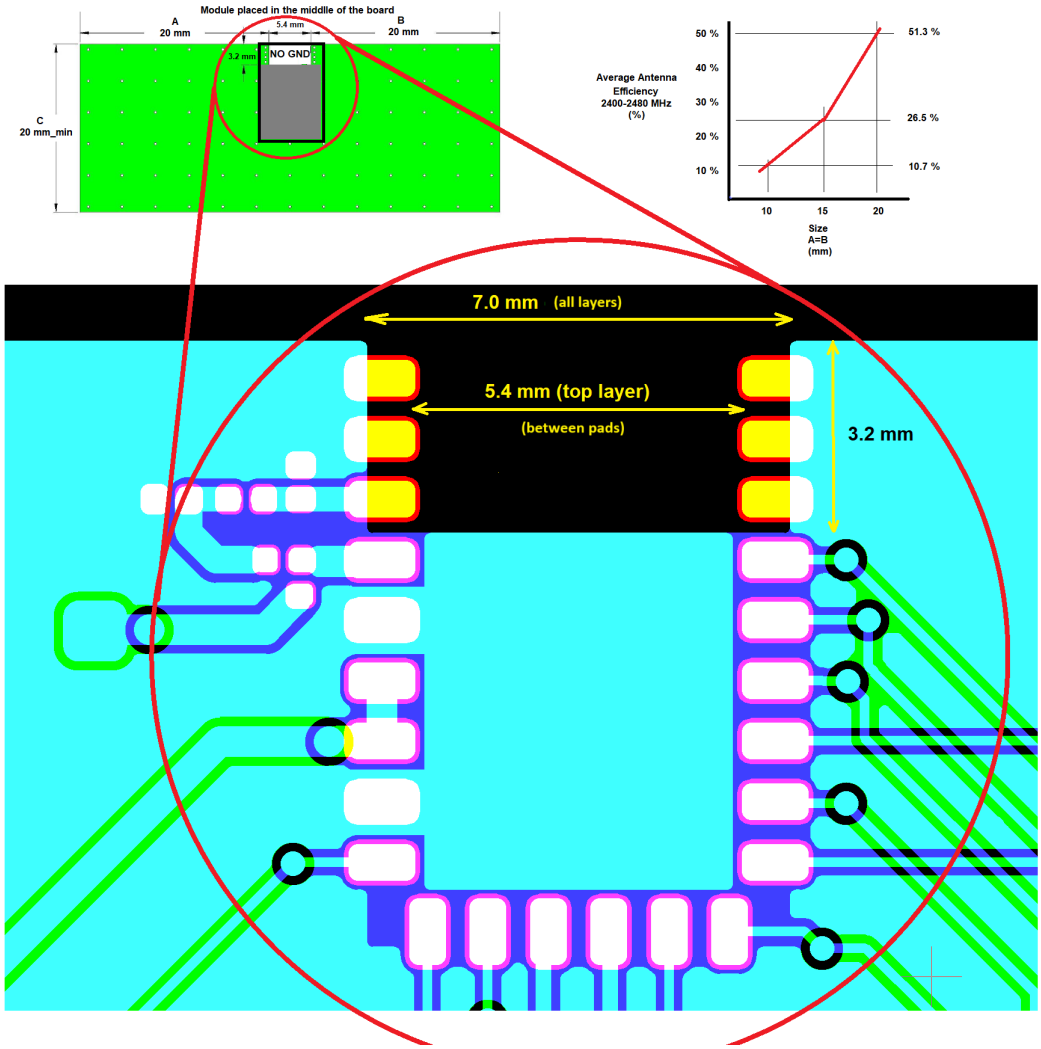


Figure 9-2. Module Layout Guidelines

Follow these RF layout recommendations for the CC2340R5MODA module when using the integrated Antenna:

- Dimensions A, B & C in Figure 9-2 should be at least 20mm for optimal antenna efficiency. These dimensions can be reduced for compact layout designs but then the antenna efficiency will be reduced. With A and B dimensions at 20mm, the antenna efficiency will be around 50%. If A and B are reduced to 15mm; then the expected antenna efficiency will be around 25%. If A and B are reduced to 10mm; then the expected antenna efficiency will be around 10%. It is not recommended to have A or B dimensions less than 10mm.
- Components Z60, Z61 & Z62 are for antenna matching purposes. The optimum antenna match values for Z60, Z61 & Z62 will be dependent on the layout, final product casing and material, and size of the GND plane. For the Launchpad ref design, Z60: DNM, Z61: 0 ohm & Z62 is 1pF. It is always recommended to use a pi-filter (Z60, Z61 & Z62) for the antenna matching for flexibility to match the antenna and to minimize mismatch losses.
- It is not recommended to have A or B dimensions less than 10mm in Figure 9-2
- There must be at least a ground-reference plane under the module on the main PCB

9.3.1.2 RF Layout Recommendations with External Antenna

When using the external antenna option, it is critical that the RF section be laid out correctly to make sure optimal module performance. A poor layout can cause low-output power and sensitivity degradation. Figure 9-3 shows the RF placement and routing of the CC2340R5MODA module routed for use with an external SMA connector.

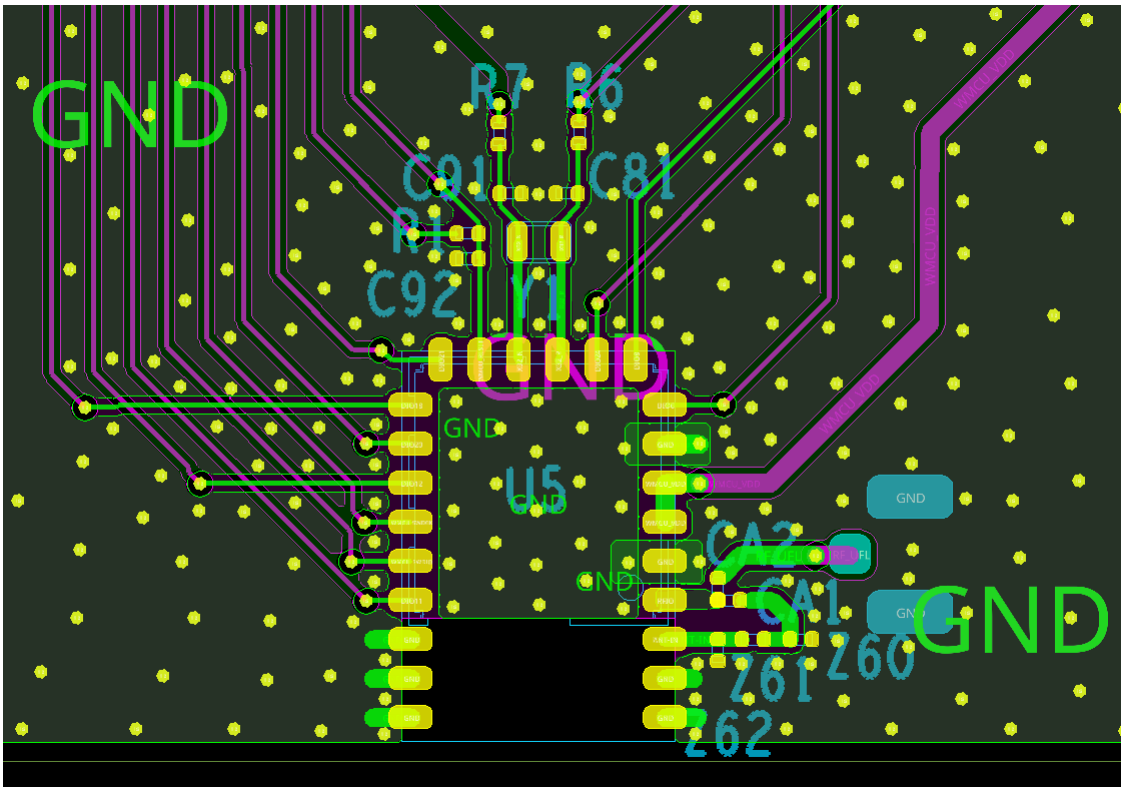


Figure 9-3. Module Layout Guidelines with External Antenna

Follow these RF layout recommendations for the CC2340R5MODA module when connecting to an external antenna:

- RF traces must have 50-Ω impedance.
- RF trace bends must be made with gradual curves, and 90° bends must be avoided.
- RF traces must not have sharp corners.
- There must be no traces or ground under the antenna section.
- RF traces must have via stitching on the ground plane beside the RF trace on both sides.
- RF traces must be as short as possible.
- The module must be as close to the PCB edge in consideration of the product enclosure and type of antenna being used.

9.4 Reference Designs

The following reference designs should be followed closely when implementing designs using the CC2340R5MODA devices.

Special attention must be paid to RF component placement, decoupling capacitors, and DCDC regulator components, as well as ground connections for all of these.

LP-EM-CC2340R5MODA	The CC2340R5MODA LaunchPad Design Files contain detailed schematics and layouts to build application-specific boards using the CC2340R devices in the WCSP YBG package.

Sub-1GHz and 2.4GHz Antenna Kit for LaunchPad™ Development Kit and SensorTag	The antenna kit allows real-life testing to identify the optimal antenna for your application. The antenna kit includes 16 antennas for frequencies from 169MHz to 2.4GHz, including: • PCB antennas • Helical antennas • Chip antennas • Dual-band antennas for 868MHz and 915MHz combined with 2.4GHz The antenna kit includes a JSC cable to connect to the Wireless MCU LaunchPad Development Kits and SensorTags.

10 Environmental Requirements and SMT Specifications

10.1 PCB Bending

The PCB follows IPC-A-600J for PCB twist and warpage < 0.75% or 7.5 mil per inch.

10.2 Handling Environment

10.2.1 Terminals

The product is mounted with motherboard through land-grid array (LGA). To prevent poor soldering, do not make skin contact with the LGA portion.

10.2.2 Falling

The mounted components will be damaged if the product falls or is dropped. Such damage may cause the product to malfunction.

10.3 Storage Condition

10.3.1 Moisture Barrier Bag Before Opened

A moisture barrier bag must be stored in a temperature of less than 30°C with humidity under 85% RH. The calculated shelf life for the dry-packed product will be 24 months from the date the bag is sealed.

10.3.2 Moisture Barrier Bag Open

Humidity indicator cards must be blue, < 30%.

10.4 PCB Assembly Guide

The wireless MCU modules are packaged in a substrate base Leadless Quad Flatpack (QFM) package. The modules are designed with pull back leads for easy PCB layout and board mounting.

10.4.1 PCB Land Pattern & Thermal Vias

We recommended a solder mask defined land pattern to provide a consistent soldering pad dimension in order to obtain better solder balancing and solder joint reliability. PCB land pattern are 1:1 to module soldering pad dimension. Thermal vias on PCB connected to other metal plane are for thermal dissipation purpose. It is critical to have sufficient thermal vias to avoid device thermal shutdown. Recommended vias size are 0.2mm and position not directly under solder paste to avoid solder dripping into the vias.

10.4.2 SMT Assembly Recommendations

The module surface mount assembly operations include:

- Screen printing the solder paste on the PCB
- Monitor the solder paste volume (uniformity)
- Package placement using standard SMT placement equipment
- X-ray pre-reflow check - paste bridging
- Reflow
- X-ray post-reflow check - solder bridging and voids

10.4.3 PCB Surface Finish Requirements

A uniform PCB plating thickness is key for high assembly yield. For an electroless nickel immersion gold finish, the gold thickness should range from 0.05µm to 0.20µm to avoid solder joint embrittlement. Using a PCB with Organic Solderability Preservative (OSP) coating finish is also recommended as an alternative to Ni-Au.

10.4.4 Solder Stencil

Solder paste deposition using a stencil-printing process involves the transfer of the solder paste through pre-defined apertures with the application of pressure. Stencil parameters such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of package is highly recommended to improve board assembly yields.

10.4.5 Package Placement

Packages can be placed using standard pick and place equipment with an accuracy of ±0.05mm. Component pick and place systems are composed of a vision system that recognizes and positions the component and a mechanical system that physically performs the pick and place operation. Two commonly used types of vision systems are:

- A vision system that locates a package silhouette
- A vision system that locates individual pads on the interconnect pattern

The second type renders more accurate placements but tends to be more expensive and time consuming. Both methods are acceptable since the parts align due to a self-centering features of the solder joint during solder reflow. It is recommended to avoid solder bridging to 2 mils into the solder paste or with minimum force to avoid causing any possible damage to the thinner packages.

10.4.6 Solder Joint Inspection

After surface mount assembly, transmission X-ray should be used for sample monitoring of the solder attachment process. This identifies defects such as solder bridging, shorts, opens, and voids. It is also recommended to use side view inspection in addition to X-rays to determine if there are "Hour Glass" shaped solder and package tilting existing. The "Hour Glass" solder shape is not a reliable joint. 90° mirror projection can be used for side view inspection.

10.4.7 Rework and Replacement

TI recommends removal of modules by rework station applying a profile similar to the mounting process. Using a heat gun can sometimes cause damage to the module by overheating.

10.4.8 Solder Joint Voiding

TI recommends to control solder joint voiding to be less than 30% (per IPC-7093). Solder joint voids could be reduced by baking of components and PCB, minimized solder paste exposure duration, and reflow profile optimization.

10.5 Baking Conditions

Products require baking before mounting if:

- Humidity indicator cards read > 30%
- Temp < 30°C, humidity < 70% RH, over 96 hours

Baking condition: 90°C, 12 to 24 hours

Baking times: 1 time

10.6 SMT Recommendations

Figure 10-1 shows the recommended reflow profile for the CC2340R5MODA module.

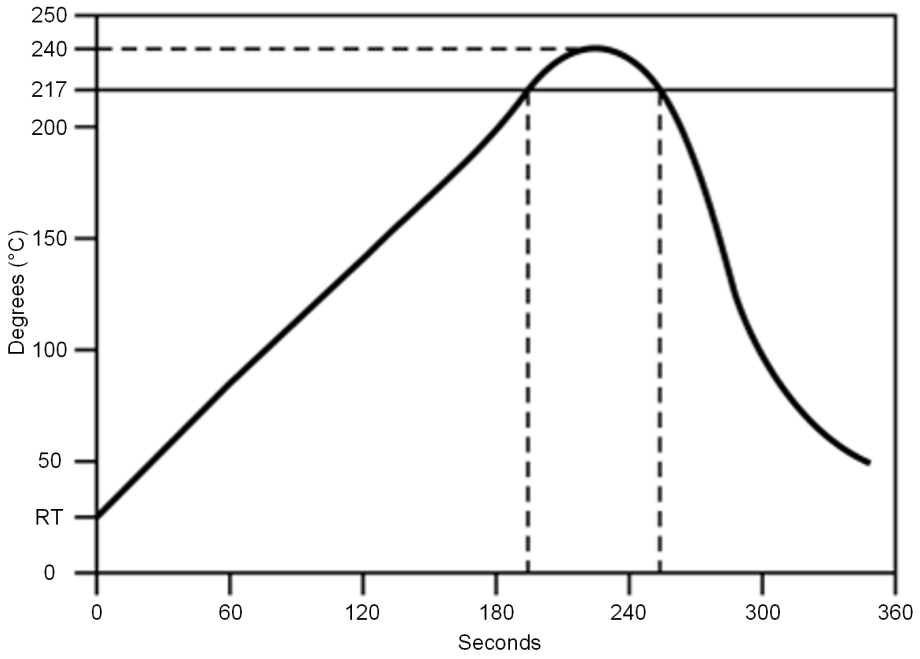


Figure 10-1. Reflow Profile for the CC2340R5MODA Module

Table 10-1. Recommended reflow profile

Profile Elements	Convection or IR[1]
Peak temperature range	235 to 240°C Typical (250°C maximum)
Pre-heat / soaking time (150 to 200°C)	60 to 120 seconds
Soldering time (above 217°C)	60 to 75 seconds
Time with 5°C to peak	20 to 40 seconds
Heating rate	3°C / second
Cooling rate	-3°C / second

- Solder paste alloy: SAC305 (Sn96.5, Ag3.0, Cu0.5)

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed as follows.

11.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to all part numbers and/or date-code. Each device has one of three prefixes/identifications: X, P, or null (no prefix) (for example, X is in preview; therefore, an X prefix/identification is assigned).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Production devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, *MHA*).

For orderable part numbers of CC2340R5MODAin the MHA package type, see the *Package Option Addendum* of this document, the Device Information in Section 3, the TI website (www.ti.com), or contact your TI sales representative.

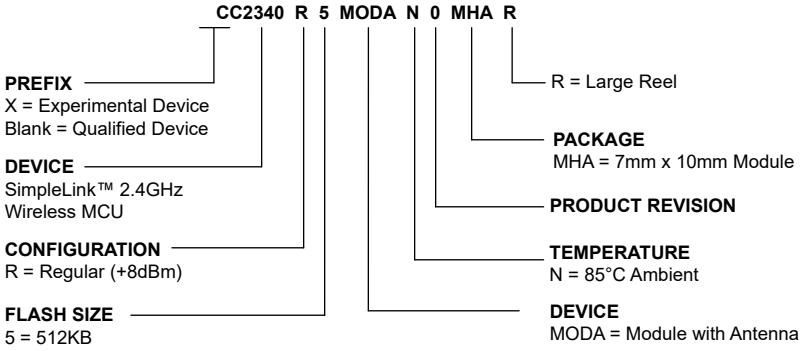


Figure 11-1. Device Nomenclature

11.2 Tools and Software

The CC2340R5MODA device is supported by a variety of software and hardware development tools.

Development Kit

CC2340R53 LaunchPad™ Development Kit	The CC2340R53 LaunchPad™ Development Kit enables development of high-performance wireless applications that benefit from low-power operation. The kit features the CC2340R53 SimpleLink Wireless MCU, which allows you to quickly evaluate and prototype 2.4GHz wireless applications such as Bluetooth 5 Low Energy. The kit works with the LaunchPad ecosystem, enabling additional functionality like sensors, display, and more.

Software

SimpleLink™ Low Power F3 software development kit (SDK)

The SimpleLink™ Low Power F3 software development kit (SDK) provides a complete package for the development of wireless applications on the CC2340R family of devices. The SDK includes a comprehensive software package for the CC2340R5MODA device, including the following protocol stacks:

- Bluetooth Low Energy

The SimpleLink Low Power F3 SDK is part of TI's SimpleLink MCU platform, offering a single development environment that delivers flexible hardware, software, and tool options for customers developing wired and wireless applications. For more information about the SimpleLink MCU Platform, visit https://www.ti.com/simplelink.

Development Tools

Code Composer Studio™ Integrated Development Environment (IDE)

Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before.

CCS has support for all SimpleLink Wireless MCUs and includes support for EnergyTrace™ software (application energy usage profiling).

Code Composer Studio is provided free of charge when used in conjunction with the XDS debuggers included on a LaunchPad Development Kit.

Code Composer Studio™ Cloud IDE

Code Composer Studio (CCS) Cloud is a web-based IDE that allows you to create, edit, and build CCS projects. After you have successfully built your project, you can download and run on your connected LaunchPad. Basic debugging, including features like setting breakpoints and viewing variable values, is now supported with CCS Cloud.

IAR Embedded Workbench® for Arm®

IAR Embedded Workbench® is a set of development tools for building and debugging embedded system applications using Assembler, C and C++. It provides a completely integrated development environment that includes a project manager, editor, and build tools. IAR has support for all SimpleLink Wireless MCUs. It offers broad debugger support, including XDS110, IAR I-jet™, and Segger J-Link™. IAR is also supported out-of-the-box on most software examples provided as part of the SimpleLink SDK.

SmartRF™ Studio

SmartRF™ Studio is a Windows® application that can be used to evaluate and configure SimpleLink Wireless MCUs from Texas Instruments. The application will help designers of RF systems to easily evaluate the radio at an early stage in the design process. It is especially useful for generation of configuration register values and for practical testing and debugging of the RF system. SmartRF Studio can be used either as a standalone application or together with applicable evaluation boards or debug probes for the RF device. Features of the SmartRF Studio include:

- Link tests - send and receive packets between nodes
- Antenna and radiation tests - set the radio in continuous wave TX and RX states
- Export radio configuration code for use with the TI SimpleLink SDK RF driver
- Custom GPIO configuration for signaling and control of external switches

UniFlash

UniFlash is a standalone tool used to program on-chip flash memory on TI MCUs. UniFlash has a GUI, command line, and scripting interface. UniFlash is available free of charge.

11.2.1 SimpleLink™ Microcontroller Platform

The SimpleLink microcontroller platform sets a new standard for developers with the broadest portfolio of wired and wireless Arm® MCUs (System-on-Chip) in a single software development environment. Delivering flexible hardware, software and tool options for your IoT applications. Invest once in the SimpleLink software development kit and use throughout your entire portfolio. Learn more at ti.com/simplelink.

11.3 Documentation Support

To receive notification of documentation updates on data sheets, errata, application notes and similar, navigate to the device product folder (CC2340R5). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the MCU, related peripherals, and other technical collateral is listed as follows.

TI Resource Explorer

TI Resource Explorer	Software examples, libraries, executables, and documentation are available for your device and development board.

Errata

CC2340R Silicon Errata	The silicon errata describes the known exceptions to the functional specifications for each silicon revision of the device and description on how to recognize a device revision.

Application Reports

All application reports for the CC2340R5MODA devices are found on the device product folder (CC2340R5).

Technical Reference Manual (TRM)

CC23xx SimpleLink™ Wireless MCU TRM	The TRM provides a detailed description of all modules and peripherals available in the device family.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

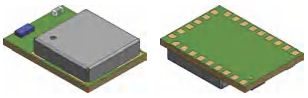
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2026	*	Initial Release

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

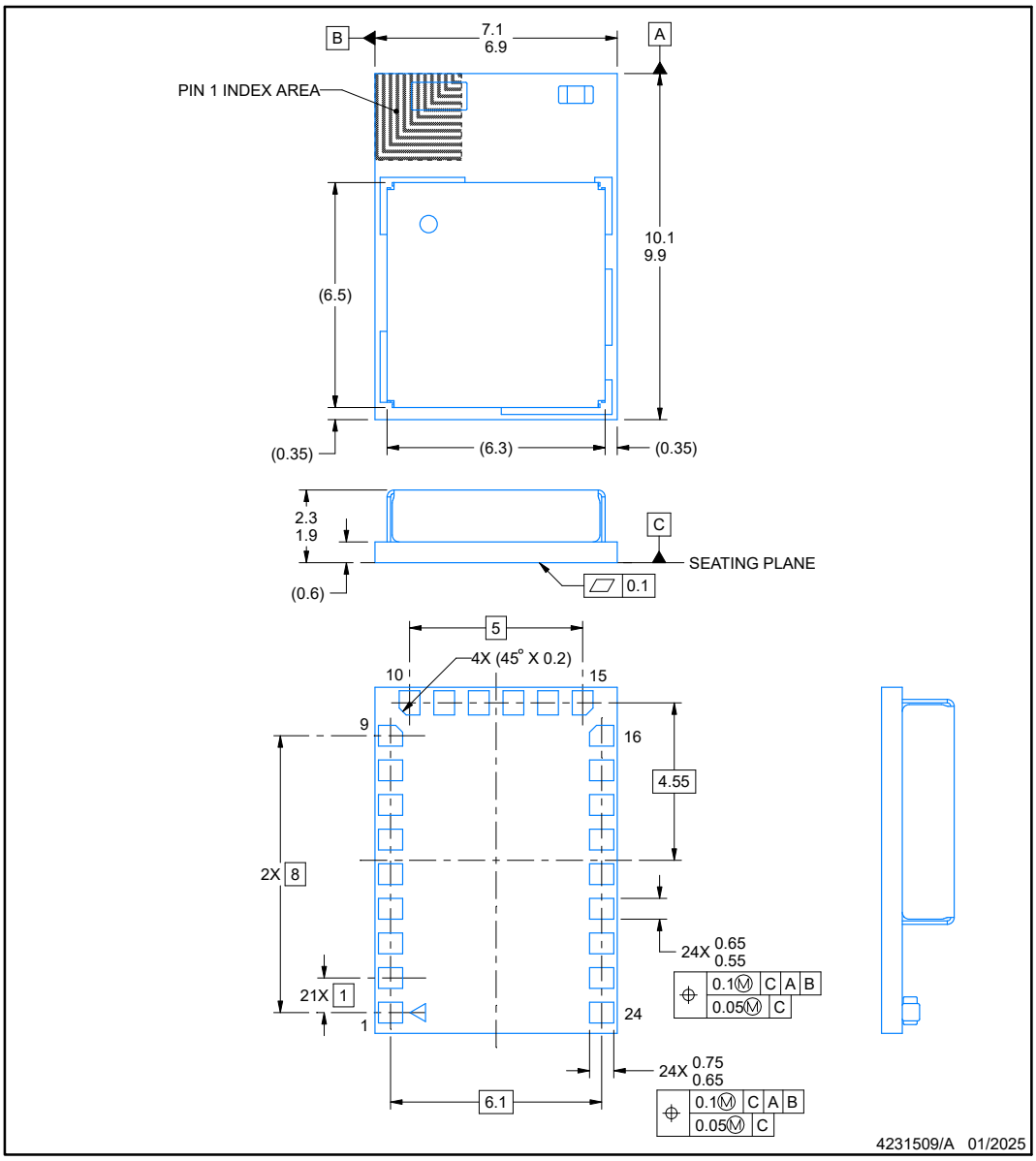
MHA0024A



PACKAGE OUTLINE

QFM - 2.3 mm max height

QUAD FLAT MODULE



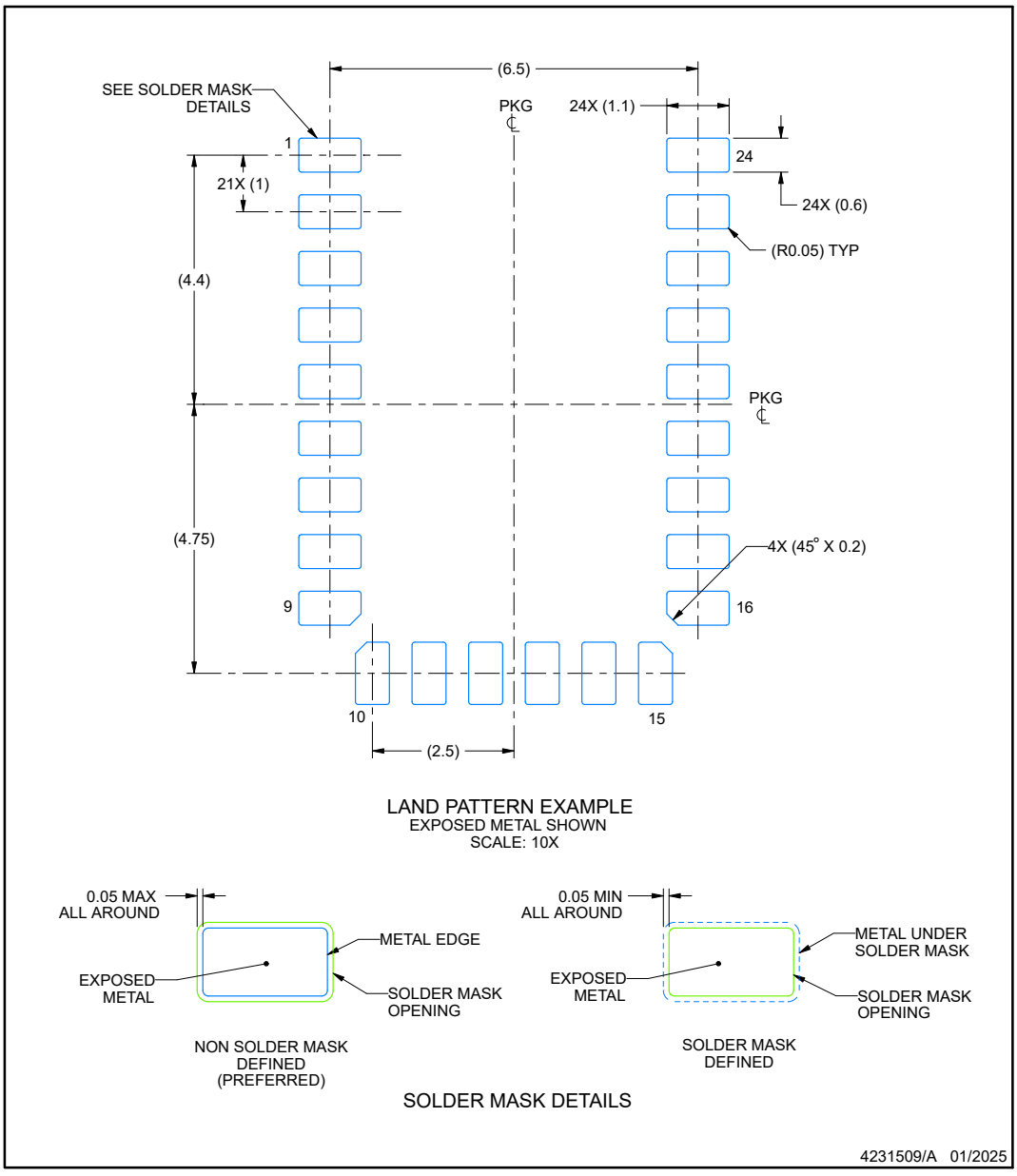
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

MHA0024A — **QFM - 2.3 mm max height**

QUAD FLAT MODULE



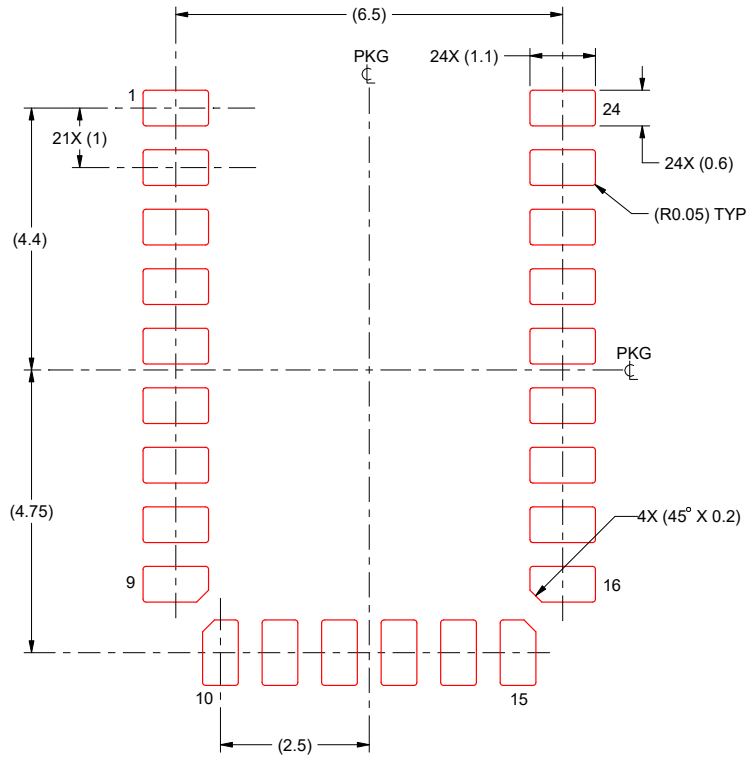
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

MHA0024A — **QFM - 2.3 mm max height**

QUAD FLAT MODULE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4231509/A 01/2025

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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