

## CDx4AC138 3-Line to 8-Line Decoders/Demultiplexers

## 1 Features

- AC types feature 1.5V to 5.5V operation and balanced noise immunity at 30% of the supply voltage
- Speed of bipolar F, AS, and S, with significantly reduced power consumption
- Designed specifically for high-speed memory decoders and data-transmission systems
- Incorporate three enable inputs to simplify cascading and/or data reception
- Balanced propagation delays
- $\pm 24\text{mA}$  output drive current
  - Fanout to 15 F Devices
- SCR-latchup-resistant CMOS process and circuit design
- Exceeds 2kV ESD protection per MIL-STD-883, method 3015

## 2 Description

The 'AC138 decoders/demultiplexers are designed for high-performance memory-decoding and data-routing applications that require very short propagation-delay times. In high-performance memory systems, these decoders can be used to minimize the effects of system decoding.

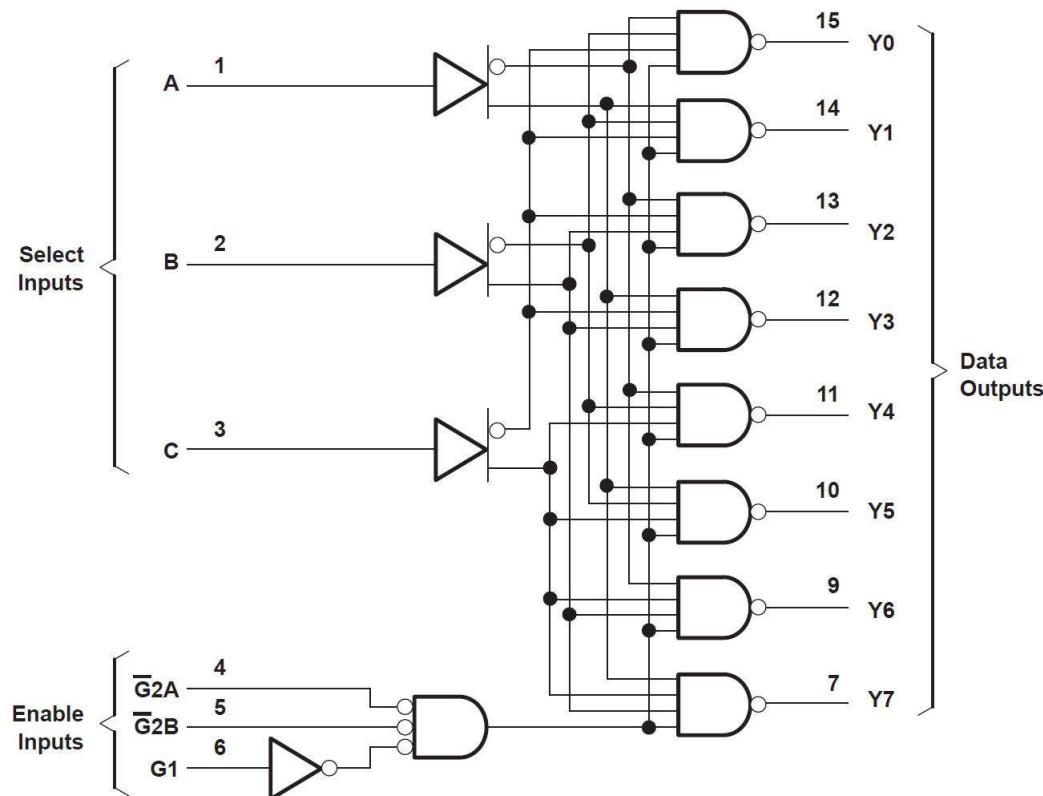
## Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>	BODY SIZE <sup>(3)</sup>
CDx4AC138	BQB (WQFN, 16)	3.5mm × 2.5mm	3.5mm × 2.5mm
	D (SOIC, 16)	9.9mm × 6mm	9.9mm × 3.9mm
	N (PDIP, 16)	19.3mm × 9.4mm	19.3mm × 6.35mm
	PW (TSSOP, 16)	5.00mm × 6.4mm	5.00mm × 4.40mm

(1) For more information, see [Section 10](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.

(3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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### 3 Pin Configuration and Functions

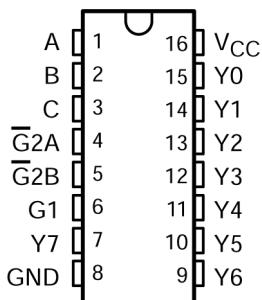


Figure 3-1. CD54AC138 J Package; CD74AC138 D, N, or PW Package; 16-Pin CDIP, SOIC, PDIP, or TSSOP (Top View)

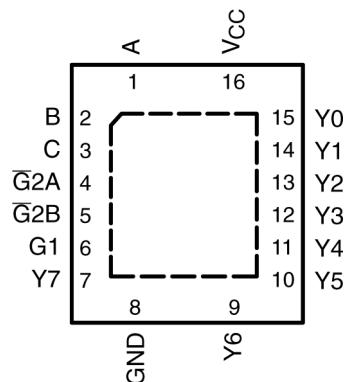


Figure 3-2. CD74AC138 BQB Package, 16-Pin WQFN

Table 3-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
A	1	I	Input A
B	2	I	Input B
C	3	I	Input C
$\overline{G2A}$	4	I	Strobe Input 2A, active low
$\overline{G2B}$	5	I	Strobe Input 2B, active low
G1	6	I	Strobe Input
Y7	7	O	Output 7
GND	8	G	Ground
Y6	9	O	Output 6
Y5	10	O	Output 5
Y4	11	O	Output 4
Y3	12	O	Output 3
Y2	13	O	Output 2
Y1	14	O	Output 1
Y0	15	O	Output 0
V <sub>CC</sub>	16	P	Positive Supply
Thermal Pad <sup>(2)</sup>		—	Thermal Pad

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

(2) BQB package only

## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		-0.5	6	V
I <sub>IK</sub> <sup>(2)</sup>	Input clamp current	(V <sub>I</sub> < 0 V or V <sub>I</sub> > V <sub>CC</sub> )		±20	mA
I <sub>OK</sub> <sup>(2)</sup>	Output clamp current	(V <sub>O</sub> < 0 V or V <sub>O</sub> > V <sub>CC</sub> )		±50	mA
I <sub>O</sub>	Continuous output current	(V <sub>O</sub> > 0 V or V <sub>O</sub> < V <sub>CC</sub> )		±50	mA
	Continuous current through V <sub>CC</sub> or GND			±100	mA
T <sub>stg</sub>	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 4.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		T <sub>A</sub> = 25°C		-55°C to 125°C		-40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	1.5	5.5	1.5	5.5	1.5	5.5	V
V <sub>IH</sub>	V <sub>CC</sub> = 1.5 V	1.2		1.2		1.2		V
	V <sub>CC</sub> = 3 V	2.1		2.1		2.1		
	V <sub>CC</sub> = 5.5 V	3.85		3.85		3.85		
V <sub>IL</sub>	V <sub>CC</sub> = 1.5 V		0.3		0.3		0.3	V
	V <sub>CC</sub> = 3 V		0.9		0.9		0.9	
	V <sub>CC</sub> = 5.5 V		1.65		1.65		1.65	
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 4.5 V to 5.5 V		-24		-24		-24 mA
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 4.5 V to 5.5 V		24		24		24 mA
Δt/ΔV	V = 1.5 V to 3 V			50		50		50 ns/V
	V <sub>CC</sub> = 3.6 V to 5.5 V			20		20		20

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

#### 4.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		CD74AC138				UNIT
		BQB (WQFN)	D (SOIC)	N (PDIP)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.9	106.6	67	126.2	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

#### 4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	TA = 25 °C		-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$V_{OH}$	$V_I = V_{IH}$ or $V_{IL}$	$I_{OH} = -50 \mu A$	1.5 V	1.4	1.4		1.4		V
			3 V	2.9	2.9		2.9		
			4.5 V	4.4	4.4		4.4		
		$I_{OH} = -4 \text{ mA}$	3 V	2.58	2.4		2.48		
		$I_{OH} = -24 \text{ mA}$	4.5 V	3.94	3.7		3.8		
		$I_{OH} = -50 \text{ mA}^{(1)}$	5.5 V		3.85				
		$I_{OH} = -75 \text{ mA}^{(1)}$	5.5 V				3.85		
$V_{OL}$	$V_I = V_{IH}$ or $V_{IL}$	$I_{OL} = 50 \mu A$	1.5 V	0.1	0.1		0.1		V
			3 V	0.1	0.1		0.1		
			4.5 V	0.1	0.1		0.1		
		$I_{OL} = 12 \text{ mA}$	3 V	0.36	0.5		0.44		
		$I_{OL} = 24 \text{ mA}$	4.5 V	0.36	0.5		0.44		
		$I_{OL} = 50 \text{ mA}^{(1)}$	5.5 V		1.65		-		
		$I_{OL} = 75 \text{ mA}^{(1)}$	5.5 V				1.65		
$I_I$	$V_I = V_{CC}$ or GND		5.5 V	$\pm 0.1$	$\pm 1$		$\pm 1$	$\mu A$	
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$		5.5 V	8	160		80	$\mu A$	
$C_i$				10	10		10	$pF$	

(1) Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50- $\Omega$  transmission-line drive capability at 85°C and 75- $\Omega$  transmission-line drive capability at 125°C.

#### 4.6 Switching Characteristics, $V_{CC} = 1.5V$

over recommended operating free-air temperature range,  $V_{CC} = 1.5V$ ,  $C_L = 50pF$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
$t_{PLH}$	A, B, C	Any Y		138		125	ns
$t_{PHL}$				138		125	
$t_{PLH}$	G1	Any Y		138		125	ns
$t_{PHL}$				138		125	
$t_{PLH}$	$\bar{G}2A, \bar{G}2B$	Any Y		125		114	ns
$t_{PHL}$				125		114	

#### 4.7 Switching Characteristics, $V_{CC} = 3.3V \pm 0.3V$

over recommended operating free-air temperature range,  $V_{CC} = 3.3V \pm 0.3V$ ,  $C_L = 50pF$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
$t_{PLH}$	A, B, C	Any Y	3.9	15.4	4	14	ns
$t_{PHL}$			3.9	15.4	4	14	
$t_{PLH}$	G1	Any Y	3.9	15.4	4	14	ns
$t_{PHL}$			3.9	15.4	4	14	
$t_{PLH}$	$\overline{G}2A, \overline{G}2B$	Any Y	3.5	14	3.6	12.7	ns
$t_{PHL}$			3.5	14	3.6	12.7	

#### 4.8 Switching Characteristics, $V_{CC} = 5V \pm 0.5V$

over recommended operating free-air temperature range,  $V_{CC} = 5V \pm 0.5V$ ,  $C_L = 50pF$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

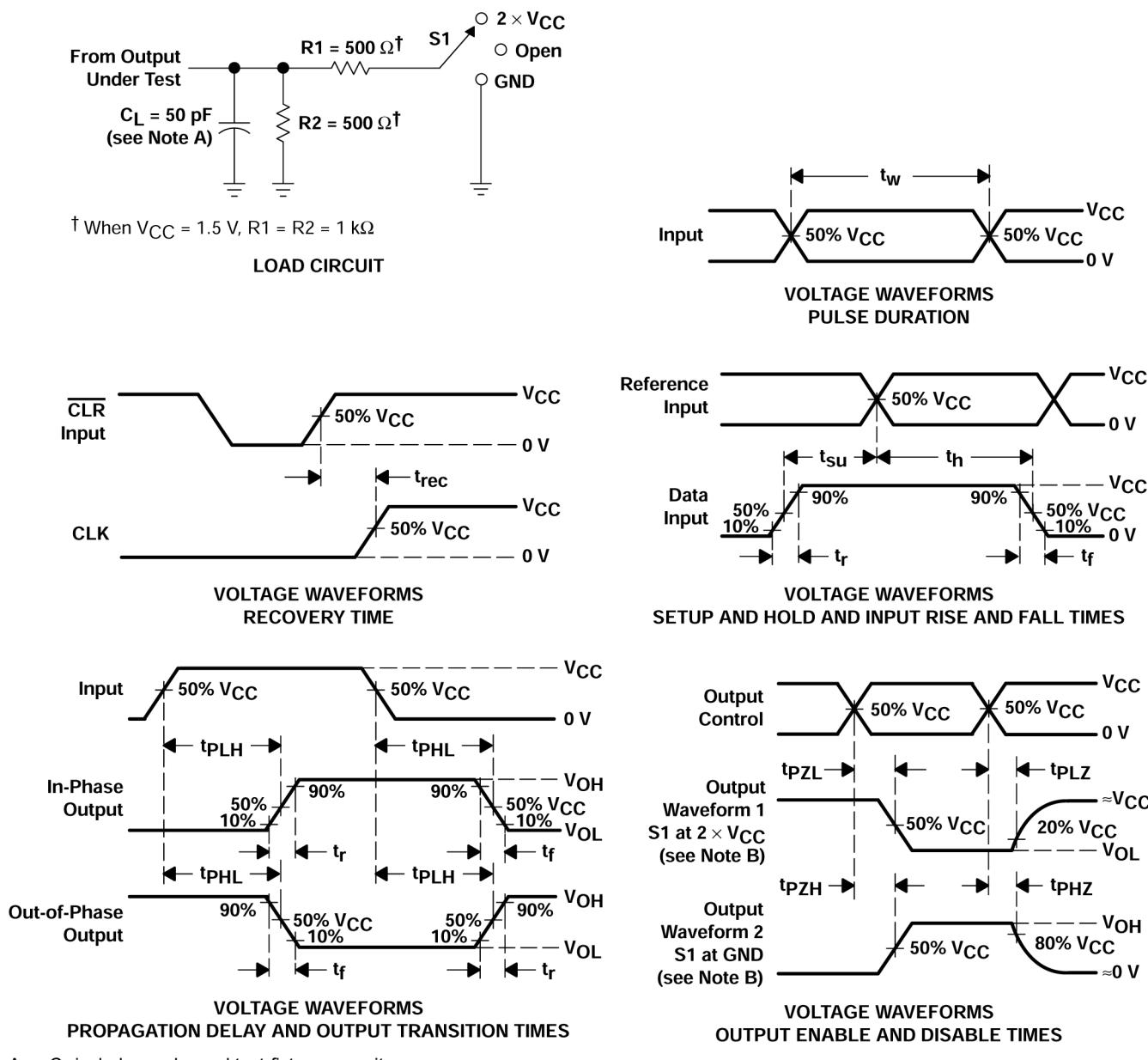
PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
$t_{PLH}$	A, B, C	Any Y	2.8	11	2.8	10	ns
$t_{PHL}$			2.8	11	2.8	10	
$t_{PLH}$	G1	Any Y	2.8	11	2.8	10	ns
$t_{PHL}$			2.8	11	2.8	10	
$t_{PLH}$	$\overline{G}2A, \overline{G}2B$	Any Y	2.5	10	2.6	9.1	ns
$t_{PHL}$			2.5	10	2.6	9.1	

#### 4.9 Operating Characteristics

$V_{CC} = 5V$ ,  $T_A = 25^\circ C$

PARAMETER	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	110	pF

## 5 Parameter Measurement Information



- A.  $C_L$  includes probe and test-fixture capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ . Phase relationships between waveforms are arbitrary.
- D. For clock inputs,  $f_{max}$  is measured with the input duty cycle at 50%.
- E. The outputs are measured one at a time with one input transition per measurement.
- F.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- G.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- H.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- I. All parameters and waveforms are not applicable to all devices.

Figure 5-1. Load Circuit and Voltage Waveforms

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

## 6 Detailed Description

### 6.1 Overview

The CDx4AC138 contains eight buffers with 3-state outputs and Schmitt-trigger inputs. The active low output enable pins ( $\overline{OE1}$  and  $\overline{OE2}$ ) control all eight channels, and are configured so that both must be low for the outputs to be active.

When the outputs are enabled, the outputs are actively driven low or high.

When the outputs are disabled, the outputs are set into the high-impedance state.

### 6.2 Functional Block Diagram

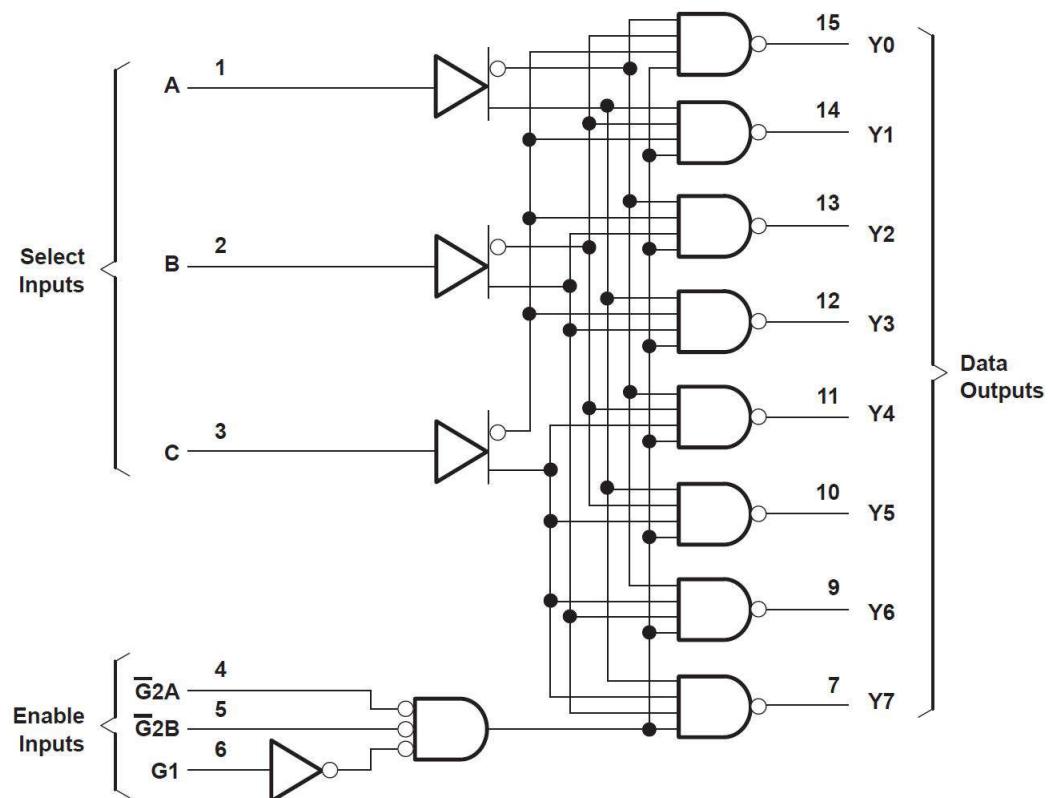
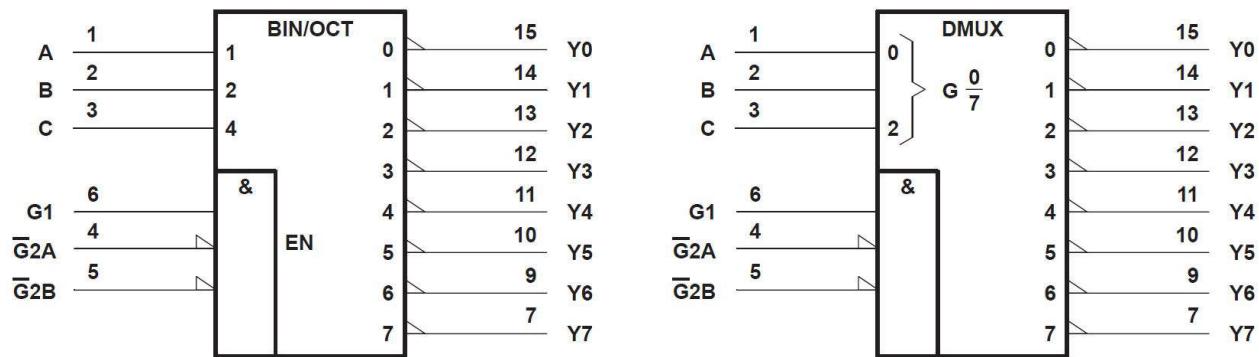


Figure 6-1. Logic Diagram (Positive Logic)



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**Figure 6-2. Logic Symbols (Alternatives)**

### 6.3 Device Functional Modes

**Table 6-1. Function Table**

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	L	H	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

## 7 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 7.1 Application Information

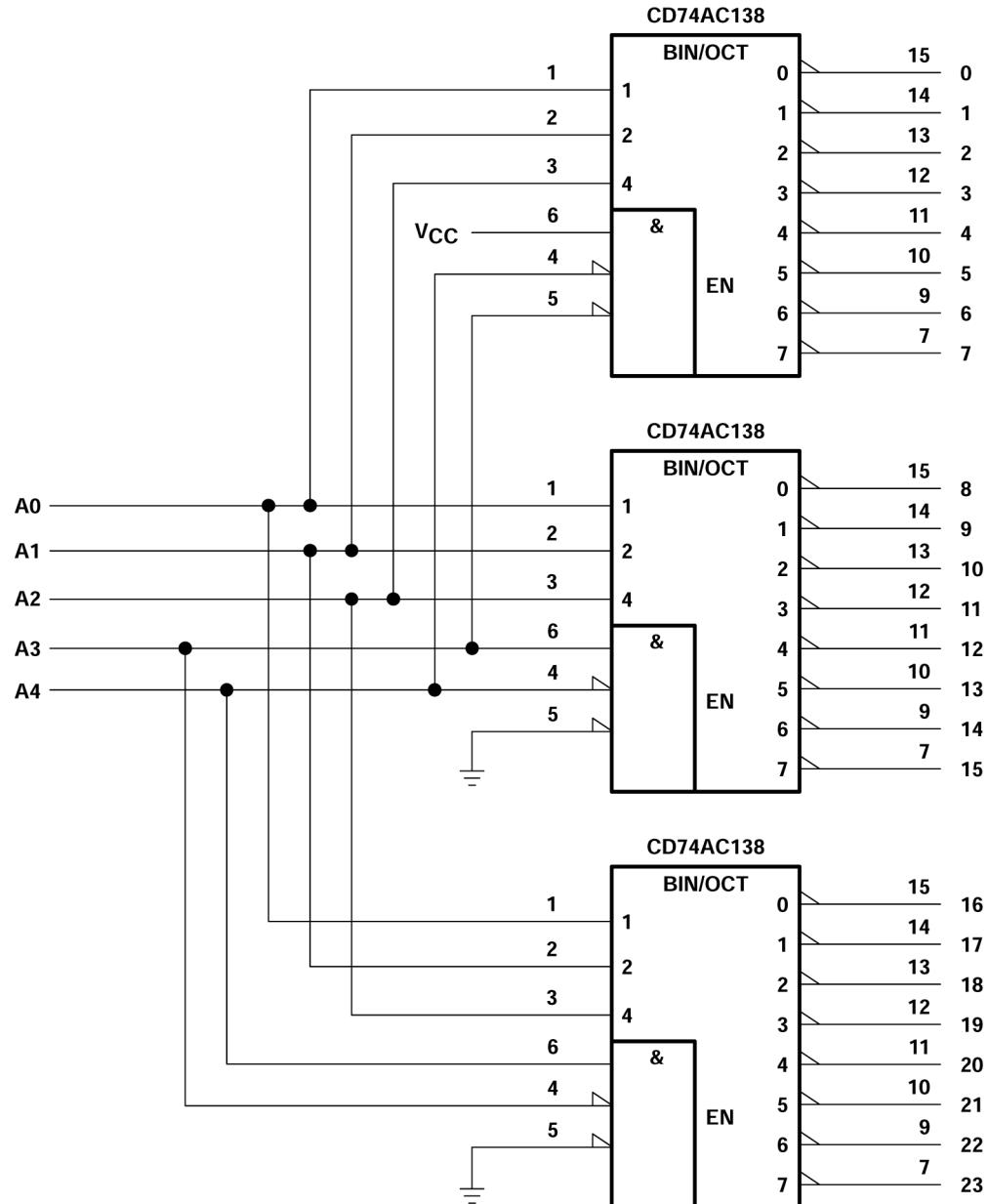
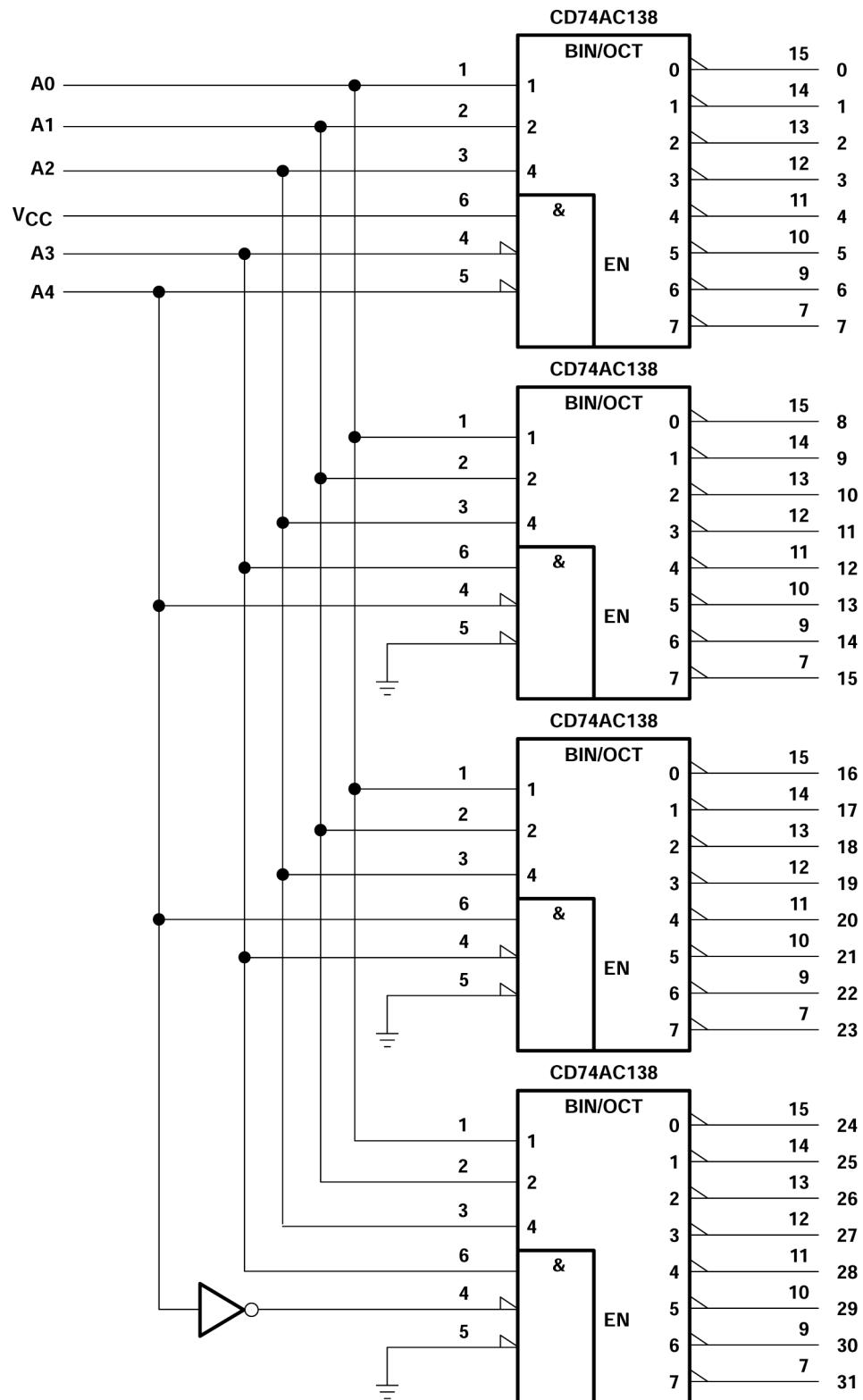


Figure 7-1. 24-Bit Decoding Scheme



**Figure 7-2. 32-Bit Decoding Scheme**

## 7.2 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A  $0.1\mu F$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The  $0.1\mu F$  and  $1\mu F$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 7.3 Layout

### 7.3.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

### 7.3.2 Layout Example

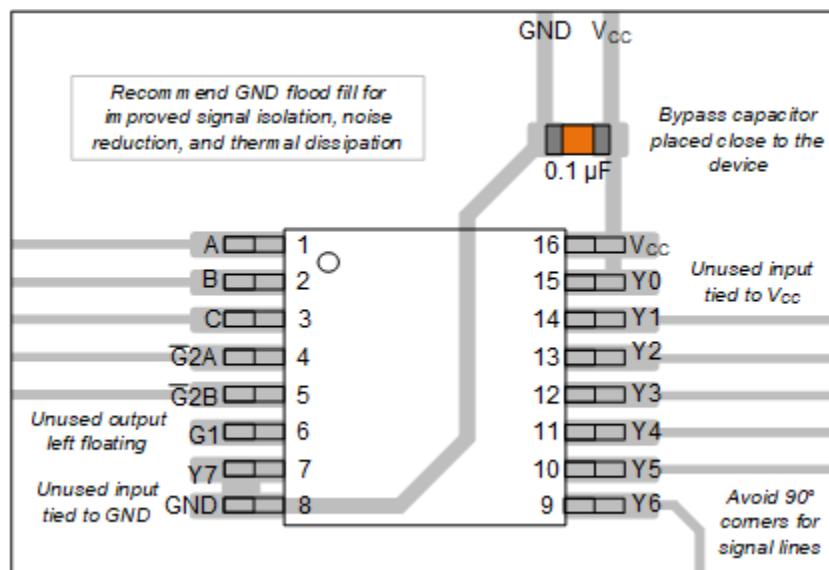


Figure 7-3. Example Layout for the CD74AC138

## 8 Device and Documentation Support

### 8.1 Documentation Support (Analog)

#### 8.1.1 Related Documentation

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CD54AC138	<a href="#">Click here</a>				
CD74AC138	<a href="#">Click here</a>				

### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

Changes from Revision B (April 2024) to Revision C (July 2024)	Page
• Added BQB and PW packages to <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, and <i>Thermal Information</i> table.....	1
• Changed E and M packages to N and D throughout data sheet.....	1

Changes from Revision A (February 2003) to Revision B (April 2024)	Page
• Added <i>Device Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1
• Updated R <sub>θJA</sub> values: D = 73 to 106.6, all values in °C/W .....	5

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">CD54AC138F3A</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54AC138F3A
CD54AC138F3A.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54AC138F3A
<a href="#">CD74AC138BQBR</a>	Active	Production	WQFN (BQB)   16	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC138
CD74AC138BQBR.A	Active	Production	WQFN (BQB)   16	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC138
<a href="#">CD74AC138E</a>	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74AC138E
CD74AC138E.A	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74AC138E
CD74AC138EE4	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74AC138E
<a href="#">CD74AC138M</a>	Obsolete	Production	SOIC (D)   16	-	-	Call TI	Call TI	-55 to 125	AC138M
<a href="#">CD74AC138M96</a>	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC138M
CD74AC138M96.A	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC138M
<a href="#">CD74AC138PWR</a>	Active	Production	TSSOP (PW)   16	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	AC138
CD74AC138PWR.A	Active	Production	TSSOP (PW)   16	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC138

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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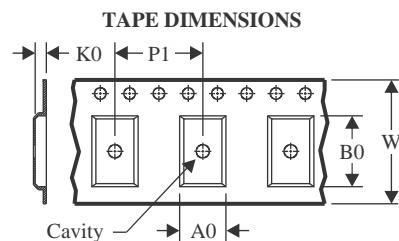
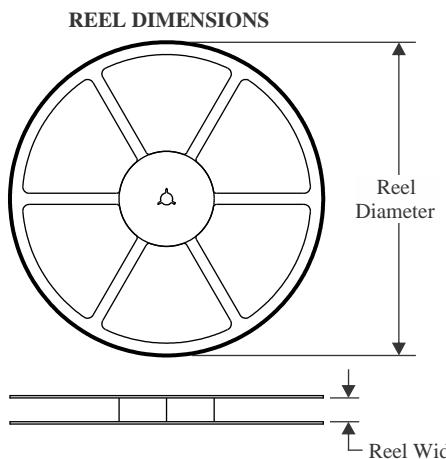
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54AC138, CD74AC138 :**

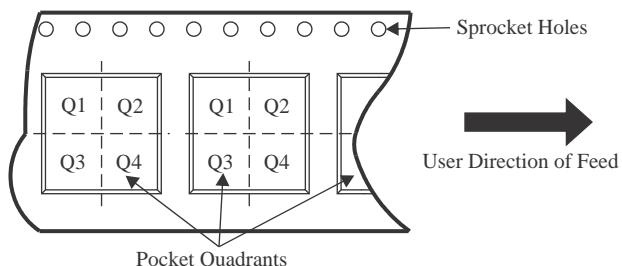
- Catalog : [CD74AC138](#)
- Military : [CD54AC138](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

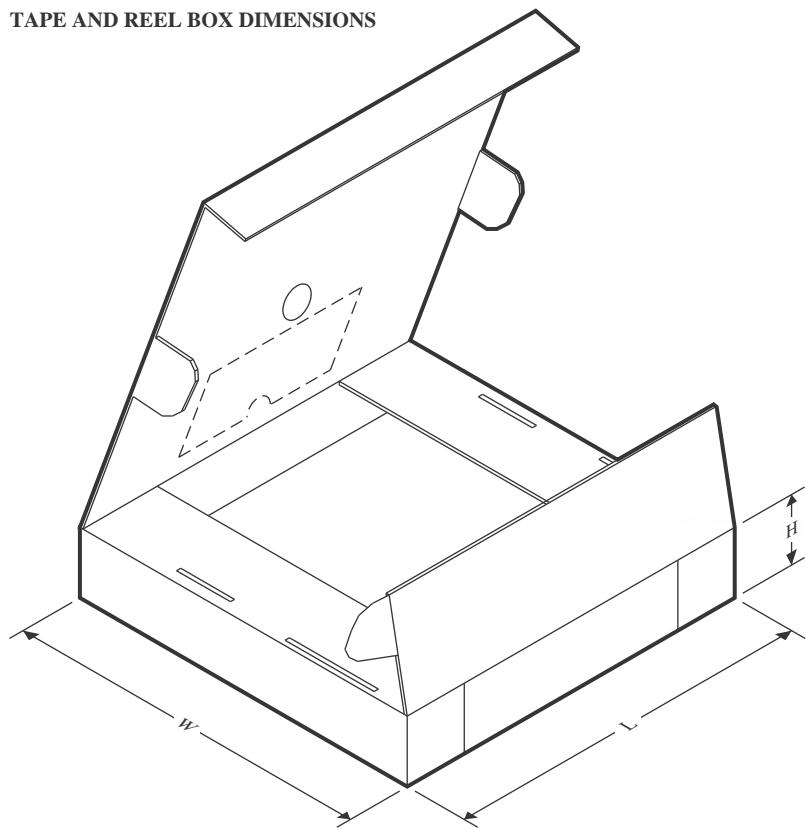
**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


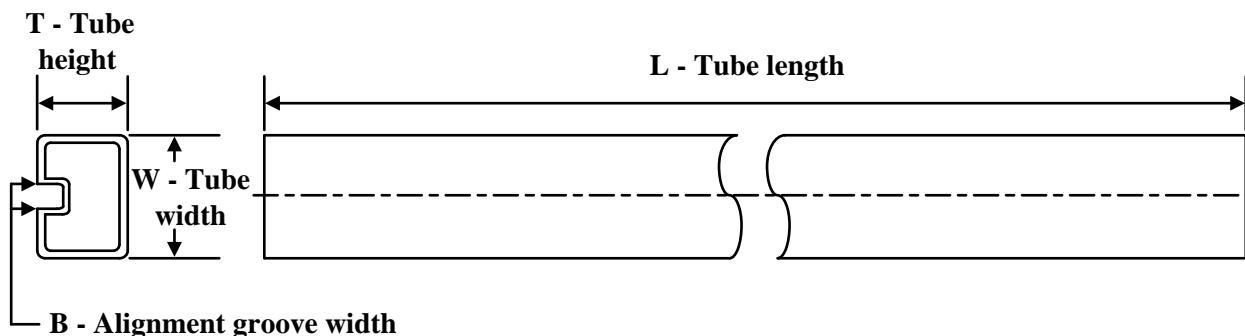
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC138BQBR	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
CD74AC138M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74AC138M96	SOIC	D	16	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
CD74AC138PWR	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74AC138PWR	TSSOP	PW	16	3000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC138BQBR	WQFN	BQB	16	3000	210.0	185.0	35.0
CD74AC138M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74AC138M96	SOIC	D	16	2500	340.5	336.1	32.0
CD74AC138PWR	TSSOP	PW	16	3000	353.0	353.0	32.0
CD74AC138PWR	TSSOP	PW	16	3000	366.0	364.0	50.0

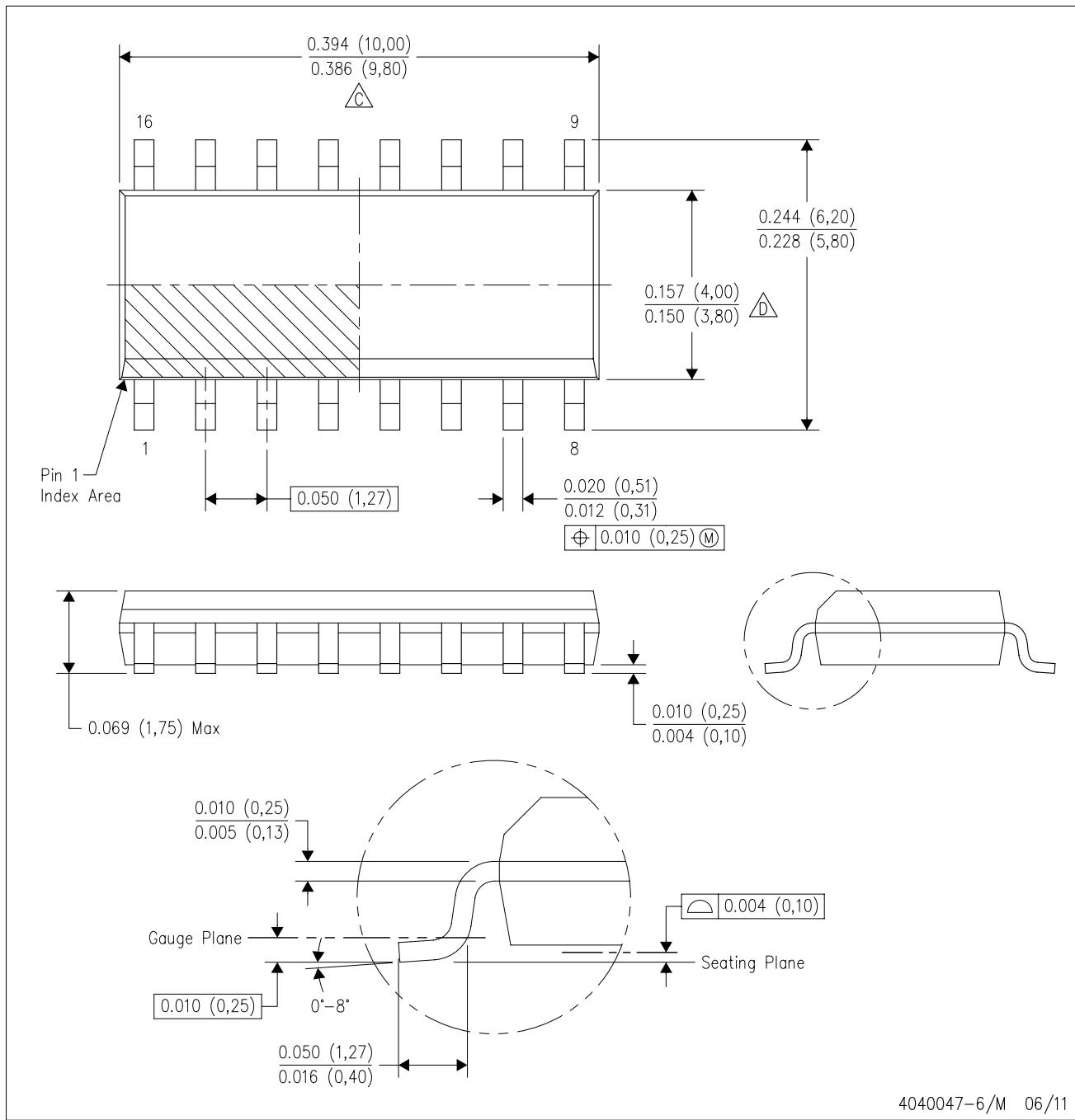
**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T ( $\mu$ m)	B (mm)
CD74AC138E	N	PDIP	16	25	506	13.97	11230	4.32
CD74AC138E	N	PDIP	16	25	506	13.97	11230	4.32
CD74AC138E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74AC138E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74AC138EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74AC138EE4	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

## GENERIC PACKAGE VIEW

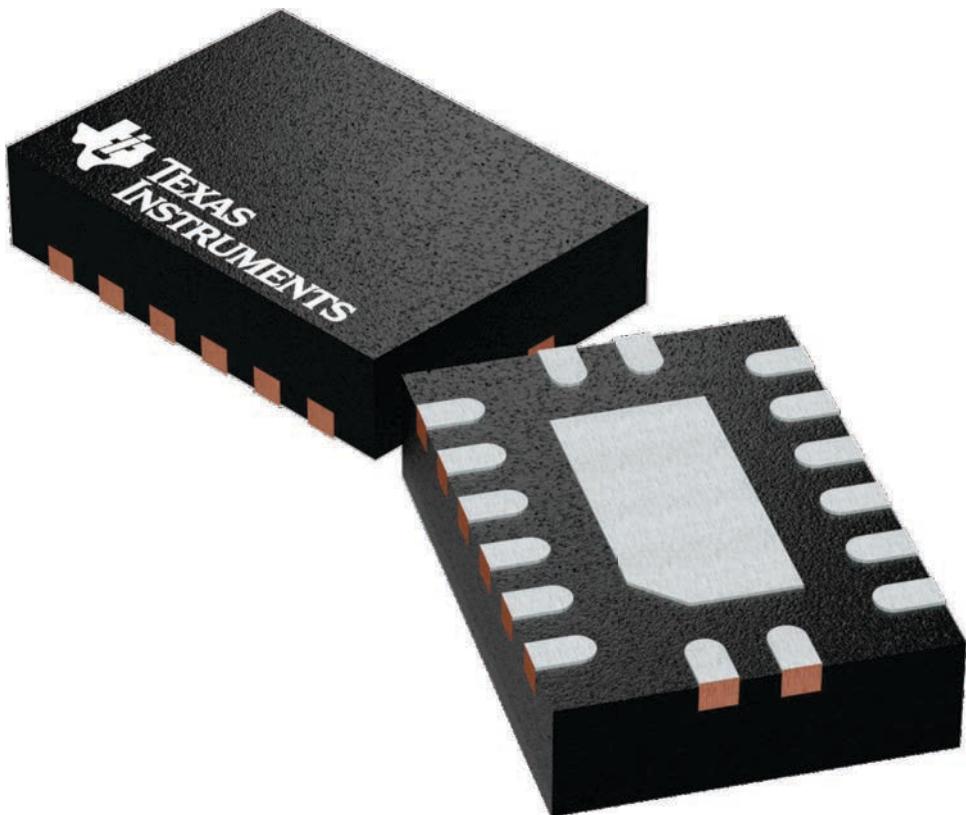
### BQB 16

### WQFN - 0.8 mm max height

2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



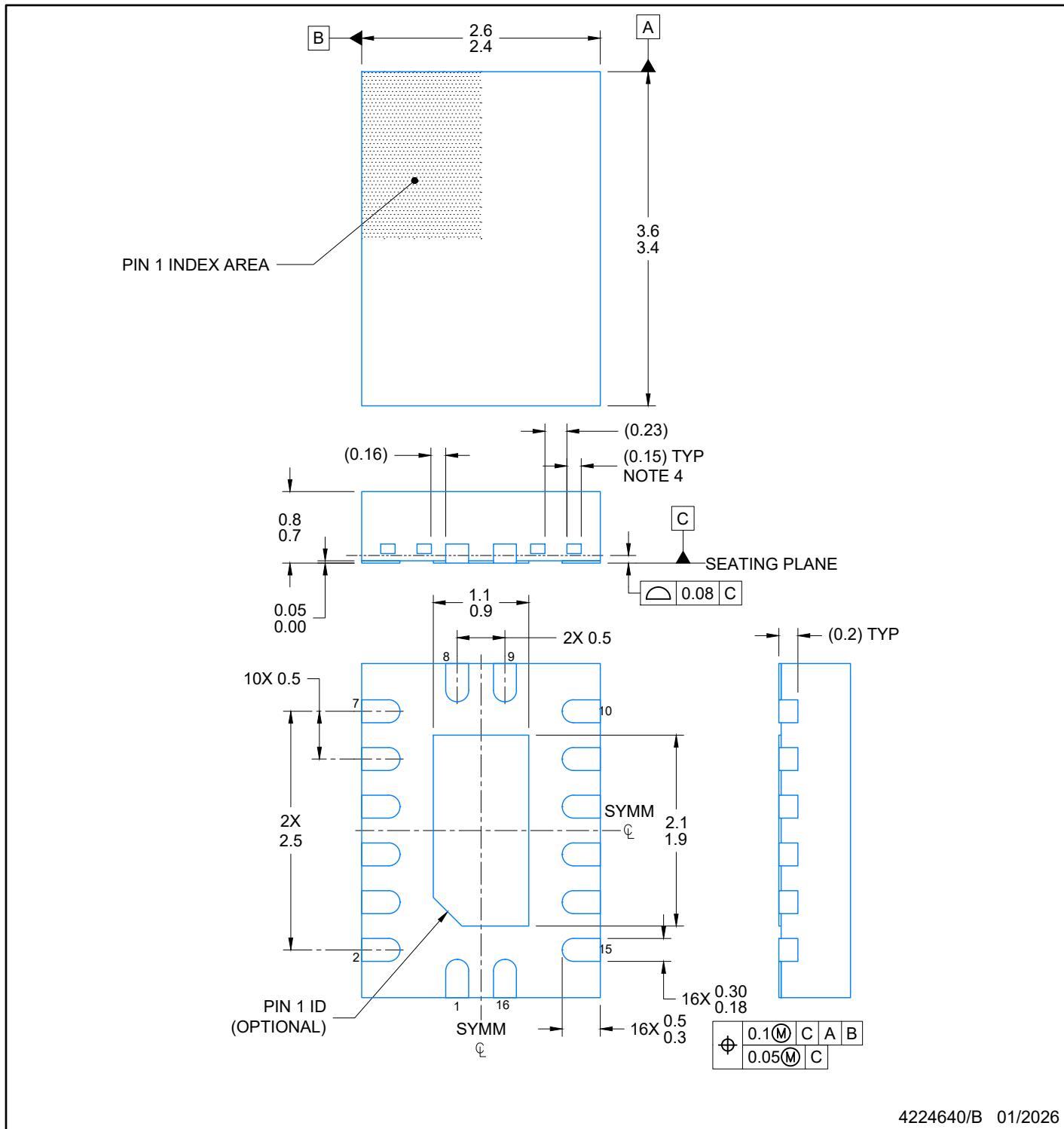
4226161/A

## PACKAGE OUTLINE

## **WQFN - 0.8 mm max height**

## PLASTIC QUAD FLAT PACK-NO LEAD

**BQB0016A**



## NOTES:

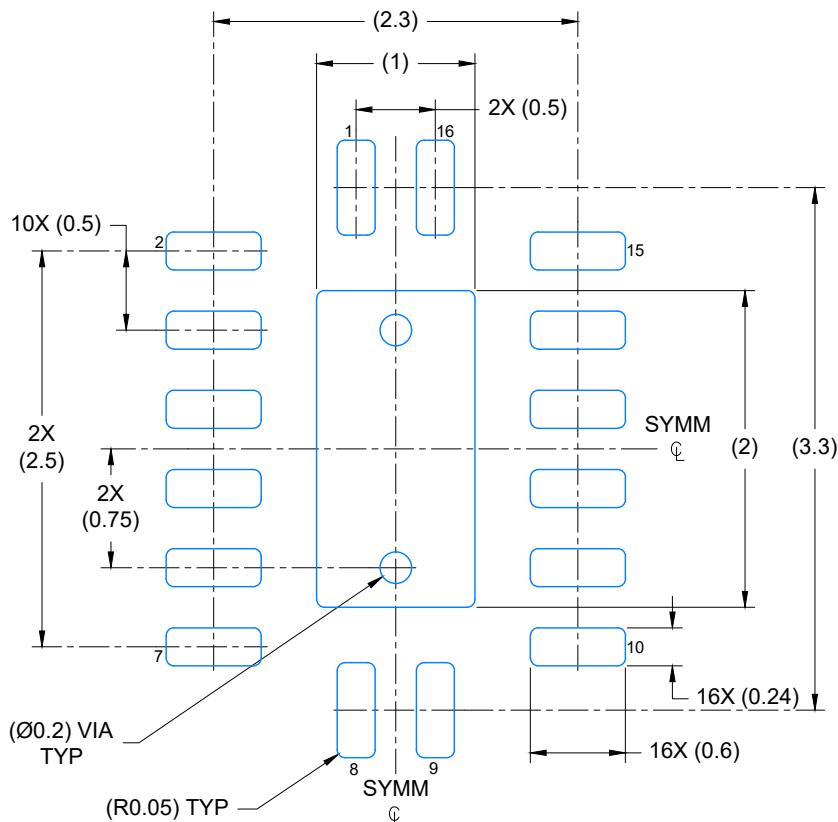
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may differ or may not be present

## EXAMPLE BOARD LAYOUT

## **WQFN - 0.8 mm max height**

## PLASTIC QUAD FLAT PACK-NO LEAD

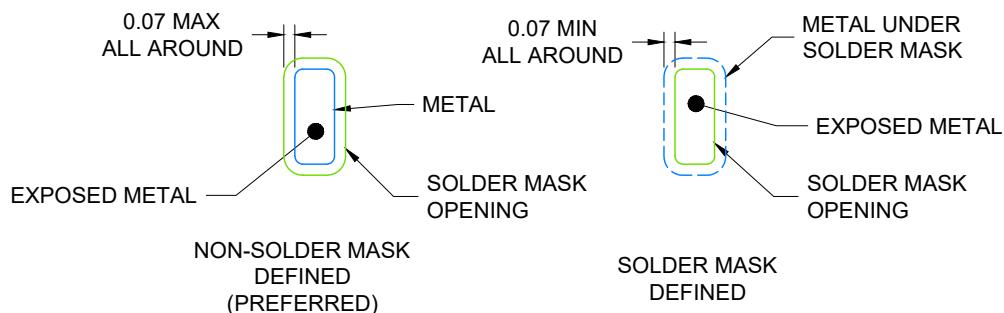
**BQB0016A**



## LAND PATTERN EXAMPLE

#### EXPOSED METAL SHOWN

SCALE: 20X



4224640/B 01/2026

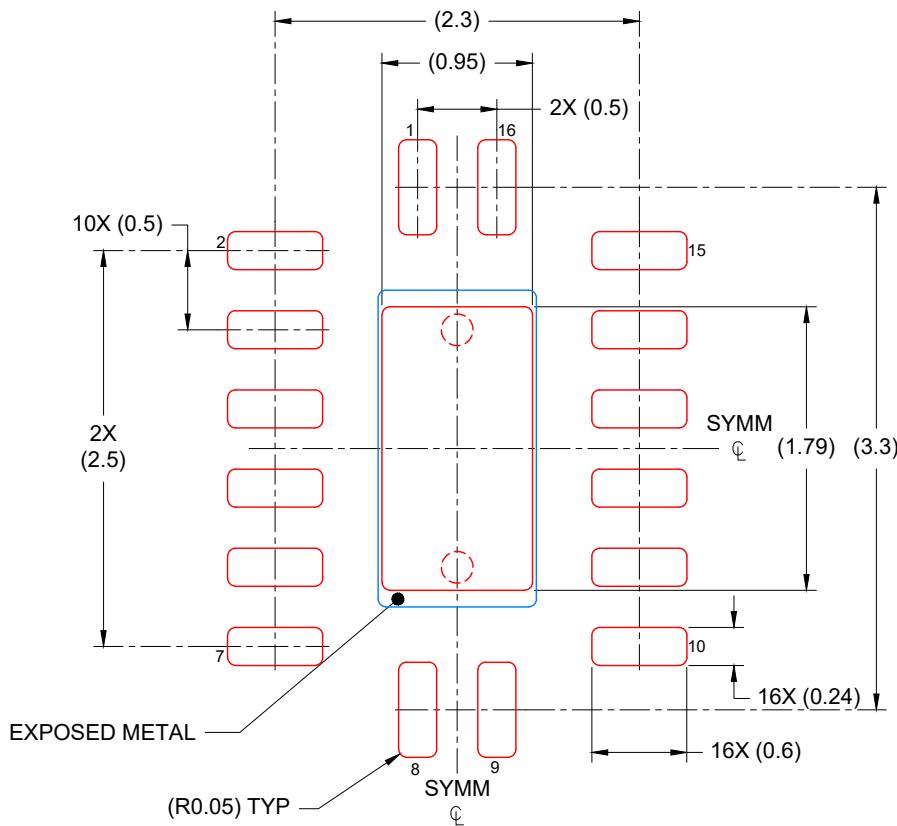
1. NOTES: (continued)
  5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
  6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

## EXAMPLE STENCIL DESIGN

## **WQFN - 0.8 mm max height**

## PLASTIC QUAD FLAT PACK-NO LEAD

**BQB0016A**



## SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
85% PRINTED COVERAGE BY AREA  
SCALE: 20X

4224640/B 01/2026

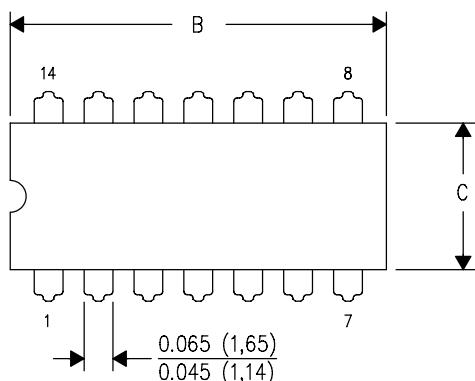
#### NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

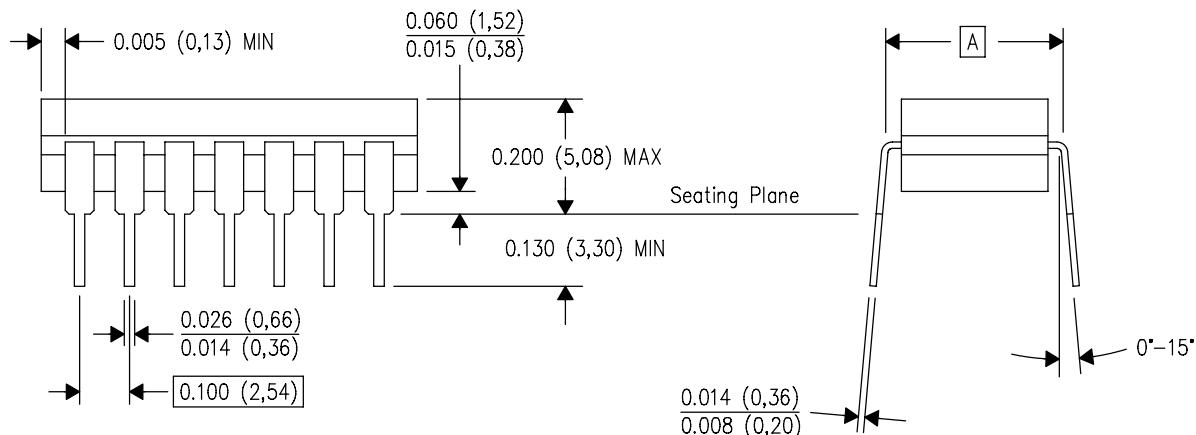
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

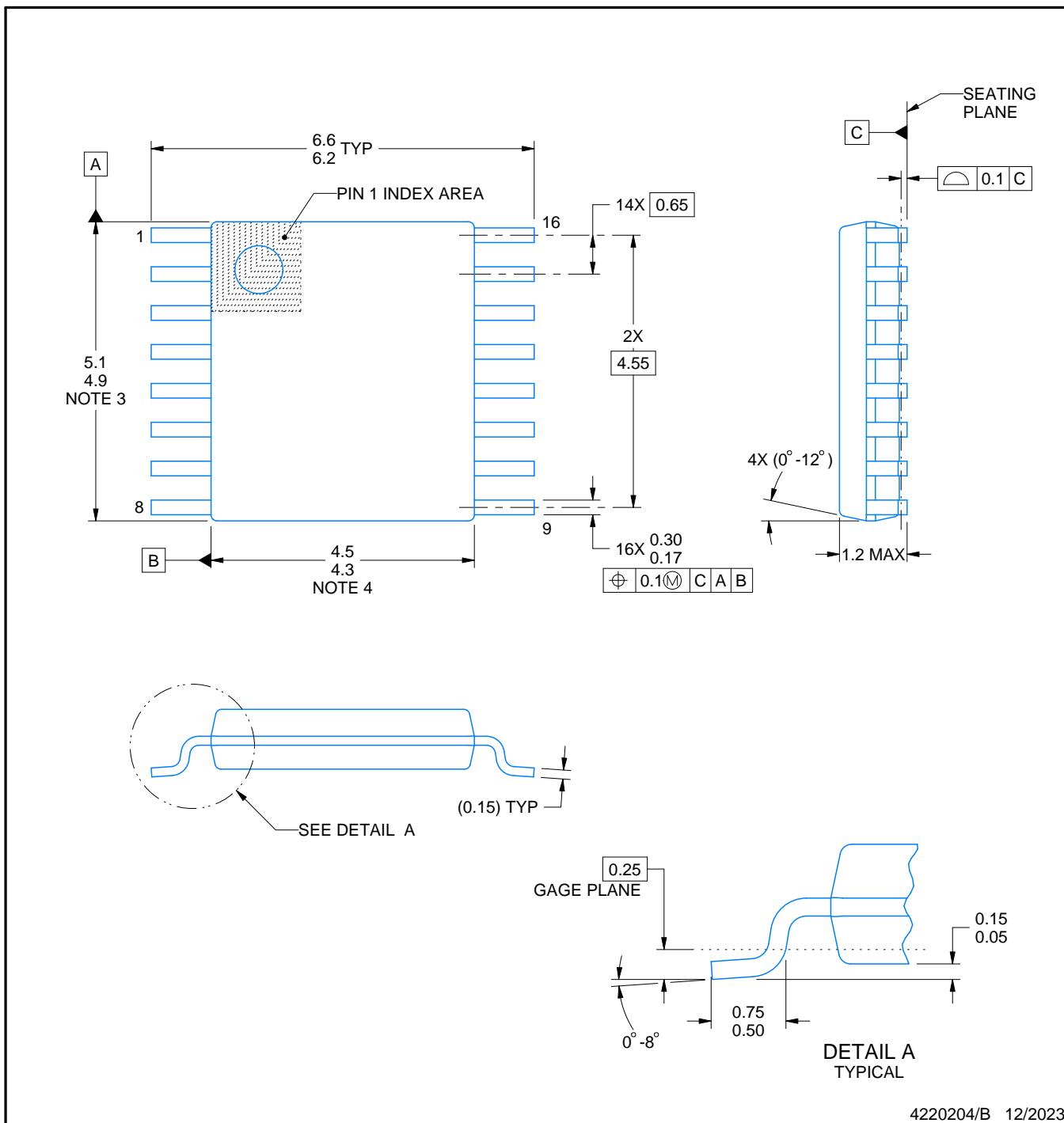
## PACKAGE OUTLINE

**PW0016A**



## **TSSOP - 1.2 mm max height**

## SMALL OUTLINE PACKAGE



## NOTES:

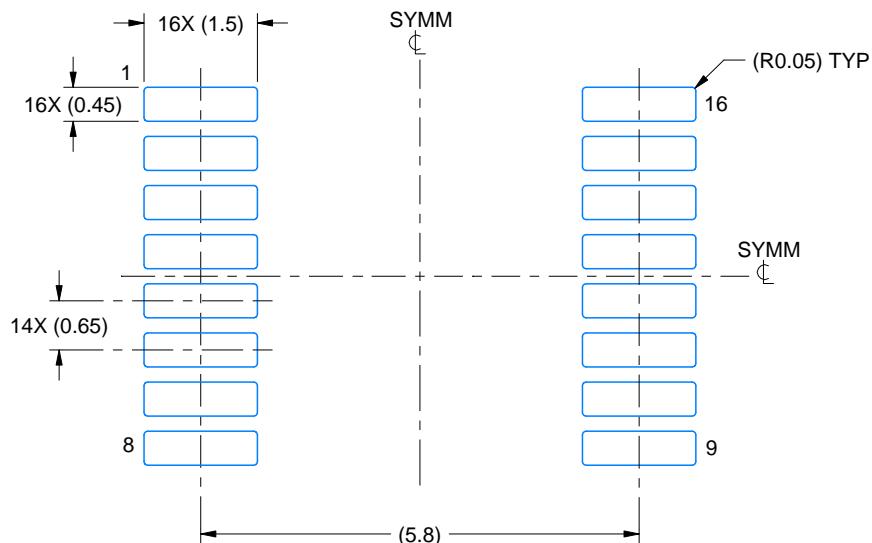
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

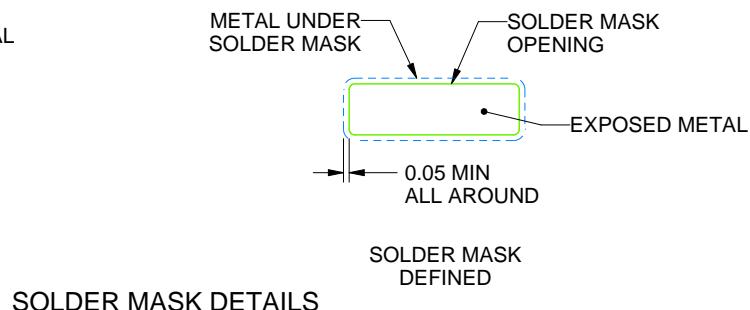
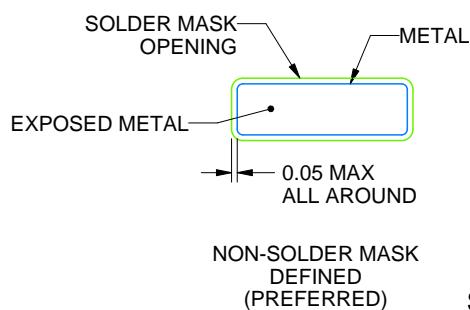
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

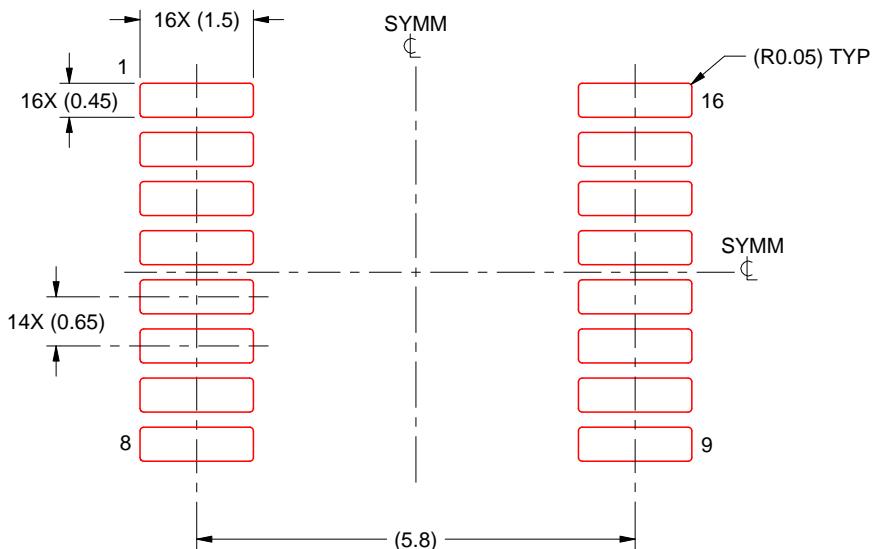
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/B 12/2023

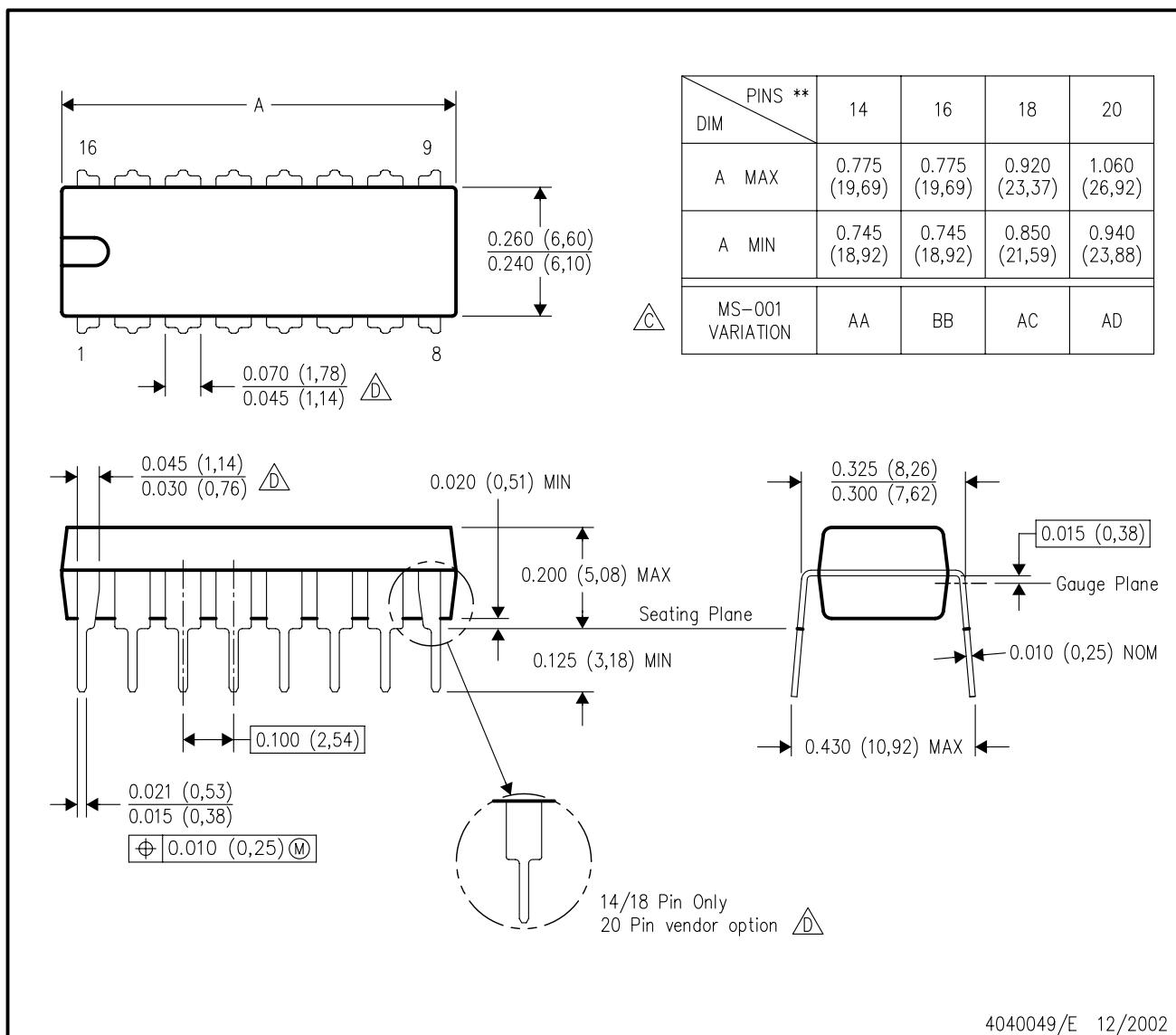
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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