

Features

- Synchronous or Asynchronous Preset
- Cascadable in Synchronous or Ripple Mode
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range ... -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_L \leq 1\mu A$ at V_{OL}, V_{OH}

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC40103F3A	-55 to 125	16 Ld CERDIP
CD74HC40103E	-55 to 125	16 Ld PDIP
CD74HC40103M	-55 to 125	16 Ld SOIC
CD74HC40103MT	-55 to 125	16 Ld SOIC
CD74HC40103M96	-55 to 125	16 Ld SOIC
CD74HCT40103E	-55 to 125	16 Ld PDIP
CD74HCT40103M	-55 to 125	16 Ld SOIC
CD74HCT40103MT	-55 to 125	16 Ld SOIC
CD74HCT40103M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

Description

The 'HC40103 and CD74HCT40103 are manufactured with high speed silicon gate technology and consist of an 8-stage synchronous down counter with a single output which is active when the internal count is zero. The 40103 contains a single 8-bit binary counter. Each has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the \overline{TC} output are active-low logic.

In normal operation, the counter is decremented by one count on each positive transition of the CLOCK (CP). Counting is inhibited when the \overline{TE} input is high. The \overline{TC} output goes low when the count reaches zero if the \overline{TE} input is low, and remains low for one full clock period.

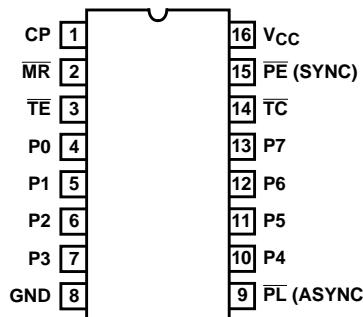
When the \overline{PE} input is low, data at the P0-P7 inputs are clocked into the counter on the next positive clock transition regardless of the state of the \overline{TE} input. When the \overline{PL} input is low, data at the P0-P7 inputs are asynchronously forced into the counter regardless of the state of the \overline{PE} , \overline{TE} , or CLOCK inputs. Input P0-P7 represent a single 8-bit binary word for the 40103. When the MR input is low, the counter is asynchronously cleared to its maximum count of 255₁₀, regardless of the state of any other input. The precedence relationship between control inputs is indicated in the truth table.

If all control inputs except \overline{TE} are high at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 100₁₆ or 256₁₀ clock pulses long.

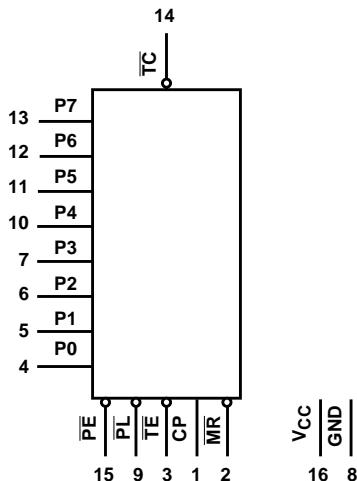
The 40103 may be cascaded using the \overline{TE} input and the \overline{TC} output, in either a synchronous or ripple mode. These circuits possess the low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits and can drive up to 10 LSTTL loads.

Pinout

**CD54HC40103
(CERDIP)
CD74HC40103, CD74HCT40103
(PDIP, SOIC)
TOP VIEW**



Functional Diagram



TRUTH TABLE

CONTROL INPUTS				PRESET MODE	ACTION
MR	PL	PE	TE		
1	1	1	1	Synchronous	Inhibit Counter
1	1	1	0		Count Down
1	1	0	X		Preset On Next Positive Clock Transition
1	0	X	X	Asynchronously	Preset Asynchronously
0	X	X	X		Clear to Maximum Count

1 = High Level.

0 = Low Level.

X = Don't Care.

Clock connected to clock input.

Synchronous Operation: changes occur on negative-to-positive clock transitions.

Load Inputs: MSB = P7, LSB = P0.

Absolute Maximum Ratings

DC Supply Voltage, V_{CC}	-0.5V to 7V
DC Input Diode Current, I_{IK} For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Diode Current, I_{OK} For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, I_O For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC V_{CC} or Ground Current, I_{CC}	$\pm 50mA$

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^{\circ}C/W$)
E (PDIP) Package	67
M (SOIC) Package	73
Maximum Junction Temperature	150 $^{\circ}C$
Maximum Storage Temperature Range	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s)	300 $^{\circ}C$
(SOIC - Lead Tips Only)	

Operating Conditions

Temperature Range, T_A	-55 $^{\circ}C$ to 125 $^{\circ}C$
Supply Voltage Range, V_{CC}	
HC Types	2V to 6V
HCT Types	4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O	0V to V_{CC}
Input Rise and Fall Time	
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS		
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
HC TYPES														
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V		
				4.5	3.15	-	-	3.15	-	3.15	-	V		
				6	4.2	-	-	4.2	-	4.2	-	V		
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V		
				4.5	-	-	1.35	-	1.35	-	1.35	V		
				6	-	-	1.8	-	1.8	-	1.8	V		
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V		
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V		
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V		
High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V		
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V		
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V		
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V		
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V		
			0.02	6	-	-	0.1	-	0.1	-	0.1	V		
Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	-	V		
			4	4.5	-	-	0.26	-	0.33	-	0.4	V		
			5.2	6	-	-	0.26	-	0.33	-	0.4	V		
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	± 0.1	-	± 1	-	± 1	μA		
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	μA		

CD54HC40103, CD74HC40103, CD74HCT40103

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT TYPES												
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I	V _{CC} and GND	0	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI _{CC} (Note 2)	V _{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTE:

2. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS (NOTE)
P0-P7	0.20
TE, MR	0.40
CP	0.60
PE	0.80
PL	1.35

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360µA max at 25°C.

Prerequisite for Switching Specifications

PARAMETER	SYMBOL	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
CP Pulse Width	t _W	2	165	-	-	205	-	250	-	ns
		4.5	33	-	-	41	-	50	-	ns
		6	28	-	-	35	-	43	-	ns
PL Pulse Width	t _W	2	125	-	-	155	-	190	-	ns
		4.5	25	-	-	31	-	38	-	ns
		6	21	-	-	26	-	32	-	ns

CD54HC40103, CD74HC40103, CD74HCT40103

Prerequisite for Switching Specifications (Continued)

PARAMETER	SYMBOL	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
MR Pulse Width	t _W	2	125	-	-	135	-	190	-	ns
		4.5	25	-	-	31	-	38	-	ns
		6	21	-	-	26	-	32	-	ns
CP Max. Frequency (Note 3)	f _{CP(MAX)}	2	3	-	-	2	-	2	-	MHz
		4.5	15	-	-	12	-	10	-	MHz
		6	18	-	-	14	-	12	-	MHz
P to CP Set-up Time	t _{SU}	2	100	-	-	125	-	150	-	ns
		4.5	20	-	-	25	-	30	-	ns
		6	17	-	-	21	-	26	-	ns
P̄E to CP Set-up Time	t _{SU}	2	75	-	-	95	-	110	-	ns
		4.5	15	-	-	19	-	22	-	ns
		6	13	-	-	16	-	19	-	ns
T̄E to CP Set-up Time	t _{SU}	2	150	-	-	190	-	225	-	ns
		4.5	30	-	-	38	-	45	-	ns
		6	26	-	-	33	-	38	-	ns
P to CP Hold Time	t _H	2	5	-	-	5	-	5	-	ns
		4.5	5	-	-	5	-	5	-	ns
		6	5	-	-	5	-	5	-	ns
T̄E to CP̄ Hold Time	t _H	2	0	-	-	0	-	0	-	ns
		4.5	0	-	-	0	-	0	-	ns
		6	0	-	-	0	-	0	-	ns
MR to CP Removal Time	t _{REM}	2	50	-	-	65	-	75	-	ns
		4.5	10	-	-	13	-	15	-	ns
		6	9	-	-	11	-	13	-	ns
P̄E to CP̄ Hold Time	t _H	2	2	-	-	2	-	2	-	ns
		4.5	2	-	-	2	-	2	-	ns
		6	2	-	-	2	-	2	-	ns
HCT TYPES										
CP Pulse Width	t _W	4.5	35	-	-	44	-	53	-	ns
PL Pulse Width	t _W	4.5	43	-	-	54	-	65	-	ns
MR Pulse Width	t _W	4.5	35	-	-	44	-	53	-	ns
CP Max. Frequency (Note 3)	f _{CP(MAX)}	4.5	14	-	-	11	-	9	-	MHz
P to CP Set-up Time	t _{SU}	4.5	24	-	-	30	-	36	-	ns
P̄E to CP Set-up Time	t _{SU}	4.5	20	-	-	25	-	30	-	ns
T̄E to CP Set-up Time	t _{SU}	4.5	40	-	-	50	-	60	-	ns
P to CP Hold Time	t _H	4.5	5	-	-	5	-	5	-	ns
T̄E to CP Hold Time	t _H	4.5	0	-	-	0	-	0	-	ns
MR to CP̄ Removal Time	t _{REM}	4.5	10	-	-	13	-	15	-	ns
P̄E to CP Hold Time	t _H	4.5	2	-	-	2	-	2	-	ns

CD54HC40103, CD74HC40103, CD74HCT40103

Switching Specifications Input $t_r, t_f = 6\text{ns}$

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay CP to any $\overline{\text{TC}}$ (Async Preset)	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	300	-	375	-	450	ns
		C _L = 50pF	4.5	-	-	60	-	75	-	90	ns
		C _L = 15pF	5	-	25	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	51	-	64	-	77	ns
CP to $\overline{\text{TC}}$ (Sync Preset)	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	300	-	375	-	450	ns
		C _L = 50pF	4.5	-	-	60	-	75	-	90	ns
		C _L = 15pF	5	-	25	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	51	-	64	-	77	ns
$\overline{\text{TE}}$ to $\overline{\text{TC}}$	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	200	-	250	-	300	ns
		C _L = 50pF	4.5	-	-	40	-	50	-	60	ns
		C _L = 15pF	5	-	17	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	34	-	43	-	51	ns
PL to $\overline{\text{TC}}$	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	275	-	345	-	415	ns
		C _L = 50pF	4.5	-	-	55	-	69	-	83	ns
		C _L = 15pF	5	-	23	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	47	-	59	-	71	ns
MR to $\overline{\text{TC}}$	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	275	-	345	-	415	ns
		C _L = 50pF	4.5	-	-	55	-	69	-	83	ns
		C _L = 15pF	5	-	23	-	-	-	-	-	ns
		C _L = 50pF	6	-	-	47	-	59	-	71	ns
Output Transition Time	t _{TLH} , t _{THL}	C _L = 50pF	2	-	-	75	-	95	-	110	ns
		C _L = 50pF	4.5	-	-	15	-	19	-	22	ns
		C _L = 50pF	6	-	-	13	-	16	-	19	ns
Input Capacitance	C _I	C _L = 50pF	-	-	-	10	-	10	-	10	pF
CP Maximum Frequency	f _{MAX}	C _L = 15pF	5	-	25	-	-	-	-	-	MHz
Power Dissipation Capacitance (Notes 4, 5)	C _{PD}	-	5	-	25	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay CP to $\overline{\text{TC}}$ (Async Preset)	t _{PLH} , t _{PHL}	C _L = 50pF	4.5	-	-	60	-	75	-	90	ns
		C _L = 15pF	5	-	25	-	-	-	-	-	ns
$\overline{\text{CE}}$ to $\overline{\text{TC}}$ (Sync Preset)	t _{PLH} , t _{PHL}	C _L = 50pF	4.5	-	-	63	-	79	-	95	ns
		C _L = 15pF	5	-	26	-	-	-	-	-	ns
$\overline{\text{TE}}$ to $\overline{\text{TC}}$	t _{PLH} , t _{PHL}	C _L = 50pF	4.5	-	-	50	-	63	-	75	ns
		C _L = 15pF	5	-	21	-	-	-	-	-	ns
PL to $\overline{\text{TC}}$	t _{PLH} , t _{PHL}	C _L = 50pF	4.5	-	-	68	-	85	-	102	ns
		C _L = 15pF	5	-	28	-	-	-	-	-	ns

Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
MR to $\overline{\text{TC}}$	t _{PLH} , t _{PHL}	C _L = 50pF	4.5	-	-	55	-	69	-	83	ns
		C _L = 15pF	5	-	23	-	-	-	-	-	ns
Output Transition Time	t _{THL} , t _{TLH}	C _L = 50pF	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	C _{IN}	C _L = 50pF	-	-	-	10	-	10	-	10	pF
CP Maximum Frequency	f _{MAX}	C _L = 15pF	5	-	25	-	-	-	-	-	MHz
Power Dissipation Capacitance (Notes 4, 5)	C _{PD}	-	5	-	27	-	-	-	-	-	pF

NOTES:

3. Noncascaded operation only. With cascaded counters clock-to-terminal count propagation delays, count enables ($\overline{\text{PE}}$ or $\overline{\text{TE}}$)-to-clock SET UP TIMES, and count enables ($\overline{\text{PE}}$ or $\overline{\text{TE}}$)-to-clock HOLD TIMES determine maximum clock frequency. For example, with these HC devices:

$$C_P f_{MAX} = \frac{1}{\text{CP-to-}\overline{\text{TC}} \text{ prop delay} + \overline{\text{TE}}\text{-to-CP Setup Time} + \overline{\text{TE}}\text{-to-CP Hold Time}} = \frac{1}{60 + 30 + 0} \approx 11\text{MHz}$$

4. C_{PD} is used to determine the dynamic power consumption, per package.

5. P_D = V_{CC}² f_i + C_L V_{CC}² f_o where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage, f_o = Output Frequency.

Timing Diagrams

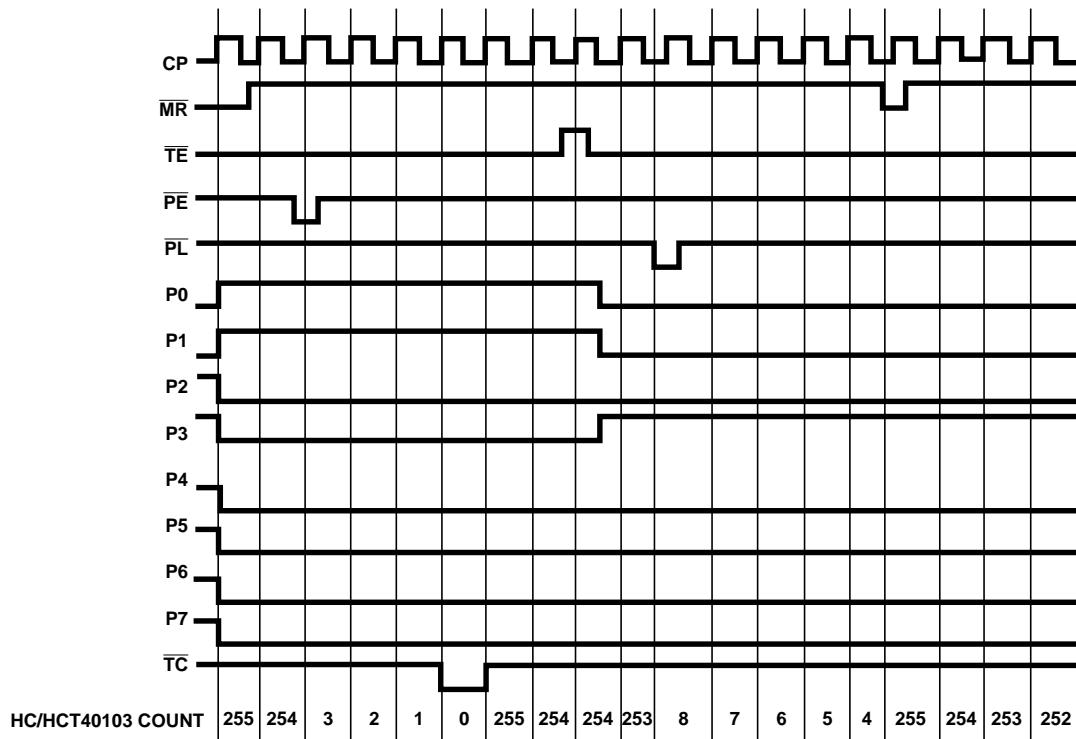


FIGURE 1.

Test Circuits and Waveforms

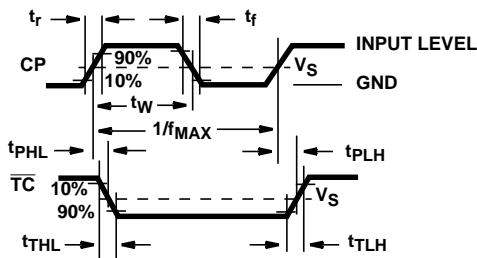


FIGURE 2.

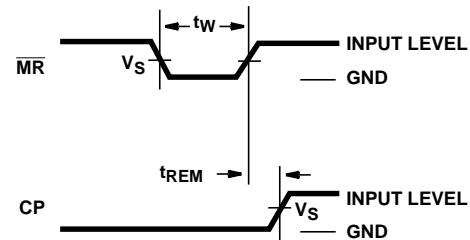


FIGURE 3.

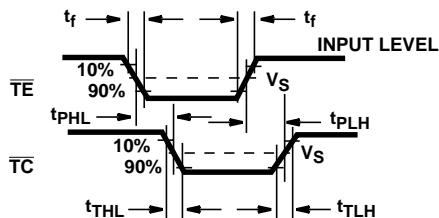


FIGURE 4.

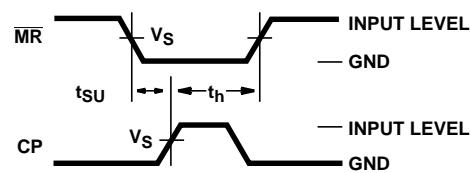


FIGURE 5.

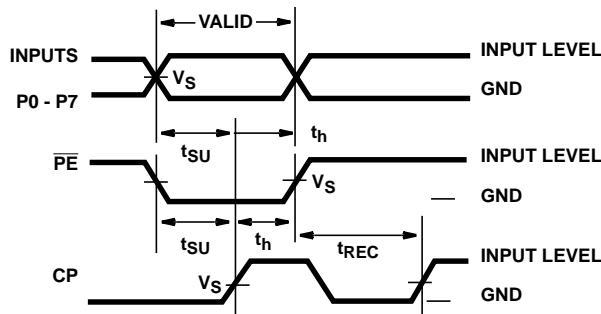


FIGURE 6.

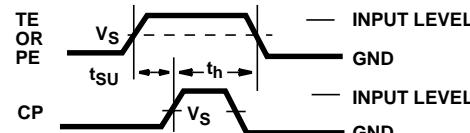
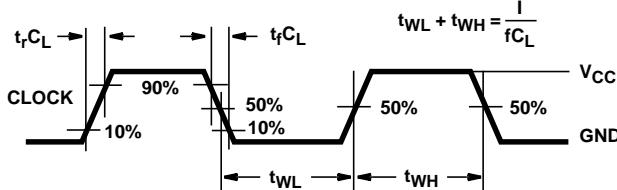
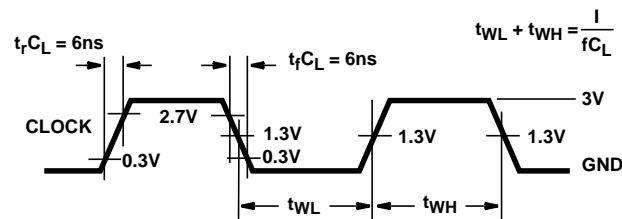


FIGURE 7.



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 8. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 9. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9055301EA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9055301EA CD54HC40103F3A
CD54HC40103F	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC40103F
CD54HC40103F.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC40103F
CD54HC40103F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9055301EA CD54HC40103F3A
CD54HC40103F3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9055301EA CD54HC40103F3A
CD74HC40103E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC40103E
CD74HC40103E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC40103E
CD74HC40103EE4	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC40103E
CD74HC40103M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HC40103M
CD74HC40103M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC40103M
CD74HC40103M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC40103M
CD74HC40103MT	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HC40103M
CD74HCT40103E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT40103E
CD74HCT40103E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT40103E
CD74HCT40103M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HCT40103M
CD74HCT40103M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT40103M
CD74HCT40103M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT40103M

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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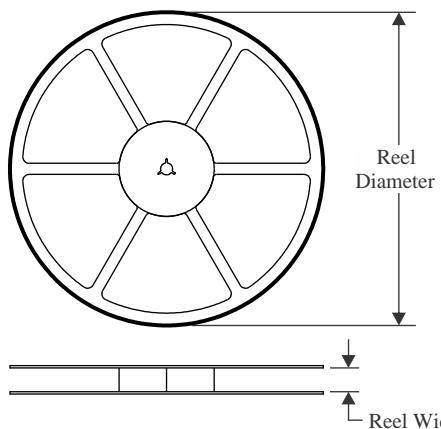
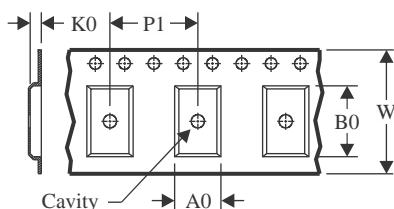
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC40103, CD74HC40103 :

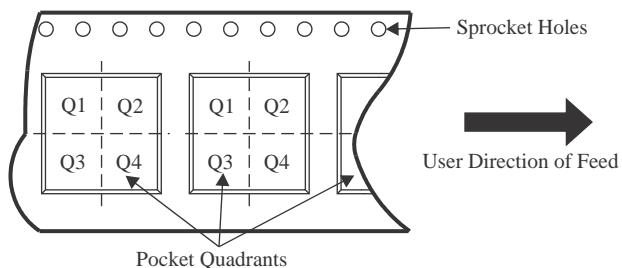
- Catalog : [CD74HC40103](#)
- Enhanced Product : [CD74HC40103-EP](#), [CD74HC40103-EP](#)
- Military : [CD54HC40103](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

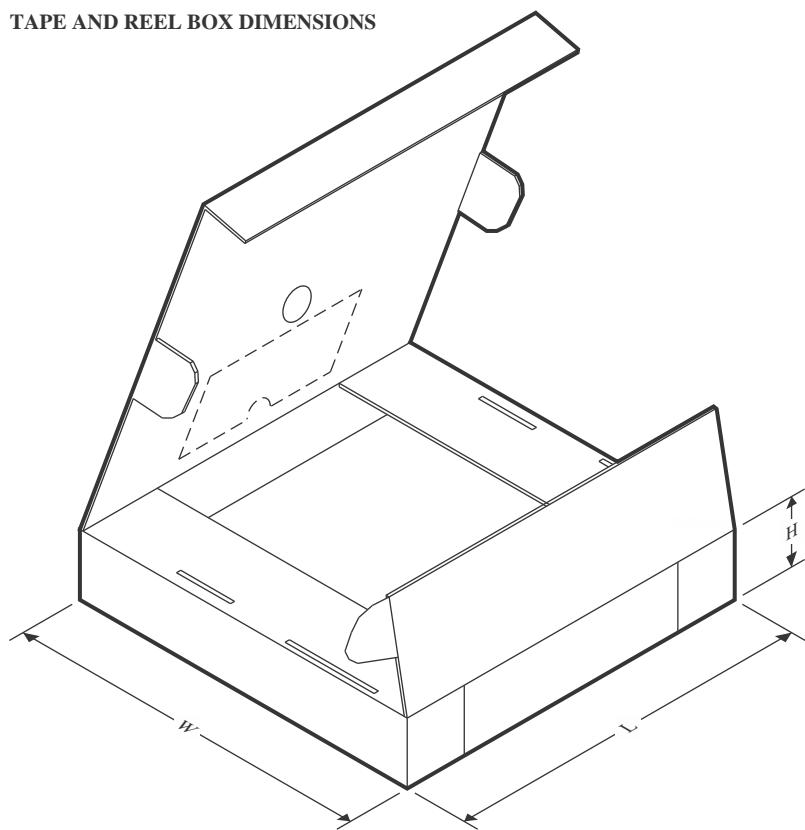
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


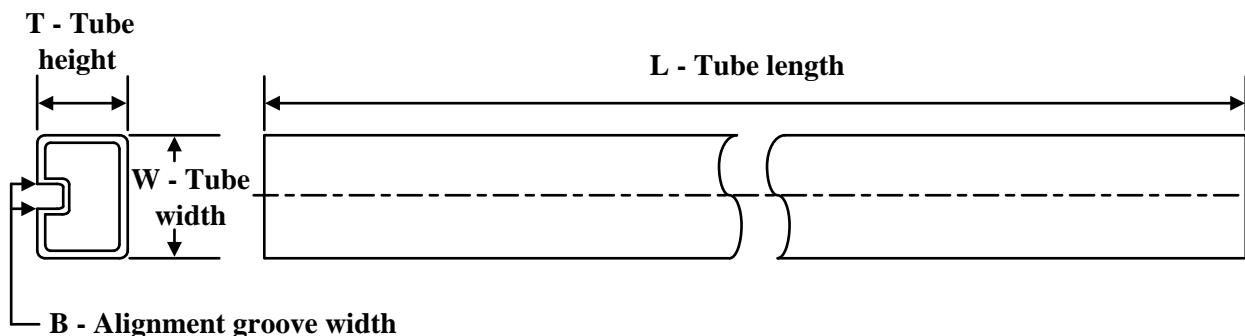
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC40103M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT40103M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC40103M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HCT40103M96	SOIC	D	16	2500	353.0	353.0	32.0

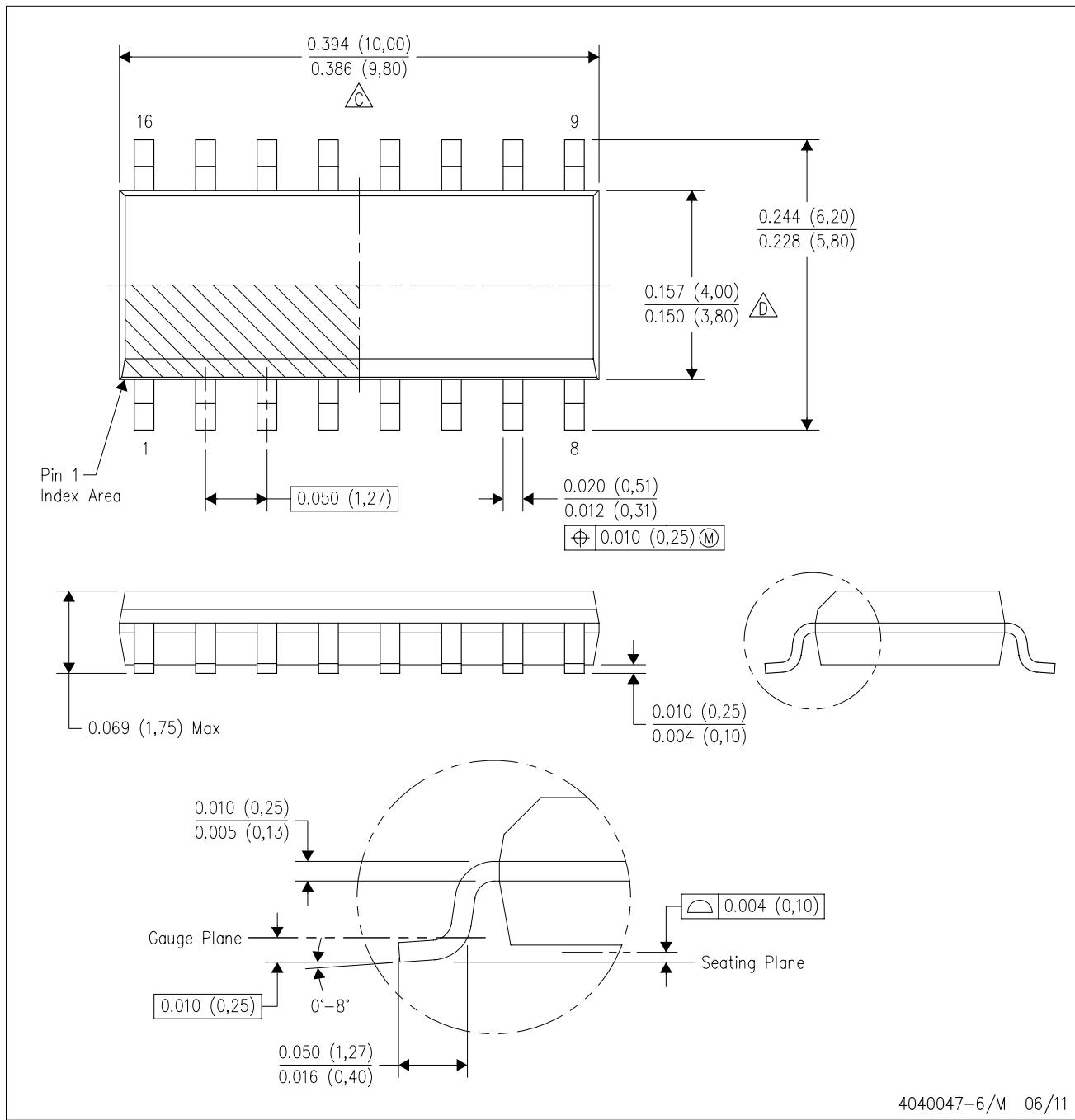
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
CD74HC40103E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC40103E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC40103E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC40103E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC40103EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC40103EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT40103E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT40103E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT40103E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT40103E.A	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

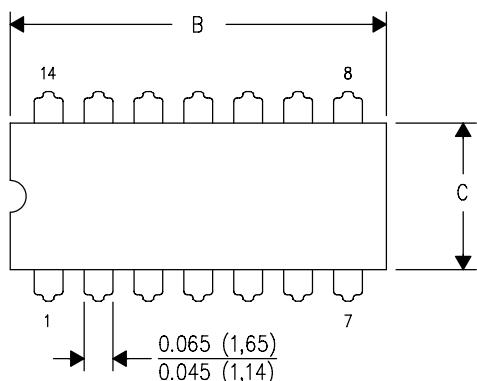
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

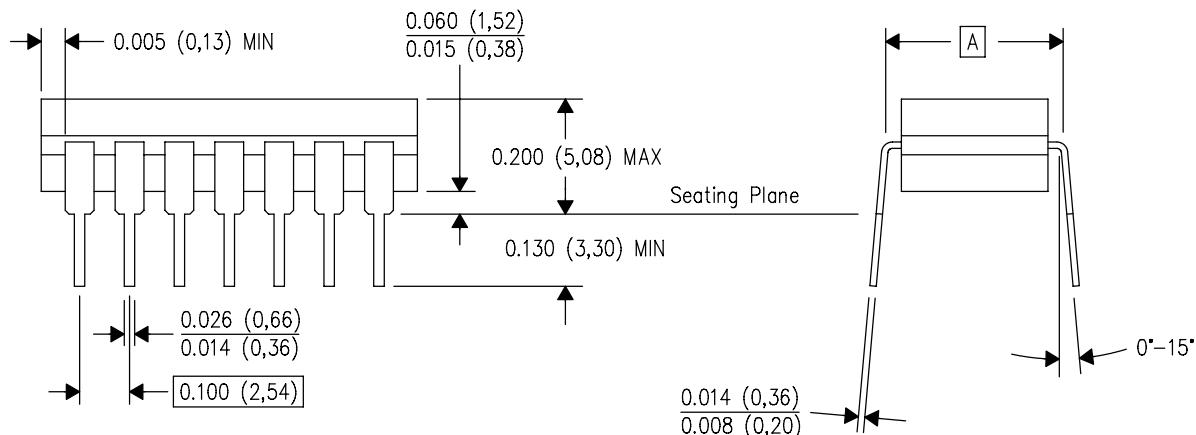
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



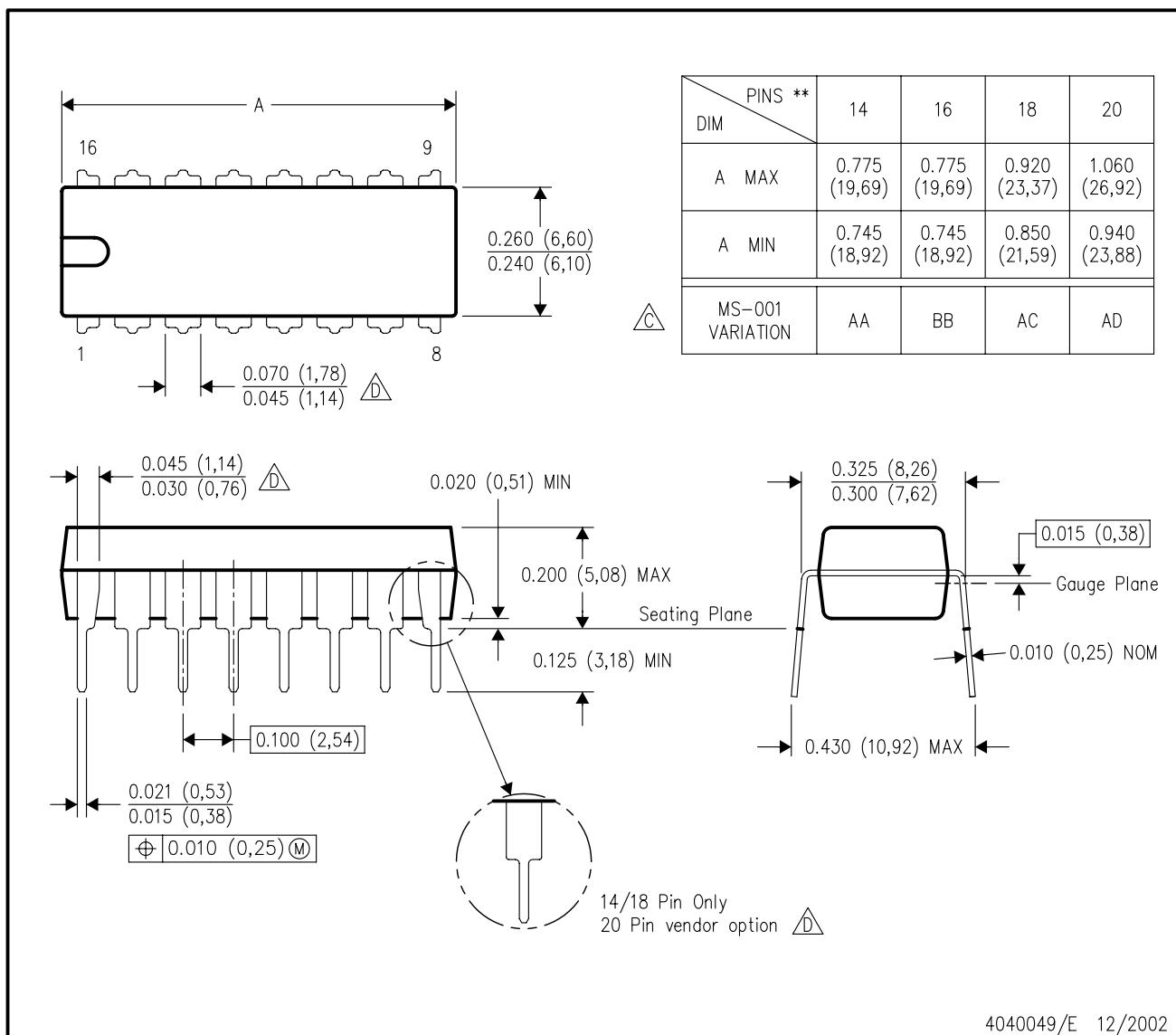
4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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