

Features

- Independent Asynchronous Inputs and Outputs
- Expandable in Either Direction
- Reset Capability
- Status Indicators on Inputs and Outputs
- Three-State Outputs
- Shift-Out Independent of Three-State Control
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

Applications

- Bit-Rate Smoothing
- CPU/Terminal Buffering
- Data Communications
- Peripheral Buffering
- Line Printer Input Buffers
- Auto-Dialers
- CRT Buffer Memories
- Radar Data Acquisition

Description

The 'HC40105 and 'HCT40105 are high-speed silicon-gate CMOS devices that are compatible, except for "shift-out" circuitry, with the CD40105B. They are low-power first-in-out (FIFO) "elastic" storage registers that can store 16 four-bit words. The 40105 is capable of handling input and output data at different shifting rates. This feature makes it particularly useful as a buffer between asynchronous systems.

Each work position in the register is clocked by a control flip-flop, which stores a marker bit. A "1" signifies that the position's data is filled and a "0" denotes a vacancy in that position. The control flip-flop detects the state of the preceding flip-flop and communicates its own status to the succeeding flip-flop. When a control flip-flop is in the "0" state and sees a "1" in the preceding flip-flop, it generates a clock pulse that transfers data from the preceding four data latches into its own four data latches and resets the preceding flip-flop to "0". The first and last control flip-flops have buffered outputs. Since all empty locations "bubble" automatically to the input end, and all valid data ripple through to the output end, the status of the first control flip-flop (DATA-IN READY) indicates if the FIFO is full, and the status of the last flip-flop (DATA-OUT READY) indicates if the FIFO contains data. As the earliest data are removed from the bottom of the data stack (the output end), all data entered later will automatically propagate (ripple) toward the output.

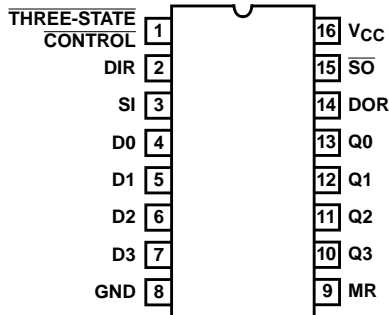
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC40105F3A	-55 to 125	16 Ld CERDIP
CD54HCT40105F3A	-55 to 125	16 Ld CERDIP
CD74HC40105E	-55 to 125	16 Ld PDIP
CD74HC40105M	-55 to 125	16 Ld SOIC
CD74HC40105MT	-55 to 125	16 Ld SOIC
CD74HC40105M96	-55 to 125	16 Ld SOIC
CD74HCT40105E	-55 to 125	16 Ld PDIP
CD74HCT40105M	-55 to 125	16 Ld SOIC
CD74HCT40105MT	-55 to 125	16 Ld SOIC
CD74HCT40105M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

Pinout

CD54HC40105, CD54HCT40105
(CERDIP)
CD74HC40105, CD74HCT40105
(PDIP, SOIC)
TOP VIEW



Loading Data

Data can be entered whenever the DATA-IN READY (DIR) flag is high, by a low to high transition on the SHIFT-IN (SI) input. This input must go low momentarily before the next word is accepted by the FIFO. The DIR flag will go low momentarily, until the data have been transferred to the second location. The flag will remain low when all 16-word locations are filled with valid data, and further pulses on the SI input will be ignored until DIR goes high.

Unloading Data

As soon as the first word has rippled to the output, the data-out ready output (DOR) goes HIGH and data of the first word is available on the outputs. Data of other words can be removed by a negative-going transition on the shift-out input (SO). This negative-going transition causes the DOR signal to go LOW while the next word moves to the output. As long as valid data is available in the FIFO, the DOR signal will go high again, signifying that the next word is ready at the output. When the FIFO is empty, DOR will remain LOW, and any further commands will be ignored until a "1" marker ripples down to the last control register and DOR goes HIGH. If during unloading SI is HIGH, (FIFO is full) data on the data input of the FIFO is entered in the first location.

Master Reset

A high on the MASTER RESET (MR) sets all the control logic marker bits to "0". DOR goes low and DIR goes high. The contents of the data register are not changed, only declared invalid, and will be superseded when the first word is loaded. Thus, MR does not clear data within the register but only the control logic. If the shift-in flag (SI) is HIGH during the master reset pulse, data present at the input (D0 to D3) are immediately moved into the first location upon completion of the reset process.

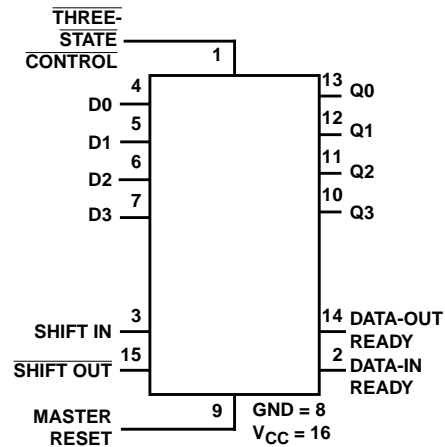
Three-State Outputs

In order to facilitate data busing, three-state outputs (Q0 to Q3) are provided on the data output lines, while the load condition of the register can be detected by the state of the DOR output. A HIGH on the three-state control flag (output enable input OE) forces the outputs into the high-impedance OFF-state mode. Note that the shift-out signal, unlike that in the CD40105B, is independent of the three-state output control. In the CD40105B, the three-state control must not be shifted from High to Low when the shift-out signal is Low (data loss would occur). In the high-speed CMOS version this restriction has been eliminated.

Cascading

The 40105 can be cascaded to form longer registers simply by connecting the DIR to SO and DOR to SI. In the cascaded mode, a MASTER RESET pulse must be applied after the supply voltage is turned on. For words wider than four bits, the DIR and the DOR outputs must be gated together with AND gates. Their outputs drive the SI and SO inputs in parallel, if expanding is done in both directions (see Figures 12 and 13).

Functional Diagram



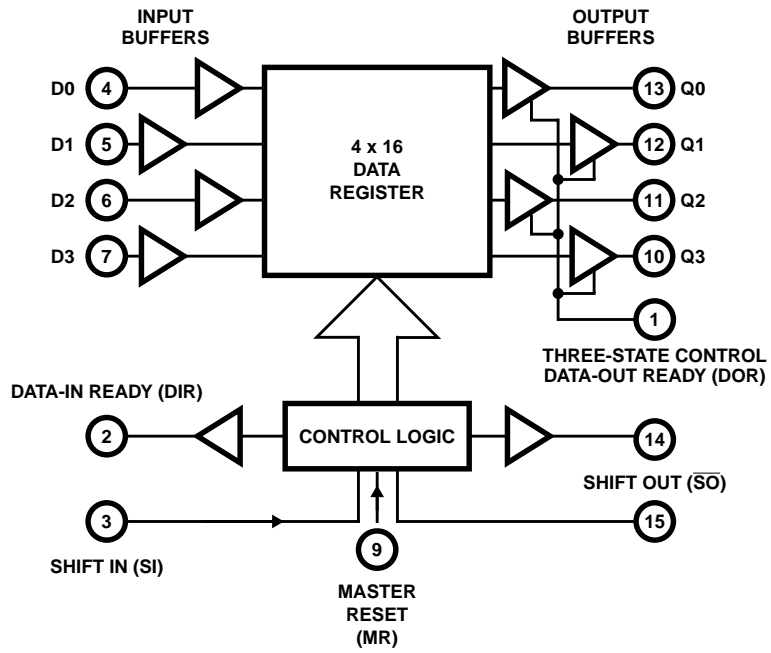
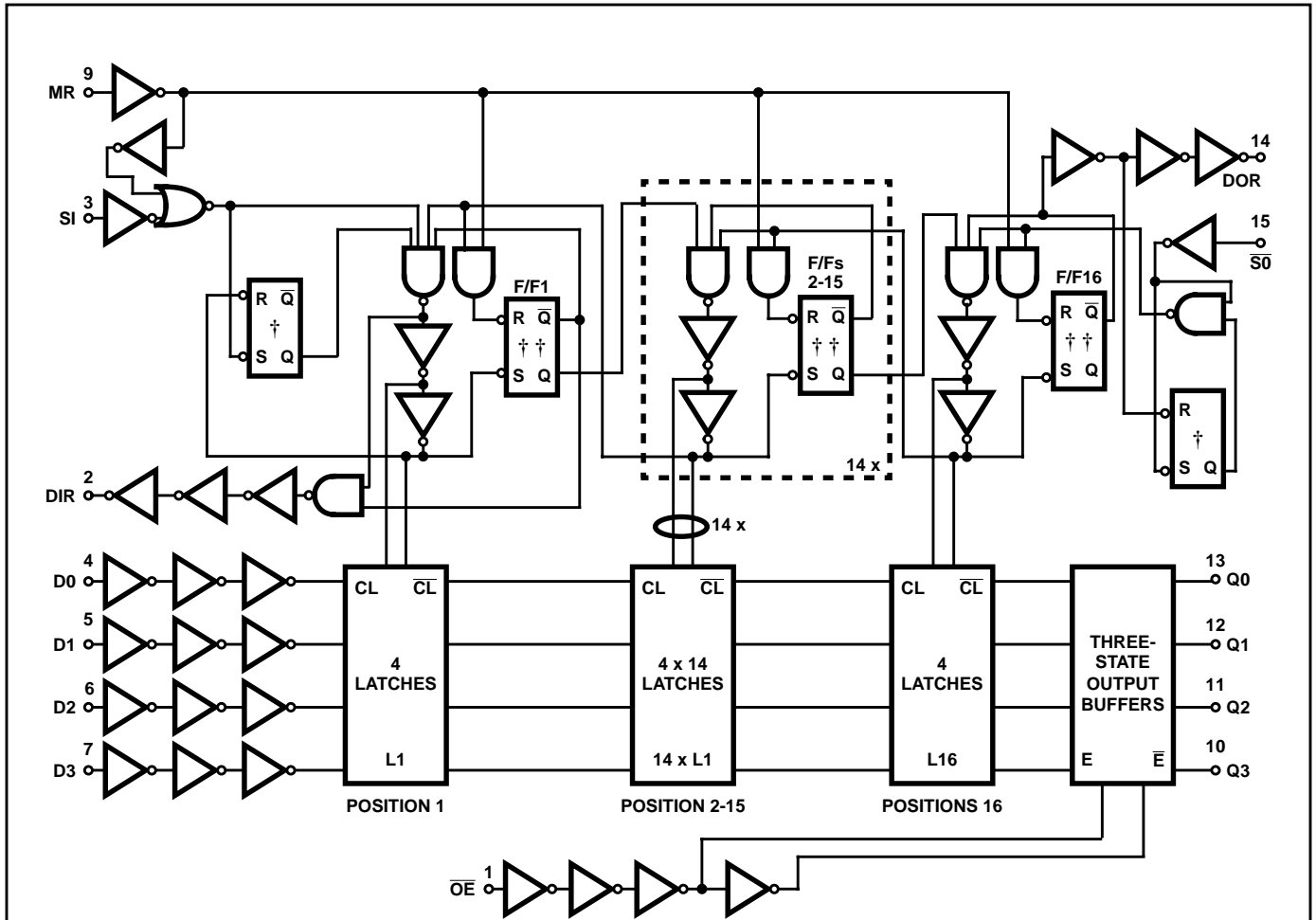


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM

CD54HC40105, CD74HC40105, CD54HCT40105, CD74HCT40105



† "S" overrides "R".
 †† "R" overrides "S".

FIGURE 2. LOGIC DIAGRAM

CD54HC40105, CD74HC40105, CD54HCT40105, CD74HCT40105

Absolute Maximum Ratings

DC Supply Voltage, V_{CC}	-0.5V to 7V
DC Input Diode Current, I_{IK}	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Diode Current, I_{OK}	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, I_O	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC V_{CC} or Ground Current, I_{CC}	$\pm 50mA$

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
E (PDIP) Package	67
M (SOIC) Package	73
Maximum Junction Temperature	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C (SOIC - Lead Tips Only)

Operating Conditions

Temperature Range (T_A)	-55°C to 125°C
Supply Voltage Range, V_{CC}	
HC Types2V to 6V
HCT Types4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O	0V to V_{CC}
Input Rise and Fall Time	
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS	
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX		
HC TYPES													
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V	
				4.5	3.15	-	-	3.15	-	3.15	-	V	
				6	4.2	-	-	4.2	-	4.2	-	V	
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V	
				4.5	-	-	1.35	-	1.35	-	1.35	V	
				6	-	-	1.8	-	1.8	-	1.8	V	
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V	
				4.5	4.4	-	-	4.4	-	4.4	-	V	
				6	5.9	-	-	5.9	-	5.9	-	V	
High Level Output Voltage TTL Loads	V_{OH}	V_{IH} or V_{IL}	-	-	-	-	-	-	-	-	-	V	
				-4	4.5	3.98	-	-	3.84	-	3.7	-	V
				-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V	
				4.5	-	-	0.1	-	0.1	-	0.1	V	
				6	-	-	0.1	-	0.1	-	0.1	V	
Low Level Output Voltage TTL Loads	V_{OL}	V_{IH} or V_{IL}	-	-	-	-	-	-	-	-	-	V	
				4	4.5	-	-	0.26	-	0.33	-	0.4	V
				5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	± 0.1	-	± 1	-	± 1	μA	
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	μA	

CD54HC40105, CD74HC40105, CD54HCT40105, CD74HCT40105

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Three-State Leakage Current	I _{OZ}	V _{IL} or V _{IH}	V _O = V _{CC} or GND	6	-	-	±0.5	-	±5	-	±10	μA
HCT TYPES												
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IH} or V _{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I	V _{CC} and GND	0	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	5.5	-	-	8	-	80	-	160	μA
Three-State Leakage Current	I _{OZ}	V _{IL} or V _{IH}	V _O = V _{CC} or GND	5.5	-	-	±0.5	-	±5	-	±10	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI _{CC} (Note 2)	V _{CC} -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

2. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
\overline{OE}	0.75
SI, \overline{SO}	0.4
Dn	0.3
MR	1.5

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g., 360μA max at 25°C.

CD54HC40105, CD74HC40105, CD54HCT40105, CD74HCT40105

Prerequisite for Switching Specifications

PARAMETER	SYMBOL	V _{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
HC TYPES									
SI Pulse Width HIGH or LOW	t _W	2	80	-	100	-	120	-	ns
		4.5	16	-	20	-	24	-	ns
		6	14	-	17	-	20	-	ns
S _O Pulse Width HIGH or LOW	t _W	2	120	-	150	-	180	-	ns
		4.5	24	-	30	-	36	-	ns
		6	20	-	26	-	31	-	ns
DIR Pulse Width HIGH or LOW	t _W	2	200	-	250	-	300	-	ns
		4.5	40	-	50	-	60	-	ns
		6	34	-	43	-	51	-	ns
DOR Pulse Width HIGH or LOW	t _W	2	200	-	250	-	300	-	ns
		4.5	40	-	50	-	60	-	ns
		6	34	-	43	-	51	-	ns
MR Pulse Width HIGH	t _W	2	120	-	150	-	180	-	ns
		4.5	24	-	30	-	36	-	ns
		6	20	-	26	-	31	-	ns
Removal Time MR to SI	t _{REM}	2	50	-	65	-	75	-	ns
		4.5	10	-	13	-	15	-	ns
		6	9	-	11	-	13	-	ns
Set-Up Time Dn to SI	t _{SU}	2	5	-	5	-	5	-	ns
		4.5	5	-	5	-	5	-	ns
		6	5	-	5	-	5	-	ns
Hold Time Dn to SI	t _H	2	125	-	155	-	190	-	ns
		4.5	25	-	31	-	38	-	ns
		6	21	-	26	-	32	-	ns
Maximum Pulse Frequency SI, S _O	f _{MAX}	2	3	-	2	-	2	-	MHz
		4.5	15	-	12	-	10	-	MHz
		6	18	-	14	-	12	-	MHz
HCT TYPES									
SI Pulse Width HIGH or LOW	t _W	4.5	16	-	20	-	24	-	ns
S _O Pulse Width HIGH or LOW	t _W	4.5	16	-	20	-	24	-	ns
DIR Pulse Width HIGH or LOW	t _W	4.5	40	-	50	-	60	-	ns
DOR Pulse Width HIGH or LOW	t _W	4.5	40	-	50	-	60	-	ns
MR Pulse Width HIGH	t _W	4.5	24	-	30	-	36	-	ns
Removal Time MR to SI	t _{REM}	4.5	15	-	19	-	22	-	ns
Set-Up Time Dn to SI	t _{SU}	4.5	0	-	0	-	0	-	ns
Hold Time Dn to SI	t _H	4.5	25	-	31	-	38	-	ns
Maximum Pulse Frequency SI, S _O	f _{MAX}	4.5	15	-	12	-	10	-	MHz

CD54HC40105, CD74HC40105, CD54HCT40105, CD74HCT40105

Switching Specifications Input $t_r, t_f = 6\text{ns}$

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay MR to DIR, DOR	t_{PHL}, t_{PLH}	$C_L = 50\text{pF}$	2	-	-	175	-	220	-	265	ns
		$C_L = 50\text{pF}$	4.5	-	-	35	-	44	-	53	ns
		$C_L = 15\text{pF}$	5	-	15	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	30	-	37	-	45	ns
SI to DIR	t_{PHL}, t_{PLH}	$C_L = 50\text{pF}$	2	-	-	210	-	265	-	315	ns
		$C_L = 50\text{pF}$	4.5	-	-	42	-	53	-	63	ns
		$C_L = 15\text{pF}$	5	-	18	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	36	-	45	-	54	ns
$\overline{S}\overline{O}$ to DOR	t_{PHL}, t_{PLH}	$C_L = 50\text{pF}$	2	-	-	210	-	265	-	315	ns
		$C_L = 50\text{pF}$	4.5	-	-	42	-	53	-	63	ns
		$C_L = 15\text{pF}$	5	-	18	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	36	-	45	-	54	ns
$\overline{S}\overline{O}$ to Qn	t_{PHL}, t_{PLH}	$C_L = 50\text{pF}$	2	-	-	400	-	500	-	600	ns
		$C_L = 50\text{pF}$	4.5	-	-	80	-	100	-	120	ns
		$C_L = 15\text{pF}$	5	-	35	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	68	-	85	-	102	ns
Propagation Delay/Ripple thru Delay SI to DOR	t_{PLH}	$C_L = 50\text{pF}$	2	-	-	2000	-	2500	-	3000	ns
			4.5	-	-	400	-	500	-	600	ns
			6	-	-	340	-	425	-	510	ns
Propagation Delay/Ripple thru Delay $\overline{S}\overline{O}$ to DIR	t_{PLH}	$C_L = 50\text{pF}$	2	-	-	2500	-	3125	-	3750	ns
			4.5	-	-	500	-	625	-	750	ns
			6	-	-	425	-	532	-	638	ns
Propagation Delay/Ripple thru Delay SI to Qn	t_{PLH}	$C_L = 50\text{pF}$	2	-	-	1500	-	1900	-	2250	ns
			4.5	-	-	300	-	380	-	450	ns
			6	-	-	260	-	330	-	380	ns
Three-State Output Enable $\overline{O}\overline{E}$ to Qn	t_{PZH}, t_{PZL}	$C_L = 50\text{pF}$	2	-	-	150	-	190	-	225	ns
			4.5	-	-	30	-	38	-	45	ns
			6	-	-	26	-	33	-	38	ns
Three-State Output Disable $\overline{O}\overline{E}$ to Qn	t_{PHZ}, t_{PLZ}	$C_L = 50\text{pF}$	2	-	-	140	-	175	-	210	ns
			4.5	-	-	28	-	35	-	42	ns
			6	-	-	24	-	30	-	36	ns
Output Transition Time	t_{TLH}, t_{THL}	$C_L = 50\text{pF}$	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Maximum SI, $\overline{S}\overline{O}$ Frequency	f_{MAX}	$C_L = 15\text{pF}$	5	-	32	-	-	-	-	MHz	
Input Capacitance	C_{IN}	$C_L = 50\text{pF}$	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	$C_L = 15\text{pF}$	5	-	83	-	-	-	-	-	pF

CD54HC40105, CD74HC40105, CD54HCT40105, CD74HCT40105

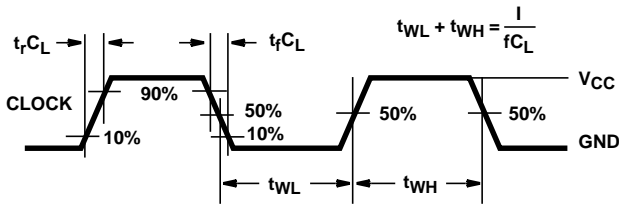
Switching Specifications Input t_r , $t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Three-State Output Capacitance	C_O	$C_L = 50\text{pF}$	-	-	-	15	-	15	-	15	pF
HCT TYPES											
Propagation Delay Time MR to DIR, DOR	t_{PLH} , t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	36	-	45	-	54	ns
		$C_L = 15\text{pF}$	5	-	15	-	-	-	-	-	ns
SI to DIR	t_{PLH} , t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	42	-	53	-	63	ns
		$C_L = 15\text{pF}$	5	-	18	-	-	-	-	-	ns
$\overline{S}O$ to DOR	t_{PLH} , t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	42	-	53	-	63	ns
		$C_L = 15\text{pF}$	5	-	18	-	-	-	-	-	ns
$\overline{S}O$ to Qn	t_{PLH} , t_{PHL}	$C_L = 50\text{pF}$	4.5	-	-	80	-	100	-	120	ns
		$C_L = 15\text{pF}$	5	-	35	-	-	-	-	-	ns
Propagation Delay/Ripple thru Delay SI to DOR	t_{PLH}	$C_L = 50\text{pF}$	4.5	-	-	400	-	500	-	600	ns
Propagation Delay/Ripple thru Delay $\overline{S}O$ to DIR	t_{PLH}	$C_L = 50\text{pF}$	4.5	-	-	500	-	625	-	750	ns
Propagation Delay/Ripple thru Delay SI to Qn	t_{PLH}	$C_L = 50\text{pF}$	4.5	-	-	300	-	380	-	450	ns
Three-State Output Enable $\overline{O}E$ to Qn	t_{PZH} , t_{PZL}	$C_L = 50\text{pF}$	4.5	-	-	35	-	44	-	53	ns
Three-State Output Disable $\overline{O}E$ to Qn	t_{PHZ} , t_{PLZ}	$C_L = 50\text{pF}$	4.5	-	-	30	-	38	-	45	ns
Output Transition Time	t_{TLH} , t_{THL}	$C_L = 50\text{pF}$	4.5	-	-	15	-	19	-	22	ns
Maximum CP Frequency	f_{MAX}	$C_L = 15\text{pF}$	5	-	32	-	-	-	-	-	MHz
Input Capacitance	C_{IN}	$C_L = 50\text{pF}$	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	$C_L = 15\text{pF}$	5	-	83	-	-	-	-	-	pF
Three-State Output Capacitance	C_O	$C_L = 50\text{pF}$	-	-	-	15	-	15	-	15	pF

NOTES:

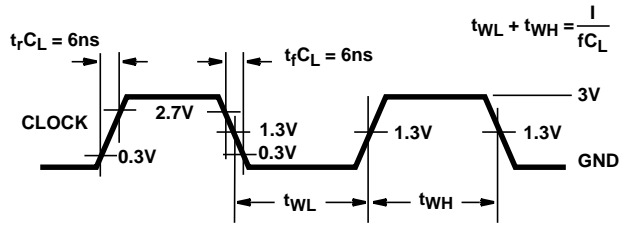
- C_{PD} is used to determine the dynamic power consumption, per package.
- $P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o)$ where f_i = Input Frequency, f_o = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 3. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 4. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

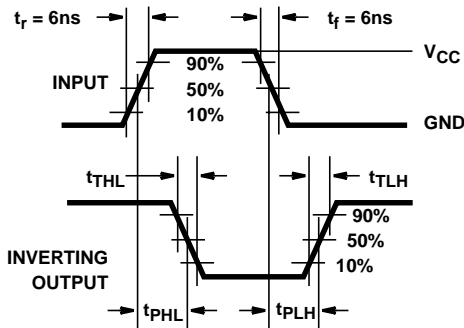


FIGURE 5. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

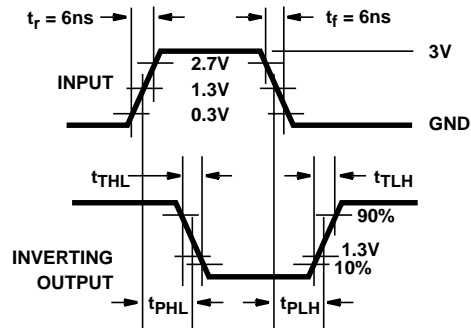


FIGURE 6. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

Test Circuits and Waveforms (Continued)

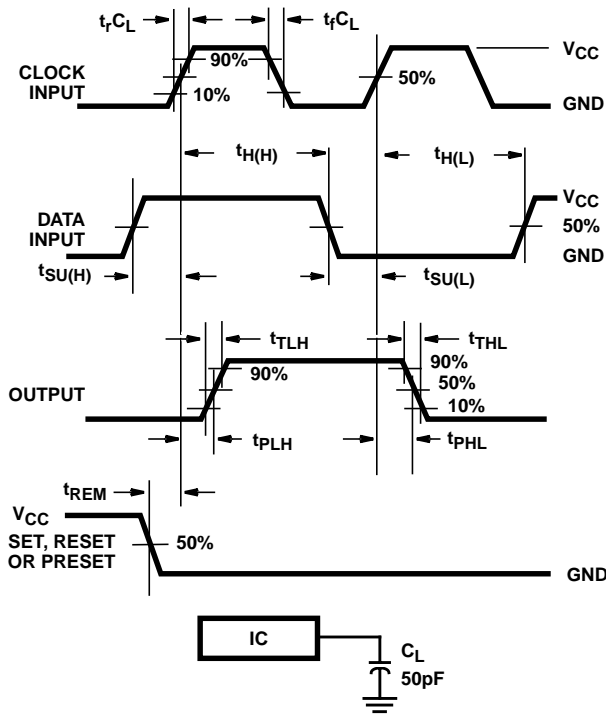


FIGURE 7. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

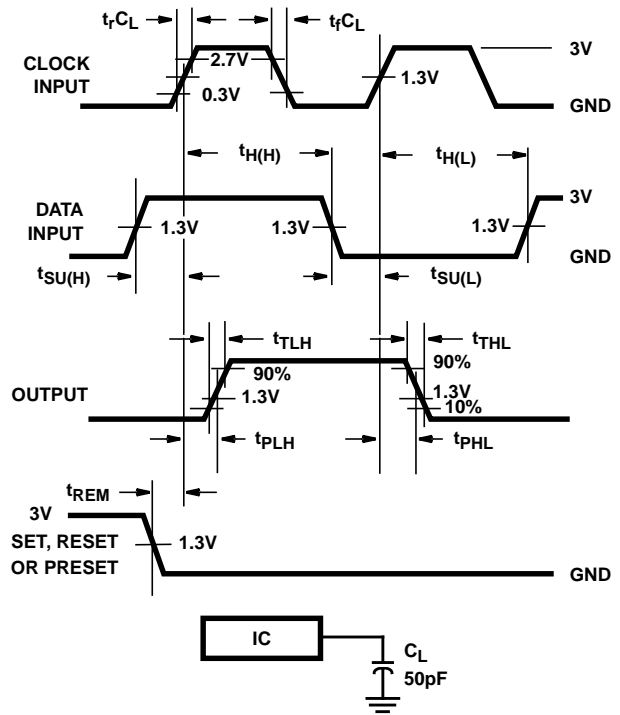


FIGURE 8. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

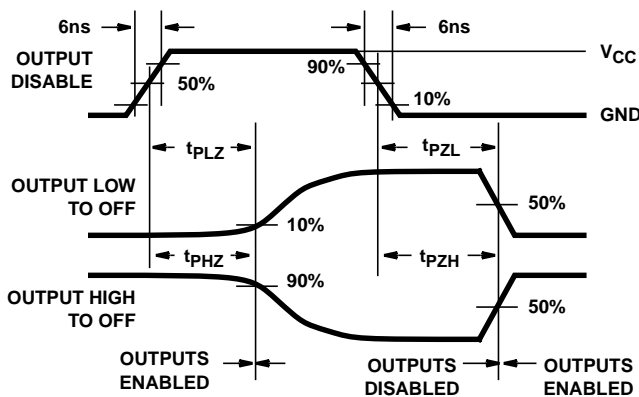


FIGURE 9. HC THREE-STATE PROPAGATION DELAY WAVEFORM

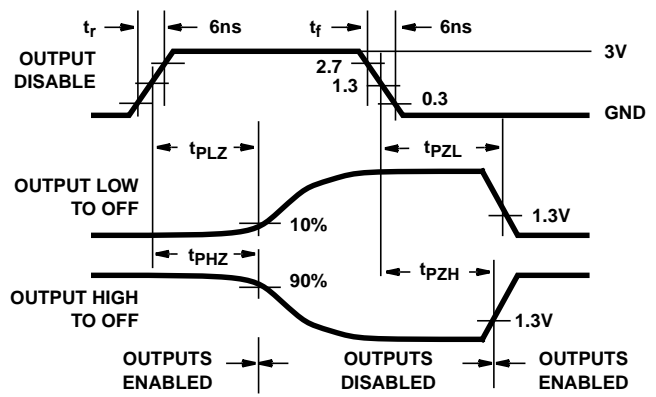
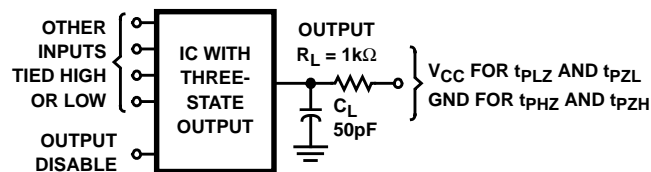
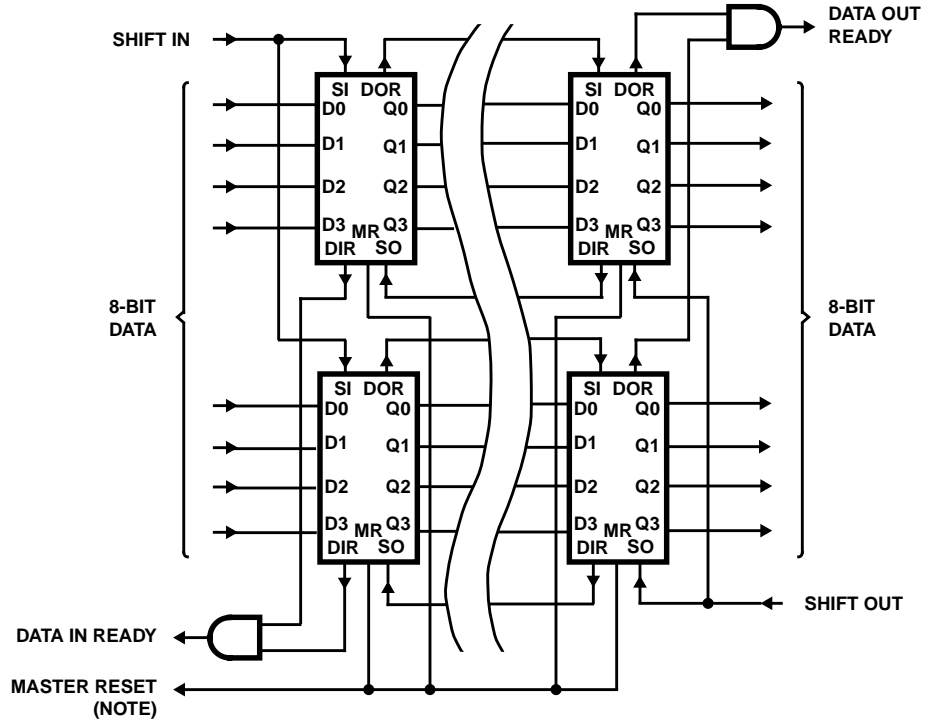


FIGURE 10. HCT THREE-STATE PROPAGATION DELAY WAVEFORM



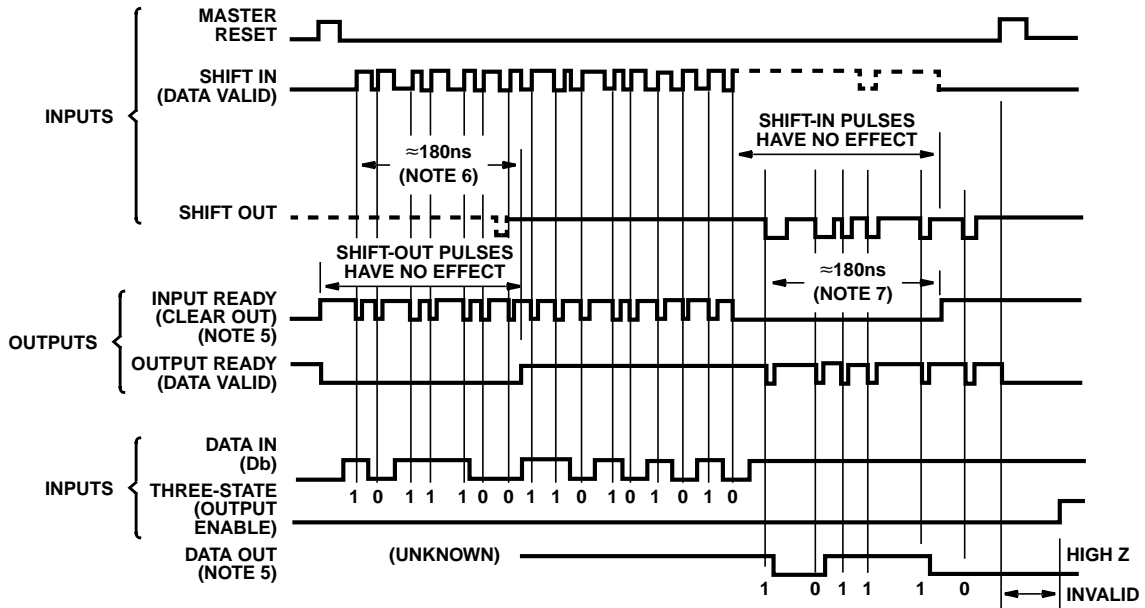
NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output $R_L = 1k\Omega$ V_{CC} , $C_L = 50pF$.

FIGURE 11. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT



NOTE: Pulse must be applied for cascading by 16 N bits.

FIGURE 12. EXPANSION, 8-BITS WIDE BY 16 N-BITS LONG USING HC/HCT40105



NOTES:

5. Data valid goes to high level in advance of the data out by a maximum of 38ns at $V_{CC} = 4.5V$ for $C_L = 50pF$ and $T_A = 25^\circ C$.
6. At $V_{CC} = 4.5V$, ripple time from position 1 to position 16.
7. At $V_{CC} = 4.5V$, ripple time from position 16 to position 1.

FIGURE 13. TIMING DIAGRAM FOR THE CD74HC/HCT40105

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD54HC40105F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC40105F3A
CD54HC40105F3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC40105F3A
CD74HC40105E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC40105E
CD74HC40105E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC40105E
CD74HC40105M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HC40105M
CD74HC40105M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC40105M
CD74HC40105M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC40105M
CD74HCT40105E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT40105E
CD74HCT40105E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT40105E
CD74HCT40105M	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT40105M
CD74HCT40105M.A	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT40105M

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF CD54HC40105, CD74HC40105 :

- Catalog : [CD74HC40105](#)
- Military : [CD54HC40105](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC40105M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC40105M96	SOIC	D	16	2500	353.0	353.0	32.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC40105E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC40105E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC40105E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC40105E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT40105E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT40105E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT40105E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT40105E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT40105M	D	SOIC	16	40	507	8	3940	4.32
CD74HCT40105M.A	D	SOIC	16	40	507	8	3940	4.32

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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Last updated 10/2025