TEXAS INSTRUMENTS
CD54HC4066, CD74HC4066, CD74HCT4066
SCHS208E – FEBRUARY 1998 – REVISED JULY 2024

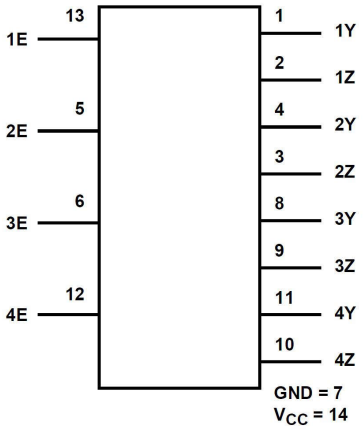
High-Speed CMOS Logic Quad Bilateral Switch

1 Features

- Wide analog-input-voltage range: 0 V – 10 V
- Low ON resistance:
  - V_{CC} = 4.5 V: 25 Ω
  - V_{CC} = 9 V: 15 Ω
- Fast switching and propagation delay times
- Low OFF leakage current
- Wide operating temperature range: –55°C to 125°C
- HC types:
  - 2 V to 10 V operation
  - High noise immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5 V and 10 V
- HCT types:
  - Direct LSTTL input logic compatibility, V_{IL}= 0.8 V (maximum), V_{IH} = 2 V (minimum)
  - CMOS input compatibility, $I_I \leq 1$ µA at V_{OL}, V_{OH}

2 Applications

- Analog signal switching and multiplexing: signal gating, modulators, squelch controls, demodulators, choppers, commutating switches
- Digital signal switching and multiplexing: Analog-to-digital and digital-to-analog conversions
- Digital control of frequency, impedance, phase, and analog-signal gain
- Building automation



Functional Block Diagram

3 Description

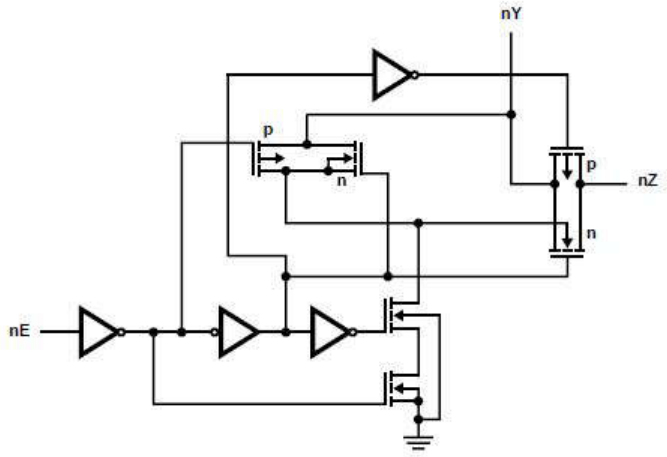
The ’HC4066 and CD74HCT4066 devices contain four independent digitally controlled analog switches that use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

These switches feature the characteristic linear ON resistance of the metal-gate CD4066B device. Each switch is turned on by a high-level voltage on its control input.

Device Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE(1)
CD74HC4066	-55 to 125	D (SOIC, 14)
	-55 to 125	PW (TSSOP, 14)
CD74HCT4066	-55 to 125	D (SOIC, 14)

(1) For more information, see Section 19.



Logic Diagram

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4 Pin Configuration and Functions

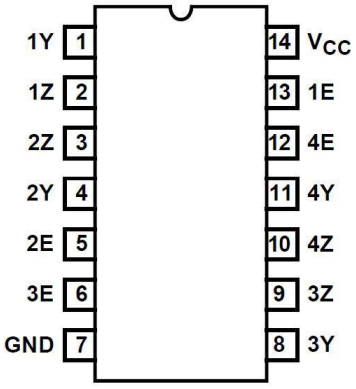

Figure 4-1. CD74HC4066 D or PW Package, 14-Pin SOIC or TSSOP CD74HCT4066 r D Package, 14-Pin SOIC (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1Y	1	I/O	Input/Output for Switch 1
1Z	2	I/O	Input/Output for Switch 1
2Z	3	I/O	Input/Output for Switch 2
2Y	4	I/O	Input/Output for Switch 2
2E	5	I	Control pin for Switch 2
3E	6	I	Control pin for Switch 3
GND	7	-	Ground Pin
3Y	8	I/O	Input/Output for Switch 3
3Z	9	I/O	Input/Output for Switch 3
4Z	10	I/O	Input/Output for Switch 4
4Y	11	I/O	Input/Output for Switch 4
4E	12	I	Control pin for Switch 4
1E	13	I	Control pin for Switch 1
V_{CC}	14	-	Power Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
V_{CC} HCT	DC Supply voltage		–0.5	7	V
V_{CC} HC(1)			-0.5	10.5	V
I_{IK}	DC input diode current	For V_I < -0.5V or V_I > V_{CC} + 0.5V	–20	20	mA
I_O	DC switch current(2)	For V_I< -0.5V or V_I > VCC + 0.5V	-20	20	mA
I_{OK}	DC Output diode current	For V_O < -0.5V or V_O > V_{CC} + -0.5V	-25	25	mA
DC Output Source or Sink Current per Output Pin, I_O	For V_O > -0.5V or V_O < V_{CC} + -0.5V		–25	25	mA
I_{CC}	DC V_{CC} or ground current		–50	50	mA
T_{JMAX}	Maximum junction temperature (Plastic Package)			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) In certain applications, the external load-resistor current may include both VCC and signal-line components. To avoid drawing VCC current when switch current flows into the transmission gate inputs, (terminals 1, 4, 8 and 11) the voltage drop across the bidirectional switch must not exceed 0.6V (calculated from RON values shown in the DC Electrical Specifications Table). No VCC current will flow through RLif the switch current flows into terminals 2, 3, 9 and 10. 2.

6 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7 Thermal Information

THERMAL METRIC		CD74HCx4066		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.4	133.9	°C/W

8 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage range (T_A = full package temperature range)(2)	CD54 and 74HC types	2		10	V
		CD54 and 74HCT types	4.5		5.5	
V_{IS}	Analog switch I/O voltage		0		V_{CC}	V
T_A	Ambient temperature		–55		125	°C
t_r , t_f	Input rise and fall times	2 V	0		1000	ns
		4.5 V	0		500	
		6 V	0		400	

9 Electrical Characteristics: HC Devices

Over operating free-air temperature range, V_{SUPPLY} = ±5 V, and R_L = 100 Ω, (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS})									
		V_{IS} (V)	V_I (V)	V_{CC} (V)	T_A				
High Level Input Voltage	V_{IH}			2	25°C			1.5	V
					–40°C to +85°C			1.5	
					–55°C to +125°C			1.5	
				4.5	25°C			3.15	
					–40°C to +85°C			3.15	
					–55°C to +125°C			3.15	
				9	25°C			6.3	
					–40°C to +85°C			6.3	
					–55°C to +125°C			6.3	
Low Level Input Voltage	V_{IL}			2	25°C	0.5			V
					–40°C to +85°C	0.5			
					–55°C to +125°C	0.5			
				4.5	25°C	1.35			
					–40°C to +85°C	1.35			
					–55°C to +125°C	1.35			
				9	25°C	2.7			
					–40°C to +85°C	2.7			
					–55°C to +125°C	2.7			
"ON" Resistance IO = 1mA	R_{ON}	V_{CC} or GND	VCC	4.5	25°C		25	80	Ω
					–40°C to +85°C			106	
					–55°C to +125°C			128	
				6	25°C		20	75	
					–40°C to +85°C			94	
					–55°C to +125°C			113	
				9	25°C		15	60	
					–40°C to +85°C			78	
					–55°C to +125°C			95	
		V_{CC} to GND		4.5	25°C		35	95	Ω
					–40°C to +85°C			118	
					–55°C to +125°C			142	
				6	25°C		24	84	
					–40°C to +85°C			105	
					–55°C to +125°C			126	
				9	25°C		31	70	
					–40°C to +85°C			88	
					–55°C to +125°C			105	
"ON" Resistance Between Any Two Switches	▲R_{ON}		VCC	4.5	25°C		1		Ω
			VCC	6	25°C		0.75		
			VCC	9	25°C		0.5		
Off-Switch Leakage Current	I_Z	V_{CC} or GND	V_{IL}	10	25°C			±0.1	µA
					–55°C to 85°C			±1	
					–55°C to 125°C			±1	

Over operating free-air temperature range, V_{SUPPLY} = ±5 V, and R_L = 100 Ω, (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
Input Leakage Current (Any Control)	I_{IL}		V_{CC} or GND	10	25°C			±0.1	μA
					–55°C to 85°C			±1	
					–55°C to 125°C			±1	
Quiescent Device Current	I_{CC}		V_{CC} or GND	6	25°C			18.5	μA
					–55°C to 85°C			20	
					–55°C to 125°C			40	
				10	25°C			35	
					–55°C to 85°C			160	
					–55°C to 125°C			320	
CONTROL (ADDRESS OR INHIBIT), V_C									

(1) Peak-to-Peak voltage symmetrical about (V_{DD} – V_{EE}) / 2.

10 Electrical Characteristics: HCT Devices

Over operating free-air temperature range, V_{SUPPLY} = ±5 V, and R_L = 100 Ω, (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS})									
		V_{IS} (V)	**V_I (V)**	**V_{CC} (V)**	**T_A**				
High Level Input Voltage	V_{IH}			4.5 to 5.5	25°C	2			V
					–40°C to +85°C	2			
					–55°C to +125°C	2			
Low Level Input Voltage	V_{IL}				25°C			0.8	V
					–40°C to +85°C			0.8	
					–55°C to +125°C			0.8	
"ON" Resistance IO = 1mA	R_{ON}	V_{CC} or GND	VCC	4.5	25°C		25	80	Ω
					–40°C to +85°C			106	
					–55°C to +125°C			128	
		V_{CC} to GND			25°C		35	95	Ω
					–40°C to +85°C			118	
					–55°C to +125°C			142	
"ON" Resistance Between Any Two Switches	▲R_{ON}		VCC	4.5	25°C		1		Ω
Off-Switch Leakage Current	I_Z	V_{CC} or GND	V_{IL}	5.5	25°C			±0.1	μA
					–55°C to 85°C			±1	
					–55°C to 125°C			±1	
Input Leakage Current (Any Control)	I_{IL}		V_{CC} or GND	5.5	25°C			±0.1	μA
					–55°C to 85°C			±1	
					–55°C to 125°C			±1	
Quiescent Device Current	I_{CC}		V_{CC} or GND	5.5	25°C			2	μA
					–55°C to 85°C			20	
					–55°C to 125°C			40	
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	▲I_{CC}		V_{CC} - 2.1	4.5 to 5.5	25°C		100	360	
					–55°C to 85°C			450	
					–55°C to 125°C			490	

Over operating free-air temperature range, V_{SUPPLY} = ±5 V, and R_L = 100 Ω, (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CONTROL (ADDRESS OR INHIBIT), V_C					

(1) Peak-to-Peak voltage symmetrical about (V_{DD} – V_{EE}) / 2.

11 Switching Characteristics HC

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions		C_L (pF)	MIN	NOM	MAX	UNIT
Propagation Delay Time Switch In to Out	t_{PHL}, t_{PLH}	2	25°C	50			60	ns
			-40°C to 85°C				75	ns
			-55°C to 125°C				90	ns
		4.5	25°C				12	ns
			-40°C to 85°C				15	ns
			-55°C to 125°C				18	ns
		9	25°C				8	ns
			-40°C to 85°C				11	ns
			-55°C to 125°C				13	ns
		5	25°C	15		4		ns
Propagation Delay Time Switch Turn On Delay	t_{PZH}, t_{PZL}	2	25°C	50			100	ns
			-40°C to 85°C				125	ns
			-55°C to 125°C				150	ns
		4.5	25°C				20	ns
			-40°C to 85°C				25	ns
			-55°C to 125°C				30	ns
		9	25°C				12	ns
			-40°C to 85°C				15	ns
			-55°C to 125°C				18	ns
		5	25°C	15		4		ns
Propagation Delay Time Switch Turn Off Delay	t_{PHZ}, t_{PLZ}	2	25°C	50			150	ns
			-40°C to 85°C				190	ns
			-55°C to 125°C				225	ns
		4.5	25°C				30	ns
			-40°C to 85°C				38	ns
			-55°C to 125°C				45	ns
		9	25°C				24	ns
			-40°C to 85°C				30	ns
			-55°C to 125°C				36	ns
		5	25°C	15		9.5		ns
Input (Control) Capacitance	C_I		25°C				10	pF
			-40°C to 85°C				10	
			-55°C to 125°C				10	
C_{PD} Power dissipation capacitance(1)	C_{PD}	5	25°C			25		

12 Switching Characteristics HCT

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions		C_L (pF)	MIN	NOM	MAX	UNIT
Propagation Delay Time Switch In to Out	t_{PHL}, t_{PLH}	4.5	25°C	50			12	ns
			-40°C to 85°C				15	ns
			-55°C to 125°C				18	ns
		5	25°C	15		1.3		ns
Propagation Delay Time Switch Turn On Delay	t_{PZH}, t_{PZL}	4.5	25°C	50			24	ns
			-40°C to 85°C				30	ns
			-55°C to 125°C				36	ns
		5	25°C	15		5		ns
Propagation Delay Time Switch Turn Off Delay	t_{PHZ}, t_{PLZ}	4.5	25°C	50			35	ns
			-40°C to 85°C				44	ns
			-55°C to 125°C				53	ns
		5	25°C	15		5.5		ns
Input (Control) Capacitance	C_I		25°C				10	pF
			-40°C to 85°C				10	
			-55°C to 125°C				10	
C_{PD} Power dissipation capacitance(1)	C_{PD}	5	25°C			38		

13 Analog Channel Specifications

over operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions		V_{CC} (V)	HC	HCT	UNIT
Switch Frequency Response Bandwidth at -3dB				4.5	200	200	MHz
Cross Talk Between Any Two Switches				4.5	-72	-72	dB
Total Harmonic Distortion		1kHz, V_{IS}= $4V_{PP}$		4.5	0.022	0.023	%
		1kHz, V_{IS}= $8V_{PP}$		9	0.019	N/A	%
Control to Switch Feedthrough Noise	Control to Switch Feedthrough Noise			4.5	200	130	mV
Control to Switch Feedthrough Noise				4.5	200	130	mV
				9	550	N/A	
Switch "OFF" signal feedthrough				4.5	-72	-72	dB
C_I Switch input capacitance					5	5	pF

14 Analog Test Circuits

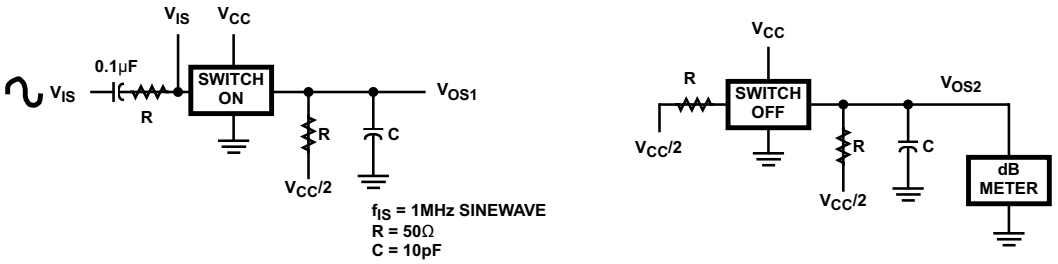

Figure 14-1. Crosstalk Between Two Switches Test Circuit

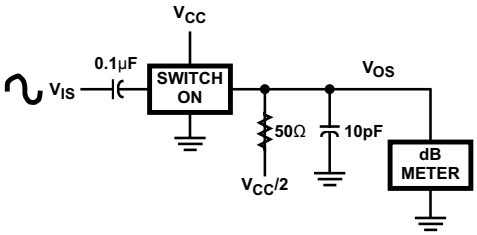

Figure 14-2. Frequency Response Test Circuit

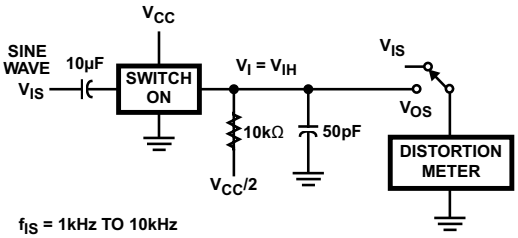

Figure 14-3. Total Harmonic Distortion Test Circuit

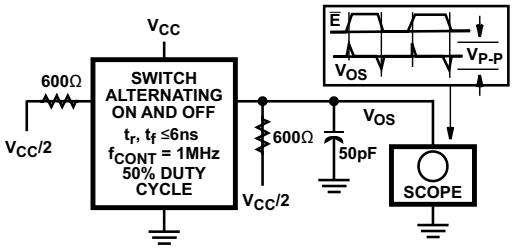

Figure 14-4. Control-To-Switch Feedthrough Noise Test Circuit

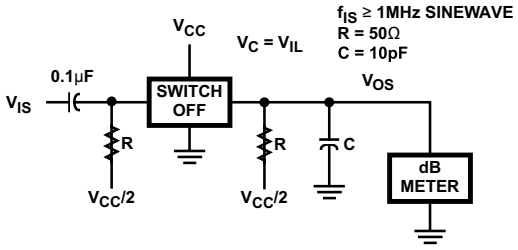

Figure 14-5. Switch OFF Signal Feedthrough

15 Test Circuits and Waveforms

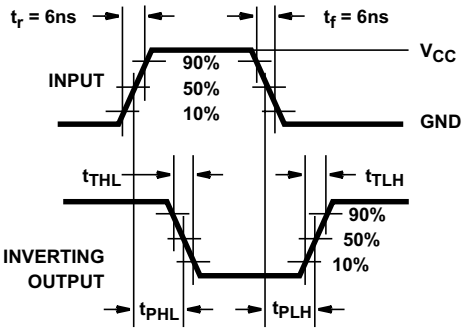

Figure 15-1. HC Transition Times and Propagation Delay Times, Combination Logic

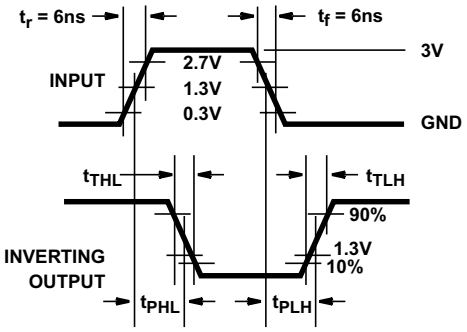

Figure 15-2. HCT Transition Times and Propagation Delay Times, Combination Logic

16 Detailed Description

16.1 Functional Block Diagram

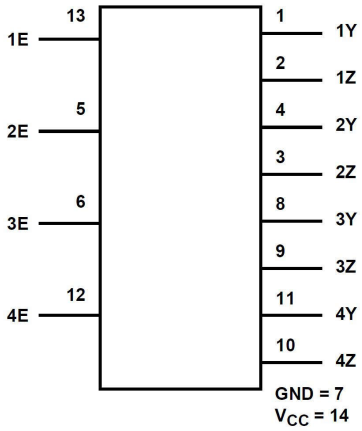

Figure 16-1. Functional Block Diagram

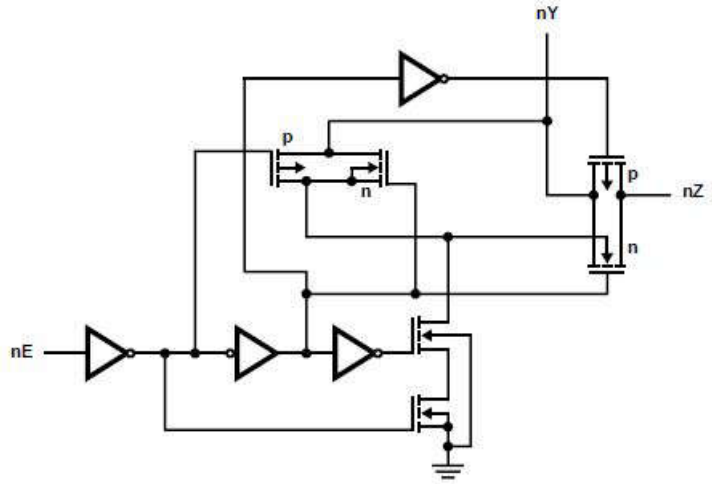

Figure 16-2. Logic Diagram

16.2 Device Functional Modes

Table 16-1. Truth Table

INPUTnE	SWITCH
L(2)	Off
H(1)	On

(1) H = High Level
(2) L = Low Level

17 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

17.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

17.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

17.3 Trademarks

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17.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

17.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

18 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (August 2003) to Revision E (July 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated thermal information	4
• Updated electrical specifications	6
• Updated switching specifications	8
• Updated analog channel specifications	9
• Updated ordering information	12

19 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8950701CA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8950701CA CD54HC4066F3A
CD54HC4066F3A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8950701CA CD54HC4066F3A
CD54HC4066F3A.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8950701CA CD54HC4066F3A
CD74HC4066E	NRND	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4066E
CD74HC4066E.A	NRND	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4066E
CD74HC4066EE4	NRND	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4066E
CD74HC4066M	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	HC4066M
CD74HC4066M96	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4066M
CD74HC4066M96.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4066M
CD74HC4066M96E4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4066M
CD74HC4066MT	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	HC4066M
CD74HC4066PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HP4066
CD74HC4066PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HP4066
CD74HC4066PWT	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-55 to 125	HP4066
CD74HCT4066E	NRND	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT4066E
CD74HCT4066E.A	NRND	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT4066E
CD74HCT4066M	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	HCT4066M
CD74HCT4066M96	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4066M
CD74HCT4066M96.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4066M
CD74HCT4066MT	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	HCT4066M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

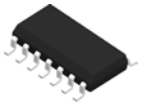
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF CD54HC4066, CD74HC4066, CD74HCT4066 :

- Catalog : CD74HC4066
- Automotive : CD74HCT4066-Q1
- Military : CD54HC4066

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

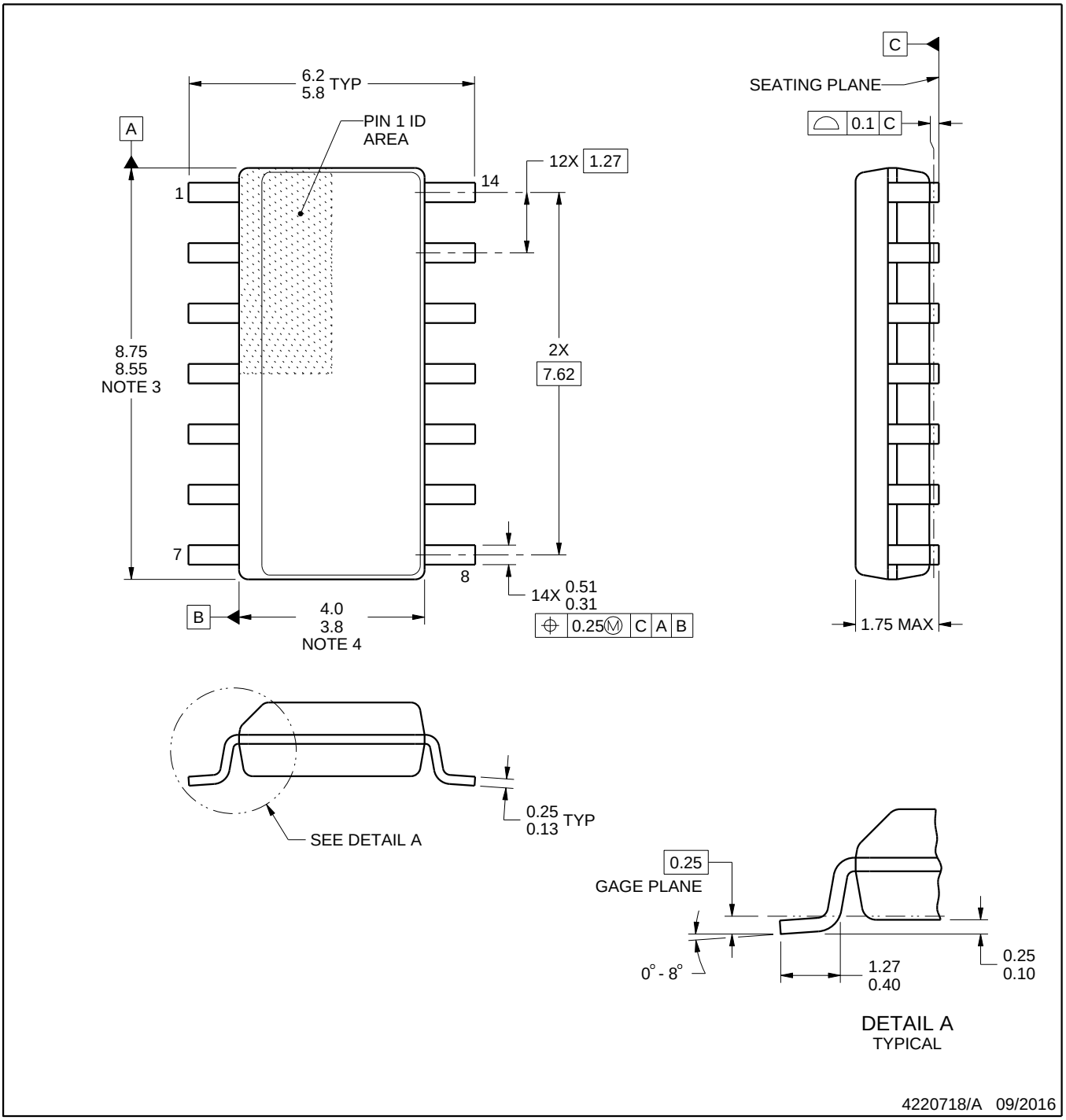


PACKAGE OUTLINE

D0014A

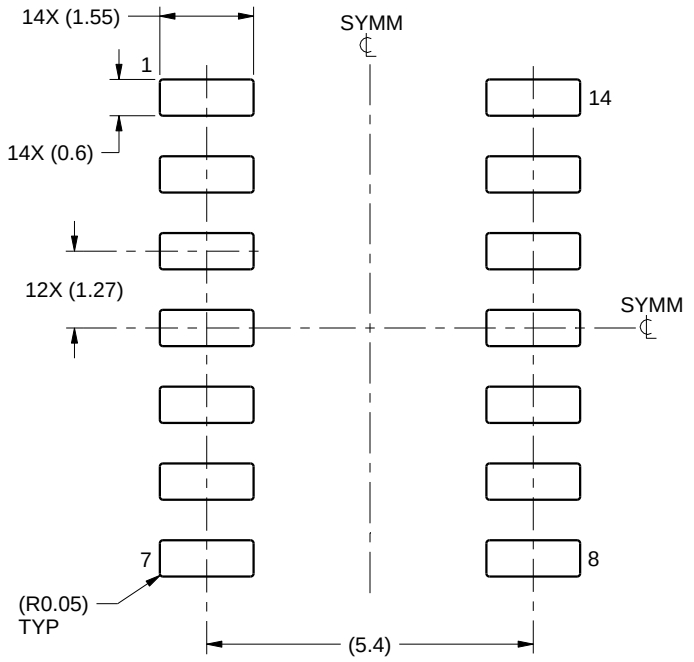
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

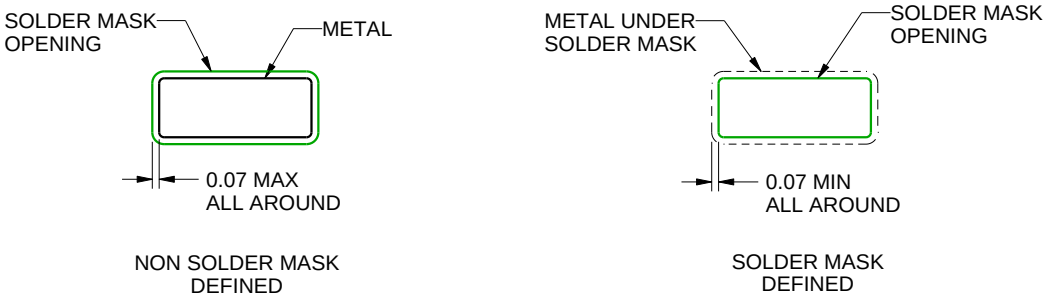


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

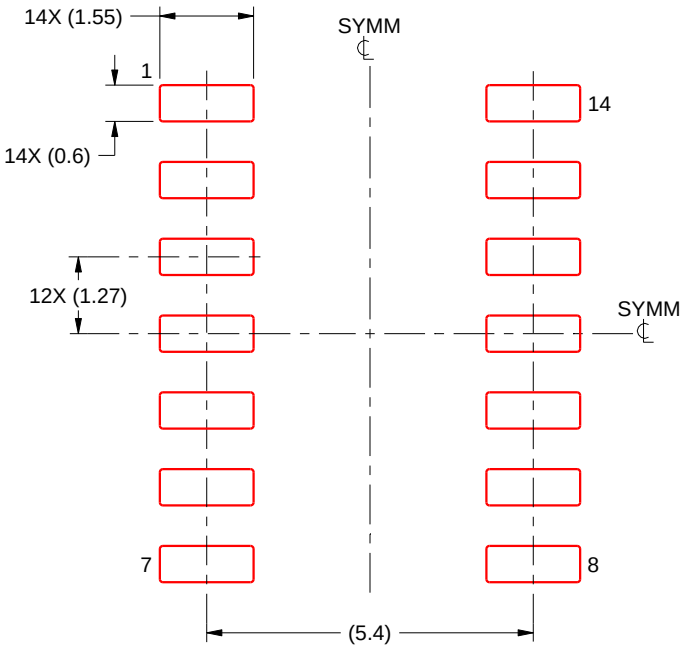
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

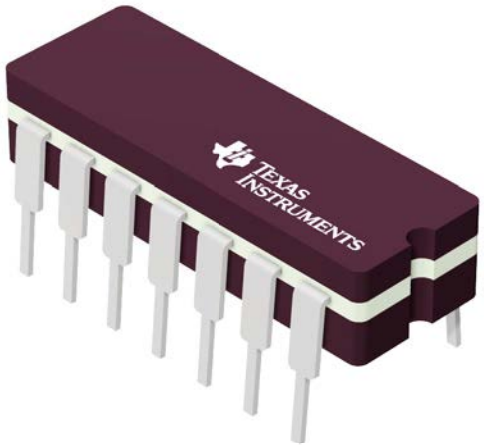
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

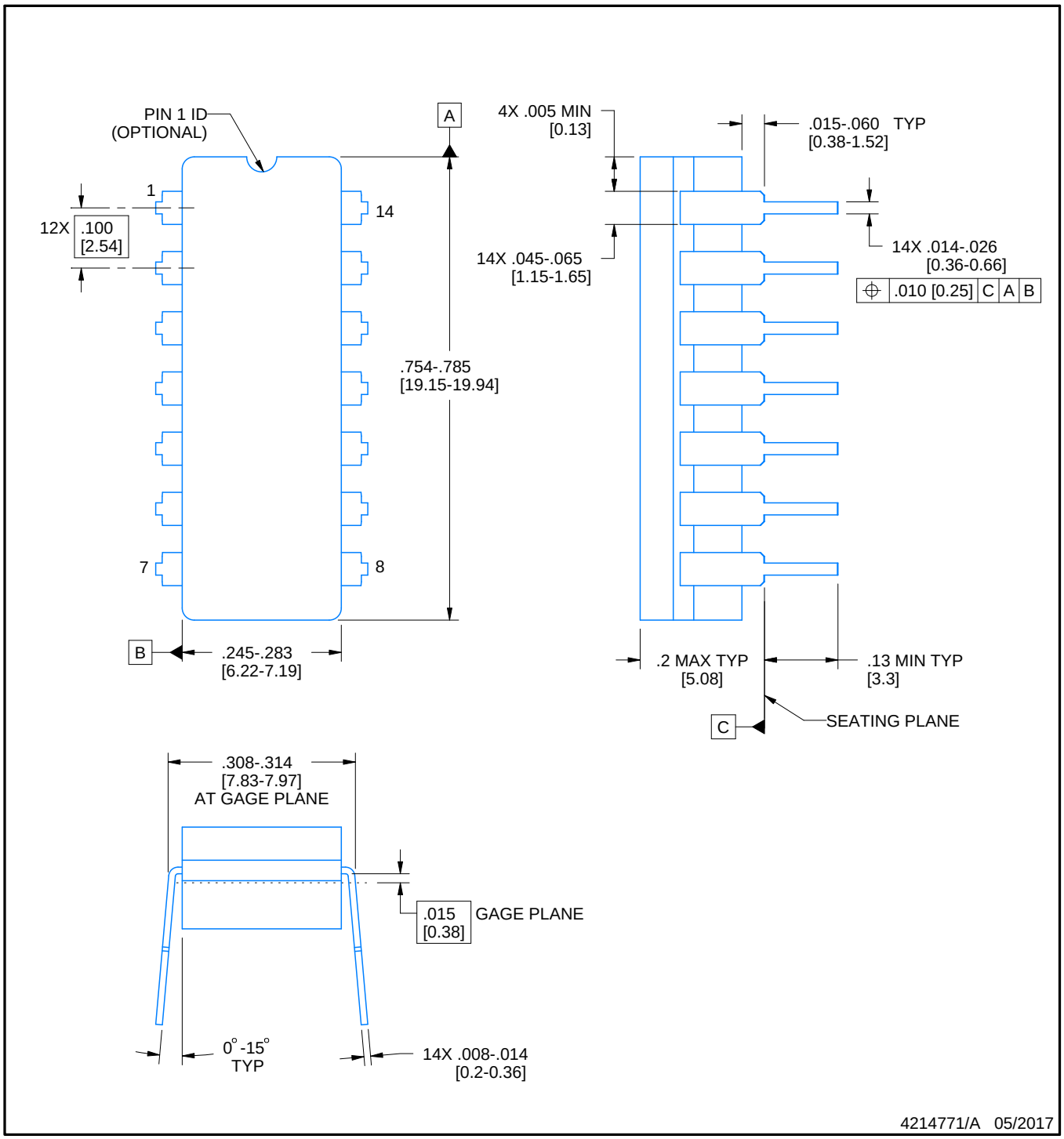
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

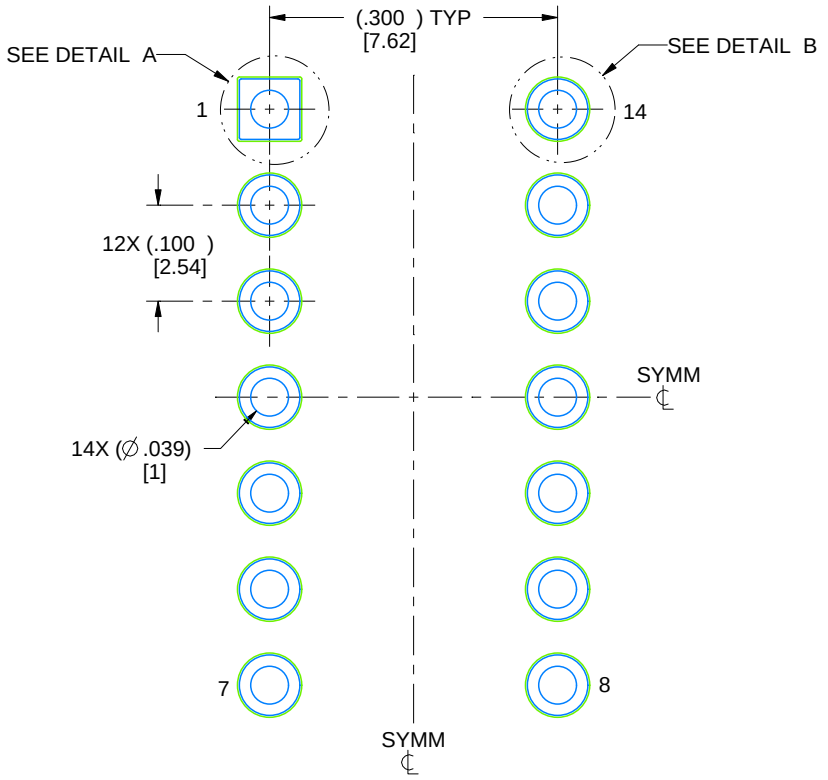
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

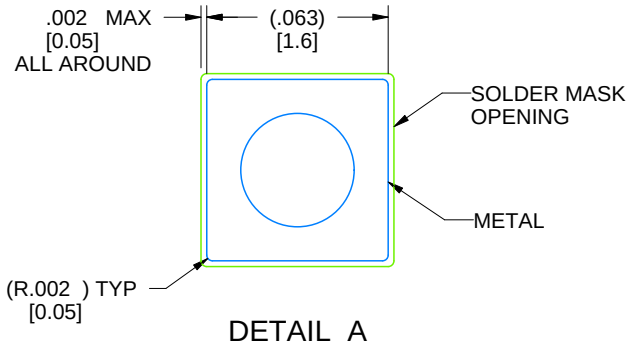
J0014A

CDIP - 5.08 mm max height

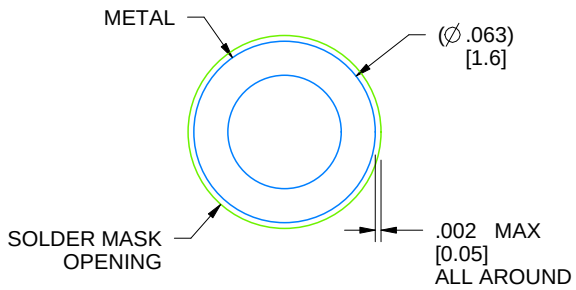
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



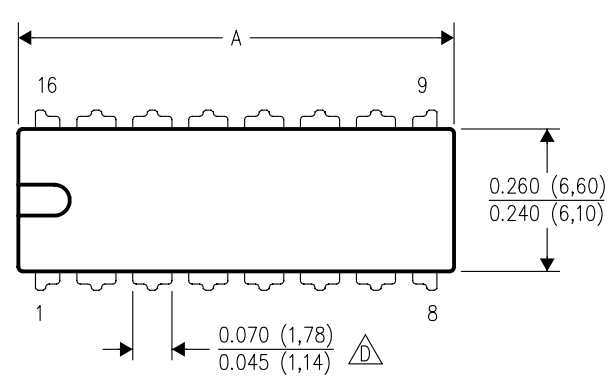
DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

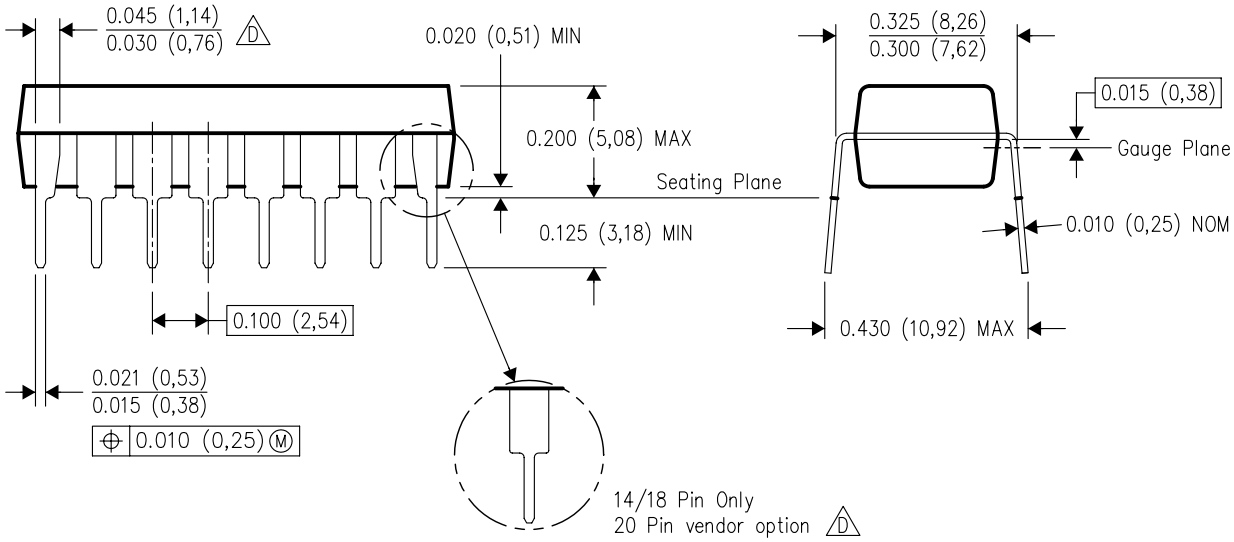
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

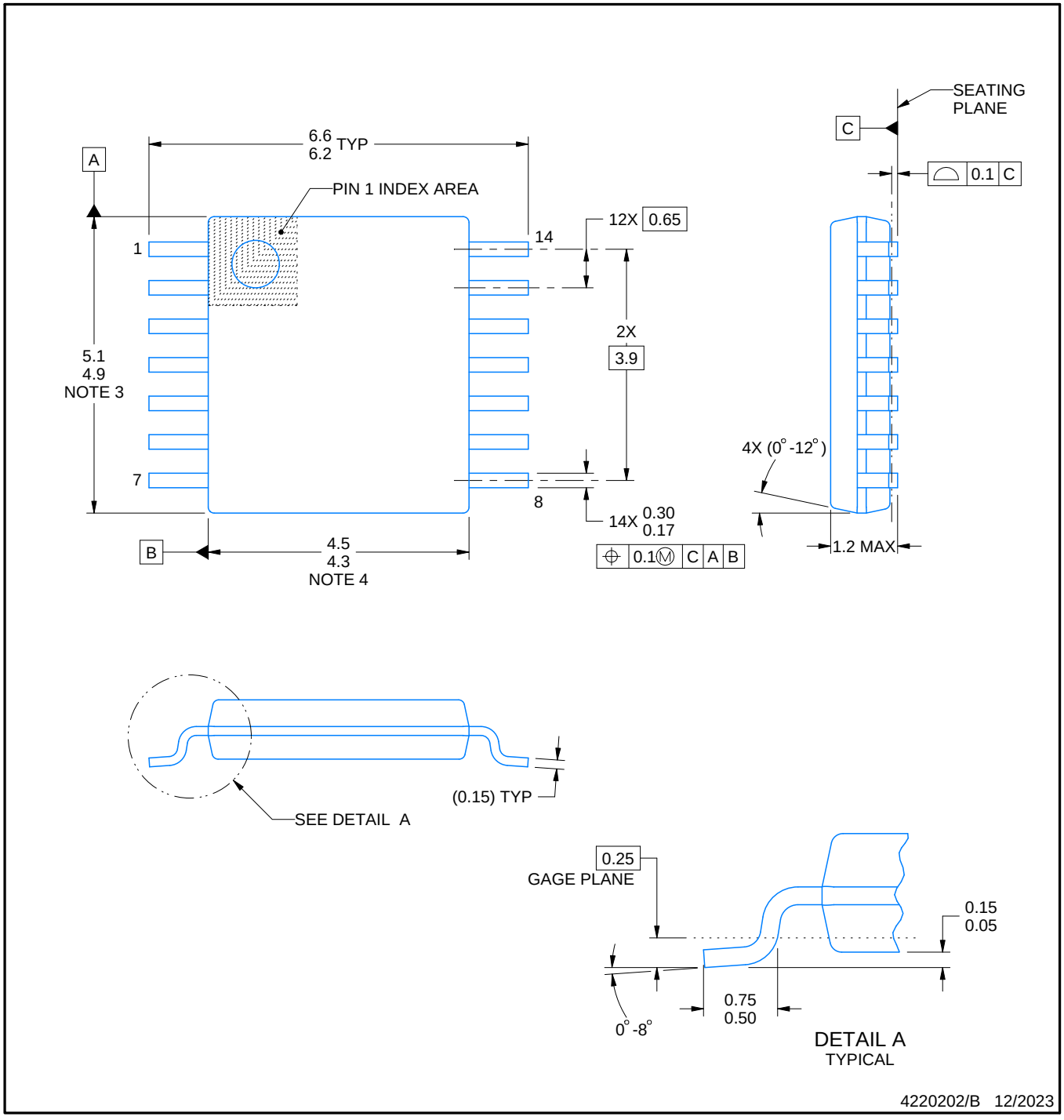
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

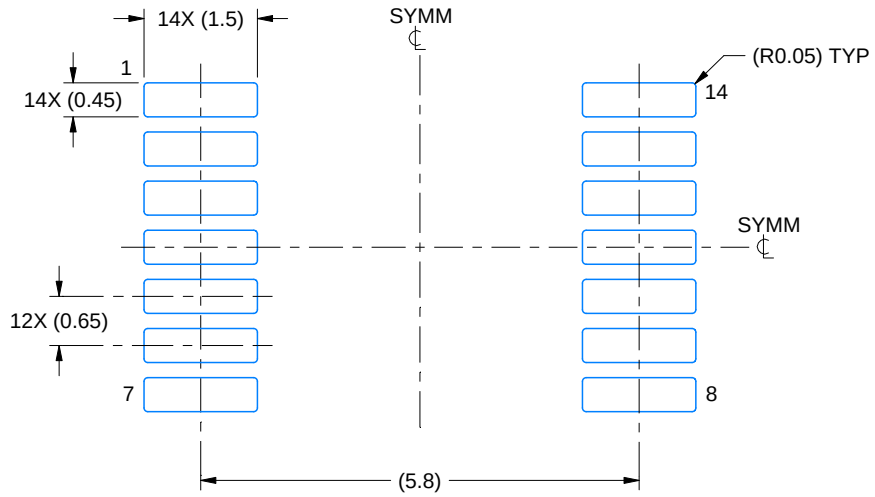
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

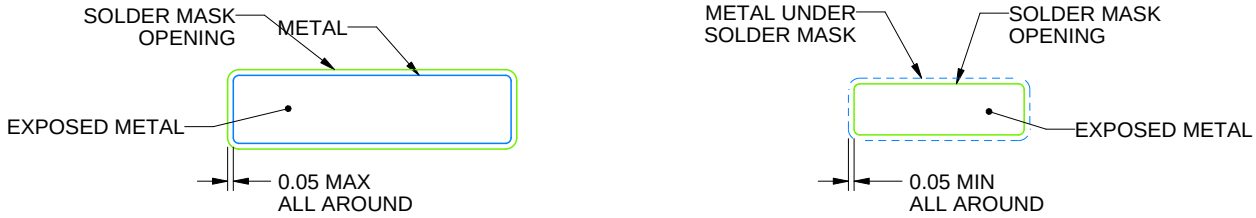


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

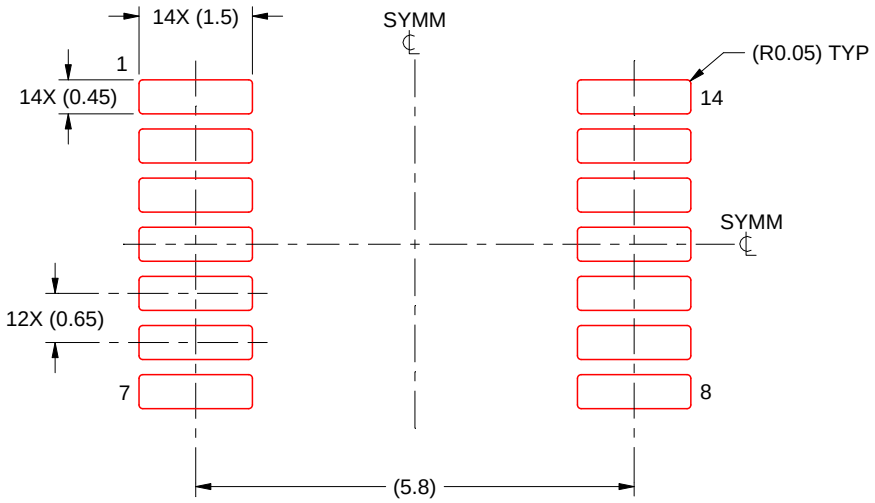


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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