

CD74HCT574-Q1

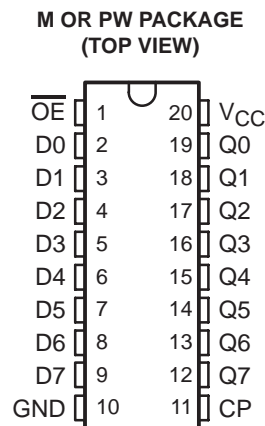
HIGH-SPEED CMOS LOGIC OCTAL D-TYPE FLIP-FLOP 3-STATE, POSITIVE-EDGE TRIGGERED

SCLS570A – FEBRUARY 2004 – REVISED APRIL 2008

- Qualified for Automotive Applications
- Buffered Inputs
- Common 3-State Output-Enable Control
- 3-State Outputs
- Bus-Line Driving Capability
- Typical Propagation Delay (Clock to Q):
15 ns at $V_{CC} = 5\text{ V}$, $C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$
- Fanout (Over Temperature Range)
 - Standard Outputs . . . 10 LSTTL Loads
 - Bus Driver Outputs . . . 15 LSTTL Loads
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- V_{CC} Voltage = 4.5 V to 5.5 V
- Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8\text{ V (Max)}$, $V_{IH} = 2\text{ V (Min)}$
- CMOS Input Compatibility, $I_I \leq 1\ \mu\text{A}$ at V_{OL} , V_{OH}

description/ordering information

The CD74HCT574 is an octal D-type flip-flop with 3-state outputs and the capability to drive 15 LSTTL loads. The eight edge-triggered flip-flops enter data into their registers on the low-to-high transition of the clock (CP). The output enable (\overline{OE}) controls the 3-state outputs and is independent of the register operation. When \overline{OE} is high, the outputs are in the high-impedance state.



ORDERING INFORMATION†

T _A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	SOIC – M	Tape and reel		
–40°C to 125°C	SOIC – M	Tape and reel	CD74HCT574QM96Q1	HCT574Q
	TSSOP – PW	Tape and reel	CD74HCT574QPWRQ1	HCT574Q

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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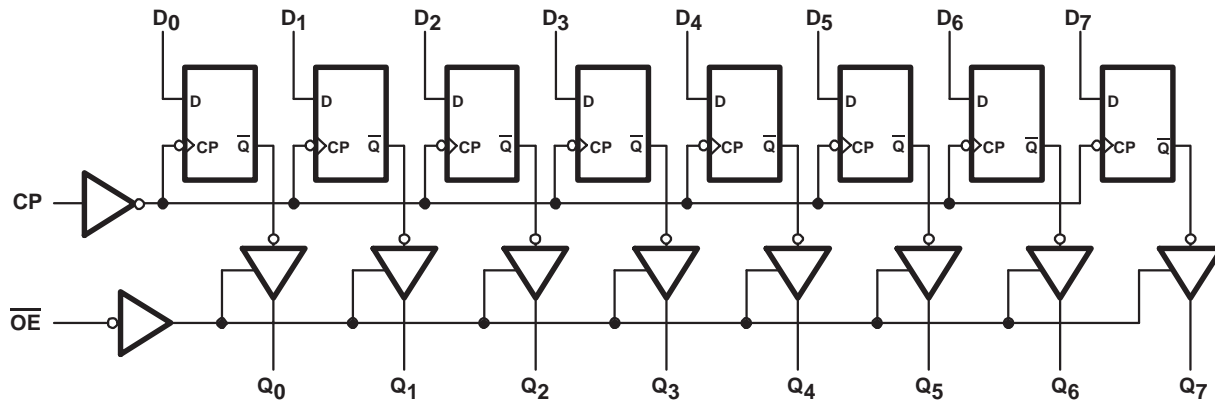
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FUNCTION TABLE

INPUTS			OUTPUT
\overline{OE}	CP	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

NOTE: H = High voltage level (steady state)
 L = Low voltage level (steady state)
 X = Don't care
 ↑ = Transition from low to high level
 Q_0 = Level before the indicated steady-state conditions were established
 Z = High-impedance state

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	±20 mA
Output clamp current, I_{OK} ($V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	±20 mA
Drain current per output, I_O ($V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	±35 mA
Output source or sink current per output, I_O ($V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	±25 mA
Continuous current through V_{CC} or GND, I_{CC}	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): M package	58°C/W
PW package	69°C/W
Maximum junction temperature, T_J	150°C
Lead temperature (during soldering):	
At distance $1/16 \pm 1/32$ inch ($1,59 \pm 0,79$ mm) from case for 10 s max	300°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages referenced to GND unless otherwise specified.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 4.5$ V to 5.5 V		V
V_{IL}	Low-level input voltage	$V_{CC} = 4.5$ V to 5.5 V		V
V_I	Input voltage	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	V
t_t	Input transition (rise and fall) time	$V_{CC} = 2$ V		ns
		$V_{CC} = 4.5$ V		
		$V_{CC} = 6$ V		
T_A	Operating free-air temperature	–40	125	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		I _O (mA)	V _{CC}	T _A = 25°C			T _A = -40°C TO 125°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	CMOS loads	-0.02	4.5 V	4.4			4.4		V
		TTL loads	-6	4.5 V	3.98			3.7		
V _{OL}	V _I = V _{IH} or V _{IL}	CMOS loads	0.02	4.5 V				0.1		V
		TTL loads	6	4.5 V				0.26	0.4	
I _I	V _I = V _{CC} or GND		0	5.5 V			±0.1	±1		µA
I _{OZ}	V _I = V _{IL} or V _{IH} , V _O = V _{CC} or GND			6 V			±0.5	±10		µA
I _{CC}	V _I = V _{CC} or GND		0	5.5 V			8	160		µA
ΔI _{CC}	V _I = V _{CC} - 2.1 V, See Note 4			4.5 V to 5.5 V		100	360	490		µA
C _{IN}	C _L = 50 pF						10	10		pF
C _{OUT}	3-state						20	20		pF

NOTE 4: For dual-supply systems, theoretical worst-case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT input loading

TYPE	INPUT	UNIT LOADS†
'574	D0-D7	0.4
	CP	0.75
	$\overline{\text{OE}}$	0.6

†Unit load is ΔI_{CC} limit specified in electrical characteristics table, e.g., 360 µA max at 25°C.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER		V _{CC}	T _A = 25°C		T _A = -40°C TO 125°C		UNIT
			MIN	MAX	MIN	MAX	
f _{max}	Maximum clock frequency	4.5 V	30		20		MHz
t _w	Clock pulse duration	4.5 V	16		24		ns
t _{su}	Setup time, data before clock↑	4.5 V	12		18		ns
t _h	Hold time, data after clock↑	4.5 V	5		5		ns



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V _{CC}	T _A = 25°C			T _A = -40°C TO 125°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
t _{pd}	CP	Q	C _L = 50 pF	4.5 V			33		50	ns
			C _L = 15 pF	5 V		15				
t _{dis}	$\overline{\text{OE}}$	Q	C _L = 50 pF	4.5 V				28	42	ns
			C _L = 15 pF	5 V		11				
t _{en}	$\overline{\text{OE}}$	Q	C _L = 50 pF	4.5 V				30	45	ns
			C _L = 15 pF	5 V		12				
t _f		Q	C _L = 50 pF	4.5 V				12	18	ns
f _{max}	CP		C _L = 15 pF	5 V			60			MHz

operating characteristics, V_{CC} = 5 V, T_A = 25°C, input t_r, t_f = 6 ns

PARAMETER		TYP	UNIT
C _{pd}	Power dissipation capacitance (see Note 5)	47	pF

NOTE 5: C_{pd} is used to determine the dynamic power consumption (P_D), per package.

$$P_D = (C_{PD} \times V_{CC}^2 \times f_I) + \Sigma (C_L \times V_{CC}^2 \times f_O)$$

f_I = input frequency

f_O = output frequency

C_L = output load capacitance

V_{CC} = supply voltage

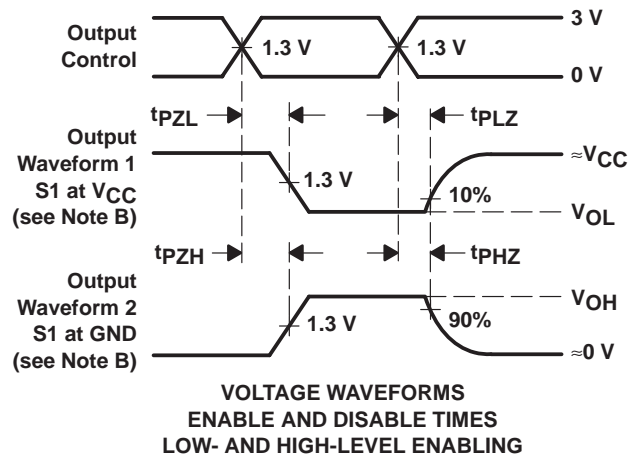
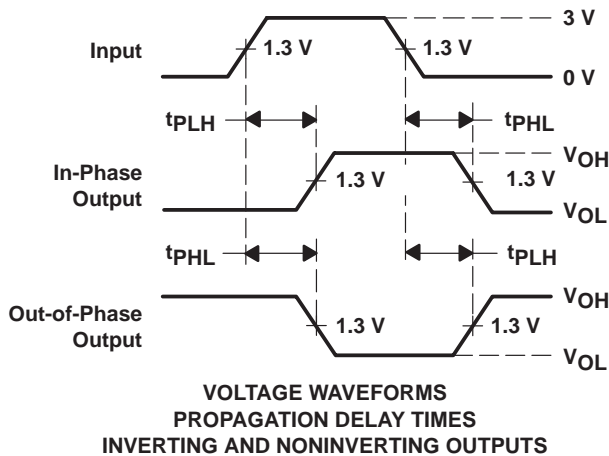
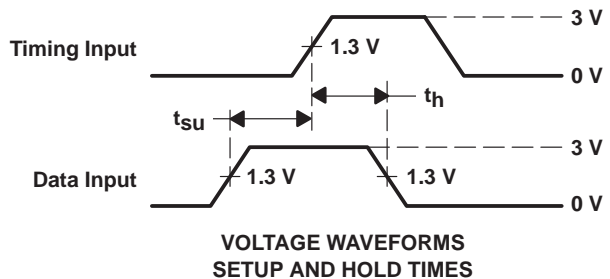
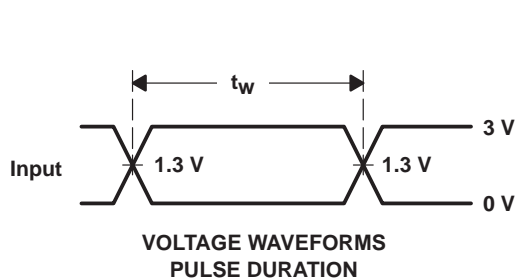
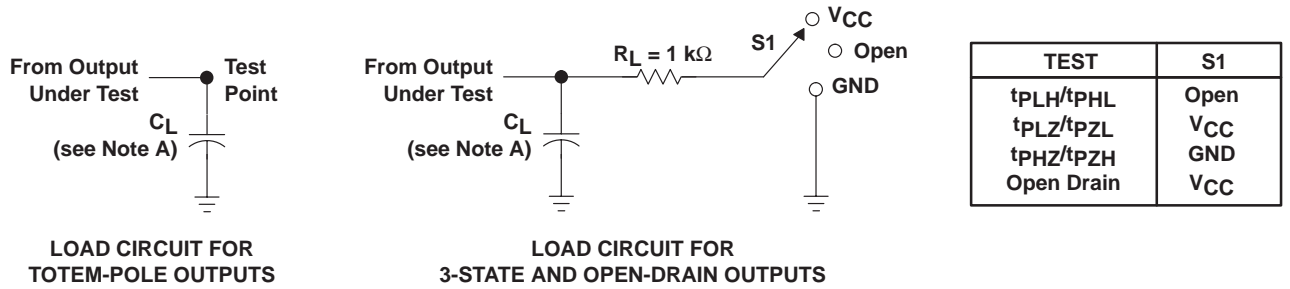
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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 6\text{ ns}$, $t_f \leq 6\text{ ns}$.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. All parameters and waveforms are not applicable to all devices.
 - F. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - G. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - H. t_{PZH} and t_{PZL} are the same as t_{en} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74HCT574QM96G4Q1	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCT574Q1
CD74HCT574QM96G4Q1.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCT574Q1
CD74HCT574QPWRG4Q1	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCT574Q1
CD74HCT574QPWRG4Q1.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCT574Q1

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF CD74HCT574-Q1 :

- Catalog : [CD74HCT574](#)
- Enhanced Product : [CD74HCT574-EP](#)
- Military : [CD54HCT574](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HCT574QM96G4Q1	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HCT574QPWRG4Q1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HCT574QM96G4Q1	SOIC	DW	20	2000	356.0	356.0	45.0
CD74HCT574QPWRG4Q1	TSSOP	PW	20	2000	353.0	353.0	32.0

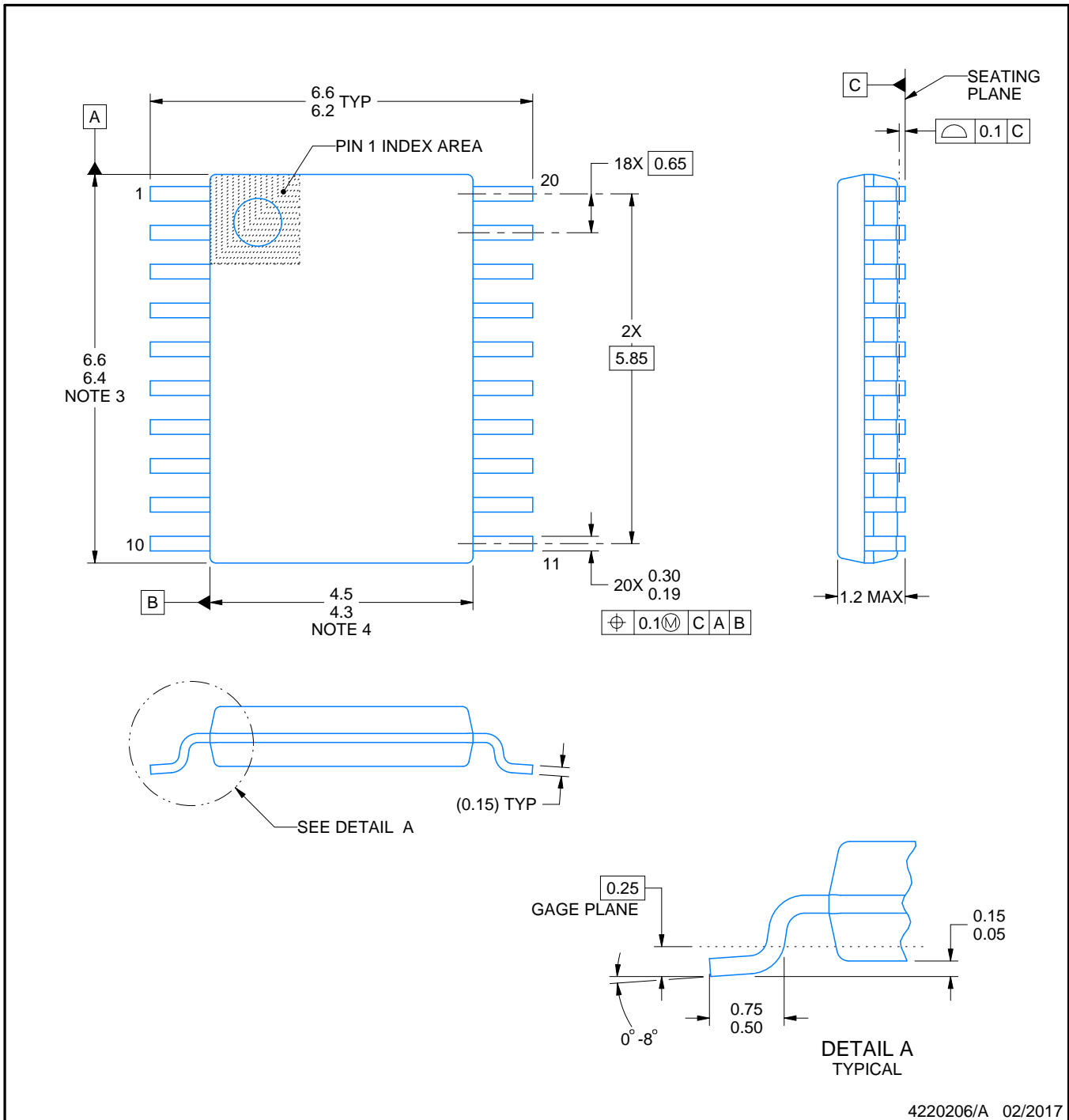
PW0020A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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