DRV8844A Quad Half-Bridge Driver with Independent Grounds

1 Features

- Four-channel half-bridge driver
  - **Independent control** of each half-bridge
  - Can be used as low-side or high-side switch
  - Outputs can be connected in parallel
- Low MOSFET $R_{DS(ON)}$: **210mΩ** per FET
  - **2.5A** Maximum Drive Current at 24V, 25°C
- **Bipolar power supply** support up to ±32.5V
- **8V** to **65V** operating supply voltage range
- **Separate power grounds** for connection of optional sense resistors
- Can drive various types of loads -
  - Four solenoids, valves, or relays
  - Two brushed-DC motors
  - One stepper motor
  - One or two Peltier thermoelectric coolers (TEC)
  - One 3-phase brushless-DC (BLDC) motor
- Built-in 3.3V, 10mA LDO regulator
- Industry standard **IN/EN** digital control interface
- Protection features
  - VM undervoltage lockout (UVLO)
  - Overcurrent protection (OCP)
  - Thermal shutdown (TSD)
  - Fault condition output (nFAULT)

2 Applications

- Textile Machines
- Office Automation Machines
- Gaming Machines
- Factory Automation
- Motor Drive
- Stage Lighting
- Thermoelectric Coolers (TEC)

3 Description

The DRV8844A is a four-channel, individually controllable half-bridge driver for a wide range of applications. The device supports up to 2.5A peak or 1.75A RMS output current at 24V and 25°C with proper PCB heatsinking. The output stage of the device consists of N-channel power MOSFETs configured as four independent half-bridges, allowing the device to be used for driving two DC motors, one stepper motor, four solenoids, or other loads. Each output can be a LS switch (low-side switch), HS switch (high-side switch), or a push-pull output driver.

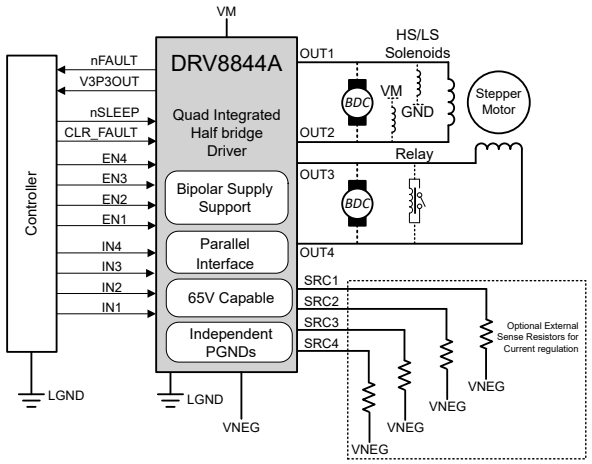
Separate inputs to independently control each 1/2-H-bridge are provided. To allow operation with split (positive and negative) power supplies, the logic inputs and nFAULT output are referenced to a separate floating ground pin. Additionally, the DRV8844A supports the connection of sense resistors on each individual half-bridge, allowing for current sensing at the system level for applications such as motor control.

Internal shutdown functions are provided for over current protection, short circuit protection, undervoltage lockout, and overtemperature.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8844A	HVSSOP (28)(DGQ)	7.30mm x 4.90mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

Table of Contents

4 Pin Configuration and Functions

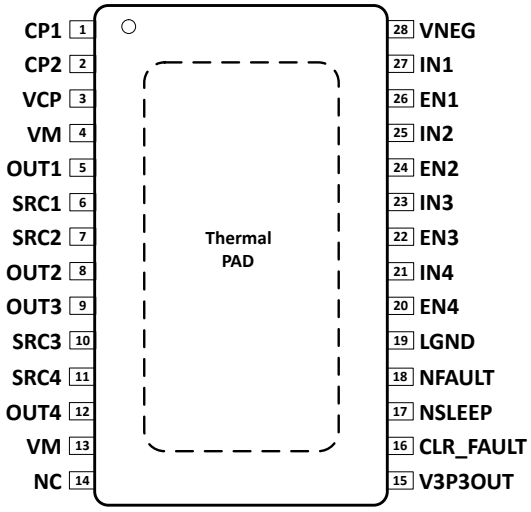


Figure 4-1. DGQ Package 28-Pin HVSSOP Top View

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
POWER AND GROUND				
CP1	1	P	Charge pump flying capacitor	Connect a 0.01µF 100V capacitor between CP1 and CP2.
CP2	2	P	Charge pump flying capacitor	
LGND	19	P	Logic input reference ground	Connect to logic ground. This can be any voltage between VNEG and VM – 8V.
V3P3OUT	15	P	3.3V regulator output	Bypass to VNEG with a 0.47µF 6.3V ceramic capacitor. Can be used to supply VREF.
VCP	3	P	High-side gate drive voltage	Connect a 0.1µF 16V ceramic capacitor to VM.
VM	4, 13	P	Main power supply	Connect to motor supply (8V to 60V). Both pins must be connected to same supply. Bypass to VNEG with a 10µF (minimum) capacitor.
SRC1	6	P	Low-side FET source for OUT1	Connect to VNEG directly or through optional current-sense resistor
SRC2	7	P	Low-side FET source for OUT2	
SRC3	10	P	Low-side FET source for OUT3	
SRC4	11	P	Low-side FET source for OUT4	
VNEG	28, PPAD	P	Negative power supply (dual supplies) or ground (single supply)	
CONTROL				
EN1	26	I	Channel 1 enable	Logic high enables OUT1. Internal pulldown.
EN2	24	I	Channel 2 enable	Logic high enables OUT2. Internal pulldown.
EN3	22	I	Channel 3 enable	Logic high enables OUT3. Internal pulldown.
EN4	20	I	Channel 4 enable	Logic high enables OUT4. Internal pulldown.
IN1	27	I	Channel 1 input	Logic input controls state of OUT1. Internal pulldown.
IN2	25	I	Channel 2 input	Logic input controls state of OUT2. Internal pulldown.
IN3	23	I	Channel 3 input	Logic input controls state of OUT3. Internal pulldown.
IN4	21	I	Channel 4 input	Logic input controls state of OUT4. Internal pulldown.
CLR_FAULT	16	I	Clear Fault input	Negative Edge clears latched faults in affected channels

Table 4-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
nSLEEP	17	I	Sleep mode input	Logic high to enable device, logic low to enter low-power sleep mode. Internal pulldown.

Table 4-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
STATUS				
nFAULT	18	OD	Fault	Logic low when in fault condition (overtemperature, overcurrent, UVLO). Open-drain output.
OUTPUT				
OUT1	5	O	Output 1	Connect to loads
OUT2	8	O	Output 2	
OUT3	9	O	Output 3	
OUT4	12	O	Output 4	
NO CONNECT				
NC	14	—	No connect	No connection to these pins

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VM	Power supply voltage	–0.3	70	V
	Logic ground voltage (LGND)	–0.5	VM - 8	V
	Digital pin voltage	LGND – 0.5	LGND + 7	V
	SRC1, SRC2, SRC3, SRC4 (pins 6, 7, 10 and 11 with optional sense resistor) to VNEG pin (pin 28)	–0.6	0.6	V
	Peak motor drive output current, t < 1 µs	Internally limited		A
	Continuous motor drive output current(2)		2.5	A
T_J	Operating virtual junction temperature	–40	150	°C
T_{stg}	Storage temperature	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Power dissipation and thermal limits must be observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range, all voltages relative to VNEG terminal (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_M	Motor power supply voltage(1)	8		65	V
I_{V3P3}	V3P3OUT load current	0		10	mA
T_A	Ambient temperature	–40		125	°C

(1) All V_M pins must be connected to the same supply voltage.

5.4 Thermal Information

THERMAL METRIC[1]		DRV8844A DGQ (HVSSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 Electrical Characteristics

T_A = 25°C, over operating free-air temperature range, all voltages relative to VNEG terminal (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VM}	VM operating supply current	V_M = 24 V, f_{PWM} < 50 kHz		1	5	mA
I_{VMQ}	VM sleep mode supply current	V_M = 24 V		500	800	µA
V_{UVLO}	VM undervoltage lockout voltage	V_M rising		6.3	8	V
V3P3OUT REGULATOR						
V_{3P3}	V3P3OUT voltage	IOUT = 0 to 1 mA	3.18	3.3	3.52	V
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage			LGND + 0.6	LGND + 0.7	V
V_{IH}	Input high voltage		LGND + 2.2		LGND + 5.25	V
V_{HYS}	Input hysteresis		50		600	mV
I_{IL}	Input low current	VIN = LGND	–5		5	µA
I_{IH}	Input high current	VIN = LGND + 3.3 V			100	µA
R_{PD}	Internal pulldown resistance			100		kΩ
nFAULT OUTPUT (OPEN-DRAIN OUTPUT)						
V_{OL}	Output low voltage	I_O = 5 mA			LGND + 0.5	V
I_{OH}	Output high leakage current	V_O = LGND + 3.3 V			1	µA
H-BRIDGE FETS						
$R_{DS(ON)}$	HS FET on resistance	V_M = 24 V, I_O = 1 A, T_J = 25°C		0.21		Ω
		V_M = 24 V, I_O = 1 A, T_J = 85°C		0.25	0.34	
	LS FET on resistance	V_M = 24 V, I_O = 1 A, T_J = 25°C		0.21		
		V_M = 24 V, I_O = 1 A, T_J = 85°C		0.25	0.34	
I_{OFF}	Off-state leakage current		–2		2	µA
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		5			A
t_{DEAD}	Output dead time			90		ns
t_{OCP}	Overcurrent protection deglitch time			5		µs
t_{CLR_FAULT}	Minimum pulse width to clear fault		5			µs
T_{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	°C

5.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)(1) (see Figure 5-1)

NUMBER	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
1	t_1	Delay time, ENx high to OUTx high, INx = 1	130	330	ns
2	t_2	Delay time, ENx low to OUTx low, INx = 1	275	475	ns
3	t_3	Delay time, ENx high to OUTx low, INx = 0	100	300	ns
4	t_4	Delay time, ENx low to OUTx high, INx = 0	200	400	ns
5	t_5	Delay time, INx high to OUTx high	300	500	ns
6	t_6	Delay time, INx low to OUTx low	275	475	ns
7	t_R	Output rise time, resistive load to VNEG	30	150	ns
8	t_F	Output fall time, resistive load to VNEG	30	150	ns

(1) Not production tested

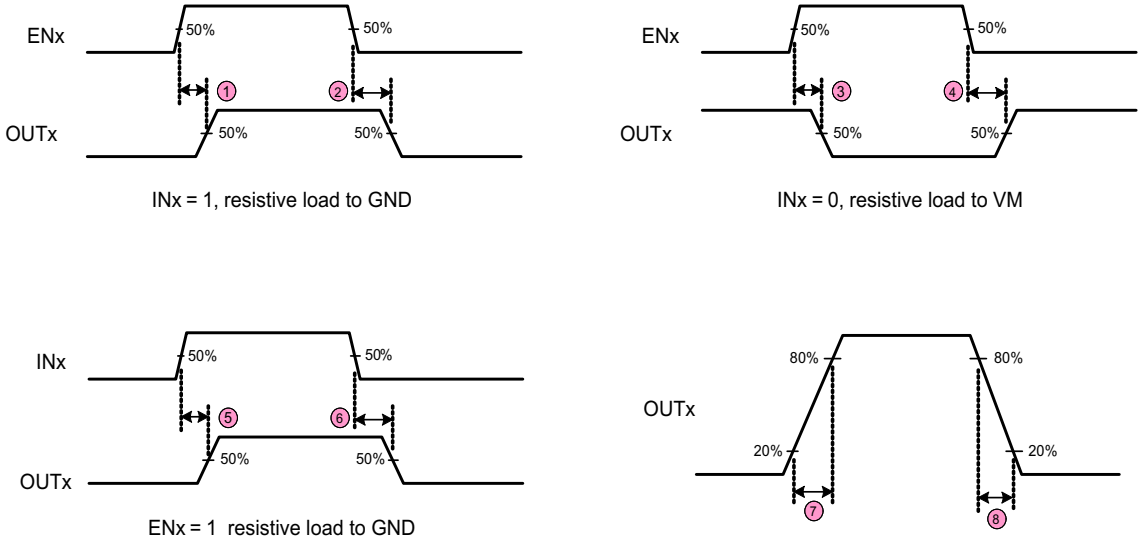


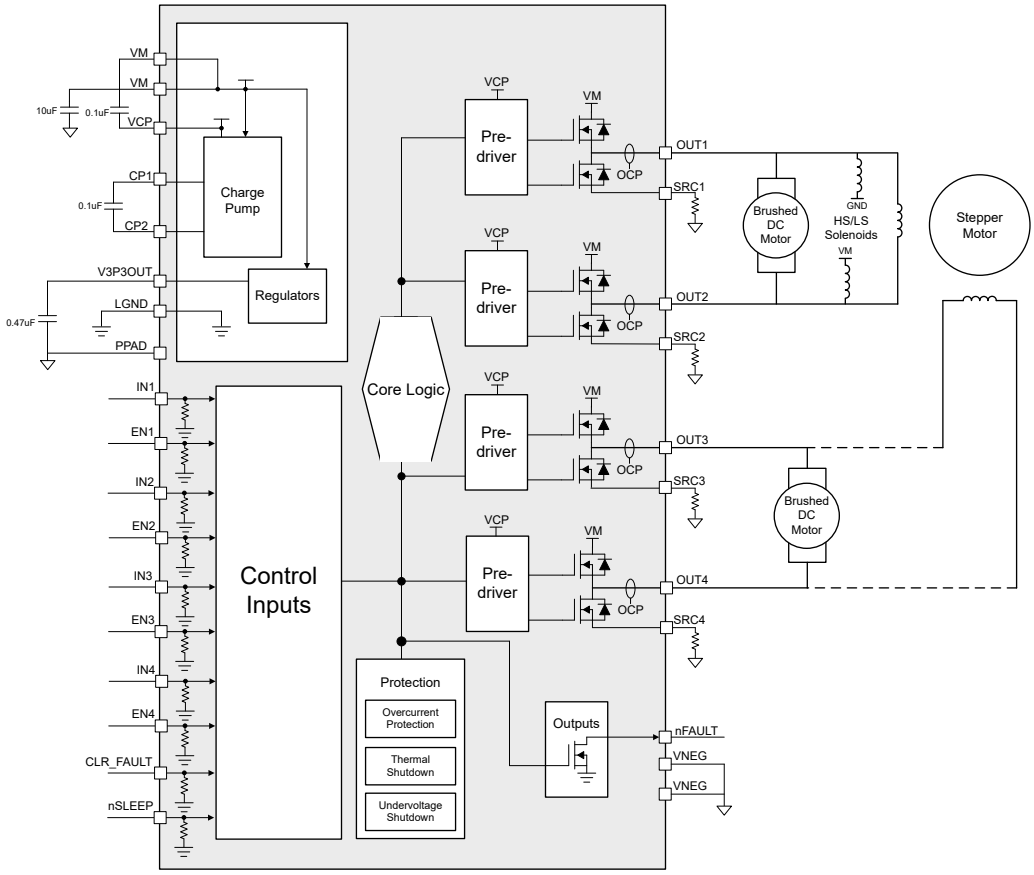
Figure 5-1. DRV8844A Switching Characteristics

6 Detailed Description

6.1 Overview

The DRV8844A integrates four independent 2.5A half-H bridges, protection circuits, sleep mode, and fault reporting. The device has a single power supply supports a wide 8 to 60V, making the device well-suited for motor drive applications, including brushed DC, steppers, and solenoids.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Output Stage

The DRV8844A contains four 1/2-H-bridge drivers using N-channel MOSFETs. A block diagram of the output circuitry is shown in Figure 6-1.

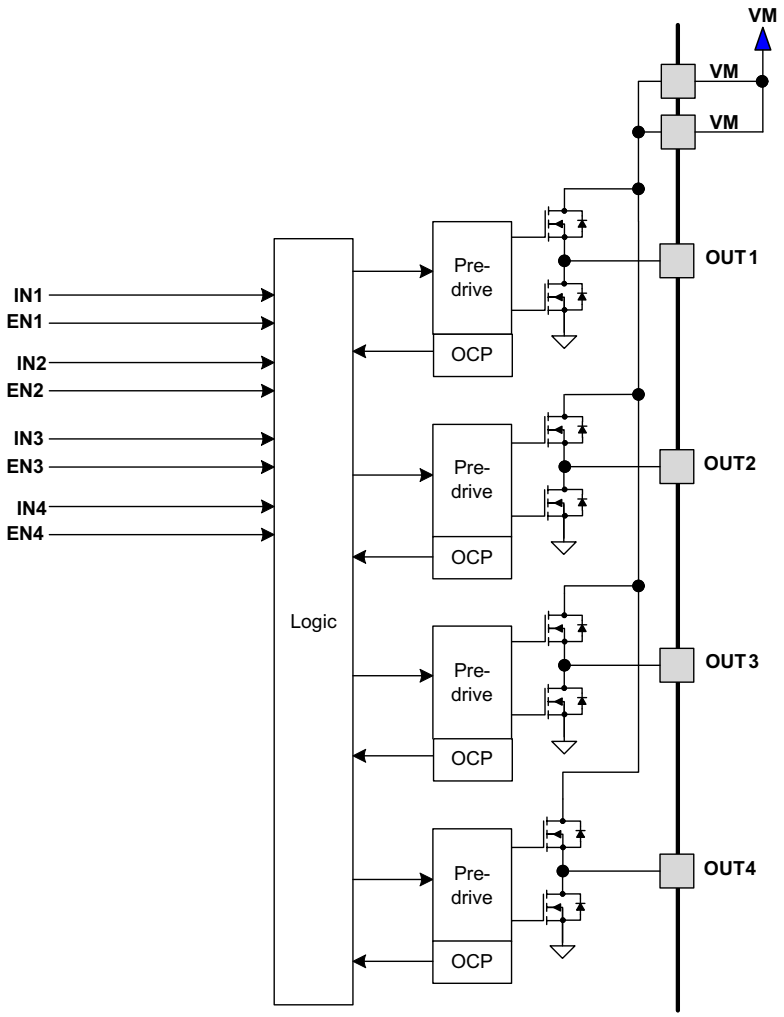


Figure 6-1. Motor Control Circuitry

The output pins are driven between VM and VNEG. VNEG is normally ground for single supply applications, and a negative voltage for dual supply applications.

Note that there are multiple VM motor power supply pins. All VM pins must be connected together to the motor supply voltage.

6.3.2 Logic Inputs

The logic inputs and nFAULT output are referenced to the LGND pin. This pin is connected to the logic ground of the source of the logic signals (for example, microcontroller). This allows LGND to be at a different voltage than VNEG; for example, the designer can drive a load with bipolar power supplies by driving VM with +24V and VNEG with -24V, and connect LGND to 0V (ground).

6.3.3 Bridge Control

The INx input pins directly control the state (high or low) of the OUTx outputs; the ENx input pins enable or disable the OUTx driver. Table 6-1 shows the logic.

Table 6-1. H-Bridge Logic

INx	ENx	OUTx
X	0	Z
0	1	L
1	1	H

The inputs can also be used for PWM control of, for example, the speed of a DC motor. When controlling a winding with PWM, when the drive current is interrupted, the inductive nature of the motor requires that the current must continue to flow. This is called recirculation current. To handle this recirculation current, the H-bridge can operate in two different states, fast decay or slow decay. In fast decay mode, the H-bridge is disabled and recirculation current flows through the body diodes; in slow decay, the motor winding is shorted.

To PWM using fast decay, the PWM signal is applied to the ENx pin; to use slow decay, the PWM signal is applied to the INx pin. Table 6-2 is an example of driving a DC motor using OUT1 and OUT2 as an H-bridge:

Table 6-2. PWM Function

IN1	EN1	IN2	EN2	FUNCTION
PWM	1	0	1	Forward PWM, slow decay
0	1	PWM	1	Reverse PWM, slow decay
1	PWM	0	PWM	Forward PWM, fast decay
0	PWM	1	PWM	Reverse PWM, fast decay

Figure 6-2 shows the current paths in different drive and decay modes:

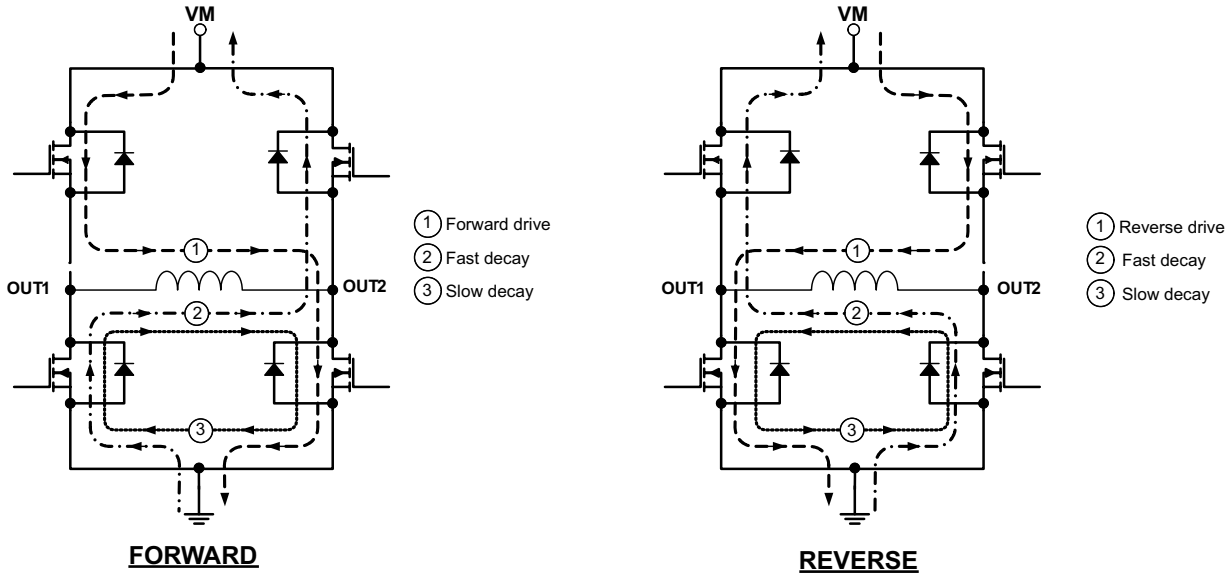


Figure 6-2. Current Paths

6.3.4 Charge Pump

Because the output stages use N-channel FETs, a gate drive voltage higher than the VM power supply is needed to fully enhance the high-side FETs. The DRV8844A integrates a charge pump circuit that generates a voltage above the VM supply for this purpose.

The charge pump requires two external capacitors for operation. Refer to the block diagram and pin descriptions for details on these capacitors (value, connection, and so forth).

The charge pump is shut down when nSLEEP is low.

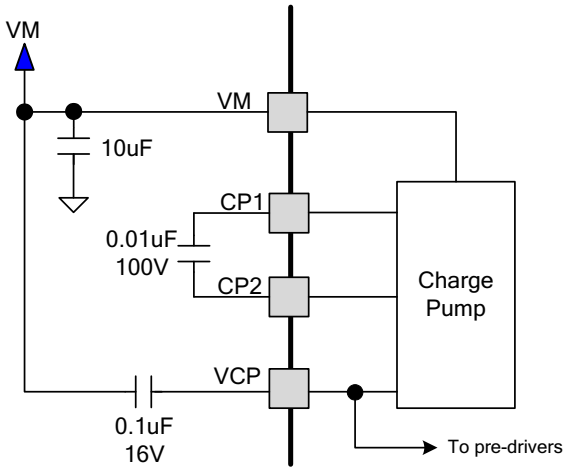


Figure 6-3. Charge Pump

6.3.5 Protection Circuits

The DRV8844A is fully protected against undervoltage, overcurrent and overtemperature events.

6.3.5.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP deglitch time, the channel experiencing the overcurrent is disabled and the nFAULT pin is driven low. The driver remains off until either RESET is asserted or VM power is cycled.

Overcurrent conditions on both high and low side devices; for example, a short to ground, supply, or across the motor winding all results in an overcurrent shutdown.

6.3.5.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge is disabled and the nFAULT pin is driven low. Once the die temperature has fallen to a safe level operation automatically resumes.

6.3.5.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pins falls below the undervoltage lockout threshold voltage, all outputs are disabled, internal logic is reset, and the nFAULT pin is driven low. Operation resumes when VM rises above the UVLO threshold.

6.3.6 CLR_FAULT and nSLEEP Operation

The CLR_FAULT pin can be used to clear Latched Over current Faults. Falling edge on this Pin resets latched OCP fault. If NFAULT is pulled low due to OCP condition, NFAULT is released by a falling edge on CLR_FAULT pin. Once latched fault is cleared, affected channels behave as dictated by the state of corresponding IN, EN pin.

Driving nSLEEP low puts the device into a low power sleep state. In this state, the H-bridges are disabled, the gate drive charge pump is stopped and all internal clocks are stopped. In this state all inputs are ignored until nSLEEP returns inactive high. When returning from sleep mode, some time (approximately 1ms) needs to pass before the motor driver becomes fully operational. Note that nRESET and nSLEEP have internal pulldown resistors of approximately 100kΩ. These signals need to be driven to logic high for device operation.

The V3P3OUT LDO regulator remains operational in sleep mode.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

7.2 Application Information

The DRV8844A can be used to drive the following types of loads

- One stepper motor
- Two brushed DC motors
- Upto four solenoid loads
  - Unipolar solenoids
  - Bipolar Solenoids

The outputs can be connected in parallel to increase the drive current. If connecting the outputs as in a full-bridge configuration, any two outputs can be connected in parallel.

7.2.1 Driving Solenoid Loads

Solenoids can be unipolar or bipolar(bistable). DRV8844A supports a unipolar (VM,0) as well as a bipolar (+VM, -VM) supply and can hence be used to drive both types of solenoid loads.

Additionally DRV8844A has independent IN and EN pins for each of the four half-bridges. All the four half-bridges also have separate SRC pins which allows a current sense resistor to be placed if desired.

The DRV8844A supports dual rail operation. Here a voltage -24V relative to LGND can be applied on VNEG and a voltage +24V relative to LGND is applied to VM. This allows a load to LGND to be pulled up to VM (charge) or pulled down to VNEG (discharge)

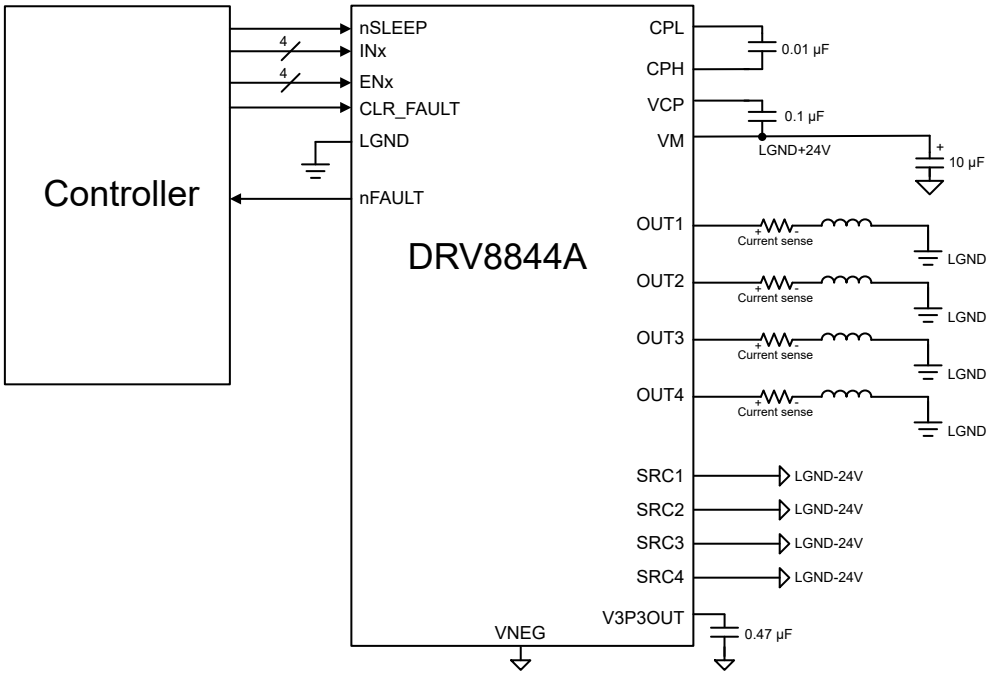


Figure 7-1. DRV8844A used to drive Bipolar solenoid load

Load connection from OUT to VLOAD allows DRV8844A to work as a pull down with active high side recirculation

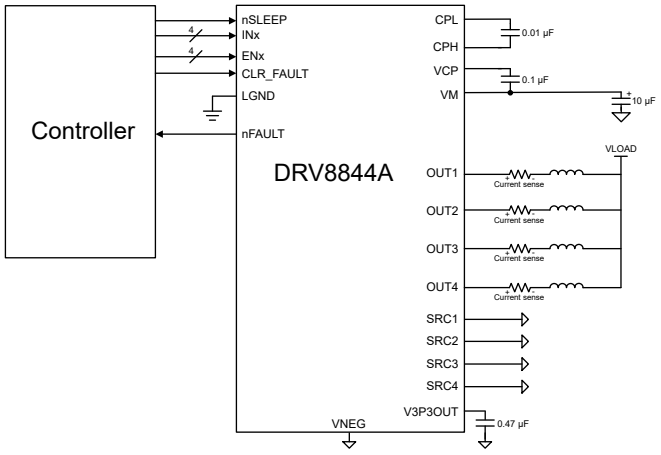


Figure 7-2. DRV8844A drive unipolar load to VLOAD (sink)

Load connection from OUT to VNEG allows DRV8844A to work as a pull up with active low side recirculation

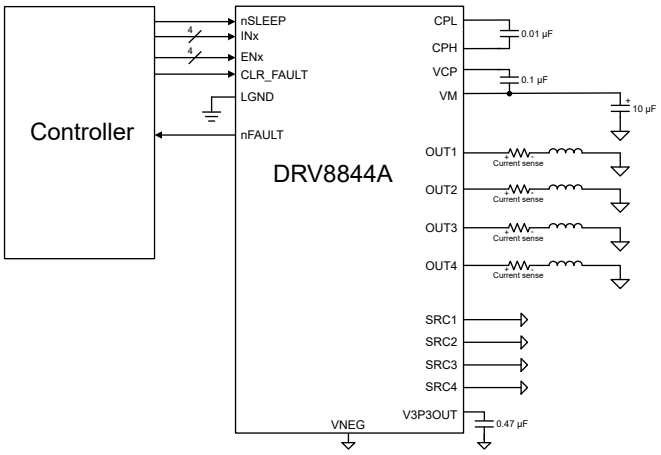


Figure 7-3. DRV8844A drive unipolar load to VNEG(source)

7.2.2 Driving Stepper Motor

The DRV8844A can drive one stepper motor using the PWM input interface.

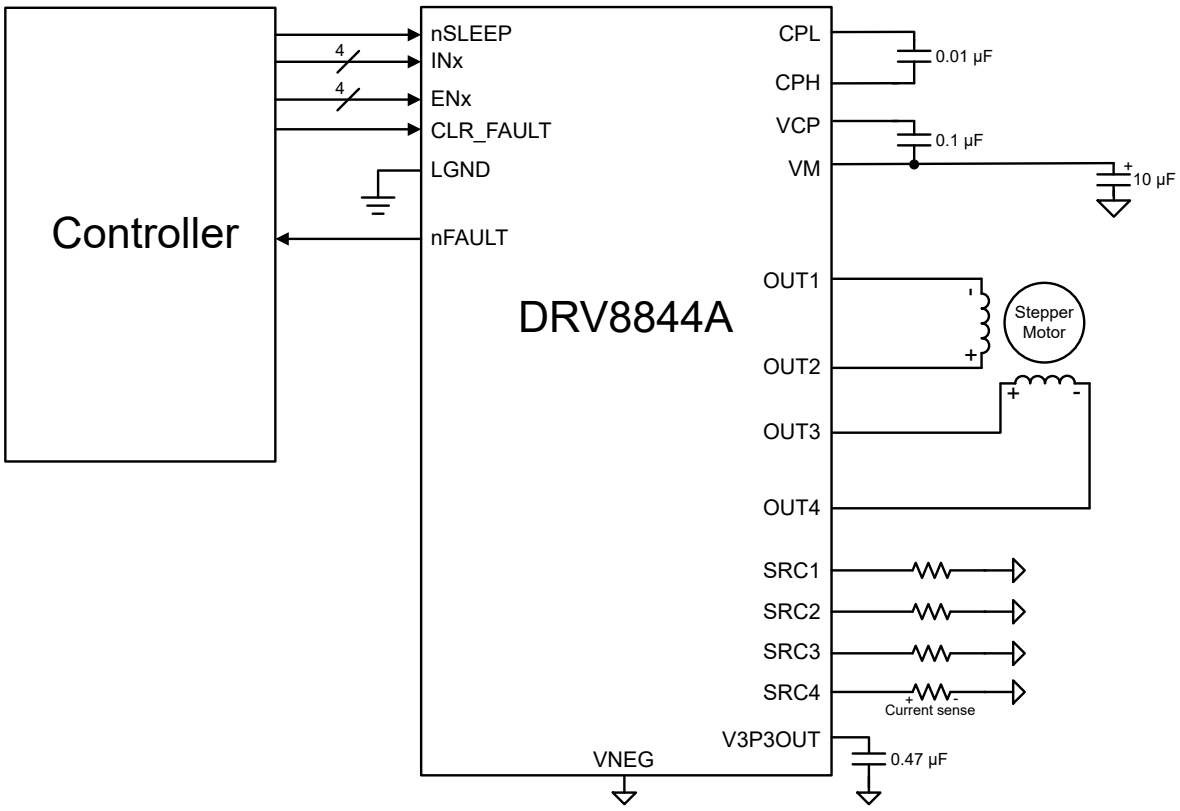


Figure 7-4. DRV8844A Used to Drive a Stepper Motor

DRV8844A allows user to connect current sense resistor for each individual half bridge for Stepper motor current regulation control

The full-scale current (I_{FS}) is the maximum current driven through either winding. The DRV8844A allows the connection of current sense resistors on the Source terminals of all 4 Half bridges which enables true bidirectional current sense needed in motor control applications. Additionally the on board 3.3V LDO can be used to provide a reference voltage for current regulation.

Note

The I_{FS} current must also follow given equation so as to avoid saturating the motor. VM is the motor supply voltage, and R_L is the motor winding resistance.

$$I_{FS}\ (A) < \frac{VM\ (V)}{R_L\ (\Omega) + 2 \times R_{DS(ON)}\ (\Omega)} \quad (1)$$

If the target motor speed is too high, the motor does not spin. Make sure that the motor can support the target speed.

For a desired motor speed (v), microstepping level (n_m), and motor full step angle (θ_{step}), determine the frequency of the input waveform as follows -

$$f_{step}\ (steps/s) = \frac{v\ (rpm) \times 360\ (°/rot)}{\theta_{step}\ (°/step) \times n_m\ (steps/microstep) \times 60\ (s/min)} \quad (2)$$

θ_{step} can be found in the stepper motor data sheet or written on the motor.

The frequency f_{step} gives the frequency of input change on the DRV8962. 1/ f_{step} = t_{STEP} on the diagram below. shows an example calculation for a 120 rpm target speed and 1/2 step.

$$f_{step}\,(\text{steps}/\text{s}) = \frac{120\ \text{rpm} \times 360^\circ/\text{rot}}{1.8^\circ/\text{step} \times 1/2\ \text{steps}/\text{microstep} \times 60\ \text{s}/\text{min}} = 800\,\text{Hz} \quad (3)$$

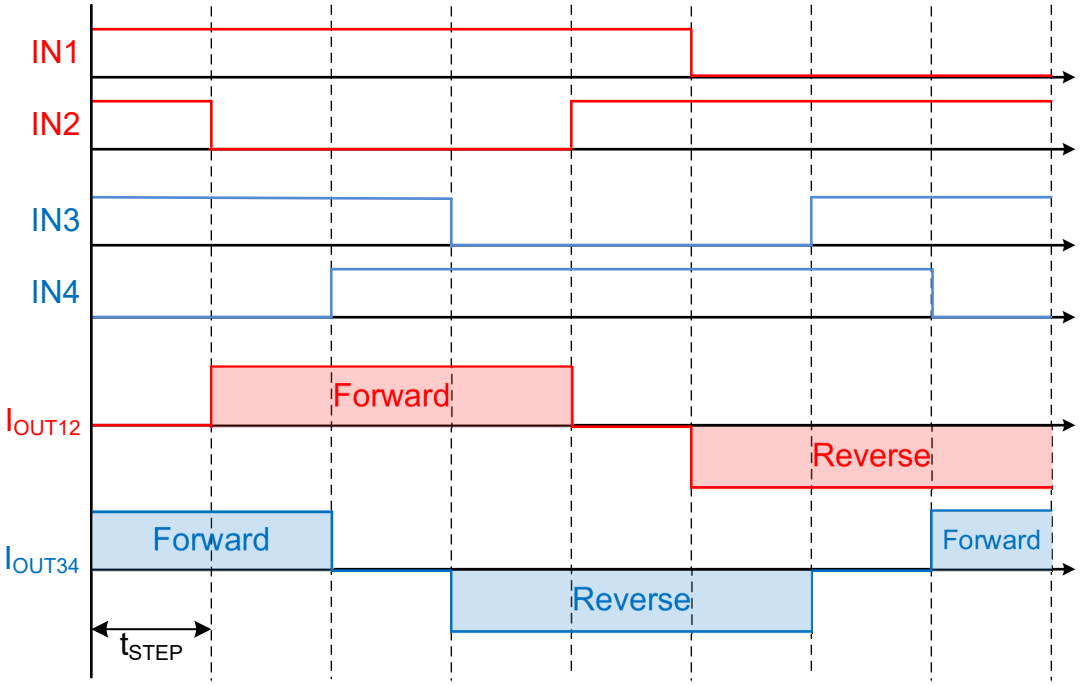


Figure 7-5. Example 1/2 Stepping Operation

7.2.3 Driving Brushed DC motor

DRV8844A can also be used to drive two BDC motors in following configuration

SRC pins of the corresponding OUTs can be tied together and common sense current resistor can be used

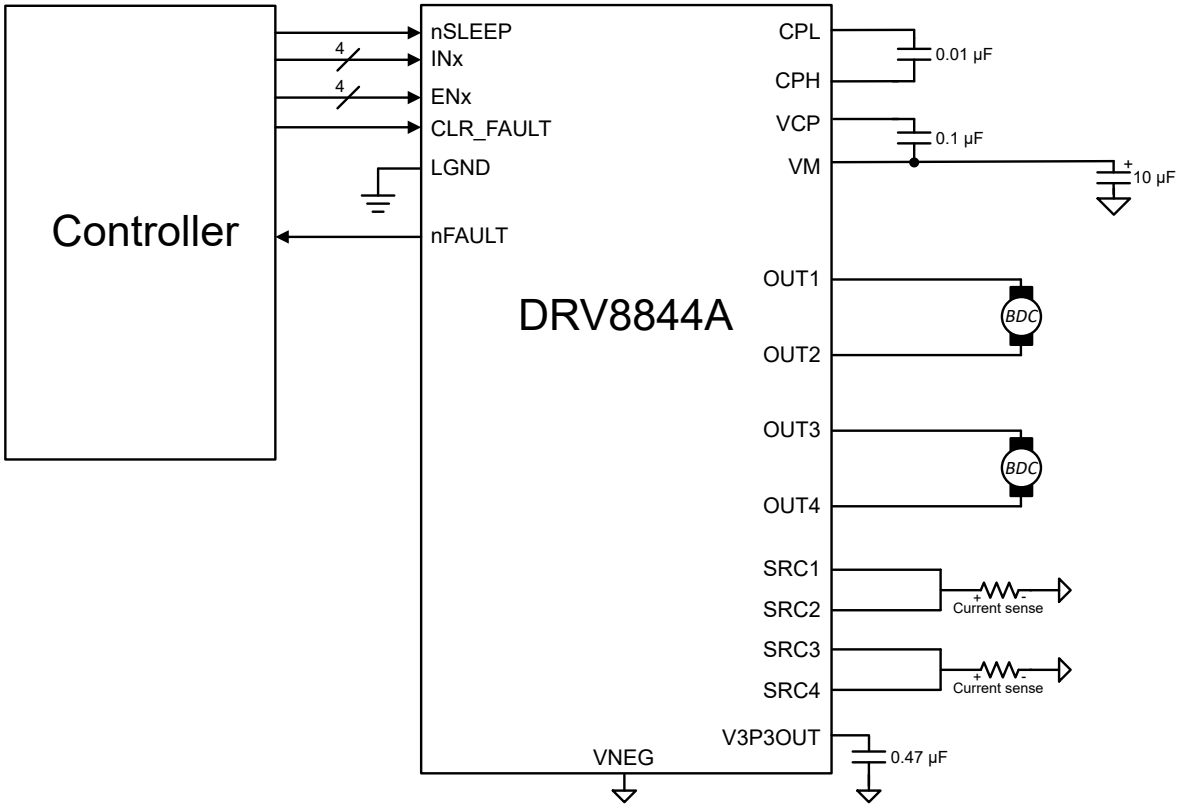


Figure 7-6. DRV8844A used to drive two BDC motors

The following truth table describes how to control brushed-DC motors.

Table 7-1. Brushed DC Motor

FUNCTION	EN1	EN2	IN1	IN2	OUT1	OUT2
Forward	1	1	PWM	0	H	L
Reverse	1	1	0	PWM	L	H
Brake	1	1	0	0	L	L
Brake	1	1	1	1	H	H
Coast	0	X	X	X	Z	X
Coast	X	0	X	X	X	Z

7.3 Power Supply Recommendations

The DRV8844A is designed to support floating logic rail referenced to LGND. The LGND can be any voltage between VNEG and VM-8V. VM can be 8V-70V relative to VNEG. A 10µF capacitor must bypass to the VNEG pin.

7.3.1 Bulk Capacitance

Appropriate local bulk capacitance is an important factor in motor drive system design. Having more bulk capacitance is generally beneficial, although the disadvantages include increased cost and physical size. Bulk capacitors near the motor driver act as a local reservoir of electrical charge to smooth out the motor current variation.

Experienced engineers often use general guidelines about bulk capacitance to select the capacitor values. One such guideline says to use at least 1 to 4µF of capacitance for each Watt of motor power. For example, a motor which draws 2 Amps from a 24V supply has a power of 48 Watts, leading to bulk capacitance of 48 to 192µF, using this general guideline.

The voltage rating for bulk capacitors must be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

A large value of bulk capacitance is desired to provide a constant motor supply voltage during current transitions, such as motor start-up, changes in load torque, or PWM operation. A working estimate of the required capacitance for consistent supply is essential to reduce complexity, cost and size of board electronics. We can use a general guideline method to find an appropriate capacitor size based on the expected load current variation and allowable motor supply voltage variation:

$$C_{BULK} > k \quad \times \quad \Delta I_{MOTOR} \times T_{PWM} / \Delta V_{SUPPLY} \tag{4}$$

Where:

C_{BULK} is the bulk capacitance

k is a scale factor to account for the ESR for typical capacitors in this type of application; based on the lab measurements with DRV8718-Q1EVM, k ≈ 3 is practical for these cases.

ΔI_{MOTOR} is the expected variation in motor current, $i_{max} - i_{min}$

T_{PWM} is the PWM period which is the reciprocal of the PWM frequency

ΔV_{SUPPLY} is the allowable variation in the motor supply voltage

Figure 7-7 plots several data points and applies this general guideline, showing relatively good agreement.

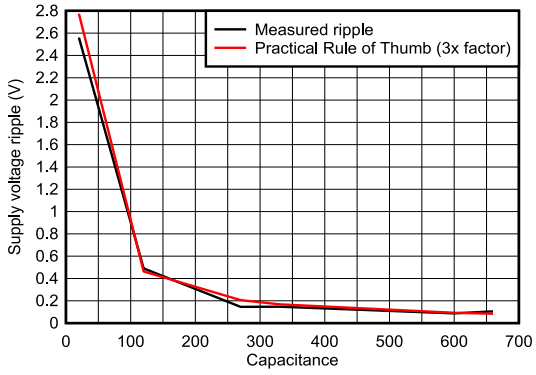


Figure 7-7. Measured Results and 3x General Guideline, Accounting for Real-World Non-Zero ESR Values of Electrolytic Capacitors

For more information please see the Application Note Bulk Capacitor Sizing for DC Motor Drive Applications .

7.4 Layout

7.4.1 Layout Guidelines

- The VM pins are bypassed to VNEG pins using low-ESR ceramic bypass capacitors with a recommended value of 0.1µF rated for VM. The capacitors are placed as close to the VM pins as possible with a thick trace or ground plane connection to the device VNEG pins.
- A low-ESR ceramic capacitor must be placed in between the CP1 and CP2 pins. A value of 0.01µF rated for VM is recommended. Place this component as close to the pins as possible.
- A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. A value of 0.1µF rated for 16V is recommended. Place this component as close to the pins as possible.
- Bypass the V3P3OUT pin to ground with a low-ESR ceramic capacitor. A value of 0.47µF rated for 6.3V is recommended. Place this bypassing capacitor as close to the pin as possible.
- In general, inductance between the power supply pins and decoupling capacitors must be avoided.
- The thermal PAD of the package must be connected to system ground.
  - Try to use a big unbroken single ground plane for the whole system / board. The ground plane can be made at bottom PCB layer. Figure 7-8 shows an example of temperature rise from constricted versus continuous ground pours underneath the driver.
  - To minimize the impedance and inductance, the traces from ground pins are as short and wide as possible, before connecting to bottom layer ground plane through vias.
  - Multiple vias are suggested to reduce the impedance.
  - Try to clear the space around the device as much as possible especially at bottom PCB layer to improve the heat spreading.
  - Single or multiple internal ground planes connected to the thermal PAD also help spread the heat and reduce the thermal resistance.
- For more layout guidelines and best practices see the Application Note Best Practices for Board Layout of Motor Drivers.

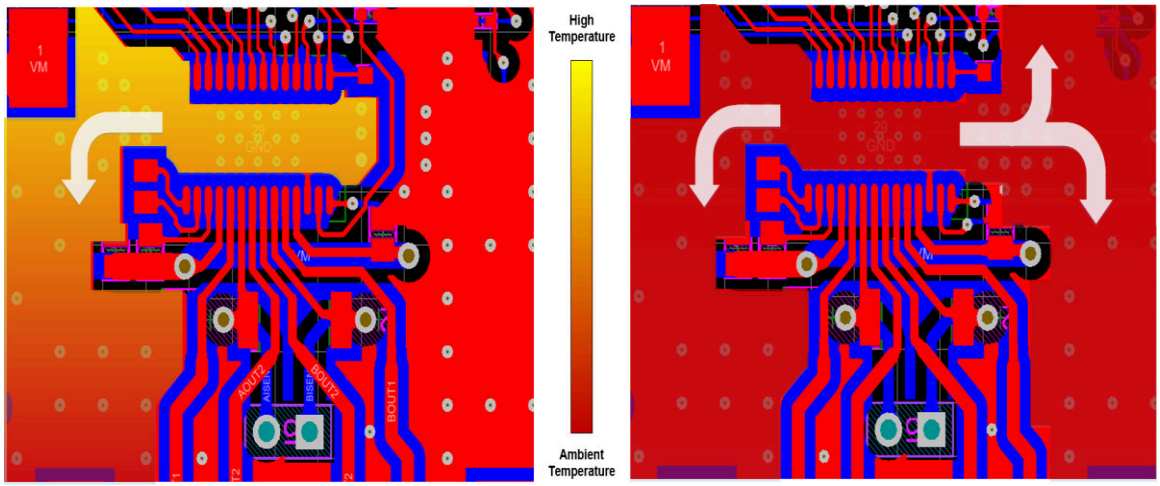


Figure 7-8. Broken Ground vs Continuous Ground Pour Heat Map

7.4.2 Layout Example

Follow the layout example of the DRV8844A EVM. The Altium design files can be downloaded from the DRV8844AEVM product folder.

7.4.3 Thermal Considerations

The DRV8844A has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device is disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

7.4.3.1 Heatsinking

The DGQ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

In general, the more copper area that can be provided, the more power can be dissipated.

7.4.4 Power Dissipation

Power dissipation in the DRV8844A is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Average power dissipation of each H-bridge when running a DC motor can be roughly estimated by Equation 5.

$$P = 2 \times R_{DS(ON)} \times (I_{OUT})^2 \quad (5)$$

where

- P is the power dissipation of one H-bridge
- $R_{DS(ON)}$ is the resistance of each FET
- I_{OUT} is the RMS output current being applied to each winding

I_{OUT} is equal to the average current drawn by the DC motor. Note that at start-up and fault conditions this current is much higher than normal running current; these peak currents and the duration also need to be taken into consideration. The factor of 2 comes from the fact that at any instant two FETs are conducting winding current (one high-side and one low-side).

The total device dissipation is the power dissipated in each of the two H-bridges added together.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

- *Calculating Motor Driver Power Dissipation*, SLVA504
- *DRV8844A Evaluation Module*
- *Understanding Motor Driver Current Ratings*, SLVA505

8.2 Community Resources

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2025	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8844ADGQR	Active	Production	HVSSOP (DGQ) | 28	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	8844A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

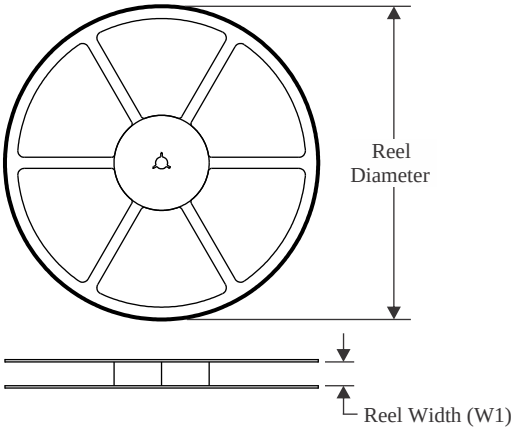
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

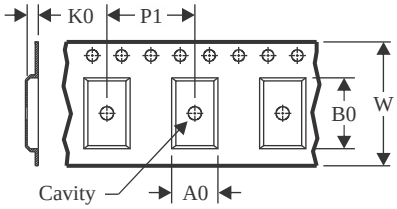
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

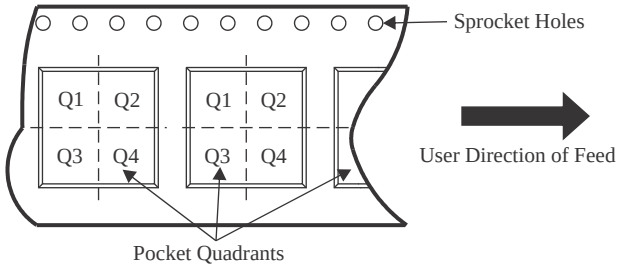


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

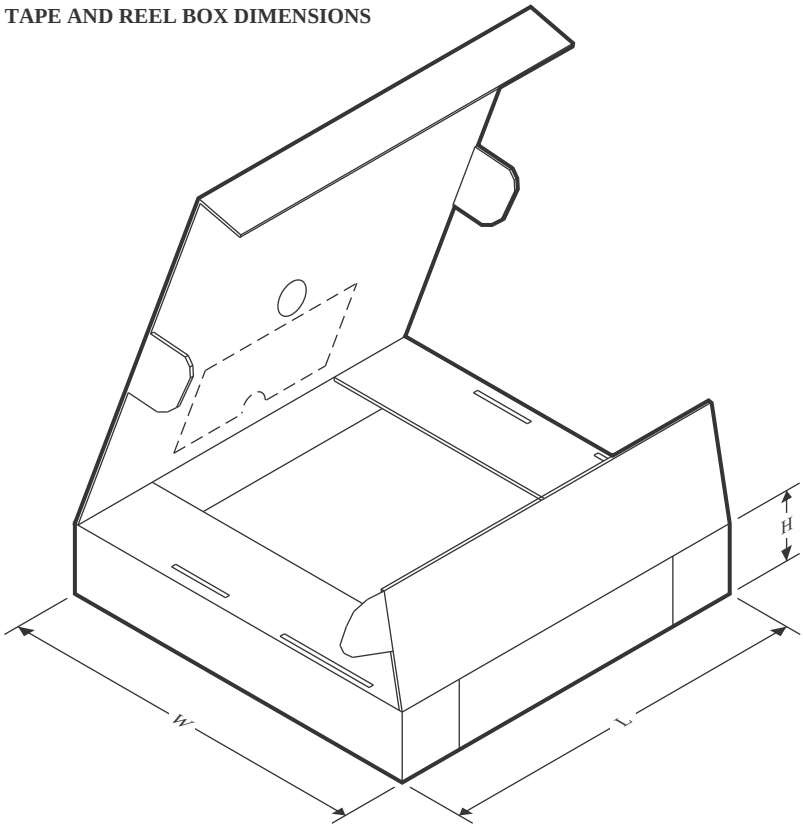
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8844ADGQR	HVSSOP	DGQ	28	2500	330.0	16.4	5.5	7.4	1.45	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8844ADGQR	HVSSOP	DGQ	28	2500	353.0	353.0	32.0

GENERIC PACKAGE VIEW

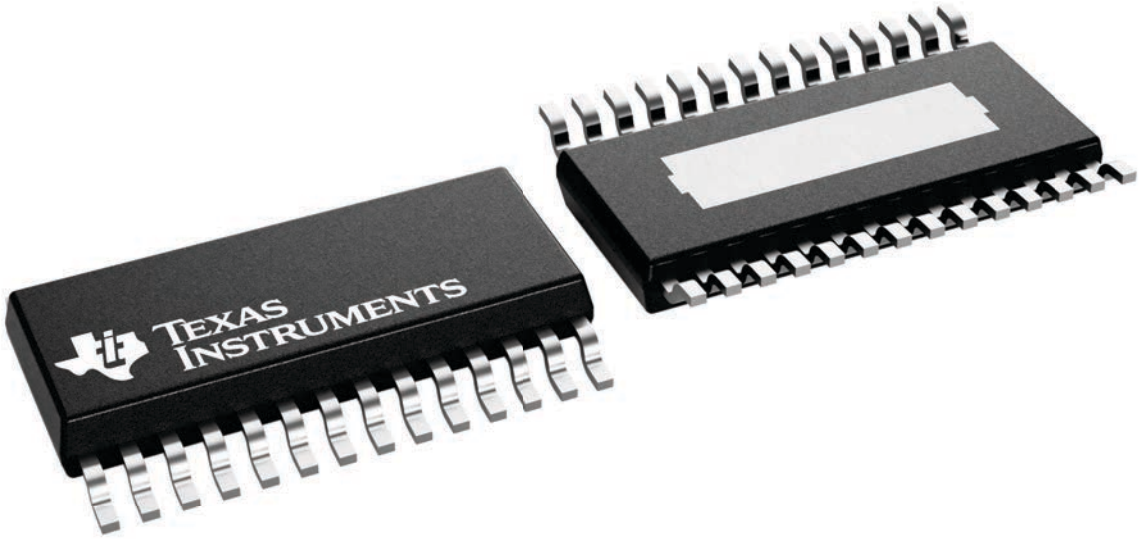
DGQ 28

HVSSOP - 1.1 mm max height

3 x 7.1, 0.5 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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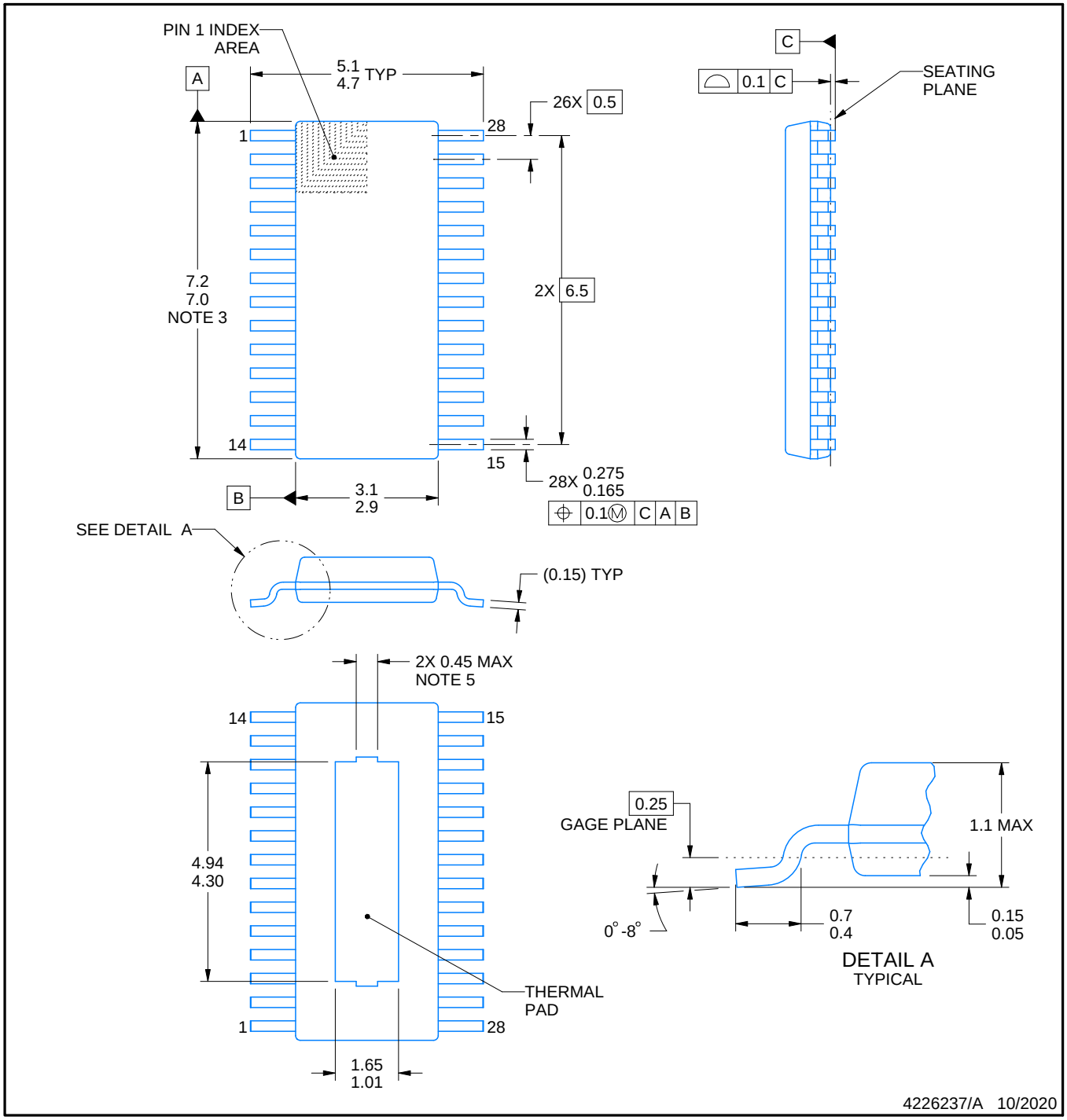
PACKAGE OUTLINE

DGQ0028A

PowerPAD™ VSSOP - 1.1 mm max height

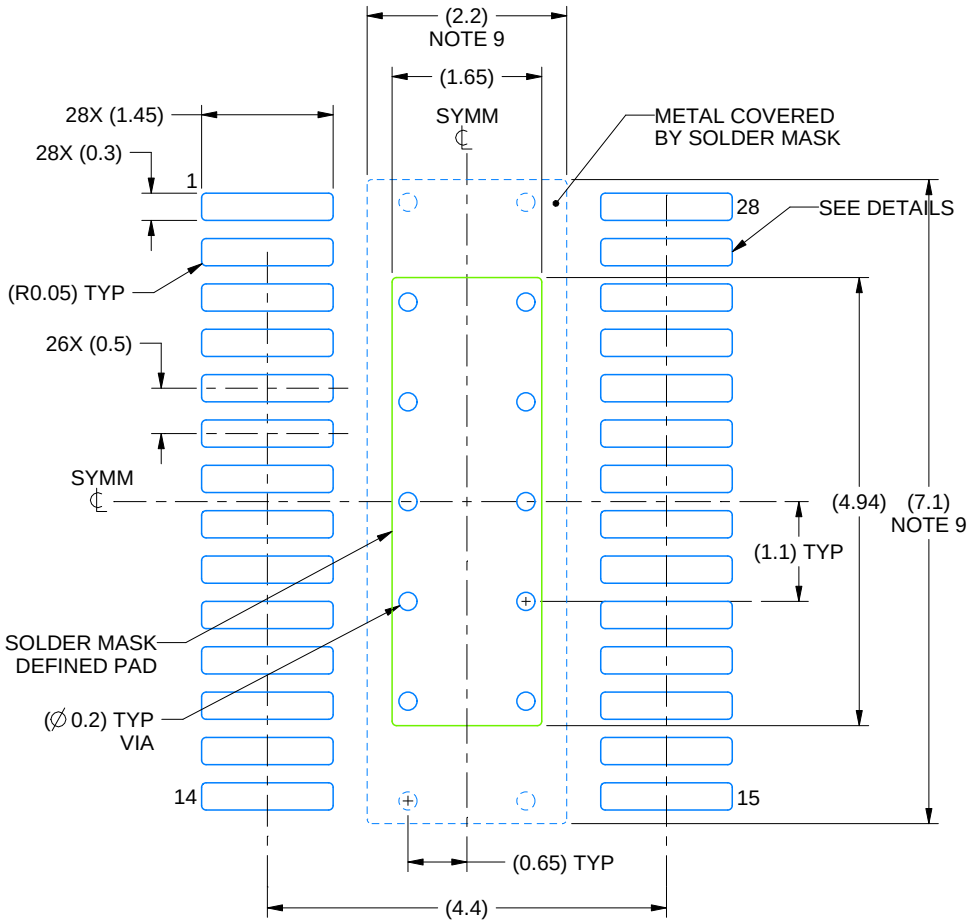
SMALL OUTLINE PACKAGE



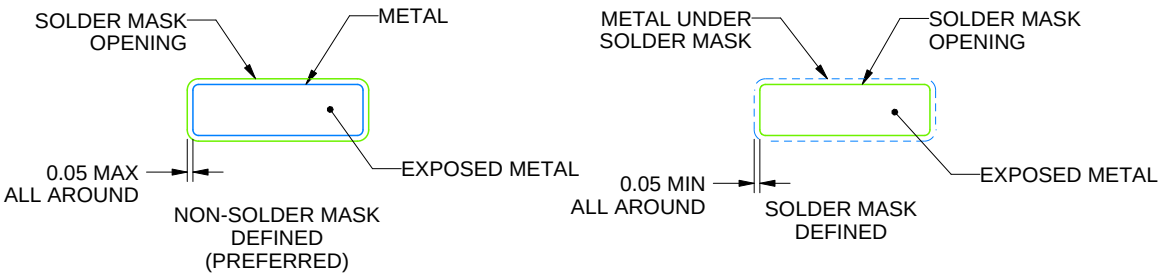
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

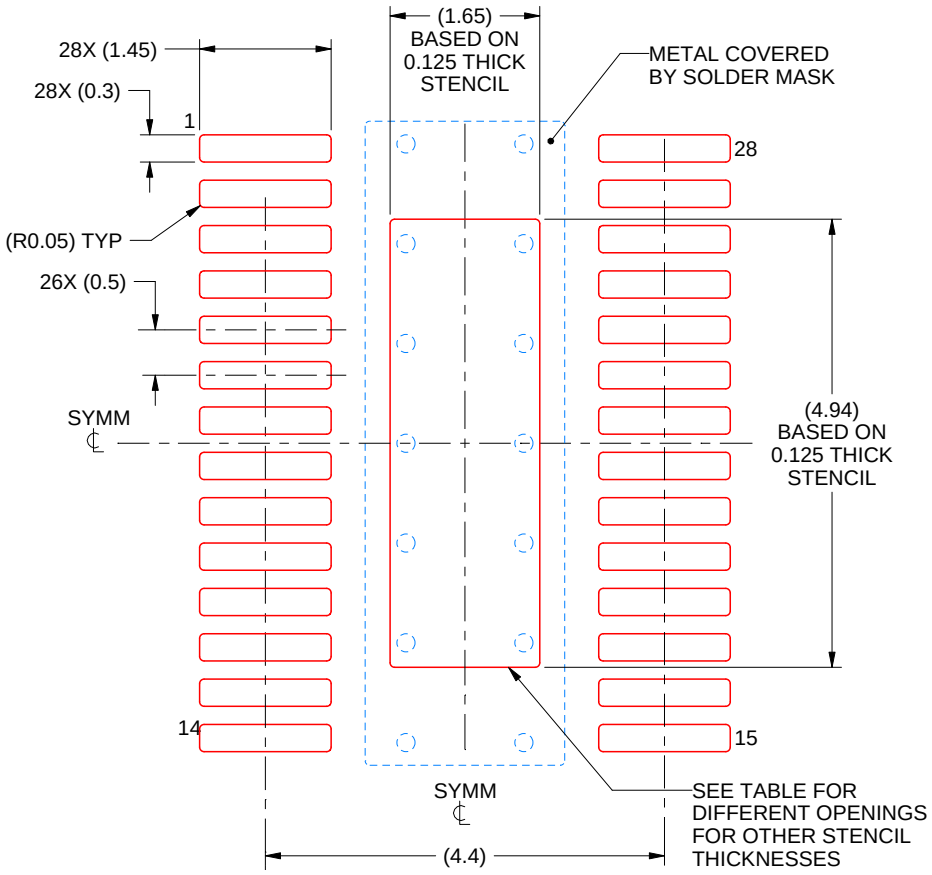


SOLDER MASK DETAILS

4226237/A 10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.84 X 5.52
0.125	1.65 X 4.94 (SHOWN)
0.15	1.51 X 4.51
0.175	1.39 X 4.18

4226237/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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