# DS560DF810 56 Gbps Multi-Rate 8-Channel Retimer with Crosspoint

## 1 Features

- -channel multi-protocol retimer with integrated signal conditioning
- All channels lock independently to both PAM4 and NRZ data rates from 19.6 to 28.9 GBd (including div-by-2 and div-by-4 sub-rates)
- Suitable for up to CEI-56G, Ethernet™ (400 GbE), fibre channel (64GFC), InfiniBand™ (HDR), and CPRI/eCPRI PCB, copper cable, and optical applications
- Automatic lane rate switching for CDR lock up to five different combinations of baud rates and modulation types
- Low latency: <2000 ps (typical) at 26.5625 GBd
- Continuously adaptive time linear equalizer (CTLE), RX feed-forward equalizer (FFE), and decision feedback equalizer (DFE) to support 30+ dB channel loss at 13.28 GHz
- Integrated 2×2 crosspoint
- Adjustable 4-tap TX FFE filter
- Gearbox mode support (NRZ/PAM4 bit mux/de-mux, NRZ/PAM4 serializer/deserializer)
- On-chip eye opening monitor (EOM), PRBS generator, and PRBS checker for debug
- Dual 1.8-V and 1.2-V supplies
- –40°C to +85°C operating temperature range
- 8.00 mm × 13.00 mm BGA package with integrated AC coupling capacitors

## 2 Applications

- Active electrical cables (AEC) (QSFP-DD, OSFP)
- Front-port C2M attachment unit interface (AUI) jitter cleaning
- Backplane (KR) and midplane C2C attachment unit interface (AUI) reach extension
- Speed doubling (gearbox) with NRZ-to-PAM4 aggregation and de-aggregation

## 3 Description

The DS560DF810 is an eight-channel multi-rate retimer with integrated signal conditioning. It extends the reach and robustness of long, lossy, crosstalk-impaired high-speed serial links.

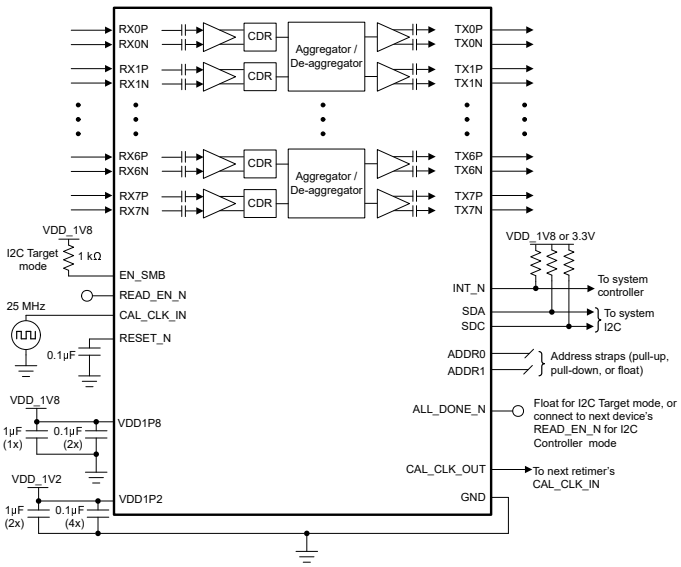
Each channel in the DS560DF810 independently locks to symbol rates (PAM4 and NRZ) in a continuous range from 19.6 to 28.9 GBd or to any supported sub-rate. The integrated CDR function is an excellent choice for front-port optical module applications to reset the jitter budget and retime the high-speed serial data. These features allow for individual lane forward error correction (FEC) pass-through. In addition, the DS560DF810 supports automatic lane rate switching for CDR lock up to five different combinations of baud rates and modulation types without host intervention.

The advanced equalization features of the DS560DF810 include a continuously adaptive continuous-time linear equalizer (CTLE), RX feed-forward equalizer (FFE), decision feedback equalizer (DFE), and a programmable, low-jitter 4-tap TX feed-forward equalizer (FFE) filter. These features enable reach extension for lossy interconnects such as direct-attach copper (DAC) cables and backplanes with multiple connectors and crosstalk.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| DS560DF810 | ALU (fcBGA, 135) | 13 mm × 8 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Simplified Schematic**

# Table of Contents



## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (December 2022) to Revision B (June 2023) | Page |
|---|---|
| • Added PAM4 serializer or deserializer support in the *Features* section | 1 |
| • Updated the *Package Information* table format to include package leads | 1 |

| Changes from Revision * (October 2021) to Revision A (December 2022) | Page |
|---|---|
| • Changed the status of the data sheet from: *Advanced Information* to: *Production Data* | 1 |

## 5 Description (continued)

The DS560DF810 is equipped with a bit mux and de-mux gearbox for simple NRZ-to-PAM4 or PAM4-to-NRZ conversion between host and module. The gearbox is capable of aggregating a pair of NRZ inputs up to 28.9 GBd into one 28.9 GBd PAM4 output as well as de-aggregating a single 28.9 GBd PAM4 input into a pair of 28.9 GBd NRZ outputs.

The DS560DF810 implements a full 2×2 crosspoint between each pair of adjacent channels after the CDR to enable fast and flexible lane switching for PCB routing flexibility, 2-to-1 multiplexing and 1-to-2 de-multiplexing for failover redundancy, and 1-to-2 fanout for diagnostic monitoring. In addition, integrated physical AC coupling capacitors (TX and RX) eliminate the need for external capacitors on the PCB. These features reduce PCB routing complexity and bill of material (BOM) cost.

Diagnostic capabilities include a non-destructive PAM4/NRZ vertical eye height monitor, a 2D PAM4/NRZ eye opening monitor (EOM), PRBS pattern generator with error injector module, PRBS error checker, and on-die temperature sensor. These features help to gauge the margin of the link and can be used to monitor the health of the system over time.

The DS560DF810 can be configured either through $I^2C$ or through an external EEPROM. Up to 16 devices can share a single EEPROM.

# 6 Device and Documentation Support

## 6.1 Documentation Support

### 6.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *DS560DFXX0 Programmer's Guide*
- Texas Instruments, *DS560DF810EVM User's Guide*
- Texas Instruments, *Implementation of TI 56Gbps PAM4 Retimers in Direct Attach Copper Cable Applications*

## 6.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 6.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 6.4 Trademarks

Ethernet™ is a trademark of Fuji Xerox Co., Ltd.
InfiniBand™ is a trademark of InfiniBand Trade Association.
TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 6.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 6.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| DS560DF810ALUR | Active | Production | FCCSP (ALU) \| 135 | 1000 \| LARGE T&R | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 85 | DS560DF8E0 |
| DS560DF810ALUT | Active | Production | FCCSP (ALU) \| 135 | 250 \| LARGE T&R | Yes | SNAGCU | Level-3-260C-168 HR | -40 to 85 | DS560DF8E0 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

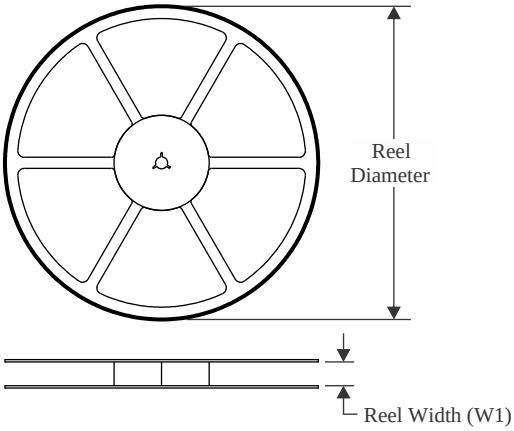
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

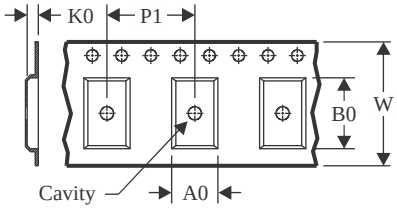
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

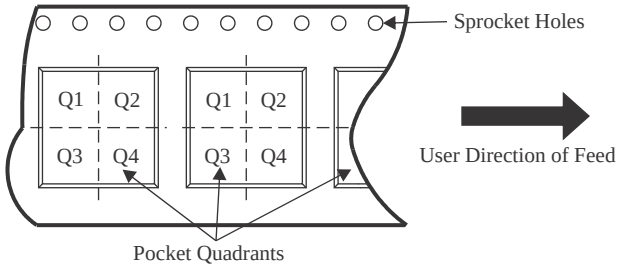



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

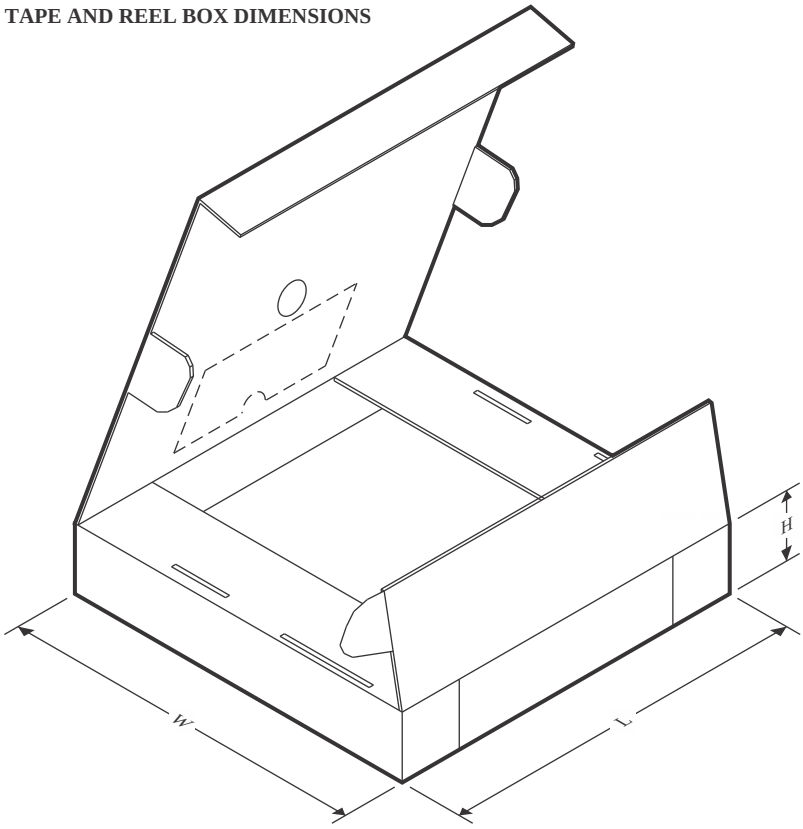
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DS560DF810ALUR | FCCSP | ALU | 135 | 1000 | 330.0 | 24.4 | 8.4 | 13.4 | 2.45 | 12.0 | 24.0 | Q2 |
| DS560DF810ALUT | FCCSP | ALU | 135 | 250 | 330.0 | 24.4 | 8.4 | 13.4 | 2.45 | 12.0 | 24.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

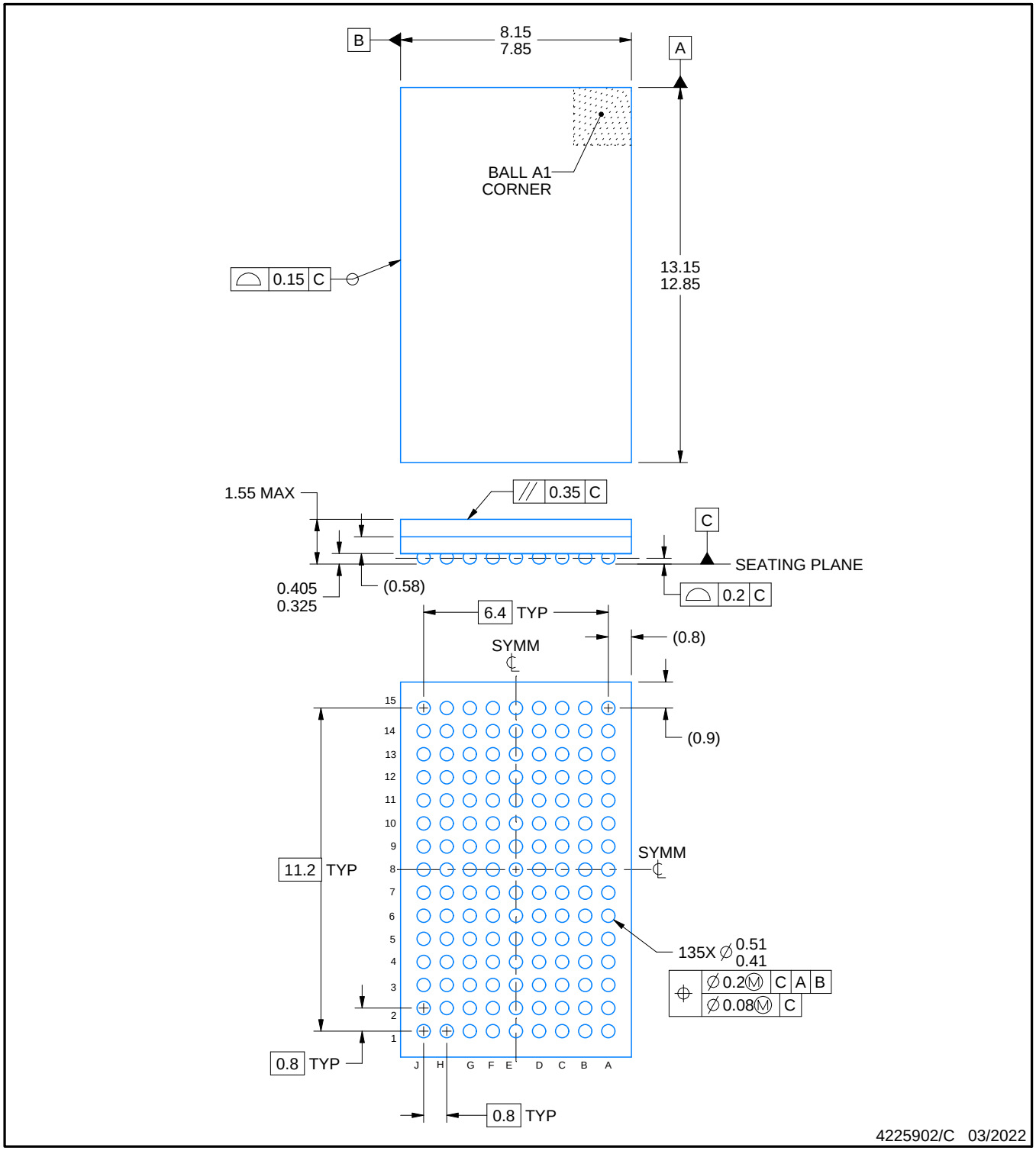
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| DS560DF810ALUR | FCCSP | ALU | 135 | 1000 | 336.6 | 336.6 | 41.3 |
| DS560DF810ALUT | FCCSP | ALU | 135 | 250 | 336.6 | 336.6 | 41.3 |

# PACKAGE OUTLINE

## ALU0135A

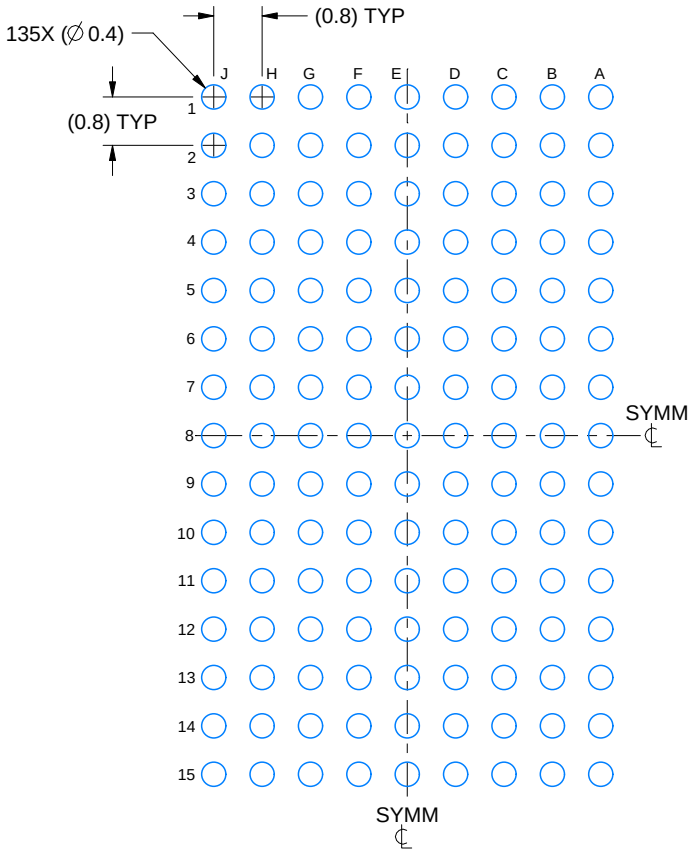
## FCBGA - 1.55 mm max height

PLASTIC BALL GRID ARRAY

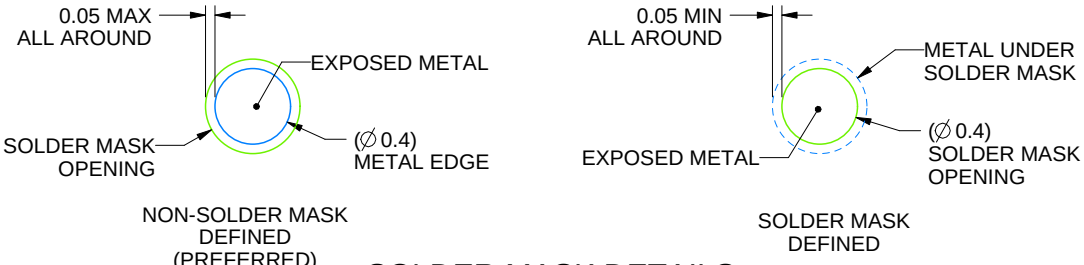



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X




SOLDER MASK DETAILS
NOT TO SCALE

4225902/C 03/2022

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

4225902/C 03/2022

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.



Last updated 10/2025