

ISO7041-Q1 Automotive, Ultra-Low Power Four-Channel Digital Isolator

1 Features

- AEC-Q100 qualified with the following results:
 - Device temperature Grade 1: -40°C to $+125^{\circ}\text{C}$ ambient operating temperature range
- **Functional Safety-Capable**
 - Documentation available to aid functional safety system design: [ISO7041-Q1](#)
- Meets VDA320 isolation requirements
- Ultra-low power consumption
 - $3.5 \mu\text{A}$ per channel quiescent current (3.3 V)
 - $15 \mu\text{A}$ per channel at 100 kbps (3.3 V)
 - $116 \mu\text{A}$ per channel at 1 Mbps (3.3 V)
- Robust isolation barrier
 - >100 -year projected lifetime
 - $3000 \text{ V}_{\text{RMS}}$ isolation rating
 - $\pm 100 \text{ kV}/\mu\text{s}$ typical CMTI
- Wide supply range: 3.0 V to 5.5 V
- Wide temperature range: -40°C to $+125^{\circ}\text{C}$
- Small 16-QSOP package (16-DBQ)
- Signaling rate: Up to 4 Mbps
- Default output *High* (ISO7041-Q1) and *Low* (ISO7041F-Q1) options
- Robust electromagnetic compatibility (EMC)
 - System-level ESD, EFT, and surge immunity
 - $\pm 8 \text{ kV}$ IEC 61000-4-2 contact discharge protection across isolation barrier
 - Very low emissions
- Safety-related certifications (planned):
 - DIN V VDE 0884-11:2017-01
 - UL 1577 Component Recognition Program
 - IEC 60950-1, IEC 62368-1, IEC 61010-1, IEC60601-1 and GB 4943.1-2011 certifications

2 Applications

- **Hybrid, electric and powertrain system (EV/HEV)**
 - **Battery management system (BMS)**
 - **On-board charger**
 - **Traction inverter**
 - **DC/DC converter**
 - **Inverter and motor control**

3 Description

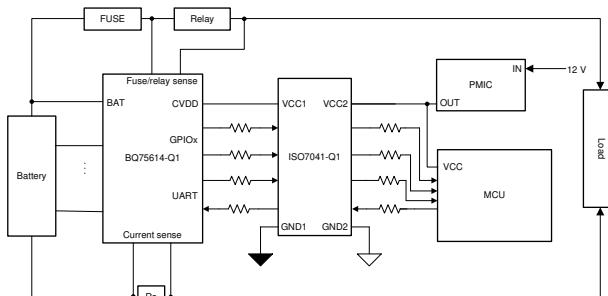
The ISO7041-Q1 device is an ultra-low power, multichannel digital isolator that can be used to isolate CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide (SiO_2) insulation barrier. Innovative edge based architecture combined with an ON-OFF keying modulation scheme allows these isolators to consume very-low power while meeting 3000-V_{RMS} isolation rating per UL1577. The per channel dynamic current consumption of the device is under 120 $\mu\text{A}/\text{Mbps}$ and the per channel static current consumption is 3.5 μA at 3.3 V, allowing for use of the ISO7041-Q1 in both power and thermal constrained system designs.

The device can operate as low as 3.0 V, as high as 5.5 V, and is fully functional with different supply voltages on each side of isolation barrier. The four channel isolator comes in a 16-QSOP package with three forward-direction channels and one reverse-direction channel. The device has default output high and low options. If the input power or signal is lost, default output is *high* for the ISO7041-Q1 device without the suffix F and *low* for the ISO7041F-Q1 device with the F suffix. See the [Device Functional Modes](#) section for more information.

Device Information

PART NUMBER ⁽¹⁾	PACKAGE	BODY SIZE (NOM)
ISO7041-Q1	QSOP (16)	4.90 mm \times 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application Schematic



An **IMPORTANT NOTICE** at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. **PRODUCTION DATA**.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2022	*	Initial Release

Device Comparison Table

Table 5-1. Device Features

PART NUMBER	CHANNEL DIRECTION	MAXIMUM DATA RATE	DEFAULT OUTPUT	PACKAGE	RATED ISOLATION
ISO7041-Q1	3 Forward, 1 Reverse	4 Mbps	High	DBQ-16	3000 V _{RMS} / 4242 V _{PK}
ISO7041-Q1 with F suffix	3 Forward, 1 Reverse	4 Mbps	Low	DBQ-16	3000 V _{RMS} / 4242 V _{PK}

5 Pin Configuration and Functions

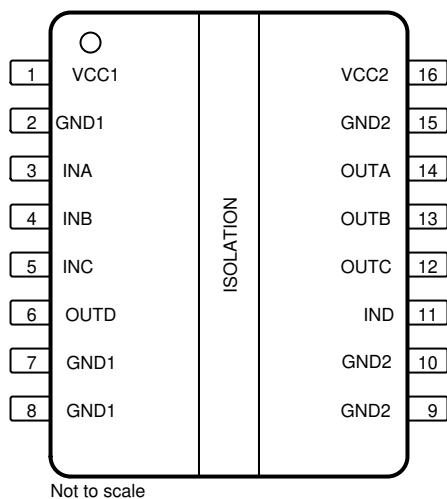


Figure 5-1. ISO7041-Q1 DBQ Package 16-Pin QSOP Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND1	2	—	Ground connection for V _{CC1}
	7		
	8		
GND2	9	—	Ground connection for V _{CC2}
	10		
	15		
INA	3	I	Input, channel A. 300- Ω series resistor recommended
INB	4	I	Input, channel B. 300- Ω series resistor recommended
INC	5	I	Input, channel C. 300- Ω series resistor recommended
IND	11	I	Input, channel D. 300- Ω series resistor recommended
OUTA	14	O	Output, channel A. 300- Ω series resistor recommended
OUTB	13	O	Output, channel B. 300- Ω series resistor recommended
OUTC	12	O	Output, channel C. 300- Ω series resistor recommended
OUTD	6	O	Output, channel D. 300- Ω series resistor recommended
V _{CC1}	1	—	Power supply, side 1
V _{CC2}	16	—	Power supply, side 2

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (2) (3)}

		MIN	MAX	UNIT
Supply Voltage	V _{CC1} to GND1	-0.5	6	V
	V _{CC2} to GND2	-0.5	6	
Input/Output Voltage	IN _x to GND _x	-0.5	V _{CCX} + 0.5	V
	OUT _x to GND _x	-0.5	V _{CCX} + 0.5	
	EN _x to GND _x	-0.5	V _{CCX} + 0.5	
Input Current	Input Channels, I _i	-15	15	mA
Output Current	I _o	-15	15	mA
Temperature	Operating junction temperature, T _J		150	°C
	Storage temperature, T _{stg}	-65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values
- (3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

^{(1) (2)}

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±5000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1500	
		Contact discharge per IEC 61000-4-2; Isolation barrier withstand test ^{(3) (4)}	±8000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
- (3) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
- (4) Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC1} ⁽¹⁾	Supply Voltage Side 1		3.0		5.5	V
V_{CC2} ⁽¹⁾	Supply Voltage Side 2		3.0		5.5	V
V_{IH}	High level Input voltage		0.7 x V_{CCI}		V_{CCI}	V
V_{IL}	Low level Input voltage		0		0.3 x V_{CCI}	V
I_{OH}	High level output current	V_{CCO} ⁽²⁾ = 5 V	-4			mA
		V_{CCO} = 3.3 V	-2			mA
I_{OL}	Low level output current	V_{CCO} = 5 V		4		mA
		V_{CCO} = 3.3 V		2		mA
DR	Data Rate		0		4	Mbps
T_A	Ambient temperature		-40		125	°C

(1) V_{CC1} and V_{CC2} can be set independent of one another

(2) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC}

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		ISO7041-Q1	UNIT
		DBQ (SOIC)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87.0	°C/W
$R_{\theta JC(\text{top})}$	Junction-to-case (top) thermal resistance	33.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	48.5	°C/W
$R_{\theta JC(\text{bot})}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150^\circ\text{C}$, $C_L = 15$ pF, Input a 1-MHz 50% duty cycle square wave			7.82	mW
P_{D1}	Maximum power dissipation (side-1)				4.46	mW
P_{D2}	Maximum power dissipation (side-2)				3.36	mW

Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATIONS		UNIT
			QSOP-16		
IEC 60664-1					
CLR	External clearance ⁽¹⁾	Side 1 to side 2 distance through air	>3.7	mm	
CPG	External Creepage ⁽¹⁾	Side 1 to side 2 distance across package surface	>3.7	mm	
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	17	μm	
CTI	Comparative tracking index	IEC 60112; UL 746A	>600	V	
	Material Group	According to IEC 60664-1	I		
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V _{RMS}	I-III		
DIN V VDE V 0884-11:2017-01⁽²⁾					
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	566	V _{PK}	
V _{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test; See TBD	400	V _{RMS}	
		DC voltage	566	V _{DC}	
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t = 60 s (qualification); V _{TEST} = 1.2 \times V _{IOTM} , t = 1 s (100% production)	4242	V _{PK}	
V _{IOSM}	Maximum surge isolation voltage ⁽³⁾	Test method per IEC 62368-1, 1.2/50 μs waveform, V _{TEST} = 1.6 \times V _{IOSM} = 6400 V _{PK} (qualification)	4000	V _{PK}	
q _{pd}	Apparent charge ⁽⁴⁾	Method a: After I/O safety test subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.2 \times V _{IORM} , t _m = 10 s	≤ 5	pC	
		Method a: After environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.6 \times V _{IORM} , t _m = 10 s	≤ 5		
		Method b1: At routine test (100% production) and preconditioning (type test), V _{ini} = V _{IOTM} , t _{ini} = 1 s; V _{pd(m)} = 1.875 \times V _{IORM} , t _m = 1 s	≤ 5		
C _{IO}	Barrier capacitance, input to output ⁽⁵⁾	V _{IO} = 0.4 \times sin (2 πf), f = 1 MHz	~1.5	pF	
R _{IO}	Insulation resistance, input to output ⁽⁵⁾	V _{IO} = 500 V, T _A = 25°C	> 10 ¹²	Ω	
		V _{IO} = 500 V, 100°C ≤ T _A ≤ 150°C	> 10 ¹¹		
		V _{IO} = 500 V at T _S = 150°C	> 10 ⁹		
	Pollution degree		2		
	Climatic category		55/125/21		
UL 1577					
V _{ISO}	Withstand isolation voltage	V _{TEST} = V _{ISO} , t = 60 s (qualification); V _{TEST} = 1.2 \times V _{ISO} , t = 1 s (100% production)	3000	V _{RMS}	

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier tied together creating a two-pin device.

6.6 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN VDE V 0884-11:2017- 01	Certified according to IEC 60950-1 and IEC 62368-1	Certified according to UL 1577 Component Recognition Program	Certified according to GB4943.1-2011	Certified according to EN 61010-1:2010/ A1:2019, EN 60950-1:2006/A2:2013 and EN 62368-1:2014
Maximum transient isolation voltage, 4242 V _{PK} ; Maximum repetitive peak isolation voltage, 566 V _{PK} ; Maximum surge isolation voltage, 4000 V _{PK}	3000 V _{RMS} insulation per CSA 60950-1-07+A1+A2, IEC 60950-1 2nd Ed.+A1+A2, CSA 62368-1- 14 and IEC 62368-1:2014 370 V _{RMS} (DBQ-16) maximum working voltage (pollution degree 2, material group I)	Single protection, 3000 V _{RMS}	Basic insulation, Altitude ≤ 5000 m, Tropical Climate, 400 V _{RMS} maximum working voltage	EN 61010- 1:2010/ A1:2019, 300 V _{RMS} basic isolation EN 60950- 1:2006/ A2:2013 and EN 62368-1:2014, 400 V _{RMS} basic isolation
Certification Planned	Certification Planned	Certification Planned	Certification Planned	Certification Planned

6.7 Safety Limiting Values

Safety limiting⁽¹⁾ intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
16-QSOP PACKAGE						
I _S	Safety input, output, or supply current	R _{θJA} = 87°C/W, V _I = 5.5 V, T _J = 150°C, T _A = 25°C			261	mA
		R _{θJA} = 87°C/W, V _I = 3.6 V, T _J = 150°C, T _A = 25°C			399	mA
P _S	Safety input, output, or total power	R _{θJA} = 87°C/W, T _J = 150°C, T _A = 25°C			1435	mW
T _S	Maximum safety temperature				150	°C

- (1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, R_{θJA}, in the table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
T_J = T_A + R_{θJA} × P, where P is the power dissipated in the device.
T_{J(max)} = T_S = T_A + R_{θJA} × P_S, where T_{J(max)} is the maximum allowed junction temperature.
P_S = I_S × V_I, where V_I is the maximum input voltage.

6.8 Electrical Characteristics 5V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT+(IN)}$	Rising input switching threshold			$0.7 \times V_{CCI}$ ⁽¹⁾	V
$V_{IT-(IN)}$	Falling input switching threshold		$0.3 \times V_{CCI}$		V
V_{OH}	High-level output voltage	$I_{OH} = -4 \text{ mA}$	$V_{CCO} - 0.4$		V
V_{OL}	Low-level output voltage	$I_{OL} = 4 \text{ mA}$		0.4	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		$0.1 \times V_{CCI}$		V
I_{IH}	High-level input current	$V_{IH} = V_{CCI}$ ⁽¹⁾ at IN_x		1	μA
I_{IL}	Low-level input current	$V_{IL} = 0 \text{ V}$ at IN_x	-1		μA
CMTI	Common mode transient immunity	$V_I = V_{CC}$ or 0 V, $V_{CM} = 1200 \text{ V}$	50	100	kV/us
C_i	Input Capacitance ⁽²⁾	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$, $f = 1 \text{ MHz}$, $V_{CC} = 5 \text{ V}$	2		pF

 (1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC}

(2) Measured from input pin to same side ground.

6.9 Supply Current Characteristics 5V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7041-Q1						
Supply current - DC signal	Refresh disable	I_{CC1}	6.2	14.3		μA
		I_{CC2}	10.1	18.5		μA
	Refresh enable $V_I = V_{CCI}$ ⁽¹⁾ (ISO7041-Q1); $V_I = 0 \text{ V}$ (ISO7041-Q1 with F suffix)	I_{CC1}	8.2	16.7		μA
		I_{CC2}	10.8	18.5		μA
Supply current - AC signal	Refresh enable $V_I = 0 \text{ V}$ (ISO7041-Q1); $V_I = V_{CCI}$ (ISO7041-Q1 with F suffix)	I_{CC1}	9.5	19.9		μA
		I_{CC2}	11.3	19.5		μA
	Refresh disable 10 kbps, No Load	I_{CC1}	6.7	19.7		μA
		I_{CC2}	11.8	20.6		μA
	Refresh disable 100 kbps, No Load	I_{CC1}	37.1	57.4		μA
		I_{CC2}	25.8	37.7		μA
	Refresh disable 1 Mbps, No Load	I_{CC1}	340.5	436.1		μA
		I_{CC2}	167.0	211.1		μA
Total Supply Current Per Channel, Refresh Disabled	Refresh enable 10 kbps, No Load	I_{CC1}	10.6	20.8		μA
		I_{CC2}	11.9	20.4		μA
	Refresh enable 100 kbps, No Load	I_{CC1}	37.1	57.4		μA
		I_{CC2}	25.8	37.7		μA
	Refresh enable 1 Mbps, No Load	I_{CC1}	338.3	436.1		μA
		I_{CC2}	166.0	211.1		μA
	DC Signal	$I_{CC1(ch)} + I_{CC2(ch)}$	4.1	7.4		μA
	10 kbps, No Load	$I_{CC1(ch)} + I_{CC2(ch)}$	5.9	10.7		μA
	100 kbps, No Load	$I_{CC1(ch)} + I_{CC2(ch)}$	17.4	23.4		μA
	1 Mbps, No Load	$I_{CC1(ch)} + I_{CC2(ch)}$	137.0	164.5		μA

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Total Supply Current Per Channel, Refresh Enabled	$V_I = V_{CCI}$ (ISO7041-Q1); $V_I = 0$ V (ISO7041-Q1 with F suffix)	$I_{CC1(ch)} + I_{CC2(ch)}$		4.8	8.5	μ A
	$V_I = 0$ V (ISO7041-Q1); $V_I = V_{CCI}$ (ISO7041-Q1 with F suffix)	$I_{CC1(ch)} + I_{CC2(ch)}$		5.3	9.6	μ A
	10 kbps, No Load	$I_{CC1(ch)} + I_{CC2(ch)}$		5.7	10.4	μ A
	100 kbps, No Load	$I_{CC1(ch)} + I_{CC2(ch)}$		16.4	22.3	μ A
	1 Mbps, No Load	$I_{CC1(ch)} + I_{CC2(ch)}$		125.9	154.0	μ A

(1) V_{CCI} = Input-side V_{CC}

6.10 Electrical Characteristics 3.3V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT+(IN)}$	Rising input switching threshold			$0.7 \times V_{CCI}$ ⁽¹⁾	V
$V_{IT-(IN)}$	Falling input switching threshold		$0.3 \times V_{CCI}$		V
V_{OH}	High-level output voltage	$I_{OH} = -2mA$	$V_{CCO} - 0.3$		V
V_{OL}	Low-level output voltage	$I_{OL} = 2mA$		0.3	V
$V_{I(HYS)}$	Input threshold voltage hysteresis		$0.1 \times V_{CCI}$		V
I_{IH}	High-level input current	$V_{IH} = V_{CCI}$ ⁽¹⁾ at IN_x		1	μA
I_{IL}	Low-level input current	$V_{IL} = 0 V$ at IN_x	-1		μA
CMTI	Common mode transient immunity	$V_I = V_{CC}$ or 0 V, $V_{CM} = 1200 V$	50	100	kV/us
C_i	Input Capacitance ⁽²⁾	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$, $f = 1$ MHz, $V_{CC} = 3.6 V$		2	pF

 (1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC}

(2) Measured from input pin to same side ground.

6.11 Supply Current Characteristics 3.3V Supply

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7041-Q1						
Supply current - DC signal	Refresh disable	I_{CC1}	5.1	8.8		μA
		I_{CC2}	8.9	14.0		μA
	Refresh enable $V_I = V_{CCI}$ ⁽¹⁾ (ISO7041-Q1); $V_I = 0 V$ (ISO7041-Q1 with F suffix)	I_{CC1}	6.8	12.2		μA
		I_{CC2}	9.6	14.0		μA
Supply current - AC signal	Refresh enable $V_I = 0 V$ (ISO7041-Q1); $V_I = V_{CCI}$ (ISO7041-Q1 with F suffix)	I_{CC1}	8.1	14.8		μA
		I_{CC2}	10.0	15.6		μA
	Refresh disable 10 kbps, No Load	I_{CC1}	7.9	13.7		μA
		I_{CC2}	10.4	15.9		μA
	Refresh disable 100 kbps, No Load	I_{CC1}	35.9	48.3		μA
		I_{CC2}	22.7	31.4		μA
	Refresh disable 1 Mbps, No Load	I_{CC1}	316.4	395.7		μA
		I_{CC2}	147.2	188.2		μA
Total Supply Current Per Channel, Refresh Disabled	Refresh enable 10 kbps, No Load	I_{CC1}	9.8	16.4		μA
		I_{CC2}	10.5	16.2		μA
	Refresh enable 100 kbps, No Load	I_{CC1}	35.9	48.3		μA
		I_{CC2}	22.7	31.4		μA
	Refresh enable 1 Mbps, No Load	I_{CC1}	315.3	395.7		μA
		I_{CC2}	146.2	188.2		μA
	DC Signal	$I_{CC1(ch)} + I_{CC2(ch)}$	3.5	5.7		μA
	10 kbps, No Load	$I_{CC1(ch)} + I_{CC2(ch)}$	5.2	8.2		μA
	100 kbps, No Load	$I_{CC1(ch)} + I_{CC2(ch)}$	14.8	19.2		μA
	1 Mbps, No Load	$I_{CC1(ch)} + I_{CC2(ch)}$	115.7	138.7		μA

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Total Supply Current Per Channel, Refresh Enabled	$V_I = V_{CC1}$ (ISO7041-Q1); $V_I = 0$ V (ISO7041-Q1 with F suffix)	$I_{CC1(ch)} + I_{CC2(ch)}$		4.2	6.8	μ A
	$V_I = 0$ V (ISO7041-Q1); $V_I = V_{CC1}$ (ISO7041-Q1 with F suffix)	$I_{CC1(ch)} + I_{CC2(ch)}$		4.6	7.7	μ A
	10 kbps, No Load	$I_{CC1(ch)} + I_{CC2(ch)}$		5.2	8.2	μ A
	100 kbps, No Load	$I_{CC1(ch)} + I_{CC2(ch)}$		14.8	19.2	μ A
	1 Mbps, No Load	$I_{CC1(ch)} + I_{CC2(ch)}$	115.7	138.7		μ A

(1) V_{CC1} = Input-side V_{CC}

6.12 Switching Characteristics

$V_{CC1}, V_{CC2} = 3.0$ V to 5.5 V (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 7-1	148	165	ns
$t_{P(dft)}$	Propagation delay drift		15		$ps/^\circ C$
t_{UI}	Minimum pulse width	See Figure 7-1	250		ns
PWD	Pulse width distortion		10		ns
$t_{sk(o)}$	Channel to channel output skew time	Same-direction channels	10		ns
		Opposite-direction channels	10		ns
$t_{sk(p-p)}$	Part to part skew time		70		ns
t_r	Output signal rise time	See Figure 7-1	16		ns
t_f	Output signal fall time	See Figure 7-1	16		ns
t_{DO}	Default output delay time from input power loss	See Figure 7-2	400	750	us
t_{PU}	Time from UVLO to valid output data		1	5	ms
F_R	Refresh rate		5	10	kbps

6.13 Insulation Characteristics Curves

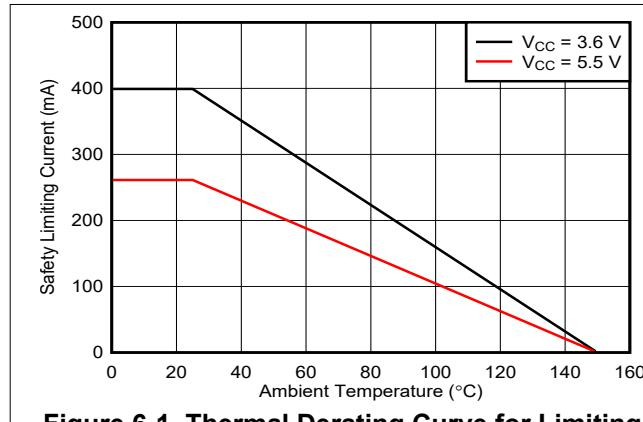


Figure 6-1. Thermal Derating Curve for Limiting Current per VDE

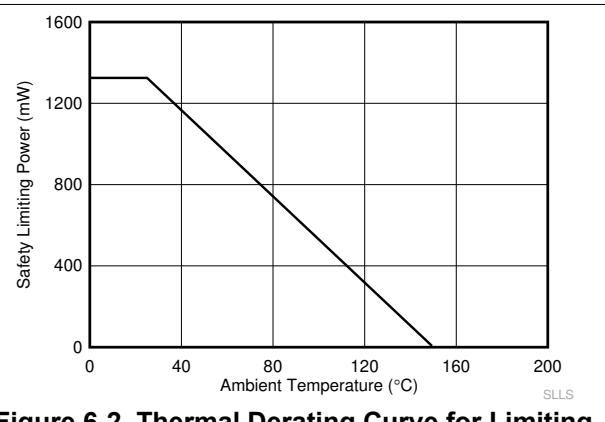


Figure 6-2. Thermal Derating Curve for Limiting Power per VDE

6.14 Typical Characteristics

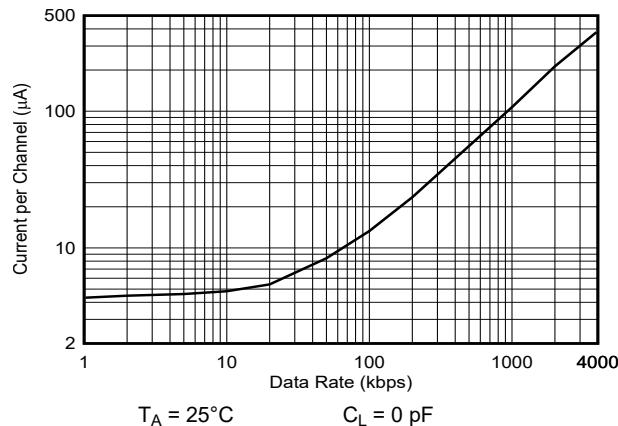


Figure 6-3. ISO7041-Q1 Supply Current vs Data Rate at 3.3 V (With No Load)

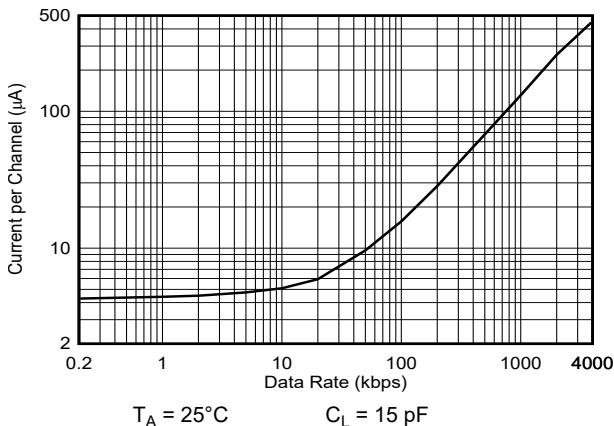


Figure 6-4. ISO7041-Q1 Supply Current vs Data Rate at 3.3 V (With 15-pF Load)

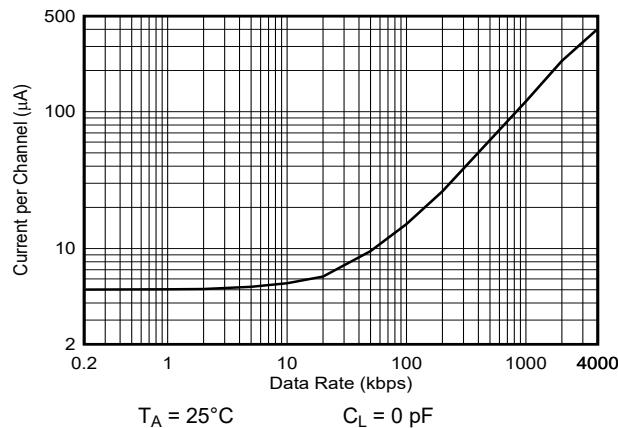


Figure 6-5. ISO7041-Q1 Supply Current vs Data Rate at 5 V (With No Load)

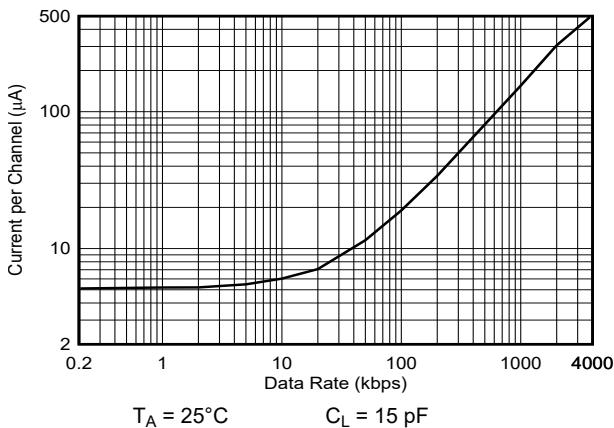
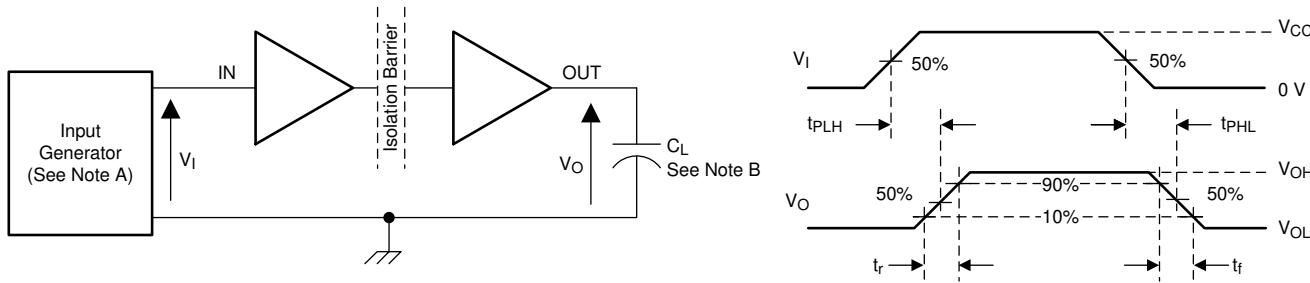


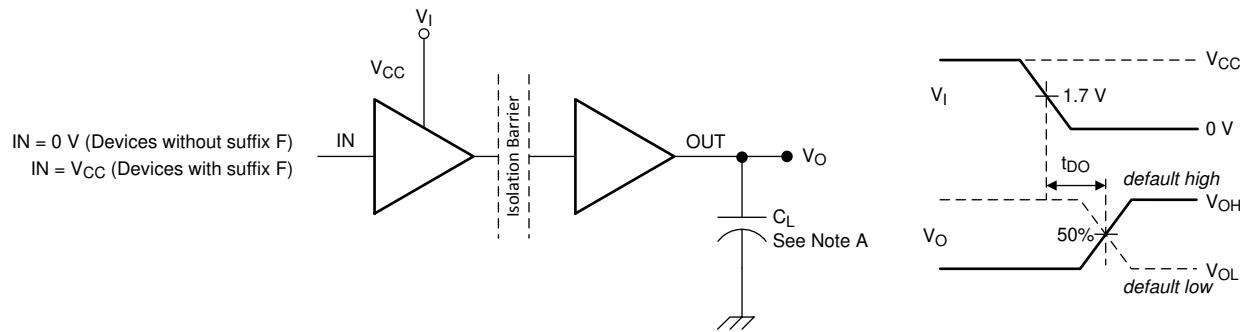
Figure 6-6. ISO7041-Q1 Supply Current vs Data Rate at 5 V (With 15-pF Load)

7 Parameter Measurement Information



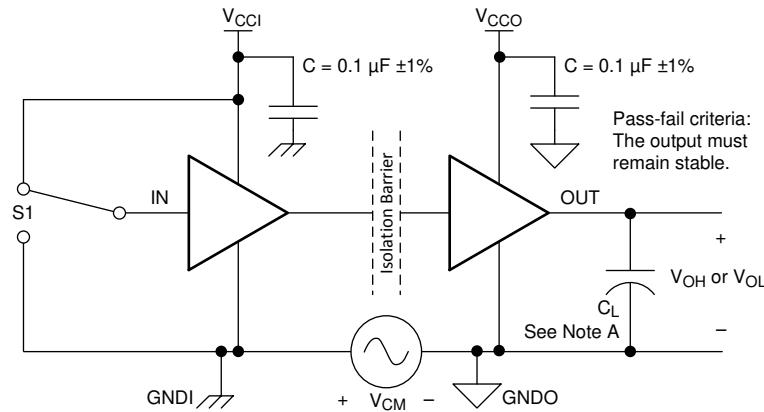
- A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 50 kHz, 50% duty cycle, $t_r \leq 3$ ns, $t_f \leq 3$ ns, $Z_O = 50 \Omega$. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.
- B. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 7-1. Switching Characteristics Test Circuit and Voltage Waveforms



- A. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.
- B. Power Supply Ramp Rate = 10 mV/ns

Figure 7-2. Default Output Delay Time Test Circuit and Voltage Waveforms



- A. $C_L = 15$ pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 7-3. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The ISO7041-Q1 device uses edge encoding of data with an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide isolation barrier. The transmitter uses a high frequency carrier signal to pass data across the barrier representing a signal edge transition. Using this method achieves very low power consumption and high immunity. The receiver demodulates the carrier signal after advanced signal conditioning and produces the output through a buffer stage. For low data rates, a refresh logic option is available to make sure the output state matches the input state. Advanced circuit techniques are used to maximize the CMTI performance and minimize the radiated emissions due to the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, [Conceptual Block Diagram of a Digital Capacitive Isolator](#), shows a functional block diagram of a typical channel.

8.2 Functional Block Diagram

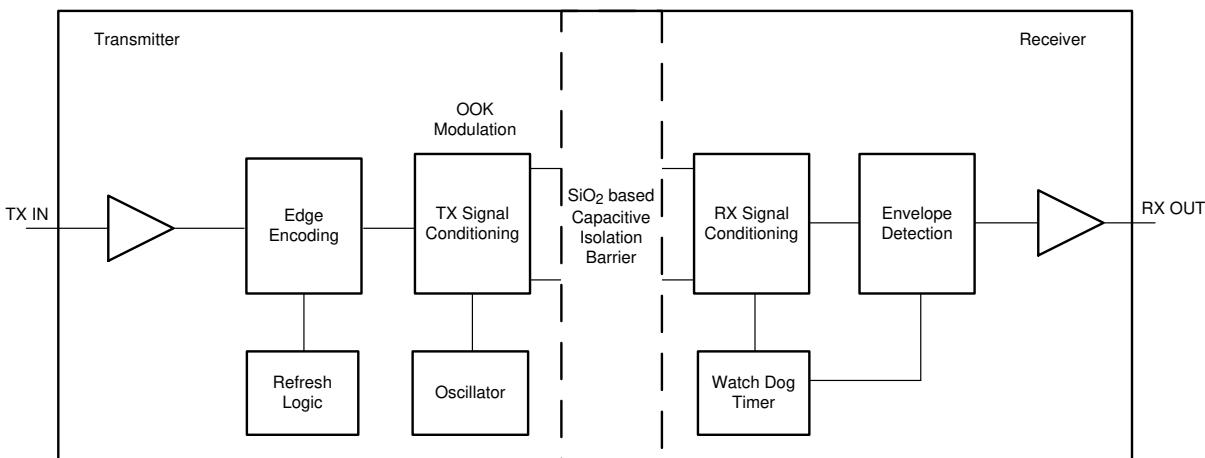


Figure 8-1. Conceptual Block Diagram of a Digital Capacitive Isolator

8.3 Feature Description

8.3.1 Refresh

The ISO7041 uses an edge based encoding scheme to transfer an input signal change across the isolation barrier versus sending across the DC state. The built in refresh function consistently validates that the DC output state of each isolator channel matches the DC input state. An internal watchdog timer monitors for activity on the individual inputs and transmits the logic state when there is no input signal transition for more than 100 μ s. This ensures that the input and output state of the isolator always match.

8.3.2 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO70xx family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.

- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

The device has no issue being able to meet either CISPR 22 Class A and CISPR22 Class B standards in an unshielded environment.

8.4 Device Functional Modes

Table 8-1 shows the functional modes for the device.

Table 8-1. Function Table

V_{CCI} ⁽¹⁾	V_{CCO}	INPUT (INx)	REFRESH ENABLE (ENx)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	L	H	Normal Operation: A channel output assumes the logic state of its input.
		L	L	L	
		X	H	Undetermined	The device needs an input signal transition to validate the output tracks the input state. Without a signal edge transition, the output will be in an undetermined state.
PD	PU	X	L	Default	When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default is <i>High</i> for the device without the F suffix and <i>Low</i> for device with the F suffix.
					When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	L	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined. ⁽²⁾ When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input.
			H	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined. ⁽²⁾ When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the selected default option.
X	X	X	Open	Undetermined	When ENx is unconnected or open, the device output will be in an undetermined and unknown state. ENx must be connected high or low for the device to behave correctly.

(1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC} ; PU = Powered up ($V_{CC} \geq 1.54$ V); PD = Powered down ($V_{CC} \leq 1.54$); X = Irrelevant; H = High level; L = Low level ; Z = High Impedance.

(2) A strongly driven input signal can weakly power the floating V_{CC} through an internal protection diode and cause undetermined output.

8.4.1 Device I/O Schematics

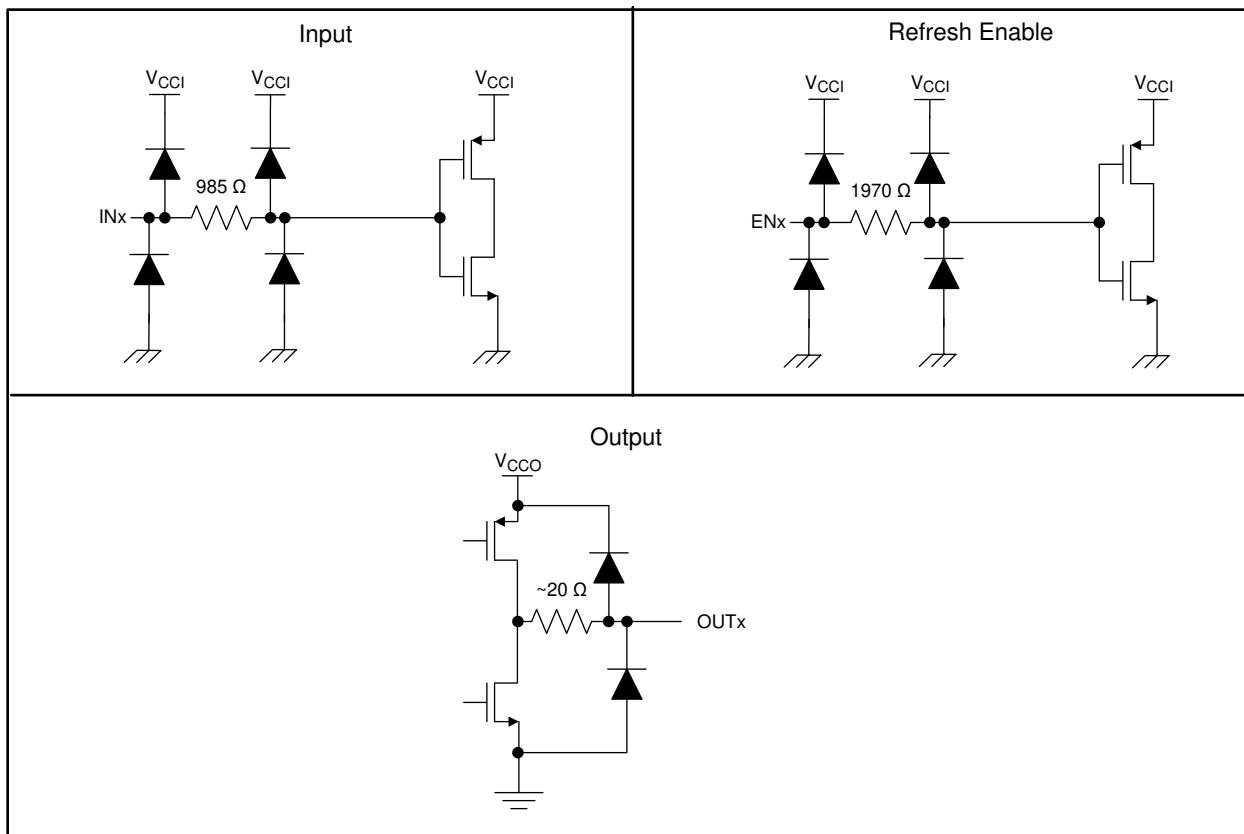


Figure 8-2. Device I/O Schematics

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO7041-Q1 device is an ultra-low power digital isolator. The device uses single-ended CMOS-logic switching technology. The voltage range is from 3.0 V to 5.5 V for both supplies, V_{CC1} and V_{CC2} , and can be set irrespective of one another. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, μ C or UART), and a data converter or a line transceiver, regardless of the interface type or standard. See [Isolated power and data interface for low-power applications reference design TI Design](#) for detailed information on designing the ISO70xx in low-power applications.

9.1.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; see [Figure 9-1](#) for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm) and a minimum insulation lifetime of 20 years. VDE standard also requires additional safety margin of 20% for working voltage and 87.5% for insulation lifetime which translates into minimum required life time of 37.5 years.

[Figure 9-2](#) shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of these devices is 400 VRMS with a lifetime of >100 years. Other factors, such as package size, pollution degree, material group, and so forth can further limit the working voltage of the component. The working voltage of the DBQ-16 package specified up to 400 VRMS. At the lower working voltages, the corresponding insulation barrier life time is much longer.

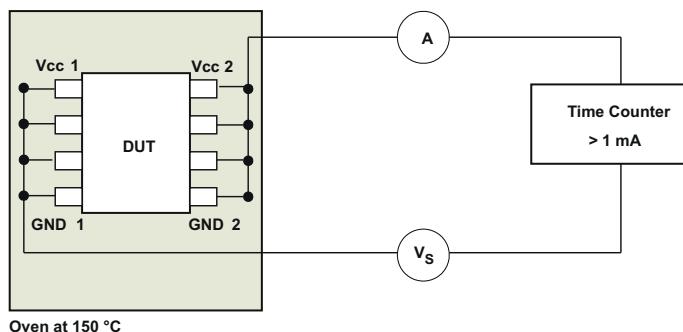


Figure 9-1. Test Setup for Insulation Lifetime Measurement

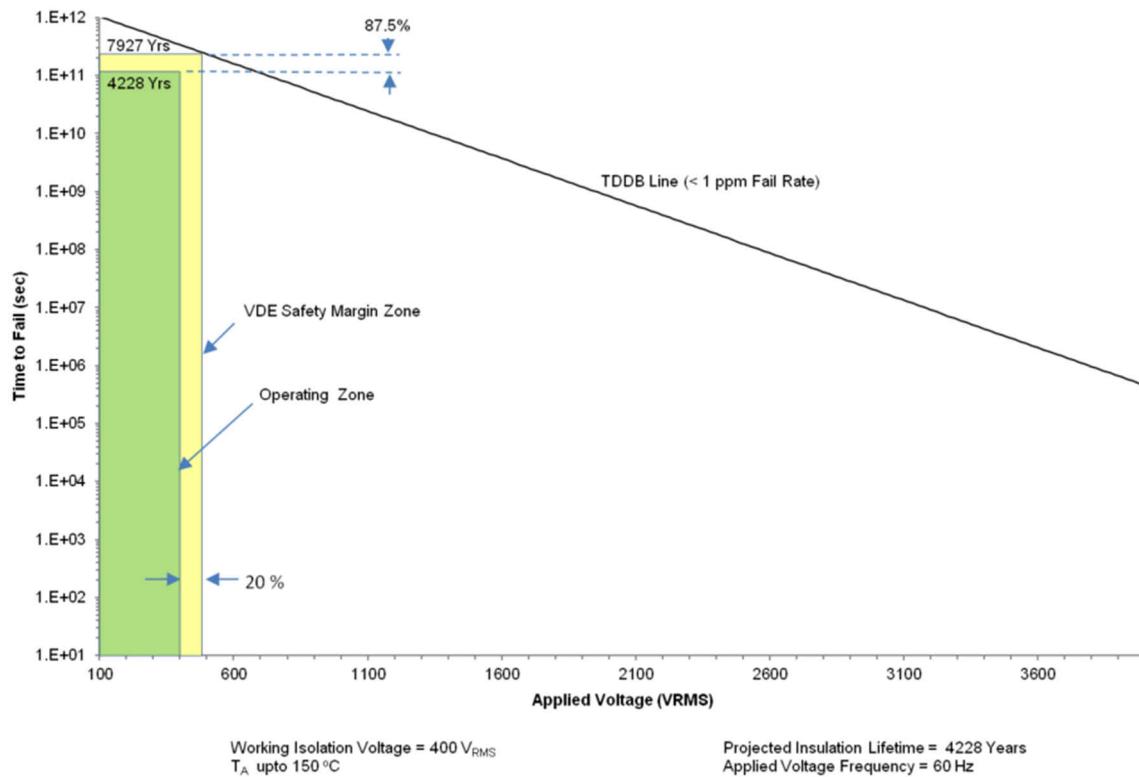
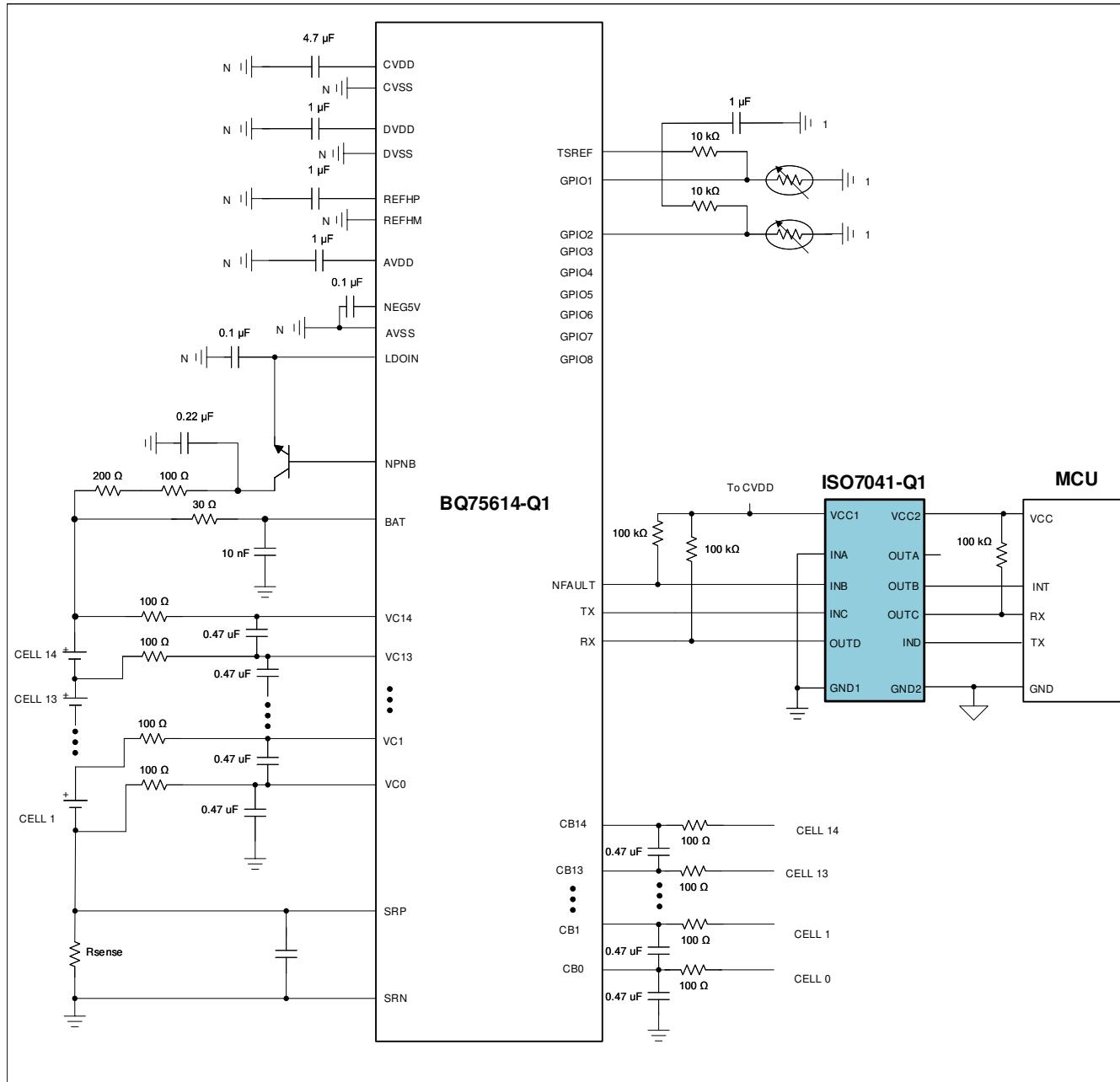


Figure 9-2. Insulation Lifetime Projection Data

9.2 Typical Application

Isolated UART for an Automotive Battery Management System shows the isolated UART and GPIO (NFAULT) interface.



9.2.1 Design Requirements

To design with these devices, use the parameters listed in [Table 9-1](#).

Table 9-1. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	3.0 V to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 μ F
Decoupling capacitor from V_{CC2} and GND2	0.1 μ F

9.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the device only require two external bypass capacitors to operate.

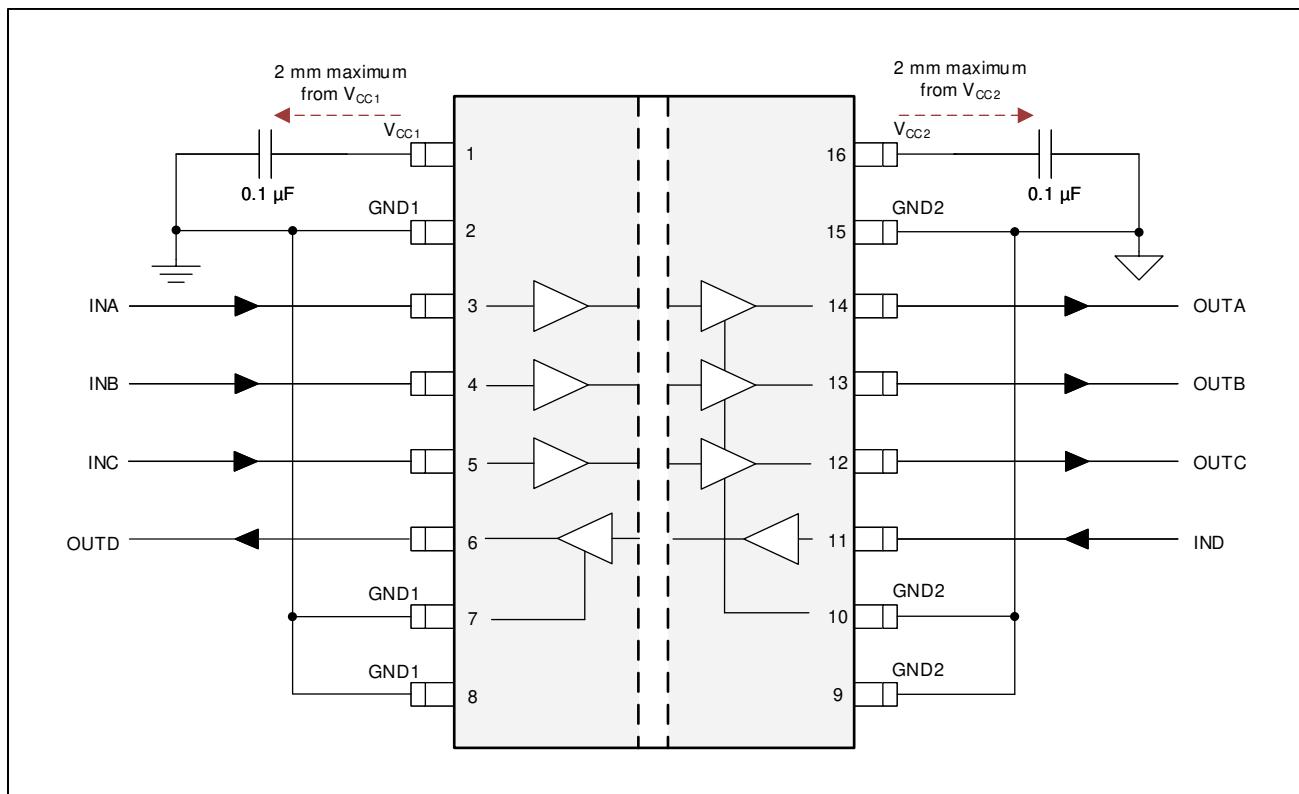


Figure 9-4. Typical ISO7041-Q1 Circuit Hook-up

9.2.3 Application Curves

The following typical eye diagrams of the device indicates wide open eye at the maximum data rate of 4 Mbps.

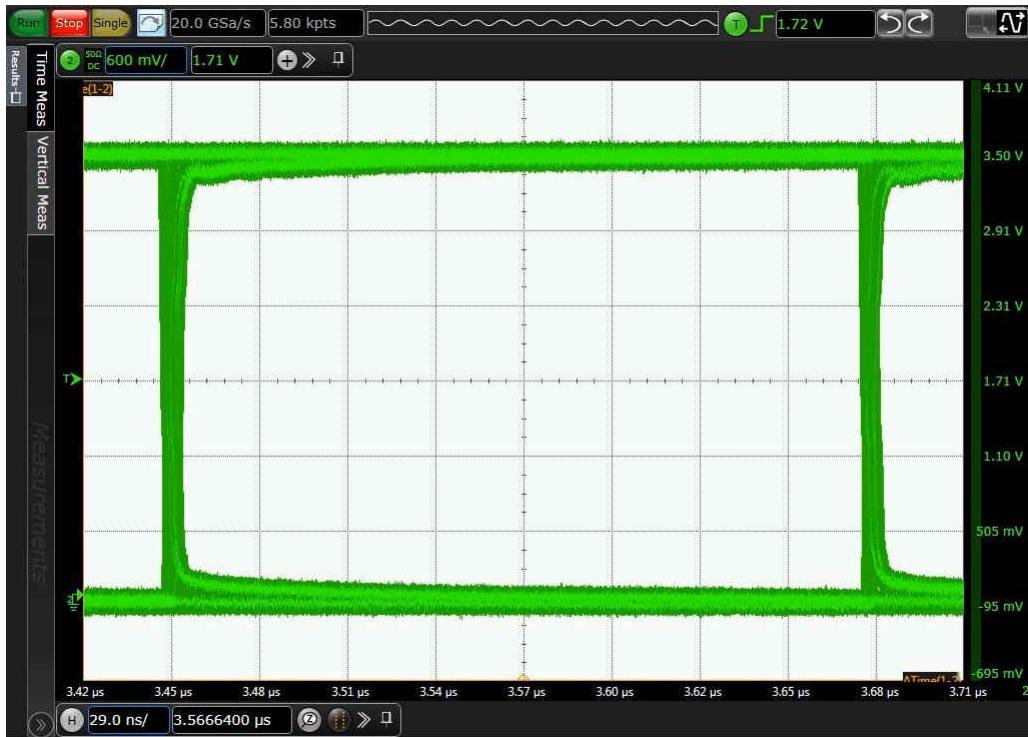


Figure 9-5. Eye Diagram at 4 Mbps PRBS $2^{16} - 1$, 3.3 V and 25°C

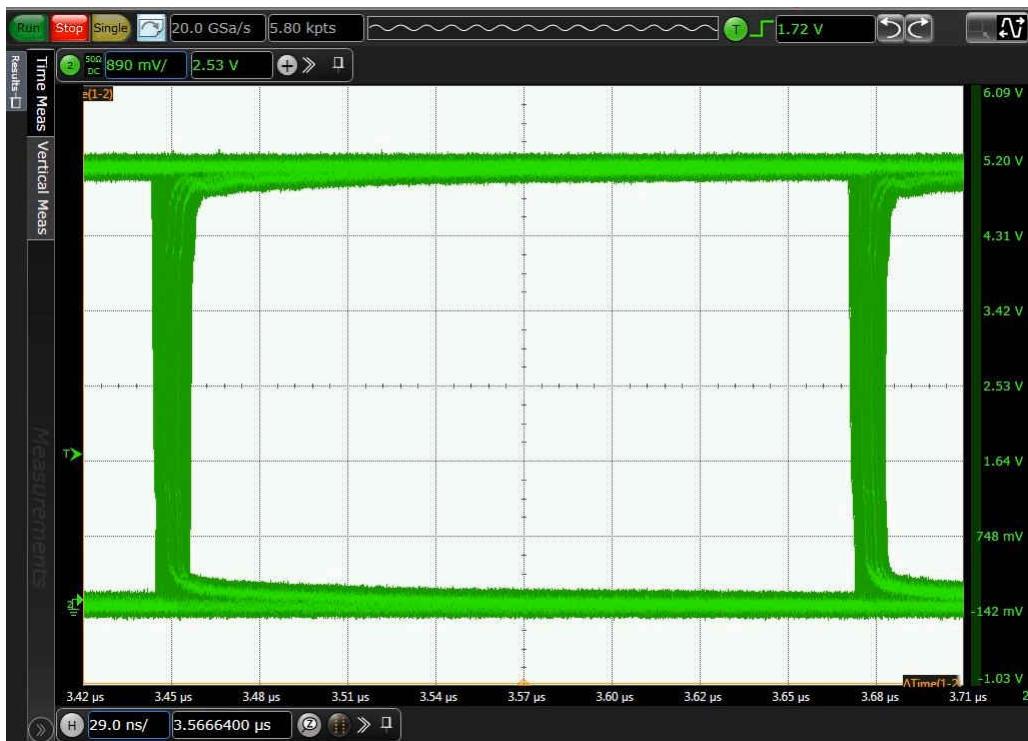


Figure 9-6. Eye Diagram at 4 Mbps PRBS $2^{16} - 1$, 5 V and 25°C

10 Power Supply Recommendations

Put a 0.1- μ F bypass capacitor at the input and output supply pins (V_{CC1} and V_{CC2}) to make sure that operation is reliable at data rates and supply voltage. Put the capacitors as near to the supply pins as possible. If only one primary-side power supply is available in an application, use a transformer driver to help generate the isolated power for the secondary-side. Texas Instruments recommends the [SN6501](#) device or [SN6505A](#) device. Refer to the [SN6501 Transformer Driver for Isolated Power Supplies data sheet](#) or [SN6505 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies data sheet](#) for detailed power supply design and transformer selection recommendations.

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see [Figure 11-1](#)). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in².
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

Refer to the [Digital Isolator Design Guide](#) for detailed layout recommendations.,

11.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

11.2 Layout Example

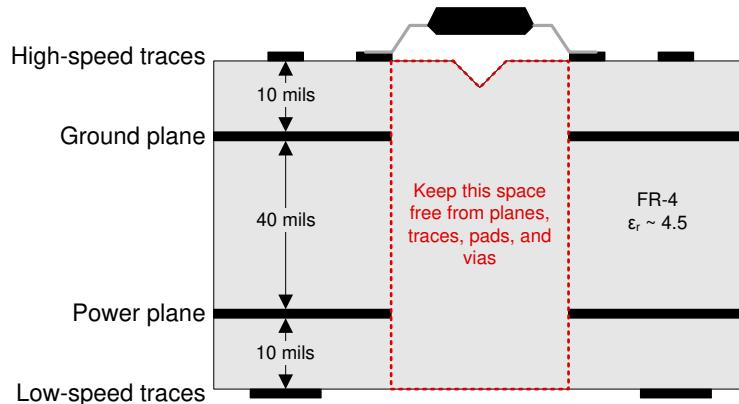


Figure 11-1. Recommended Layer Stack

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Digital Isolator Design Guide](#)
- Texas Instruments, [Isolation Glossary](#)
- Texas Instruments, [BQ75614-Q1, 14-S automotive precision battery monitor, balancer and integrated protector with ASIL-D compliance](#)
- Texas Instruments, [Uniquely Efficient Isolated DC/DC Converter for Ultra-Low Power and Low-Power Applications](#) TI Design
- Texas Instruments, [SN6501 Transformer Driver for Isolated Power Supplies](#) data sheet
- Texas Instruments, [SN6505A Low-Noise 1-A Transformer Drivers for Isolated Power Supplies](#) data sheet
- Texas Instruments, [Isolated power and data interface for low-power applications reference design](#) TI Design

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 Trademarks

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12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ISO7041FQDBQRQ1	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7041F
ISO7041QDBQRQ1	Active	Production	SSOP (DBQ) 16	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7041

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

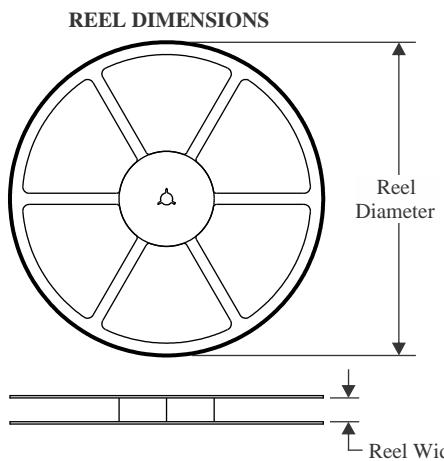
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ISO7041-Q1 :

- Catalog : [ISO7041](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7041FQDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7041QDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7041FQDBQRQ1	SSOP	DBQ	16	2500	350.0	350.0	43.0
ISO7041QDBQRQ1	SSOP	DBQ	16	2500	350.0	350.0	43.0

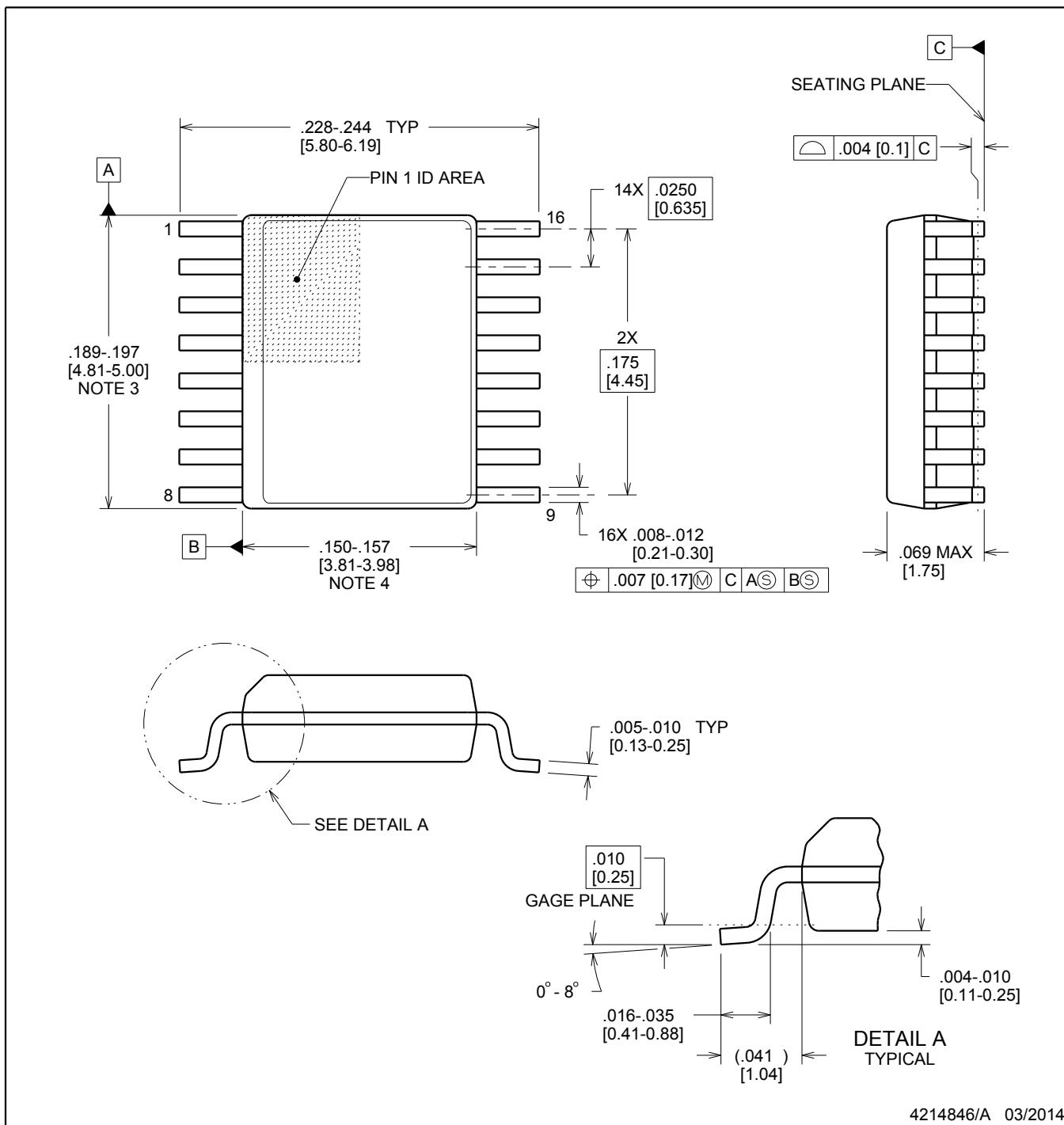


PACKAGE OUTLINE

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



NOTES:

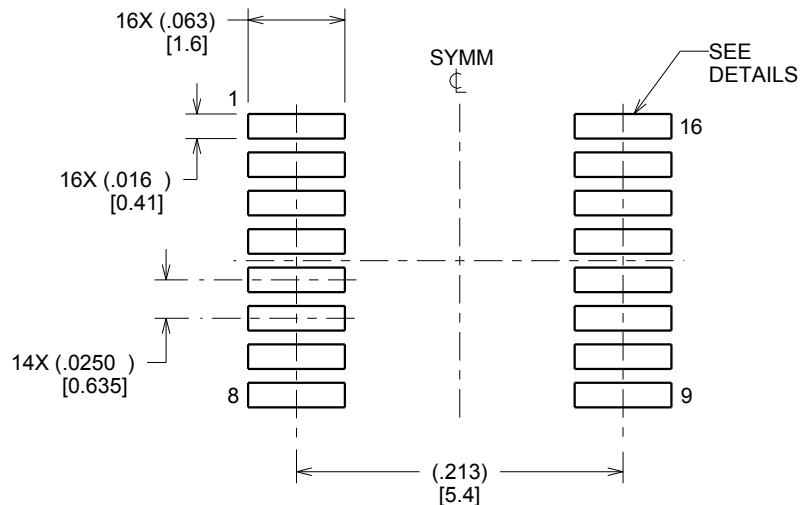
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.

EXAMPLE BOARD LAYOUT

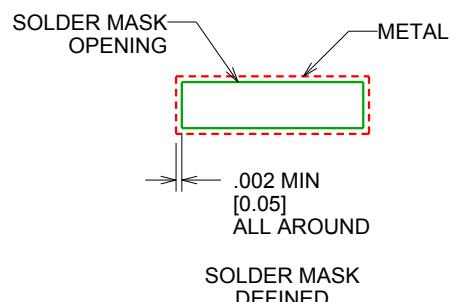
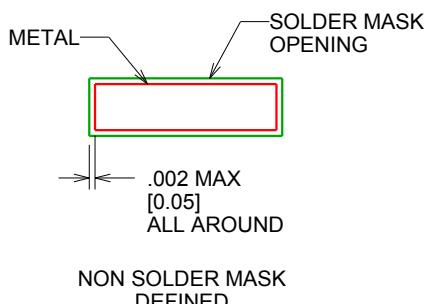
DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

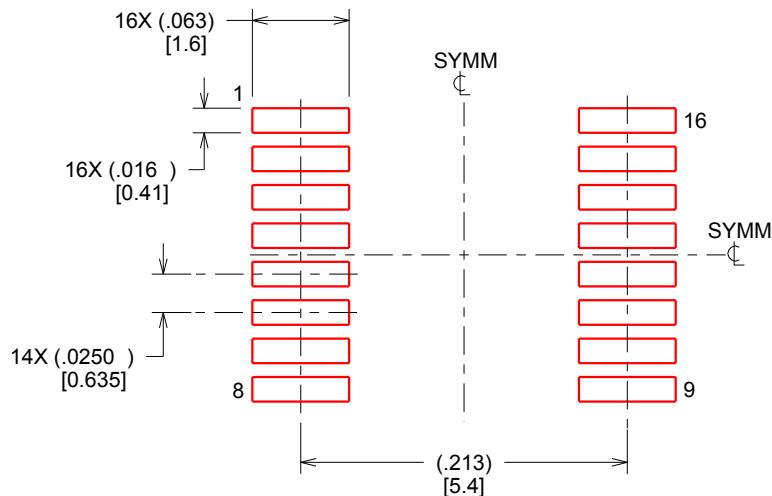
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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