LM3631 Complete LCD Backlight and Bias Power

1 Features

- Drives up to Two Strings with Maximum of Eight LEDs in Series
  - Integrated Backlight Boost with 29-V Maximum Output Voltage
  - Two Low-Side Constant-Current LED Drivers with 25-mA Maximum Output Current
- Backlight Efficiency Up to 90%
- 11-Bit Linear or Exponential Dimming with up to 17-Bit Output Resolution
- External PWM Input for CABC Backlight Operation
- LCD Bias Efficiency > 85%
- Programmable Positive LCD bias, 4-V to 6-V, 100-mA Maximum Output Current
- Programmable Negative LCD bias, –4-V to –6-V, 80-mA Maximum Output Current
- Two Positive Programmable LDO Reference Outputs
  - 4-V to 6-V, 50-mA Maximum Output Current
  - 1.8-V to 3.3-V, 80-mA Maximum Output Current
- 2.7-V to 5-V Input Voltage Range

2 Applications

Mobile Device LCD Backlighting and Bias

3 Description

The LM3631 is a complete LCD backlight and bias power solution for mobile devices. This one-chip solution has an integrated high-efficiency backlight LED driver and positive/negative bias supplies for LCD drivers addressing the power requirements of high-definition LCDs. Integrated solution allows small solution size while still maintaining high performance.

Capable of driving up to 16 LEDs, the LM3631 is ideal for small- to medium-size displays. Two additional programmable LDO regulator outputs can be used to power display controller, LCD gamma reference, or any additional peripherals.

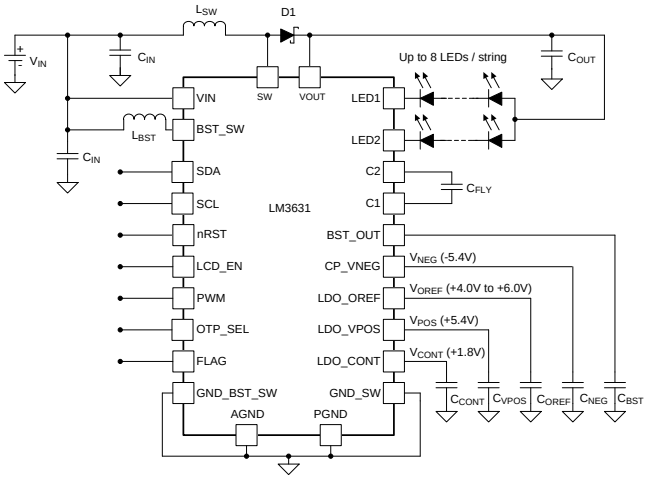
A high level of integration and programmability allows the LM3631 to address a variety of applications without the need for hardware changes. Voltage levels, backlight configuration, and power sequences are all configurable through I^2C interface.

Device Information(1)

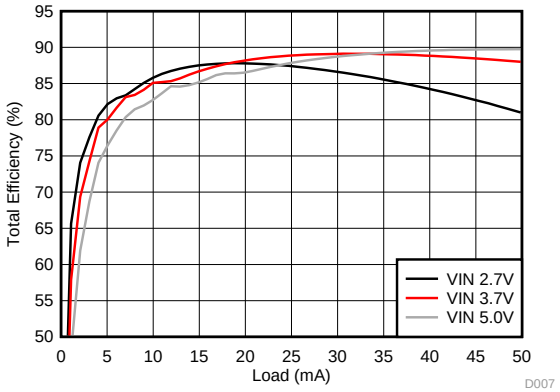
PART NUMBER	PACKAGE	BODY SIZE (MAX)
LM3631	DSBGA (24)	2.585 mm x 1.885 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



Backlight Efficiency, 2P6S



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4 Revision History

DATE	REVISION	NOTES
August 2014	*	Initial release.

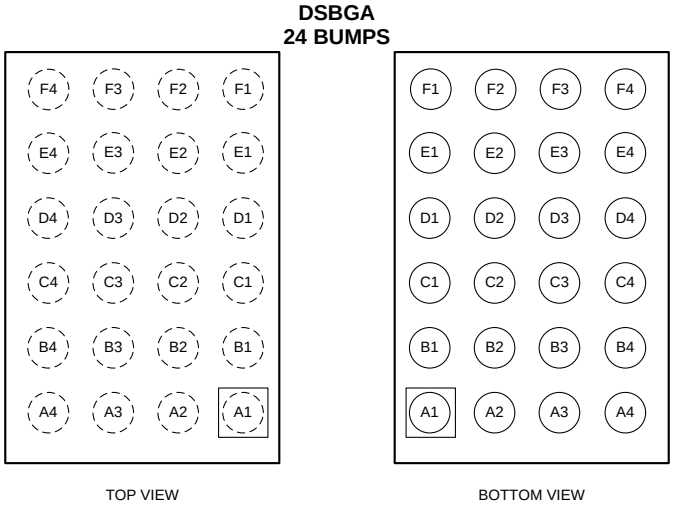
5 Device Comparison Table

Table 1. Register Default Values

I²C Address	Register	Read/Write	OTP_SEL Low	OTP_SEL High
0x00	Device Control	R/W	0x01	0x01
0x01	LED Brightness LSB	R/W	**0x00**	**0x00**
0x02	LED Brightness MSB	R/W	**0x00**	**0x00**
0x03	Faults	R/W	0x00	0x00
0x04	Faults and Power-Good	R/W	0x00	0x00
0x05	Backlight Configuration 1	R/W	**0xCF**	**0xCF**
0x06	Backlight Configuration 2	R/W	**0x07**	**0x27**
0x07	Backlight Configuration 3	R/W	**0xC7**	**0xC6**
0x08	Backlight Configuration 4	R/W	**0x49**	**0x49**
0x09	Backlight Configuration 5	R/W	**0x03**	**0x03**
0x0A	LCD_Configuration 1	R/W	**0x1E**	**0x1E**
0x0B	LCD_Configuration 2	R/W	**0x01**	**0x14**
0x0C	LCD_Configuration 3	R/W	**0xDC**	**0x1A**
0x0D	LCD_Configuration 4	R/W	**0x20**	**0x1E**
0x0E	LCD_Configuration 5	R/W	**0x20**	**0x1E**
0x0F	LCD_Configuration 6	R/W	**0x1E**	**0x1E**
0x10	LCD_Configuration 7	R/W	**0x05**	**0x0F**
0x11	LCD_Configuration 8	R/W	**0x50**	**0x60**
0x12	LCD_Configuration 9	R/W	**0x00**	**0x00**
0x13	FLAG Configuration	R/W	**0x09**	**0x09**
0x16	Revision (6 LSB bits only)	R	0x01	0x01

Values in **bold** are OTP configurable.

6 Pin Configuration and Functions



Pin Functions

PIN		DESCRIPTION
NUMBER	NAME	
A1	CP_VNEG	Negative LCD bias supply voltage. Can be left unconnected if charge pump is disabled.
A2	C2	Inverting charge pump flying capacitor negative pin. Can be left unconnected if charge pump is disabled.
A3	PGND	Power ground connection for boost converters and charge pump.
A4	C1	Inverting charge pump flying capacitor positive pin. Can be left unconnected if charge pump is disabled.
B1	LDO_OREF	LDO_OREF output voltage. Can be left unconnected if LDO is disabled.
B2	PWM	PWM input for brightness control. Must be connected to GND if not used.
B3	SDA	Serial data connection for I^2C-compatible interface. Must be pulled high to VDDIO if not used.
B4	BST_OUT	LCD bias boost output voltage. Internally connected to the input of CP_VNEG, LDO_VPOS, and LDO_OREF.
C1	LDO_VPOS	Positive LCD bias supply rail. Can be left unconnected if LDO is disabled.
C2	LDO_CONT	Positive supply voltage for display panel controller. Can be left unconnected if disabled.
C3	SCL	Serial clock connection for I^2C-compatible interface. Must be pulled high to VDDIO if not used.
C4	BST_SW	LCD bias boost switch pin.
D1	AGND	Analog ground connection for control circuitry.
D2	OTP_SEL	Default setting selection. Must be tied to GND or to VDDIO.
D3	FLAG	Programmable interrupt flag. Open drain output. Can be left unconnected if not used.
D4	GND_BST_SW	LCD bias boost and inverting charge pump ground connection.
E1	LED2	Input pin to internal LED current sink 2. Can be left unconnected if not used.
E2	LCD_EN	LCD enable input. Logic high turns on LCD bias voltages and backlight per sequencing settings.
E3	nRST	Active low reset input.
E4	VIN	Input voltage connection. Connect to 2.7-V to 5-V supply voltage.
F1	LED1	Input pin to internal LED current sink 1. Can be left unconnected if not used.
F2	VOUT	Backlight boost output voltage. Output capacitor is connected to this pin.
F3	SW	Backlight boost switch pin.
F4	GND_SW	Backlight boost ground connection.

7 Specifications

7.1 Absolute Maximum Ratings(1)

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
Voltage on VIN, nRST, LCD_EN, PWM, SCL, SDA, FLAG, LDO_CONT, OTP_SEL		–0.3	6	V
Voltage on BST_SW, BST_OUT, LDO_VPOS, LDO_OREF, C1		–0.3	7	V
Voltage on CP_VNEG, C2		–7.0	0.3	V
Voltage on SW, VOUT, LED1, LED2		–0.3	30	V
	Continuous power dissipation		Internally limited	
$T_{J(MAX)}$	Maximum junction temperature		150	°C
$T_{SOLDERING}$	Note(2)			

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For detailed soldering specifications and information, please refer to Texas Instruments Application Note 1112: DSBGA Wafer Level Chip Scale Package (AN-1112).

7.2 Handling Ratings

PARAMETER			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–45	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins except SW(1)	–1000	1000	V
		Human body model (HBM), SW pin	–600	600	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–500	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.7	3.7	5	V
Voltage on nRST, LCD_EN, PWM, SCL, SDA, FLAG, LDO_CONT, OTP_SEL		0		V_{IN} + 0.3V with 5V max	V
Voltage on LDO_VPOS, LDO_OREF, C1		0		6.5	V
Voltage on BST_SW, BST_OUT		0		7	V
Voltage on CP_VNEG, C2		–6.5		0	V
Voltage on SW, VOUT, LED1, LED2		0		29	V
T_A	Operating ambient temperature (1)	–40		85	°C

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125ºC), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (R_{\theta JA} \times P_{D-MAX})$.

7.4 Thermal Information

THERMAL METRIC(1)		DSBGA (20 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.5	°C/W
$R_{\theta JC}$	Junction-to-case (top) thermal resistance	0.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	9.4	
Ψ_{JT}	Junction-to-top characterization parameter	1.6	
Ψ_{JB}	Junction-to-board characterization parameter	9.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Unless otherwise specified, limits apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ 85°C), V_{IN} = 3.6 V, V_{POS} = V_{OREF} = 5.4 V, V_{NEG} = –5.4 V, V_{BST} = 5.7 V, V_{CONT} = 3.3V.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
CURRENT CONSUMPTION						
I_{SD}	Shutdown current	nRST = LOW, LCD_EN = LOW		1		µA
I_Q	Quiescent current, device not switching	nRST = HIGH, LCD_EN = LOW, 2.7 V ≤ V_{IN} ≤ 5 V		60		µA
I_{LCD_EN}		nRST = HIGH, LCD_EN = HIGH, 2.7 V ≤ V_{IN} ≤ 5 V, no load, Backlight disabled		1		mA
DEVICE PROTECTION						
UVLO	Undervoltage lockout	V_{IN} decreasing		2.5		V
		V_{IN} increasing		2.6		V
TSD	Thermal shutdown(1)			140		°C
TSD(hyst)	Hysteresis(1)			20		°C
LED CURRENT SINKS						
$I_{LED1/2}$	Minimum output current	Brightness code 0x001		50		µA
	Maximum output current	Brightness code 0x7FF, exponential mapping		25		mA
	Maximum output current	Brightness code 0x7FF, linear mapping		25.3		mA
$I_{ACCURACY}$	Absolute LED current accuracy (2)	2.7 V ≤ V_{IN} ≤ 5.0 V, LED Currents 0.05 mA, 1 mA, 5 mA, 25 mA	–3%		3%	
I_{MATCH}	LED1 to LED2 current matching (2)	2.7 V ≤ V_{IN} ≤ 5.0 V, LED Currents 0.05 mA, 1 mA, 5 mA, 25 mA	0%		3%	
V_{HR_MIN}	Current sink saturation voltage	I_{LED} = 95% of 5 mA		30	50	mV
BACKLIGHT BOOST CONVERTER						
V_{OVP_BL}	Backlight boost output overvoltage protection	2.7 V ≤ V_{IN} ≤ 5 V, 29-V Option		28.8		V
η_{LED_DRIVE}	LED drive efficiency (1)	I_{LED} = 10 mA/string, 2P6S LED configuration 1235AS-H-220M Inductor		88%		
V_{HR}	Regulated current sink headroom voltage	I_{LED} = 25 mA		250		mV
		I_{LED} = 5 mA		100		mV
R_{DSON}	NMOS switch on resistance	I_{SW} = 250 mA		0.5		Ω
I_{CL}	Selectable NMOS switch current limit	900-mA setting		900		mA

(1) Typical value only for reference.
(2) Output Current Accuracy is the difference between the actual value of the output current and programmed value of this current. Matching is the maximum difference from the average. For the constant current sinks on the part (LED1 and LED2), the following is determined: the maximum output current (MAX), the minimum output current (MIN), and the average output current of both outputs (AVG). Matching number is calculated: (MAX - MIN)/AVG. The typical specification provided is the most likely norm of the matching figure of all parts. LED current sinks were characterized with 1-V headroom voltage. Note that some manufacturers have different definitions in use.

Electrical Characteristics (continued)

Unless otherwise specified, limits apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ 85°C), V_{IN} = 3.6 V, V_{POS} = V_{OREF} = 5.4 V, V_{NEG} = –5.4 V, V_{BST} = 5.7 V, V_{CONT} = 3.3V.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
f_{SW}	Switching frequency	500-kHz mode	450	500	550	kHz
		1-MHz mode	900	1000	1100	
D_{MAX}	Maximum duty cycle			94%		
LCD BIAS BOOST CONVERTER						
V_{OVP_BST}	LCD bias boost output overvoltage protection			6.8		V
f_{SW_BST}	Switching frequency (1)	Load current 100mA		2500		kHz
V_{BST}	Minimum Bias boost output voltage	LCD_BST_OUT = 000000b		4.5		V
	Maximum Bias boost output voltage	LCD_BST_OUT = 100101b		6.35		
	Output voltage step size			50		mV
	Peak-to-peak ripple voltage (3)	I_{LOAD} = 50 mA, C_{BST} = 10 µF		50		mVpp
	BST_OUT line transient response (3)	V_{IN} + 500 mVp-p AC square wave, Tr = 100 mV/µs, 200 Hz, 12.5% Duty, I_{LOAD} 5 mA, C_{IN} = 10 µF, C_{BST} = 10 µF	–50	±25	50	mV
	BST_OUT load transient response (3)	Load current step 0 mA - 150 mA, $T_{RISE/FALL}$ = 100 mA/µs, C_{IN} = 10 µF, C_{BST} = 10 µF	–150		150	mV
I_{CL_BST}	Valley current limit			1000		mA
R_{DSON_BST}	High-side MOSFET on resistance	T_A = 25°C		170		mΩ
	Low-side MOSFET on resistance	T_A = 25°C		290		
η_{BST}	Efficiency (4)	80 mA < I_{BST} < 200 mA		92%		
t_{ST_BST}	Start-up time (BST_OUT), V_{BST_OUT} = 10% to 90% (5)	C_{BST} = 20 µF			1000	µs
LCD POSITIVE BIAS OUTPUT (LDO_VPOS)						
V_{POS}	Minimum output voltage	LDO_VPOS_TARGET = 000000b		4.0		V
	Maximum output voltage	LDO_VPOS_TARGET = 101000b		6.0		V
	Output voltage step size			50		mV
	Output voltage accuracy	Output voltage = 5.4 V, I_{LOAD}= 1 mA	–1.5%		1.5%	
	LDO_VPOS line transient response (5)	V_{IN} + 500 mVp-p AC square wave, Tr = 100 mV/µs, 200 Hz, I_{LOAD} 25 mA, C_{IN} = 10 µF	–25		25	mV
	LDO_VPOS load transient response (5)	5 mA to 100 mA load transient, $T_{RISE/FALL}$ = 2 µs , C_{VPOS} = 10 µF	–100		100	mV
	DC load regulation (5)	1 mA ≤ I_{LOAD} ≤ 100 mA			20	mV
PG_{RISING}	Power-good threshold, voltage increasing	% of target V_{POS}		95%		
$PG_{FALLING}$	Power-good threshold, voltage decreasing	% of target V_{POS}		90%		
I_{POS_MAX}	Maximum output current			100		mA
I_{CL_VPOS}	Output current limit			200		mA
$I_{RUSH\_PK\_VPOS}$	Peak start-up inrush current (5)	V_{BST} = 6.3 V, V_{POS} = 6 V, C_{VPOS} = 10 µF		500		mA
V_{DO_VPOS}	LDO_VPOS dropout voltage (6)	I_{LOAD} = 100 mA, V_{POS} = 4 V		80		mV

(3) Limits set by characterization and/or simulation only.
(4) Typical value only for reference.
(5) Limits set by characterization and/or simulation only.
(6) V_{BST} – V_{POS} when V_{POS} has dropped 100 mV below target.

Electrical Characteristics (continued)

Unless otherwise specified, limits apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ 85°C), V_{IN} = 3.6 V, V_{POS} = V_{OREF} = 5.4 V, V_{NEG} = –5.4 V, V_{BST} = 5.7 V, V_{CONT} = 3.3V.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$PSRR_{VPOS}$	Power supply rejection ratio, LDO_VPOS (5)	f = 10 Hz to 500 kHz, I_{LOAD}= 50 mA, V_{BST} to V_{POS}, 300 mV minimum headroom		25		dB
t_{ST_VPOS}	Start-up time LDO_VPOS, V_{LDO_VPOS} = 10% to 90% (5)	C_{VPOS} = 10 µF			1	ms
R_{PD_VPOS}	Output pull-down resistor, LDO_VPOS	LDO_VPOS pull-down enabled, LDO_VPOS disabled	52	80	110	Ω
LCD NEGATIVE BIAS OUTPUT (CP_VNEG)						
V_{OVP_VNEG}	LCD bias negative charge-pump output overvoltage protection	Below V_{NEG} output voltage target		–250		mV
V_{SHORT_VNEG}	LCD bias negative charge-pump output short circuit protection			–1		V
V_{NEG}	Minimum output voltage	CP_VNEG_TARGET = 101000b		–6.0		V
	Maximum output voltage	CP_VNEG_TARGET = 000000b		–4.0		V
	Output voltage step size			50		mV
	Output accuracy	Output voltage = –5.4V	–1.5%		1.5%	
	Peak-to-peak ripple voltage (5)	I_{LOAD} = 50 mA, C_{VNEG} = 10 µF		60		mVpp
	CP_VNEG line transient response (5)	V_{IN} + 500 mVp-p AC square wave, 100 mV/µs 200 Hz, 12.5% DS at 5 mA	–50	±25	50	mV
	CP_VNEG load transient response (5)	5 mA to 50 mA load transient, $T_{RISE/FALL}$ = 1 µs, C_{VNEG} = 10 µF	–100		100	mV
PG_{RISING}	Power good increasing	% of Target V_{NEG}		95%		
$PG_{FALLING}$	Power good decreasing	% of Target V_{NEG}		90%		
η_{CP}	Efficiency(7)	V_{IN} = 3,7V, V_{BST} = 5,7V V_{NEG} = -5.4V, 20mA < I_{LOAD} < 80mA		92%		
I_{NEG_MAX}	Maximum output current (8)	V_{IN} = 3.7 V, V_{BST} = 5.6 V, V_{NEG} = –5.4V		50		mA
		V_{IN} = 3.7 V, V_{BST} = 5.7 V, V_{NEG} = –5.4 V		80		mA
I_{CL_VNEG}	Output current limit (8)			150		mA
t_{ST_VNEG}	Start-up time, CP_VNEG, VCP_VNEG = 10 % to 90 % (8)	V_{NEG} = –6V, C_{VNEG} = 10 µF			1	ms
R_{PU_VNEG}	Output pull-up resistor, CP_VNEG (8)	CP_VNEG Pull-Up Enabled, CP_VNEG Disabled, V_{BST} > 4.8V		30	40	Ω
LCD GAMMA REFERENCE OUTPUT (LDO_OREF)						
V_{OREF}	Minimum Output voltage	LDO_OREF_TARGET = 000000b		4.0		V
	Maximum Output voltage	LDO_OREF_TARGET = 101000b		6.0		V
	Output voltage step size			50		mV
	Output accuracy	$I_{LOAD\_LDO\_OREF}$ < 5 mA, V_{OREF}= 5.4V	–1.5%		1.5%	
	LDO_OREF line transient response (8)	V_{IN} + 500 mVp-p AC Square Wave, 100 mV/µs 200 Hz at 5 mA, C_{IN} = 10 µF	–50		50	mV
	LDO_OREF load transient (8)	5 mA to 50 mA load transient @ 2 µs $T_{RISE/FALL}$, C_{IN} = 10 µF	–50		50	mV
	DC load regulation (8)	1 mA ≤ $I_{LOAD\_LDO\_OREF}$ ≤ $I_{LOAD\_LDO\_OREF\_MAX}$			20	mV
PG_{RISING}	Power good increasing	% of target V_{LDO_OREF}		95%		

(7) Typical value only for reference.
(8) Limits set by characterization and/or simulation only.

Electrical Characteristics (continued)

Unless otherwise specified, limits apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ 85°C), V_{IN} = 3.6 V, V_{POS} = V_{OREF} = 5.4 V, V_{NEG} = –5.4 V, V_{BST} = 5.7 V, V_{CONT} = 3.3V.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$PG_{FALLING}$	Power good decreasing	% of target V_{LDO_OREF}		90%		
I_{OREF_MAX}	Maximum output current			50		mA
I_{CL_OREF}	Output current limit			80		mA
$I_{RUSH\_PK\_OREF}$	Peak start-up inrush current (8)	$V_{BIASBST}$ = 5.8 V, V_{OREF} = 5.5 V, C_{OREF} = 10 µF		250		mA
V_{DO_OREF}	LDO_OREF dropout voltage (9)	$I_{LOAD\_LDO\_OREF}$ = $I_{LOAD\_LDO\_OREF\_MAX}$, V_{LDO_OREF} = 4.0 V		80		mV
$PSRR_{OREF}$	Power supply rejection ratio, LDO_OREF (8)	F = 10 Hz to 500 kHz @ $I_{max/2}$, V_{BST_OUT} to V_{LDO_OREF}, 300 mV minimum headroom		25		dB
t_{ST_OREF}	Start-up time, LDO_OREF, VLDO_OREF = 10% to 90% (8)	C_{OREF} = 10 µF, V_{LDO_OREF} = 5.5 V			1	ms
R_{PD_OREF}	Output pull-down resistor, LDO_OREF	LDO_OREF pull-down enabled, LDO_OREF disabled	130	200	270	Ω
LCD CONTROLLER SUPPLY OUTPUT (LDO_CONT)						
V_{CONT}	Output voltage	LDO_CONT_VOUT = 00		1.8		V
		LDO_CONT_VOUT = 01		2.3		
		LDO_CONT_VOUT = 10		2.8		
		LDO_CONT_VOUT = 11		3.3		
	Output accuracy	Output Voltage = 1.8 V, 1-mA load	–2%		2%	
	LDO_CONT line transient response (8)	V_{IN} + 500 mVp-p AC Square Wave, 100 mV/µs 200 Hz at 5 mA	–50		50	mV
	LDO_CONT load transient response (8)	5-mA to 80-mA load transient @ 2 µs $T_{RISE/FALL}$	–50		50	mV
	DC load regulation (8)	1 mA ≤ $I_{LOAD\_LDO\_CONT}$ ≤ 80 mA			20	mV
I_{CONT_MAX}	Maximum output current			80		mA
I_{CL_CONT}	Output current limit			130		mA
V_{DO_CONT}	LDO_CONT dropout voltage (10)	I_{LOAD} = 80 mA, V_{CONT} = 3.3 V			80	mV
$PSRR_{LDO\_CONT}$	Power supply rejection ratio, LDO_CONT (11)	F = 10 Hz to 500 kHz @ $I_{max/2}$ V_{IN} to V_{LDO_CONT}, 300-mV minimum headroom		25		dB
t_{ST_CONT}	Start-up time, LDO_CONT, V_{CONT} = 10% to 90% (11)	V_{CONT} = 1.8 V			1	ms
R_{PD_CONT}	Output pull-down resistor, LDO_CONT	LDO_CONT pull-down enabled, LDO_CONT disabled		200		Ω
LOGIC INPUTS (PWM, NRST, LCD_EN, SCL, SDA, OTP_SEL)						
V_{IL}	Input logic low		0		0.4	V
V_{IH}	Input logic high		1.2		V_{IN}	V
I_{INPUT}	Logic input current		–1		1	µA
LOGIC OUTPUTS (SDA, FLAG)						
V_{OL}	Output logic low	I_{OL} = 3 mA	0		0.4	V
$I_{LEAKAGE}$	Output leakage current				1	µA
PWM INPUT						
f_{PWM_INPUT}	PWM input frequency		100		20000	Hz
t_{MIN}	Minimum PWM ON/OFF time			400		ns
$t_{TIMEOUT}$	PWM timeout (11)			24		ms

(9) V_{BST} – V_{OREF} when V_{OREF} has dropped 100 mV below target.
(10) V_{IN} – V_{CONT} when V_{CONT} has dropped 100 mV below target.
(11) Limits set by characterization and/or simulation only.

7.6 I²C Timing Requirements (SDA, SCL) (1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	Clock frequency				400	kHz
1	Hold time (repeated) START condition		0.6			µs
2	Clock low time		1.3			µs
3	Clock high time		600			ns
4	Set-up time for a repeated START condition		600			ns
5	Data hold time		50			ns
6	Data set-up time		100			ns
7	Rise time of SDA and SCL		20 + 0.1C_b		300	ns
8	Fall time of SDA and SCL		15 + 0.1C_b		300	ns
9	Set-Up time between a STOP and a START condition		1.3			µs
C_b	Capacitive load for each bus line		10		200	pF

(1) Limits set by characterization and/or simulation only

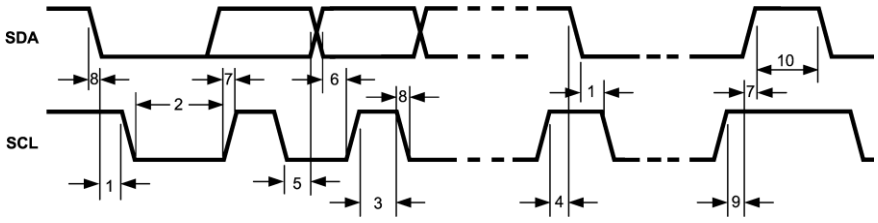
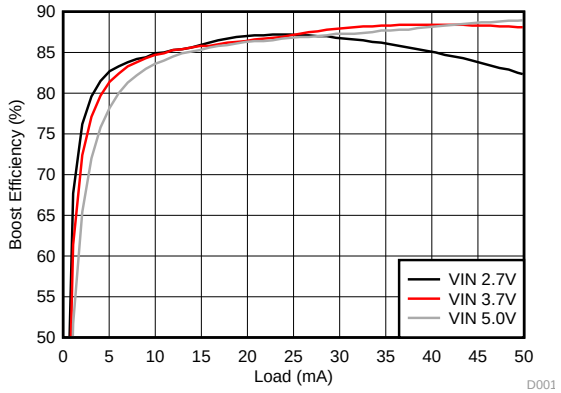


Figure 1. I²C Timing Parameters

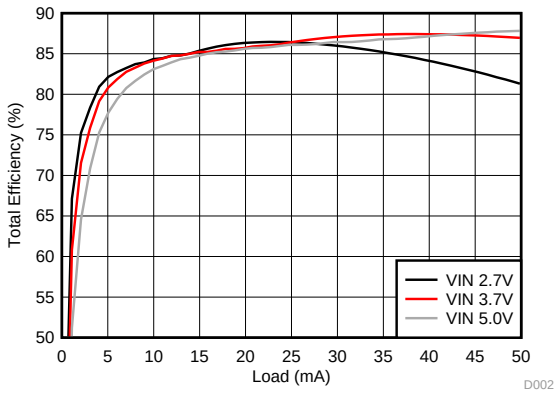
7.7 Typical Characteristics

Ambient temperature is 25°C unless otherwise noted. Backlight load is the sum of LED1 and LED2 current. Backlight Total Efficiency defined as P_{LED} / P_{IN}, where P_{LED} is actual power consumed in LEDs.



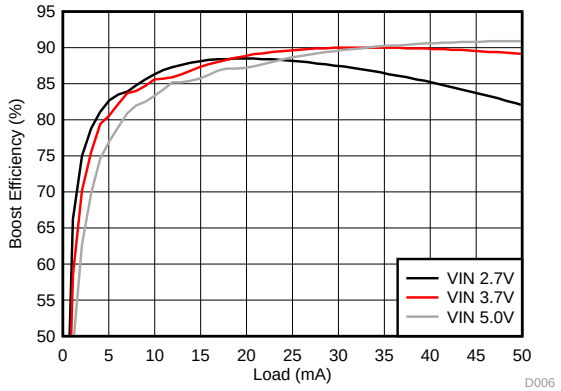
1235AS-H-220M 22-µH Inductor
2P6S LED Configuration
500-kHz Boost SW Frequency

Figure 2. Backlight Boost Efficiency



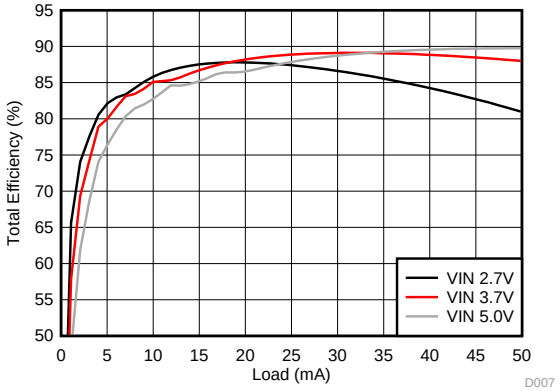
1235AS-H-220M 22-µH Inductor
2P6S LED Configuration
500-kHz Boost SW Frequency

Figure 3. Backlight Total Efficiency



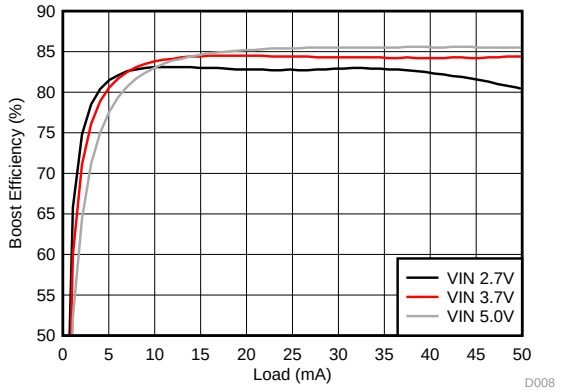
1235AS-H-220M 22-µH Inductor
2P6S LED Configuration
1-MHz Boost SW Frequency

Figure 4. Backlight Boost Efficiency



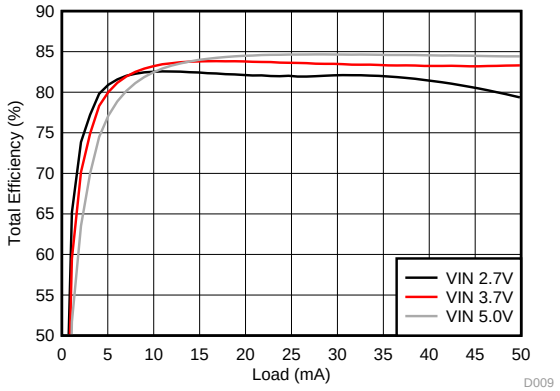
1235AS-H-220M 22-µH Inductor
2P6S LED Configuration
1-MHz Boost SW Frequency

Figure 5. Backlight Total Efficiency



VLF403210MT-100M 10-µH Inductor
2P6S LED Configuration
500-kHz Boost SW Frequency

Figure 6. Backlight Boost Efficiency

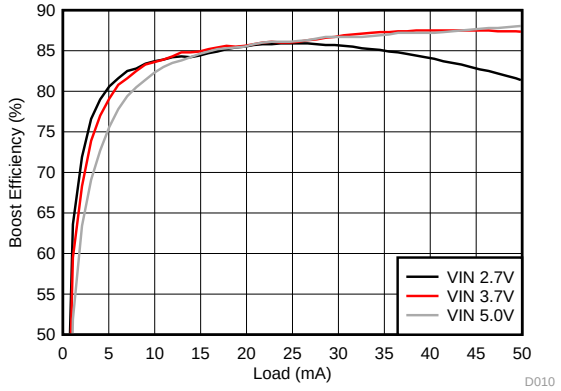


VLF403210MT-100M 10-µH Inductor
2P6S LED Configuration
500-kHz Boost SW Frequency

Figure 7. Backlight Total Efficiency

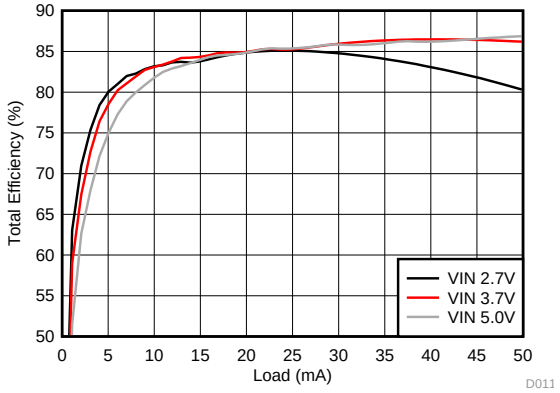
Typical Characteristics (continued)

Ambient temperature is 25°C unless otherwise noted. Backlight load is the sum of LED1 and LED2 current. Backlight Total Efficiency defined as P_{LED} / P_{IN}, where P_{LED} is actual power consumed in LEDs.



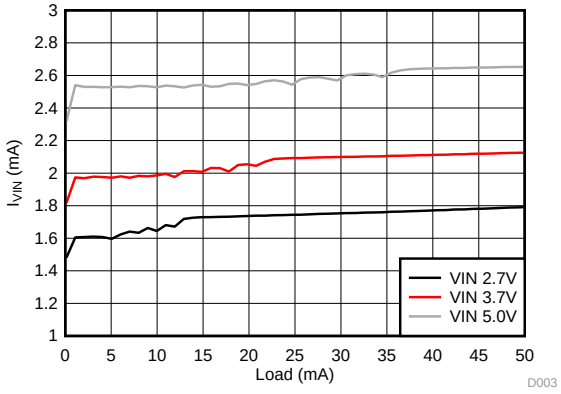
VLF403210MT-100M 10-µH Inductor
2P6S LED Configuration
1-MHz Boost SW Frequency

Figure 8. Backlight Boost Efficiency



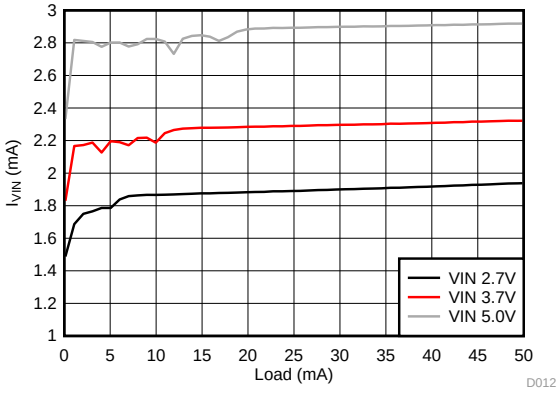
VLF403210MT-100M 10-µH Inductor
2P6S LED Configuration
1-MHz Boost SW Frequency

Figure 9. Backlight Total Efficiency



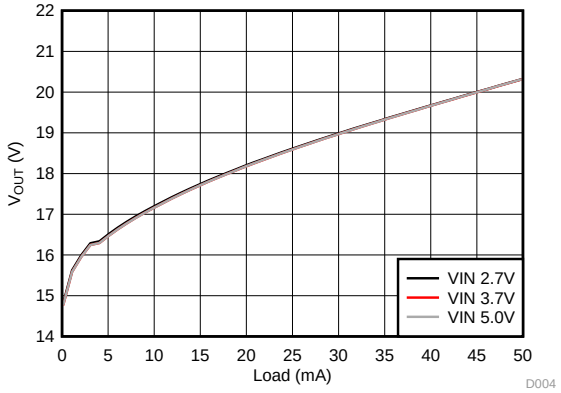
No load on LCD Bias
2P6S LED Configuration
500-kHz BL Boost SW Frequency

Figure 10. Device Current Consumption, Backlight Driving



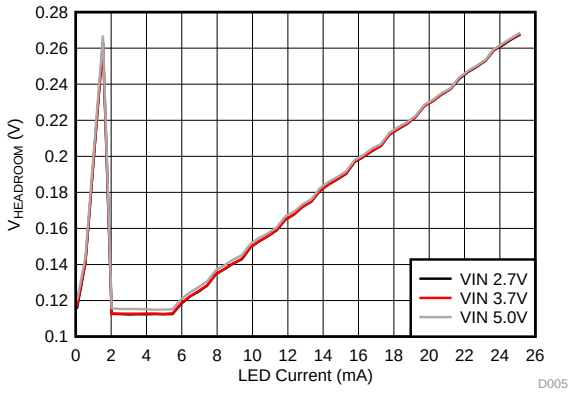
No load on LCD Bias
2P6S LED Configuration
1-MHz BL Boost SW Frequency

Figure 11. Device Current Consumption, Backlight Driving



2P6S LED Configuration

Figure 12. Backlight Boost Output Voltage

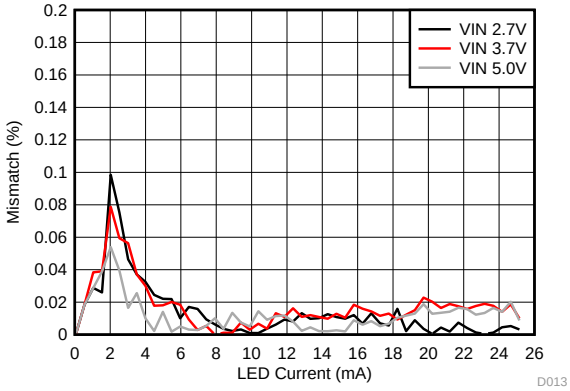


2P6S LED Configuration

Figure 13. LED Driver Headroom Voltage

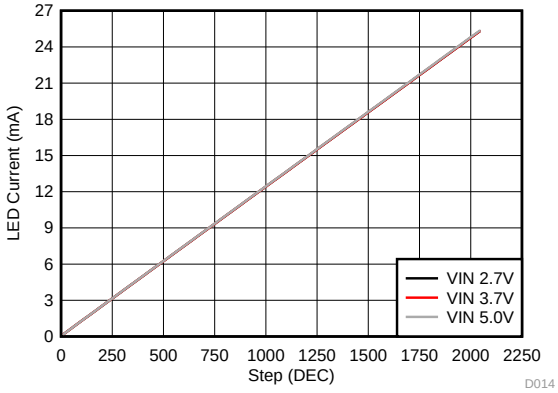
Typical Characteristics (continued)

Ambient temperature is 25°C unless otherwise noted. Backlight load is the sum of LED1 and LED2 current. Backlight Total Efficiency defined as P_{LED} / P_{IN}, where P_{LED} is actual power consumed in LEDs.



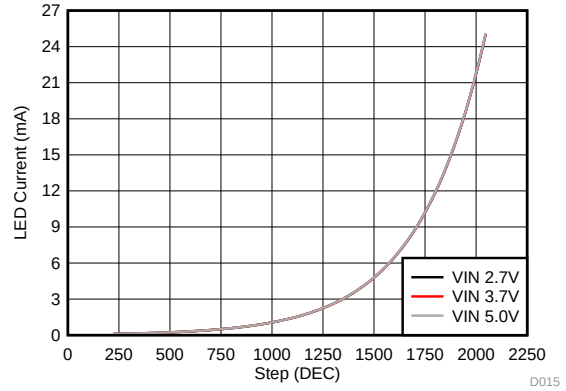
VLF403210MT-100M 10-µH Inductor
1-MHz BL Boost SW Frequency
2P6S LED Configuration

Figure 14. LED Current Matching



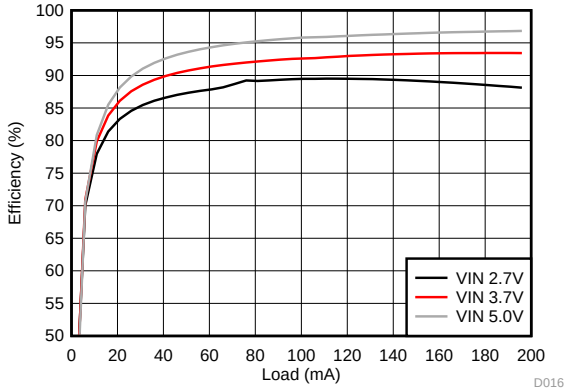
I^2C Brightness Control

Figure 15. LED Current, Linear Control



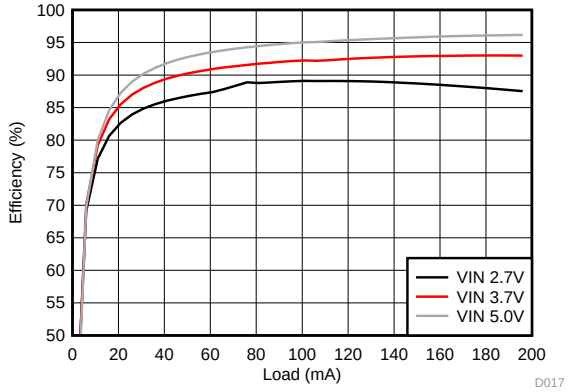
I^2C Brightness Control

Figure 16. LED Current, Exponential Control



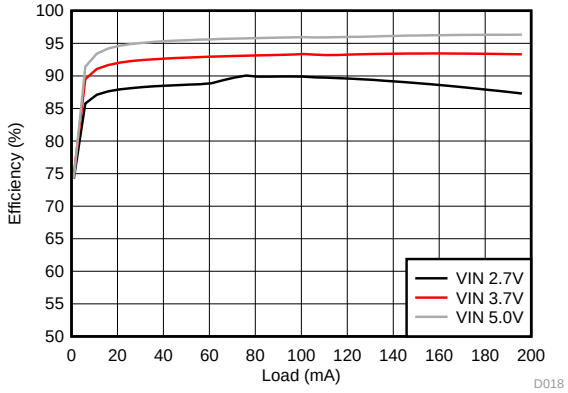
V_{BST} set to 5.2 V

Figure 17. LCD Boost Efficiency



V_{BST} set to 5.5 V

Figure 18. LCD Boost Efficiency

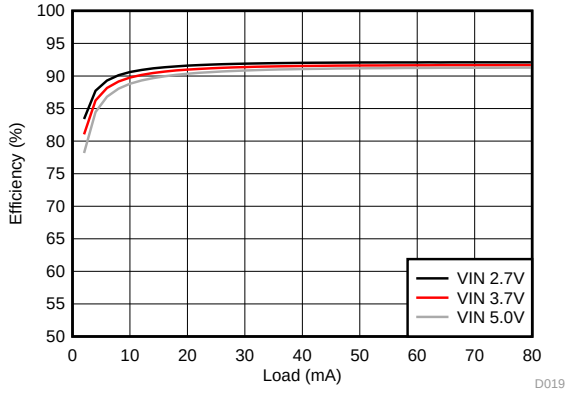


V_{BST} set to 5.9 V

Figure 19. LCD Boost Efficiency

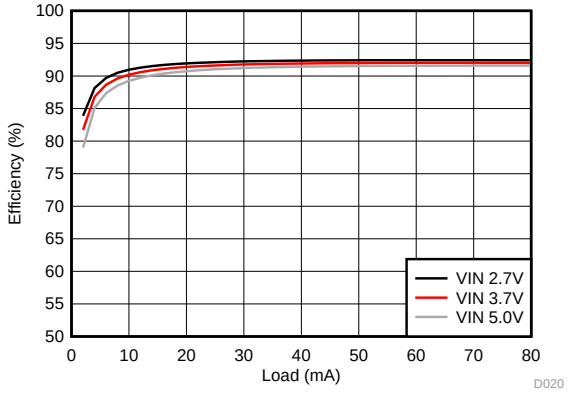
Typical Characteristics (continued)

Ambient temperature is 25°C unless otherwise noted. Backlight load is the sum of LED1 and LED2 current. Backlight Total Efficiency defined as P_{LED} / P_{IN}, where P_{LED} is actual power consumed in LEDs.



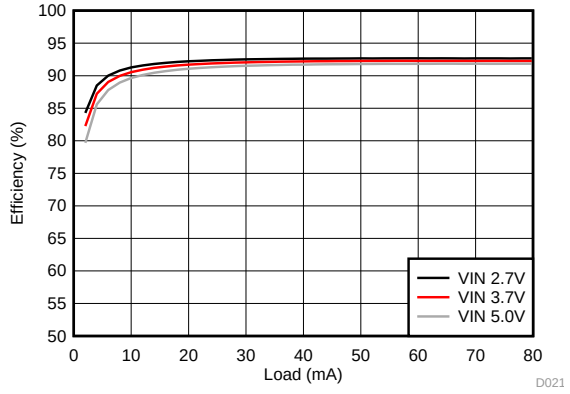
V_{NEG} set to –5 V

Figure 20. V_{NEG} Efficiency



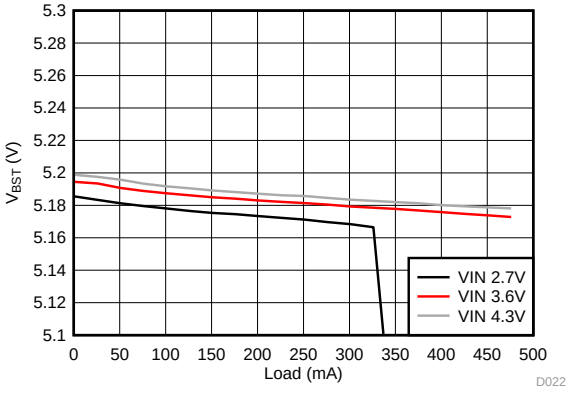
V_{NEG} set to –5.5 V

Figure 21. V_{NEG} Efficiency



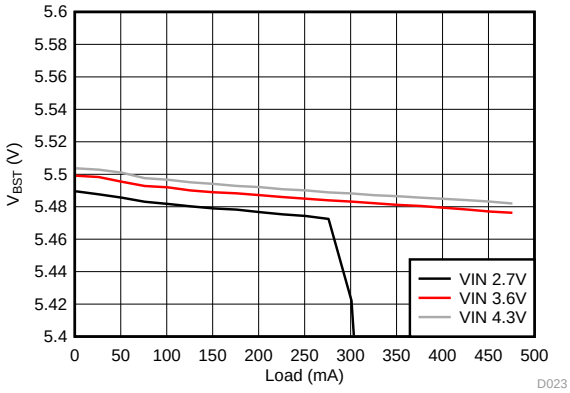
V_{NEG} set to –6 V

Figure 22. V_{NEG} Efficiency



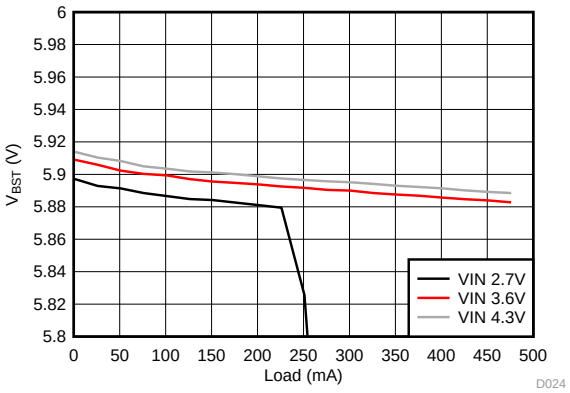
V_{BST} set to 5.2 V

Figure 23. LCD Boost Load Regulation



V_{BST} set to 5.5 V

Figure 24. LCD Boost Load Regulation

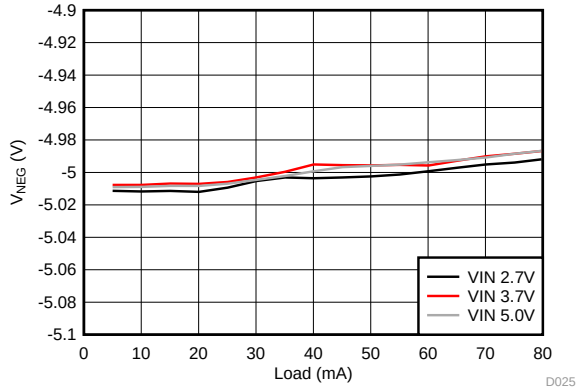


V_{BST} set to 5.9 V

Figure 25. LCD Boost Load Regulation

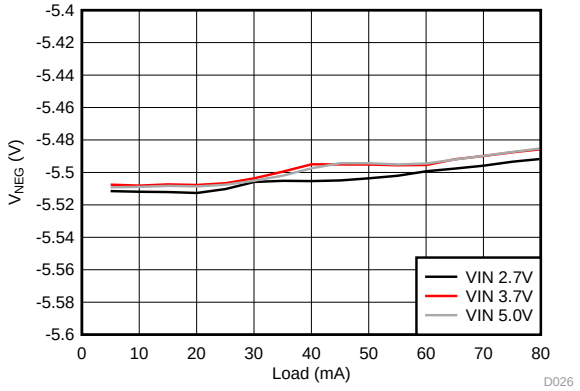
Typical Characteristics (continued)

Ambient temperature is 25°C unless otherwise noted. Backlight load is the sum of LED1 and LED2 current. Backlight Total Efficiency defined as P_{LED} / P_{IN}, where P_{LED} is actual power consumed in LEDs.



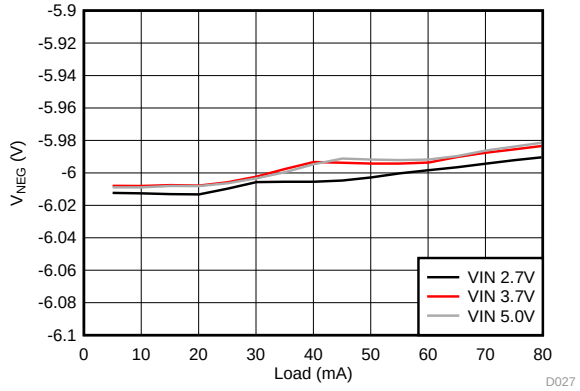
V_{NEG} set to –5 V

Figure 26. V_{NEG} Load Regulation



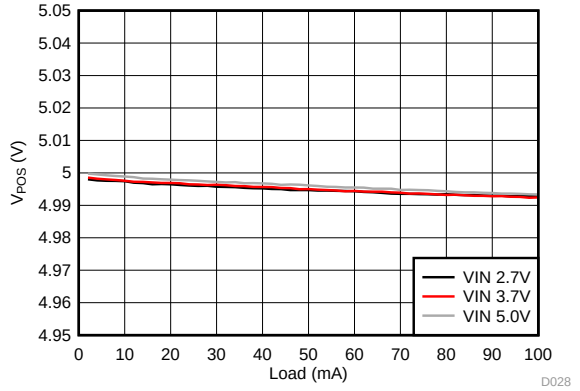
V_{NEG} set to –5.5 V

Figure 27. V_{NEG} Load Regulation



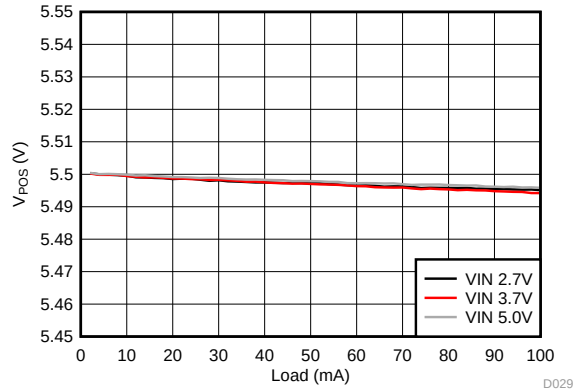
V_{NEG} set to –6 V

Figure 28. V_{NEG} Load Regulation



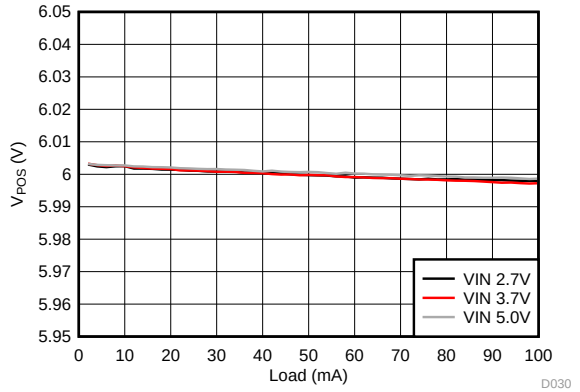
V_{POS} set to 5 V

Figure 29. V_{POS} Load Regulation



V_{POS} set to 5.5 V

Figure 30. V_{POS} Load Regulation

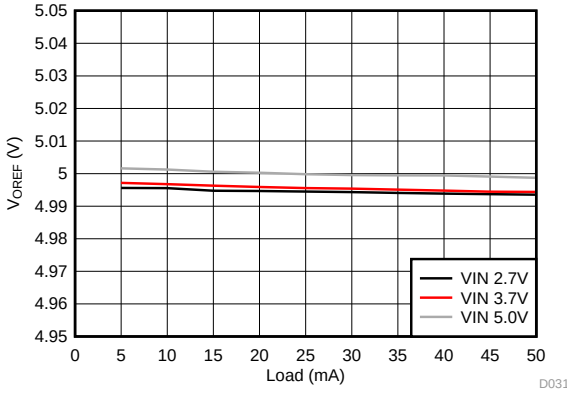


V_{POS} set to 6 V

Figure 31. V_{POS} Load Regulation

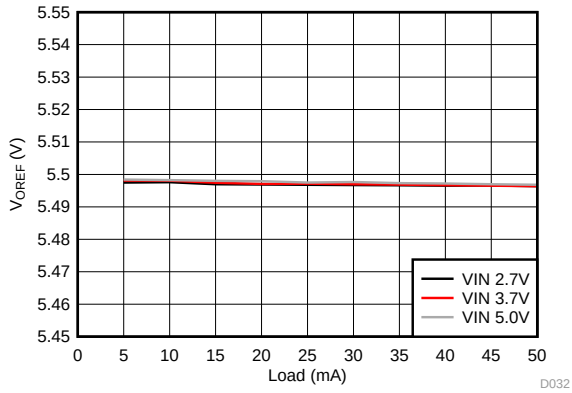
Typical Characteristics (continued)

Ambient temperature is 25°C unless otherwise noted. Backlight load is the sum of LED1 and LED2 current. Backlight Total Efficiency defined as P_{LED} / P_{IN}, where P_{LED} is actual power consumed in LEDs.



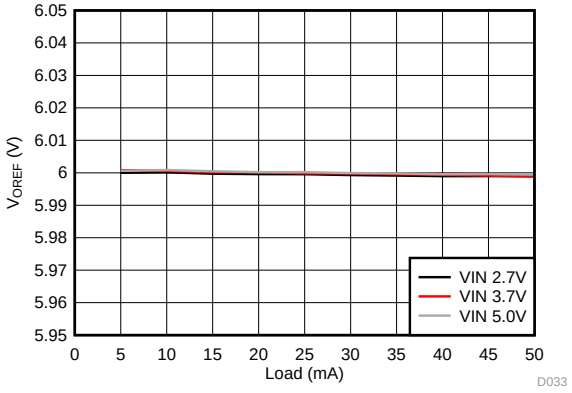
V_{OREF} set to 5 V

Figure 32. V_{OREF} Load Regulation



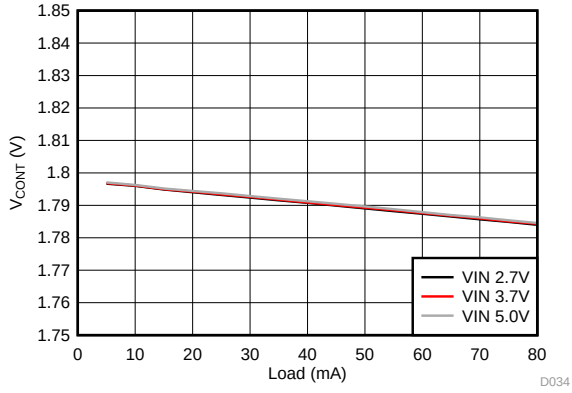
V_{OREF} set to 5.5 V

Figure 33. V_{OREF} Load Regulation



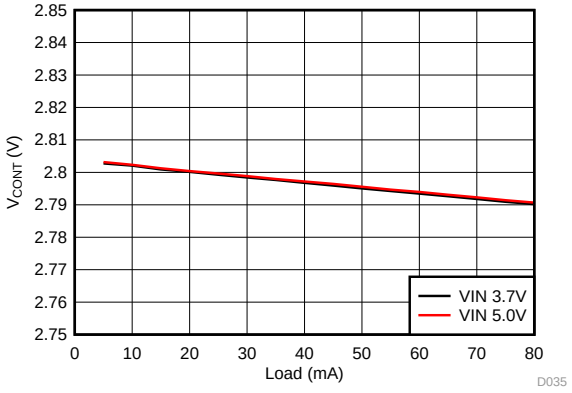
V_{OREF} set to 6 V

Figure 34. V_{OREF} Load Regulation



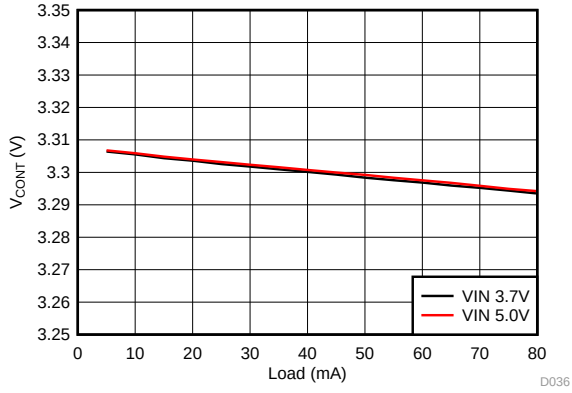
V_{CONT} set to 1.8 V

Figure 35. V_{CONT} Load Regulation



V_{CONT} set to 2.8 V

Figure 36. V_{CONT} Load Regulation



V_{CONT} set to 3.3 V

Figure 37. V_{CONT} Load Regulation

8 Detailed Description

8.1 Overview

The LM3631 is a single-chip complete LCD power and backlight solution. It can drive up to two LED strings with up to 8 LEDs each (up to 27 V typ.), with a maximum of 25 mA per string. The power for the LED strings comes from a integrated asynchronous backlight boost converter with two selectable switching frequencies (500 kHz or 1 MHz) to optimize performance or solution area. LED current is regulated by two low-headroom current sinks. Automatic voltage scaling adjust the output voltage of the backlight boost converter to minimize the LED driver head room voltage.

The LCD bias power portion of the LM3631 consists of an LCD bias boost converter, inverting charge pump, and three integrated LDOs. The device can generate all the required voltages for a LCD panel:

1. The LCD positive bias voltage V_{POS} (up to 6V). V_{POS} voltage is post-regulated from the LCD bias boost converter output voltage.
2. LCD negative bias voltage V_{NEG} (down to –6 V). V_{NEG} is generated from the LCD bias boost converter output using a regulated inverting charge pump.
3. The third output V_{OREF} can supply the LCD gamma (or VCOM reference) voltage. V_{OREF} is post-regulated from the LCD bias boost converter output voltage.
4. The fourth output V_{CONT} can be used to supply the display controller. V_{CONT} regulator is powered from the VIN input.

The LM3631 flexible control interface consists from nRST active low reset input, LCD_EN enable input, PWM input for content adaptive backlight control (CABC), and an I^2C-compatible interface. In applications with limited IO pin count the LCD_EN input pin function can be replaced with the LCD_EN I^2C register bit. In this case the LCD_EN pin needs to be connected to ground. OTP_SEL input can be used to select from two different factory-programmed default One Time Programmable Memory (OTP) settings. The default OTP settings can be overwritten using the I^2C-compatible interface. Programmable settings include LED ramp up/down profiles, LED output current and brightness control modes, enabling/disabling individual power supply outputs, and programmable LCD output power up/down sequencing. Open drain FLAG output can be used to notify host processor from various power-good signals or fault conditions.

Overview (continued)

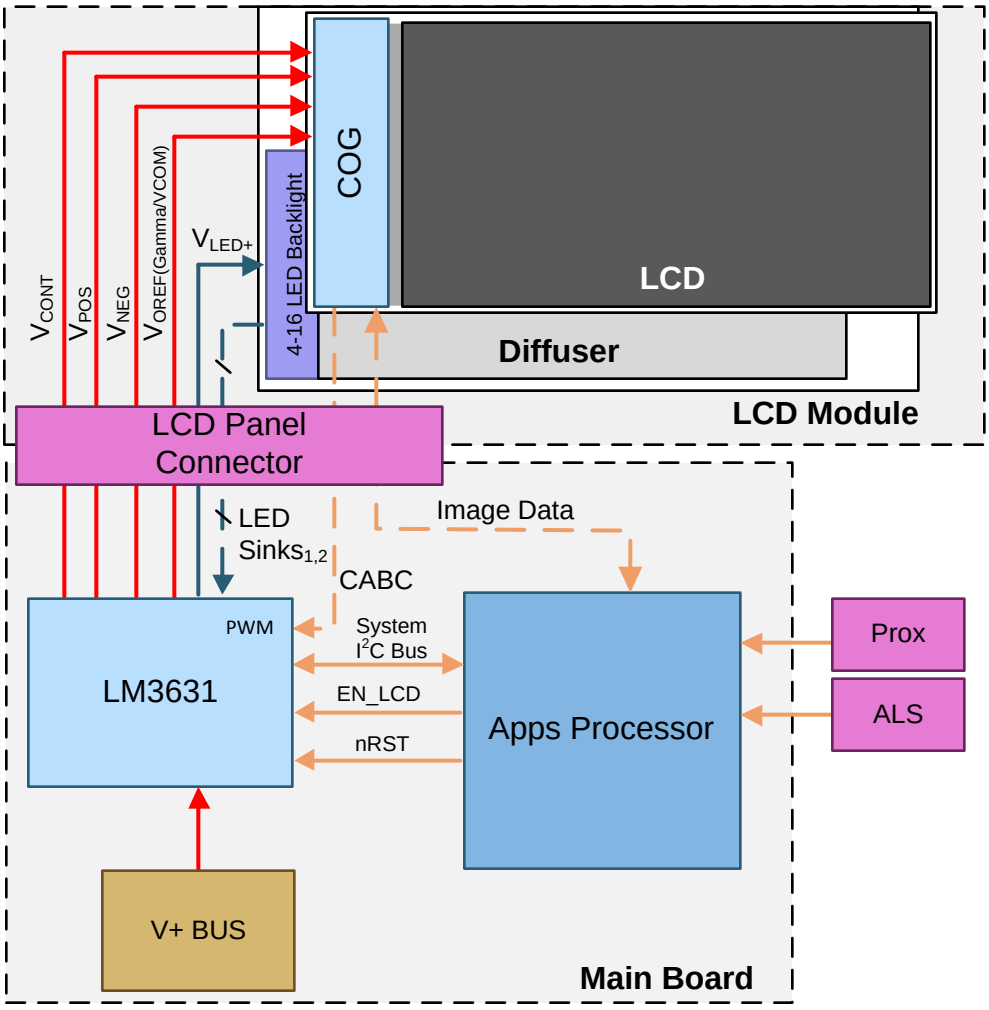
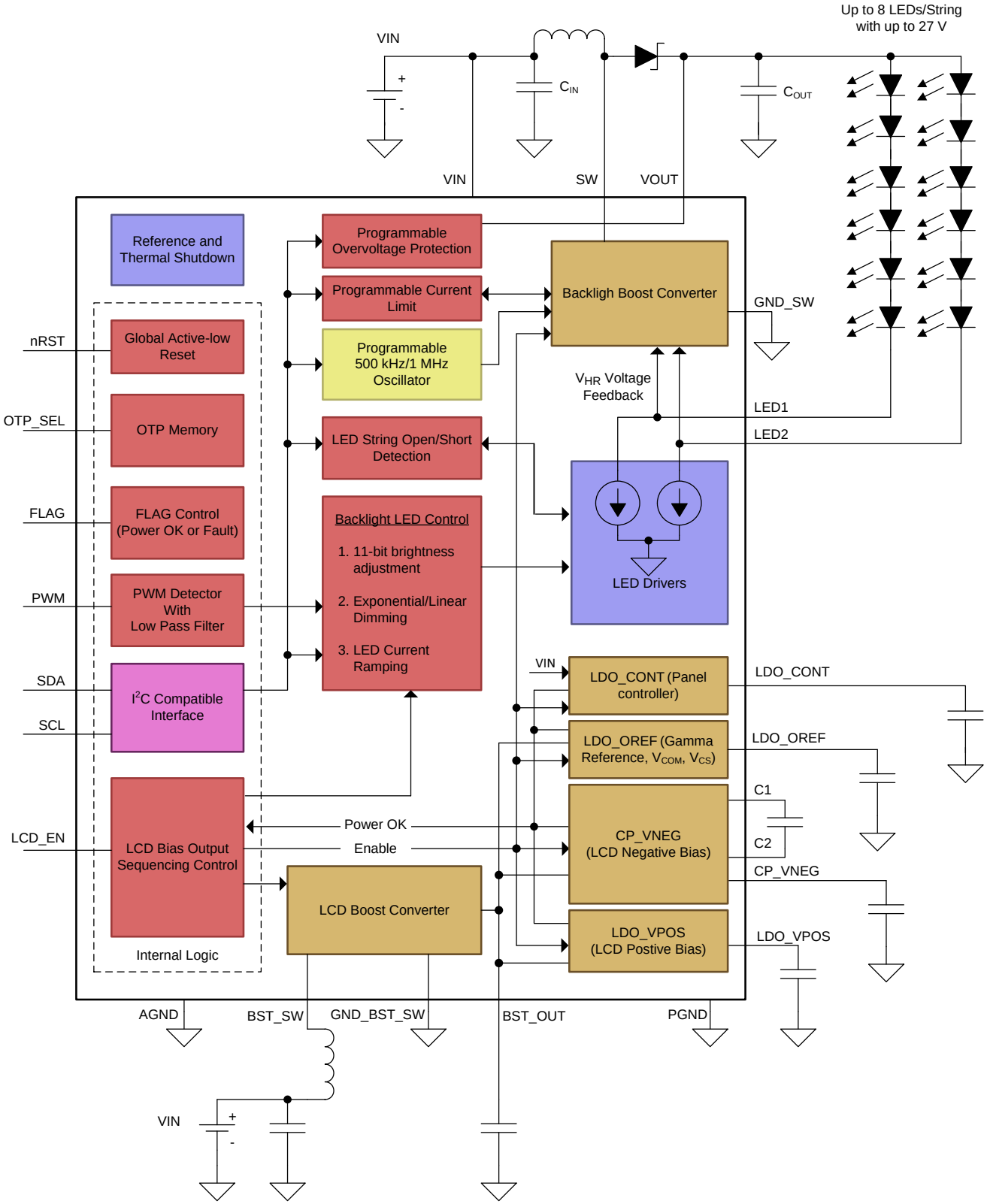


Figure 38. System Example

8.2 Functional Block Diagram



8.3 Features Description

8.3.1 Backlight

The backlight is enabled by setting the BL_EN = 1 and a brightness value higher than zero. LCD bias power rails need to reach their target voltages before the backlight can be started. Note that all bias voltages don't need to be enabled to start up the backlight. For example, if only V_{POS} and V_{NEG} are required, the backlight can be enabled once these voltages have reach their target voltages. In this case V_{CONT} and V_{OREF} can be disabled. If all four outputs (LDO_CONT, LDO_OREF, CP_VNEG, and LDO_VPOS) are disabled, the backlight can be enabled once the LCD biast boost converter has settled. The LCD bias boost is always enabled when the LCD_EN pin or bit is set high.

When the brightness value is '0', or BL_EN bit is ‘0’, the backlight is disabled. The BL_EN bit is '1' by default. The backlight can be disabled at any time by setting the brightness value to zero or by writing the BL_EN bit to ‘0’.

LED driver LED2 can be separately enabled and disabled from the I^2C register. LED driver LED1 is always enabled when the backlight is turned on.

Table 2. Backlight Control

BL_EN BIT	BRIGHTNESS VALUE (I^2C AND/OR EXTERNAL PWM)	BACKLIGHT ON/OFF
0	0	OFF
0	≥1	OFF
1	0	OFF
1	≥1	ON

8.3.1.1 Backlight Brightness Control

Brightness can be controlled either by the I^2C brightness register, with an external PWM control, or a combination of both. BRT_MODE bits select the brightness control mode. Different brightness control modes are shown in Table 3.

When controlling brightness through I^2C, registers 0x01 and 0x02 are used. Registers 0x01 and 0x02 hold the 11-bit brightness data. Register 0x02 contains the 8 MSBs, and register 0x01 contains the 3 LSBs. The LED current only transitions to the new level after a write is done to register 0x02.

When controlling brightness through I^2C, setting brightness value to '0' shuts down the backlight. When controlling the brightness with PWM input, if PWM input is low for a certain period of time (24 ms typ.), the backlight shuts down. When using the combination of a PWM input and the I^2C register, either option shuts down the backlight.

NOTE

The backlight does not start before the LCD bias start-up sequence is finished even if BL_EN bit is '1' and the brightness setting is ≥ 1.

Table 3. Brightness Control

BRT_MODE bits	BRIGHTNESS CONTROL
00	I^2C register used for brightness control
01	PWM input duty cycle used for brightness control
10	I^2C register code multiplied with PWM duty cycle before sloping
11	Sloped I^2C register code multiplied with PWM duty cycle

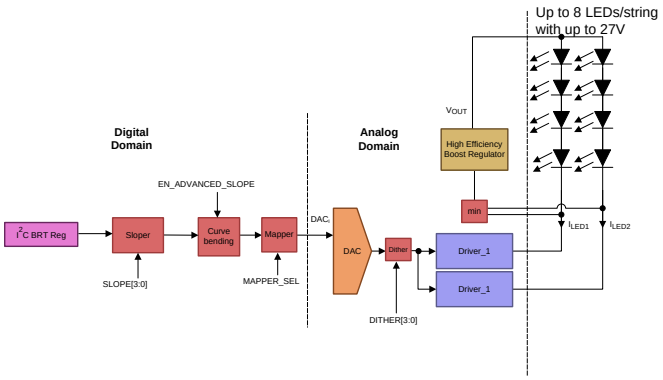


Figure 39. Brightness Control with BRT_MODE bit 00

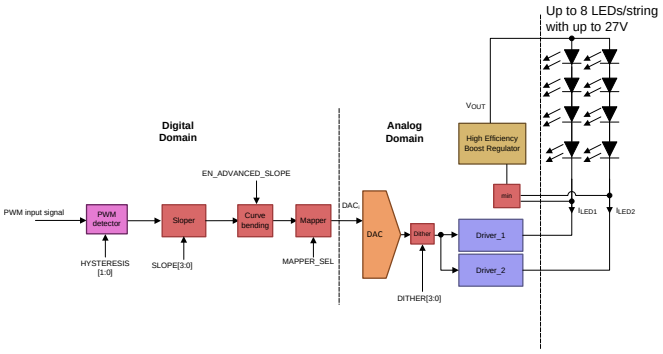


Figure 40. Brightness Control with BRT_MODE bit 01

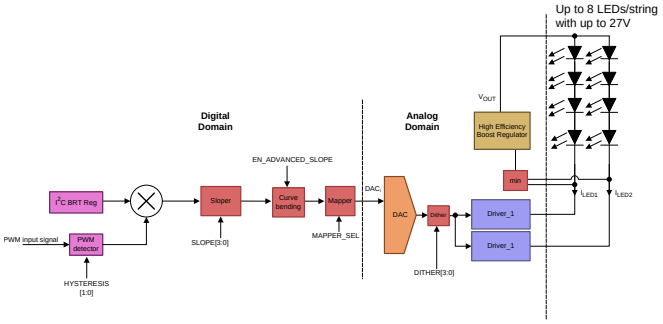


Figure 41. Brightness Control with BRT_MODE bit 10

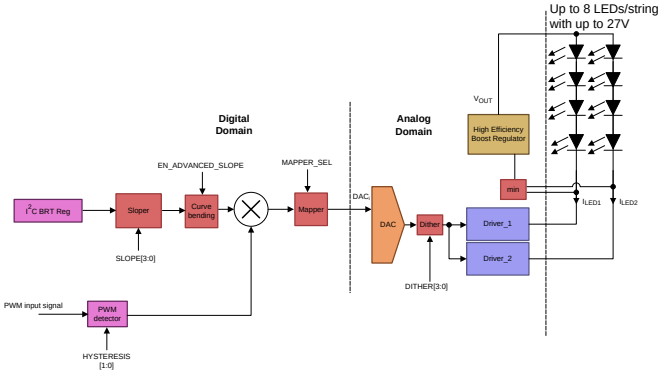


Figure 42. Brightness Control with BRT_MODE bit 11

8.3.1.1.1 LED Current With Brightness Selection '00'

When LED brightness is controlled from the I^{2}C brightness registers, the 11-bit brightness data directly controls the LED current in LED1 and LED2. LED mapping can be selected as either linear or exponential. When this mode is selected setting PWM input to 0 does not disable the backlight.

With exponential mapping the 11-bit code-to-current response is approximated by the equation:

$$I_{LED} = 50\ \mu A \times 1.003040572^{I2C\ BRT\ CODE} \text{ (for codes > 0)} \quad (1)$$

This equation is valid for I^{2}C brightness codes between 1 and 2047. Code 0 disables the backlight. Resolution achieved at the output is maximum 16-bit at low brightness levels and additional 1 bit can be achieved with the dithering resulting in up to 17-bit output resolution. Step sizes increase when the current increases with the exponential control.

Figure 43 and Figure 44 detail the exponential response of the LED current vs. brightness code. Figure 43 shows the response on a linear Y axis while Figure 44 shows the response on a log Y axis to show the low current levels at the lower codes.

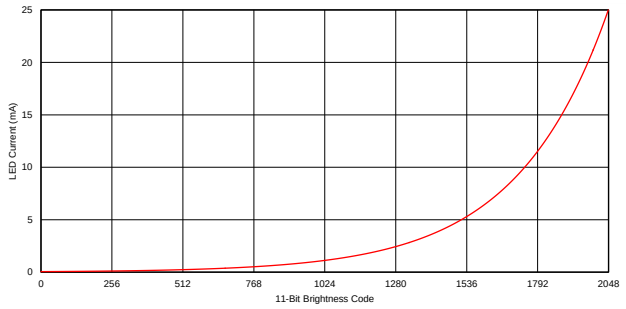


Figure 43. Exponential Response of the LED Current vs Brightness Code

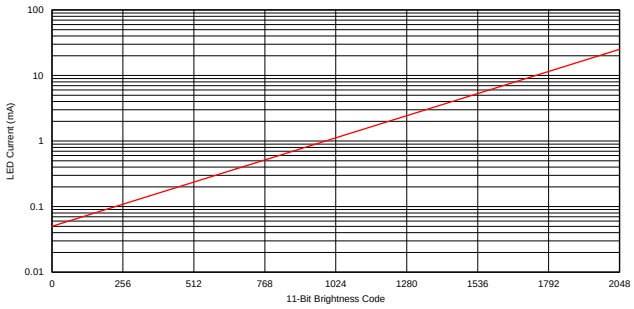


Figure 44. Response of the LED Current vs Brightness Code on a Log Y Axis

With linear mapping the 11-bit code to current response is approximated by the equation:

$$I_{LED} = 37.67\ \mu A + 12.33\ \mu A \times \text{I2C BRT CODE (for codes} > 0) \quad (2)$$

This equation is valid for codes between 1 and 2047. Code 0 disables the backlight.

8.3.1.1.2 LED Current With Brightness Selection '01'

When LED brightness is controlled from the PWM, the PWM duty cycle directly controls the LED current in LED1 and LED2. LED mapping can be selected to be either linear or exponential. When this mode is selected, setting the I^2C brightness register to 0 does not disable the backlight.

With exponential mapping the PWM duty cycle-to-current response is approximated by the equation:

$$I_{LED} = 50\ \mu A \times 1.003040572^{2047 \times \text{PWM D/C}} \text{ (PWM D/C} \neq 0) \quad (3)$$

Equation 3 is valid for PWM duty cycles other than 0. Duty cycle 0 disables the backlight.

With linear mapping the PWM duty cycle-to-current response is approximated by the equation:

$$I_{LED} = 37.67\ \mu A + (12.33\ \mu A \times 2047 \times \text{PWM D/C}) \text{ (PWM D/C} \neq 0) \quad (4)$$

Equation 4 is valid for PWM duty cycles other than 0. Duty cycle 0 disables the backlight.

8.3.1.1.3 LED Current With Brightness Selections '10' and '11'

When LED brightness is controlled with the combination of the I^2C register and the PWM duty cycle, the multiplication result of I^2C register value and PWM duty cycle controls the LED current in LED1 and LED2. LED mapping can be selected as either linear or exponential.

With exponential mapping the multiplication result-to-current response is approximated by the equation:

$$I_{LED} = 50\ \mu A \times 1.003040572^{\text{I2C BRT CODE} \times \text{PWM D/C}} \quad (5)$$

Equation 5 is valid for brightness values other than 0. Brightness value (PWM D/C or I2C BRT CODE) 0 disables the backligh.

With linear mapping the PWM duty cycle-to-current response is approximated by the equation:

$$I_{LED} = 37.67\ \mu A + (12.33\ \mu A \times \text{I2C BRT CODE} \times \text{PWM D/C}) \quad (6)$$

Equation 6 is valid for brightness values other than 0. Brightness value (PWM D/C or I2C BRT CODE) 0 programs 0 current.

The key difference between the two brightness modes is how the PWM input affects the LED output current. When brightness mode is '10', changing PWM value causes LED current to slope form the current value to the new value. With the brightness setting '11', a change in PWM value causes an instant change in the LED current. This makes brightness setting '11' suitable for CABC operation.

8.3.1.2 Linear Slope and Advanced Slope

Sloper smooths the transition from one brightness value to another. Slope time can be adjusted from 0 ms to 4000 ms with SLOPE[3:0] bits. Slope time is used for sloping up and down. Slope time always remains the same regardless of the amount of change in brightness. Advanced slope makes brightness changes smooth for the human eye.

Dithering function further smooths the slope by jumping between two adjacent current values. Dithering frequency can be programmed with DITHER_FREQ_SEL[3:0] bits. Dithering function can be disabled with DISABLE_DITHER bit.

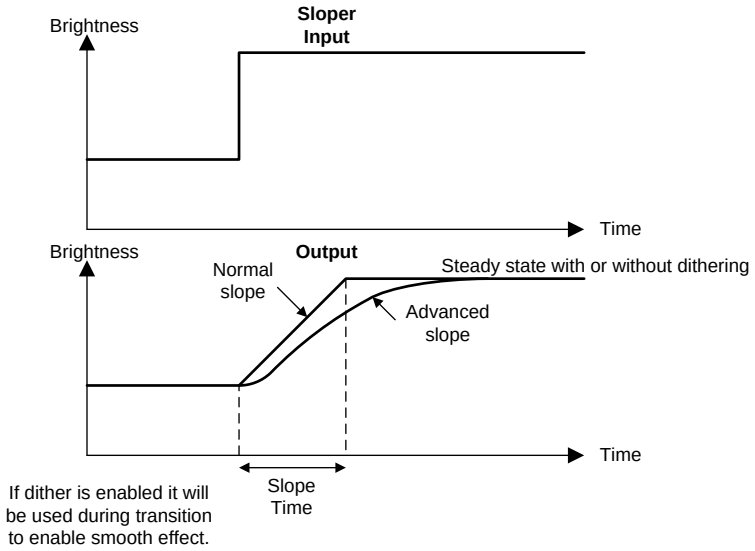


Figure 45. Sloper

Table 4. Slope Times

SLOPE BITS[3:0]	SLOPE TIME (ms)
0000	0, slope function disabled, immediate brightness change
0001	1
0010	2
0011	5
0100	10
0101	20
0110	50
0111	100
1000	250
1001	500
1010	750
1011	1000
1100	1500
1101	2000
1110	3000
1111	4000

8.3.1.3 Mapper

The mapper block maps the digital word into current code which is set for the LED driver. The user can select whether the mapping is exponential or linear with the LINEAR_MAPPER bit.

Exponential control is tailored to the response of the human eye such that the perceived change in brightness during ramp up or ramp down is linear.

8.3.1.4 PWM Detector and PWM Input

The PWM detector block measures the duty cycle in the PWM pin. The PWM period is measured from the rising/falling edge to the next rising/falling edge. PWM edge detection can be selected as rising or falling from register 0x08 bit 7. PWM polarity can be changed with register 0x08 bit 6. The PWM input block timeout is 24 ms after the last rising edge, which should be taken into account for 0% and 100% brightness settings (for setting 100% brightness, high level of PWM input signal should be at least 24 ms). Minimum on and off times for PWM input signal are 400 ns.

PWM input resolution is defined by the PWM detector sampling rate (24 MHz typ.). Resolution depends on the input signal frequency — for example, with 10-kHz PWM input frequency the resolution is 11-bit. If a higher input frequency is used, the resolution is lower. The minimum recommended PWM frequency is 100 Hz, and maximum recommended PWM frequency is 20 kHz.

PWM hysteresis selection sets the minimum allowable change to the input. If a smaller change is detected, it is ignored. With hysteresis the constant changing between two brightness values is avoided if there is small jitter in the input signal. Hysteresis is selected with HYSTERESIS bits in register 0x08. Using a higher hysteresis setting is recommended with high PWM input frequencies.

The PWM detector is disabled in I^2C brightness mode to minimize current consumption.

8.3.2 Backlight Boost Converter

The LM3631 can drive two LED strings with up to 8 LEDs per string. The high voltage required by the LED strings is generated with an asynchronous backlight boost converter. An adaptive voltage control loop automatically adjusts the output voltage based on the voltage over the LED drivers LED1 and LED2.

The LM3631 has two switching frequency modes (high and low). These are set via the Boost Frequency Select bit. The nominal low- and high-frequency set points are 500 kHz and 1 MHz, respectively. Operation in low-frequency mode results in better efficiency at lighter load currents due to the decreased switching losses. Operation in high-frequency mode gives better efficiency at higher load currents due to the reduced inductor current ripple and the resulting lower conduction losses in the MOSFETs and inductor.

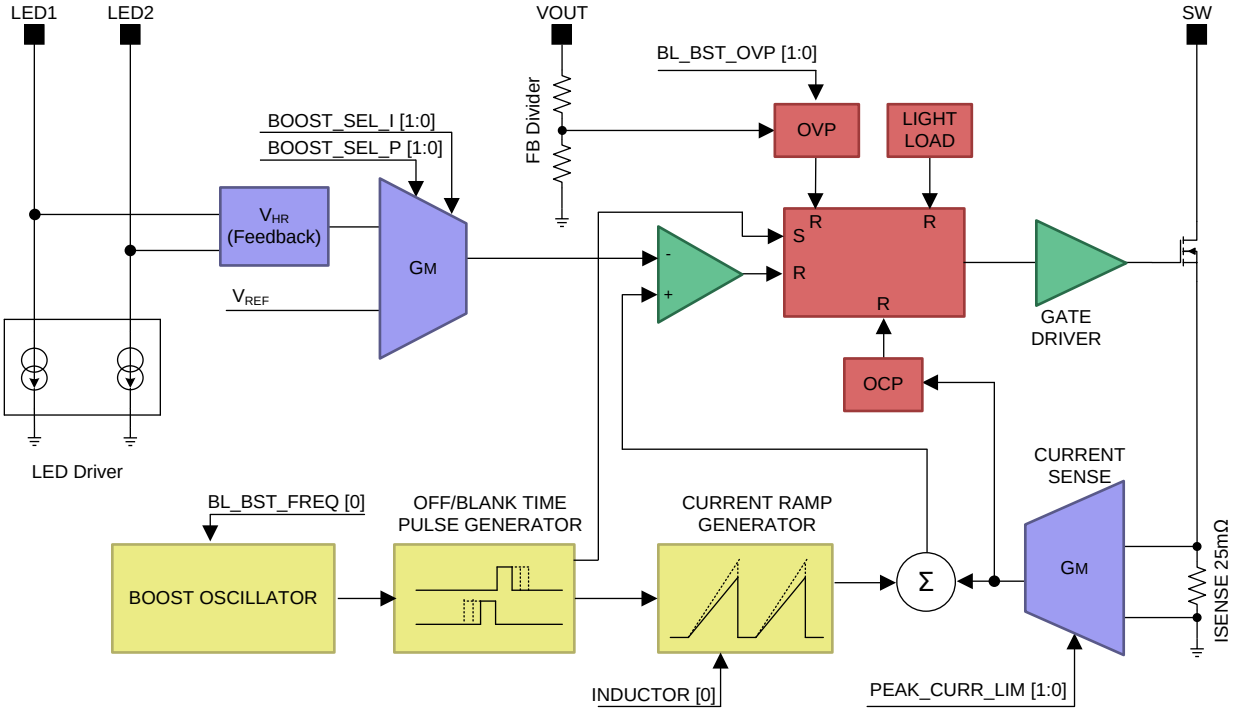


Figure 46. Backlight Boost Block Diagram

8.3.2.1 Headroom Voltage

Saturation voltage of the LED drivers depends on the output current setting. In order to optimize LED drive efficiency, while maintaining good LED current accuracy, the LED-driver-regulated headroom voltage (V_{HR}) is kept slightly above LED driver saturation voltage. To maintain good LED current accuracy with lower current settings, LED driver size is scaled down for the lower current settings (below 1/16 of max current). In order to ensure that both current sinks remain in regulation when there is a mismatch in string voltages, the boost converter output voltage is regulated based on the LED driver with lower headroom voltage. For example, if the LEDs connected to LED1 require 25 V at the programmed current, and the LEDs connected to LED2 require 25.5 V at the programmed current, the voltage at LED1 is V_{HR} + 0.5 V, and the voltage at LED2 is V_{HR}.

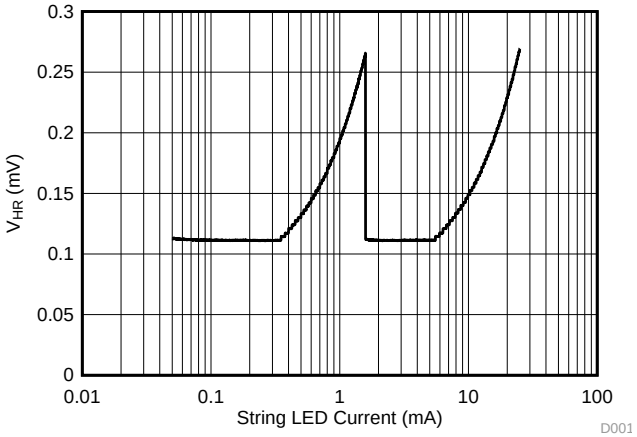


Figure 47. Regulated Headroom vs LED Current

8.3.2.2 Automatic Switching Frequency Shift

To take advantage of frequency vs load dependent losses, the LM3631 has an automatic frequency-select mode. In automatic frequency-select mode the switching-frequency bit is automatically changed based on the programmed LED current. The threshold (or LED Brightness Code) at which the frequency switchover occurs is programmable via the AUTOFREQ_THRESHOLD. This register contains an 8-bit code which is compared against the 8 MSB's of the brightness code (BRT[10:3]). When BRT[10:3] > AUTOFREQ_THRESH[7:0], the Boost Frequency Select Bit is set to a '1', and the device operates in high-frequency mode. When BRT[10:3] ≤ AUTOFREQ_THRESH[7:0], the Frequency Select Bit is automatically set to '0', and the device operates in low-frequency mode.

When automatic frequency-select mode is disabled, the switching frequency operates at the programmed high- or low-frequency setting across the entire LED current range.

8.3.2.3 Inductor Select Bit

The LM3631 can operate with a 10-µH or 22-µH inductor. However, the LM3631 backlight boost-control loop requires adjustment of internal loop compensation parameters based on the inductance value selected for the application. This is done through the INDUCTOR bit. For 10-µH inductors, the INDUCTOR bit must be set to '1'. For a 22-µH inductor, the INDUCTOR bit should be set to '0'.

8.3.2.4 PI-Compensator

The LM3631 backlight boost converter internal loop-compensation parameters (SEL_I[1:0] and SEL_P[1:0]) are factory-selected to optimize performance and stability for most backlight configurations. These settings should not need adjustment. If these settings are changed, application needs to be carefully evaluated to ensure stability and performance in all operating conditions.

8.3.3 Backlight Protection and Faults

8.3.3.1 Overvoltage Protection (OVP) and Open-Load Fault Protection

The LM3631 provides an OVP that monitors the LED boost output voltage (V_{OUT}) and protects OUT and SW from exceeding safe operating voltages. The OVP threshold can be set with the I^2C register bits. The OVP limit can be set to 17 V, 21 V, 25 V, or 29 V. The OVP monitor differentiates between two overvoltage conditions and responds accordingly as outlined below:

Case 1 (OVP Threshold hit and (VLED1 and VLED2) > 40 mV): In steady-state operation with V_{OUT} near the OVP threshold (V_{OVP}), a rapid change in V_{IN} or brightness code can result in a momentary transient excursion of V_{OUT} above the OVP threshold. In this case the boost circuitry is disabled until V_{OUT} drops below V_{OVP} - V_{HYST}. Once this happens the boost is re-enabled, and steady state regulation can commence. If the OVP pulse length is over 1 ms, an OVP fault is set.

Case 2 (OVP Threshold hit and (VLED1 and VLED2) < 40 mV): When one or all of the LED strings is open, the boost converter drives V_{OUT} above V_{OVP} and at the same time the open string(s) current sink headroom voltage(s) drops to 0. When LM3631 detects three pulses (if $V_{OUT} > V_{OVP}$ and (V_{LED1} or V_{LED2}) < 40 mV), the OVP Fault flag (BL_OVPFLT) is set. If the OVP pulse length is over 1 ms, an OVP fault is set. The flag is cleared with rising LCD_EN or an I^2C write.

8.3.3.2 Overcurrent Protection (OCP) and Overcurrent Protection Fault

The LM3631 has 4 selectable OCP thresholds. The programmable options are 600 mA, 700 mA, 800 mA, or 900 mA. The OCP threshold is a cycle-by-cycle current limit detected in the low-side NFET. Once the threshold is reached, the NFET turns off for the remainder of the switching period.

8.3.3.2.1 Overcurrent Protection Fault Flag (BL_OCPFLT)

If enough OCP threshold events occur the Overcurrent Protection Fault (BL_OCPFLT) flag is set. To avoid transient conditions from inadvertently setting the BL_OCPFLT Flag, a Pulse Density Counter monitors OCP threshold events over a 128-µs period. If the Pulse Density Counter counts 2 or more OCP events during the 128-µs period, the pulse density count is considered true. If 8 consecutive 128-µs periods occur where the pulse density count is true (1024 µs total), the BL_OCPFLT fault is set. Fault is cleared by rising edge of the LCD_EN or an I^2C write '1' to the BL_OCPFLT bit.

NOTE

The OCP signaling is ignored for 4 ms after the backlight boost is started or the brightness value is changed.

8.3.3.2.2 Short Circuit Fault Flag (BL_SCFLT)

If an OCP fault has occurred, and the headroom voltage is too low (VLED1 or VLED2 < 40 mV), the Short Circuit Fault (BL_SCFLT) fault is set, and all power is shut down. The fault must be cleared to enable power — it is cleared by the rising edge of the LCD_EN or by an I^2C write '1' to the BL_SCFLT bit.

NOTE

The OCP signaling is ignored for 4 ms after the backlight boost is started or the brightness value is changed.

8.3.4 LCD Bias

8.3.4.1 Display Bias Power (V_{POS}, V_{NEG}, V_{OREF})

A single high-efficiency boost converter provides a positive voltage rail, V_{BST_OUT}, which serves as the power rail for the LCD V_{POS} and V_{NEG} biases, as well as for an additional regulated output V_{OREF}. This can be used to supply the display gamma reference, V_{COM} and V_{CS} voltages.

- The V_{POS} output LDO, LDO_VPOS, has a programmable range from 4 V up to 6 V with 50-mV steps and can supply up to 100 mA.
- The V_{NEG} output, CP_VNEG, is generated from a regulated, inverting charge pump and has an adjustable

range of –6 V up to –4 V with 50-mV steps and a maximum load of 80 mA. During start-up there is a minimum delay of 500 µs due to biasing the flycap.

- The V_{OREF} output LDO, LDO_OREF, has programmable range from 4 V to 6 V, further adjustable in 50-mV increments and can supply up to 50 mA.

The boost voltage can be selected from the an I^2C register. When selecting suitable boost-output voltage, the following estimation can be used $V_{BST} = \max(V_{LDO\_VPOS}, |V_{CP\_VNEG}|, V_{LDO\_OREF}) + 200$ mV (with lower currents) or + 300 mV (with higher currents). When the device input voltage (V_{IN}) > sets the LCD boost output voltage, the boost voltage goes to V_{IN} + 100 mV.

Table 5. LCD Boost V_{OUT}

LCD_BOOST_VOUT BITS	LCD BOOST OUTPUT VOLTAGE (V)
000 000	4.50
000 001	4.55
000 010	4.60
000 011	4.65
000 100	4.70
000 101	4.75
000 110	4.80
...	...
011 111	6.05
100 000	6.10
100 001	6.15
100 010	6.20
100 011	6.25
100 100	6.30
100 101	6.35

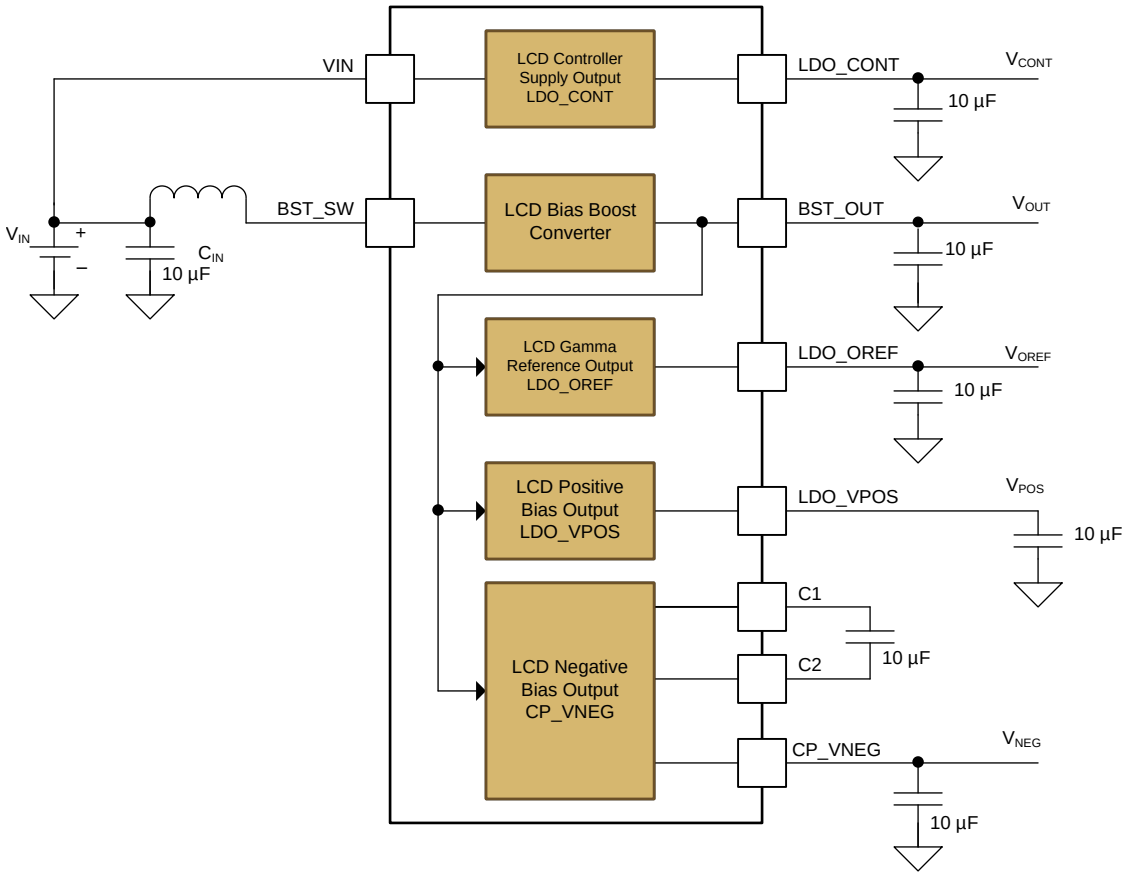


Figure 48. LCD Boost

8.3.4.2 Display Bias Power Sequencing (V_{POS}, V_{NEG}, V_{OREF}, V_{CONT})

The LM3631 supports configurable output power-up and power-down timing for V_{POS}, V_{NEG}, V_{CONT} and V_{OREF}. The LED current sinks can start up after the bias voltages power ok signals (or after the timeout period has elapsed (20 ms typ.)) and shuts down before the bias power-down sequence begins. The bias power-down sequence does not start until after the LED current sinks have turned off.

The trigger for the power-up sequence is either a change from logic LOW to logic HIGH on the LCD_EN pin or the Display Bias Outputs bit. The trigger for the power-down sequence is either a change from logic HIGH to logic LOW on the LCD_EN pin or the Display Bias Outputs bit. The pull-downs or pull-ups for each output, if enabled, disengage immediately upon start-up of each respective output and re-engages immediately upon shutdown of each respective output.

Table 6. Start-Up and Shutdown Delays

START-UP DELAY SETTING (LDO_OREF_SU_DLY, LDO_VPOS_SU_DLY, CP_VNEG_SU_DLY) (ms)	SHUTDOWN DELAY SETTING (LDO_OREF_SD_DLY, LDO_VPOS_SD_DLY, CP_VNEG_SD_DLY) (ms)
0000 = 0	0000 = 0
0001 = 1	0001 = 1
0010 = 2	0010 = 2
0011 = 3	0011 = 3
0100 = 4	0100 = 4
0101 = 5	0101 = 5
0110 = 6	0110 = 6
0111 = 7	0111 = 7
1000 = 8	1000 = 8

Table 6. Start-Up and Shutdown Delays (continued)

START-UP DELAY SETTING (LDO_OREF_SU_DLY, LDO_VPOS_SU_DLY, CP_VNEG_SU_DLY) (ms)	SHUTDOWN DELAY SETTING (LDO_OREF_SD_DLY, LDO_VPOS_SD_DLY, CP_VNEG_SD_DLY) (ms)
1001 = 9	1001 = 9
1010 = 10	1010 = 10
1011 = 11	1011 = 11
1100 = 12	1100 = 12
1101 = 13	1101 = 13
1110 = 14	1110 = 14
1111 = 15	1111 = 15

LDO_CONT start-up/shutdown delay has a 3-bit programmable range.

Table 7. LDO_CONT Start-Up/Shutdown Delays

LDO_CONT START-UP/SHUTDOWN DELAY SETTING (LDO_CONT_SU_DLY, LDO_CONT_SD_DLY)	START-UP/SHUTDOWN DELAY (ms)
000	0
001	2
010	5
011	10
100	20
101	50
110	100
111	200

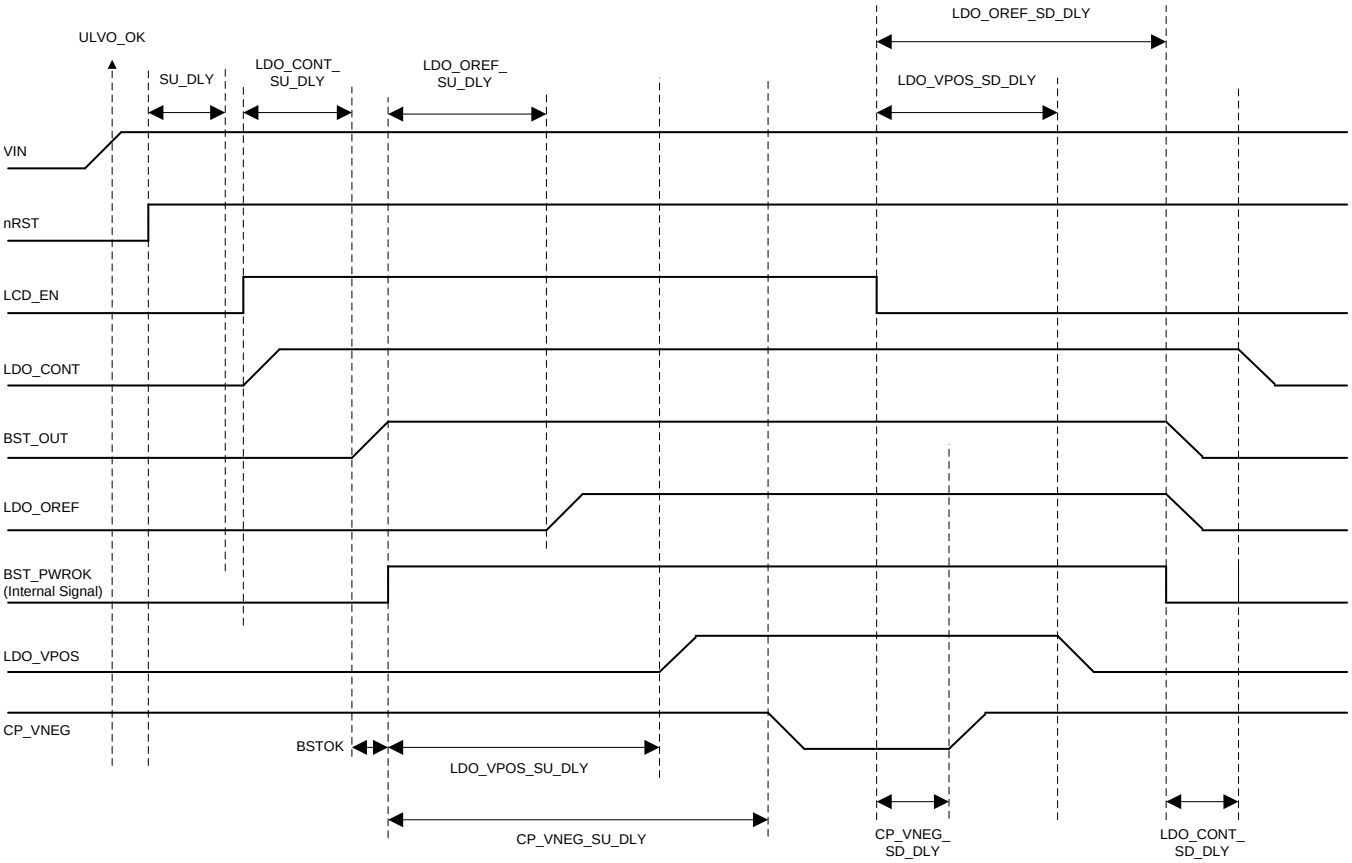


Figure 49. General LCD Bias Power Sequence Without Backlight

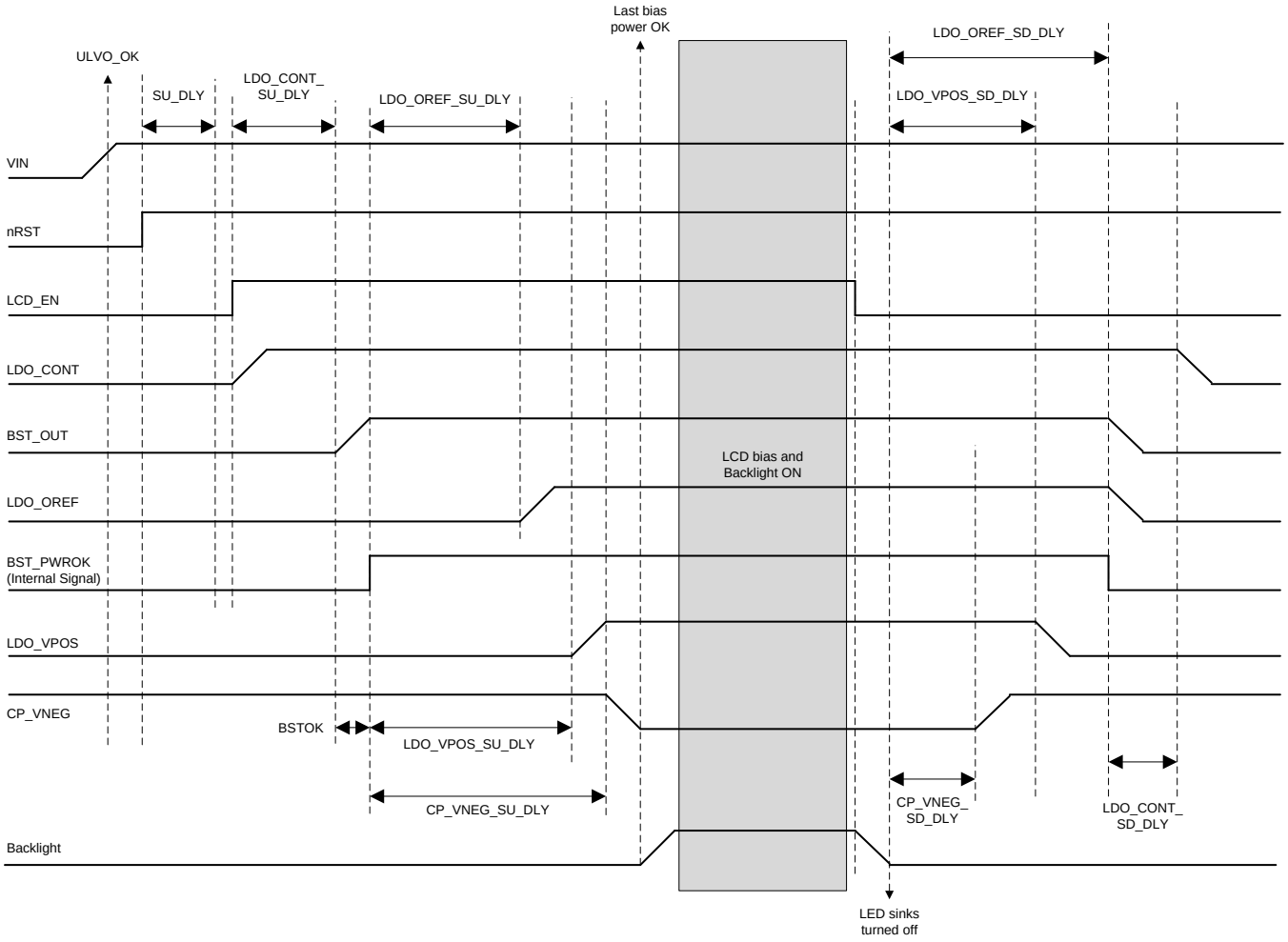


Figure 50. General LCD Bias Power Sequence With Backlight

8.3.4.2.1 Start-Up and Shutdown Delays

SU_DLY Start-up delay from LCD_EN = HIGH to start up of the internal references, bias, and oscillator.

LDO_CONT_SU_DLY Delay between the time LDO_CONT signal starts to rise 'HIGH', and the time before BST_OUT starts to rise. LDO_CONT delay can be adjusted with LDO_CONT_SU_DLY I^2C register start-up delay bits. In case LDO_CONT is disabled, BST_OUT starts to rise after LCD_EN is set 'HIGH'.

BSTOK Bias boost startup delay. Time between the time when BST_OUT voltage starts to rise and the time when BST_PWROK (internal) signal rises to 'HIGH'.

LDO_OREF_SU_DLY Delay between the time when BST_PWROK signal rises to 'HIGH' and LDO_OREF signal starts to rise. Delay can be adjusted with I^2C register start-up delay bits LDO_OREF_SU_DLY.

LDO_VPOS_SU_DLY Delay between the time when BST_PWROK signal rises to 'HIGH' and LDO_VPOS signal starts to rise. Delay can be adjusted with I^2C register start-up delay bits LDO_VPOS_SU_DLY.

CP_VNEG_SU_DLY Delay between the time when BST_PWROK signal rises to 'HIGH' and CP_VNEG signal starts to fall. Delay can be adjusted with I^2C register start-up delay bits CP_VNEG_SU_DLY. Note that there is a minimum delay of 500 µs (typ.) due to biasing of the flycap.

CP_VNEG_SD_DLY Delay between the time when LCD_EN signal is set LOW and the time when CP_VNEG signal starts to rise. Delay can be adjusted with I^2C register off delay bits CP_VNEG_SD_DLY.

LDO_VPOS_SD_DLY Delay between the time when LCD_EN signal is set LOW and the time when LDO_VPOS signal starts to fall. Delay can be adjusted with I^2C register off delay bits LDO_VPOS_SD_DLY.

LDO_OREF_SD_DLY Delay between the time when LCD_EN signal is set LOW and the time when LDO_OREF signals start to fall. Delay can be adjusted with I^2C register off delay bits LDO_OREF_SD_DLY.

LDO_CONT_SD_DLY After last of the LDO_OREF, CP_VNEG, or LDO_VPOS shutdown time has ended LDO_CONT signal starts to fall in case it is enabled.

8.3.4.2.2 Special Conditions During Display Bias Power Sequencing

Short nRST Condition During Shutdown Sequence If nRST is logic LOW for longer than the deglitch time, all appropriate outputs are sequenced down completely. If nRST is toggled or is held at logic HIGH before the all outputs are shutdown, the shutdown sequencing continues to turn off all outputs and set all the internal registers to the default state. Note that if nRST is toggled or is held at logic HIGH *before* all outputs are shut down, and FLAG pin is configured as fault, there are small glitches in the FLAG line after nRST is set HIGH.

Thermal Fault During Shutdown Sequence A thermal fault, when the die temperature is greater than T_{SD}, shuts down all outputs. When the die temperature drops by $T_{SD(HYSTERESIS)}$, the outputs can be re-started by toggling LCD_EN or the “LCD_EN” bit of register 0x00.

Backlight Sequence During LCD Bias Start-up Sequence Backlight cannot be enabled before LCD bias start-up sequence is complete. If the backlight is enabled (via either the PWM or I^2C register) before the LCD bias start-up sequence is complete, the backlight start-up sequence starts after LCD bias start-up sequence is complete.

8.3.4.3 Active Discharge

An active discharge is implemented for each output rail (LDO_OREF, LDO_VPOS, LDO_CONT and CP_VNEG) with internal switch resistance. The discharge function is programmable by I^2C interface and is triggered by LCD_EN = “LOW”. During power-up, each output programmed to be actively discharged (at power-down) is actively discharged as long as it is not enabled internally.

8.3.4.4 LCD Bias Protection

The LM3631 provides OVP that monitors the LCD Bias boost output voltage (V_{OUT}) and protects BST_OUT and BST_SW from exceeding safe operating voltages. The OVP threshold can be set with the I^2C register bits. If there is an LCD bias overvoltage fault, an LCD_OVPFLT fault is set. The fault is cleared with the rising edge of LCD_EN or an I^2C write '1' to the LCD_OVPFLT bit.

LDO_VPOS has an OCP that limits the maximum current drawn to 200 mA (typ.). If the fault condition persists over 2 ms, the LCD is shut down according to the normal shutdown sequence, and an LDO_VPOS_FLT fault is set. The fault must be cleared to enable power; the fault is cleared with rising edge of LCD_EN or an I^2C write '1' to LDO_VPOS_FLT bit.

LDO_OREF has OCP that limits the maximum current drawn to 80 mA (typ.). If the fault condition persists over 2 ms, the LCD is shut down according to the normal shutdown sequence, and an LDO_OREF_FLT fault is set. The fault must be cleared to enable powers; the fault is cleared with rising edge of LCD_EN or I^2C write '1' to LDO_OREF_FLT bit.

CP_VNEG has a short-circuit and OVP feature, which monitors the charge-pump voltage.

- If the charge-pump voltage goes 250 mv (typ.) below its target set-point, the charge pump is shut down. If the OVP persists for 2 ms, all bias outputs are turned off following the normal shutdown sequence, and a NEG_CP_OVP fault is set. The fault must be cleared, to re-enable the outputs, with the rising edge of LCD_EN or an I^2C write '1' to NEG_CP_OVP bit.
- If the charge-pump voltage goes over –1 V, the charge pump is shut down, and a NEG_CP_SC fault gets set. The fault must be cleared, to re-enable the outputs, with rising edge of LCD_EN or an I^2C write '1' to NEG_CP_SC.

8.3.5 Display Controller Power (V_{LDO_CONT})

The LM3631 supports an additional regulated output V_{LDO_CONT} which can supply, for example, the display's controller voltage. The LDO_CONT has a 2-bit programmable range with 1.8-V, 2.3-V, 2.8-V and 3.3-V values and can supply up to 80 mA. This LDO is powered directly from V_{IN} voltage.

NOTE

When the LDO voltage is set to 2.8 V, V_{IN} voltage must be kept over 2.8 V to ensure LDO proper functionality. Similarly, when LDO voltage is set to 3.3 V, the battery voltage must be kept over 3.3 V to ensure LDO proper functionality.

LDO_CONT has an OCP feature. If the OCP fault condition persists over 2 ms, a fault is set. LDO_CONT limits the current. Fault is cleared with rising edge of LCD_EN or an I^2C write '1' to the LDO_CONT_FLT bit.

8.3.6 RESET Register

I^2C register 0x14 is the register reset. Writing FFh into this register resets all I^2C register values to default values. Default values are described in Table 1.

8.3.7 nRST Input

The nRST input is a global hardware enable for the LM3631. This pin must be pulled to logic HIGH to enable the device and the I^2C-compatible interface. This pin is high-impedance and cannot be left floating. When this pin is at logic LOW, the LM3631 is placed in shutdown, the I^2C-compatible interface is disabled, and the internal registers are reset to their default state. It is recommended that V_{IN} has risen above a 2.7-V before setting nRST HIGH.

8.3.8 FLAG Pin

The FLAG pin can be used as an indicator to the application processor when the LM3631 encounters, for example, OVP. The fault conditions which set the FLAG pin to pull low can be programmed via I^2C. Additionally, the power-good flag can be set to trigger from the flag for the bias voltages.

The FLAG pin is an open-drain output. When this pin is used, a pullup resistor is needed. If not used, this pin can be left floating.

Table 8. FLAG Pin Configuration

FLAG PIN CONFIGURATION BITS	FLAG PIN INFORMATION
00	Flag disabled, no flag indication
01	Power-Good state, selectable with Power-Good flag control bits (PG_FLAG_CTRL)
10	Backlight on state
11	Fault state

8.3.9 Power-Good Flag

The Power-Good flag can be used to indicate an application processor power-good situation of the bias voltages. The Power-Good flag information can be selected with Power-Good Flag control bits (PG_FLAG_CTRL). This information can be directed to the FLAG pin with FLAG pin configuration bits.

NOTE

When nRST is pulled low before the power sequence is complete, the Power-Good Flag indication is triggered even though the condition (described in Table 9) to trigger that the Power-Good flag is not fulfilled. When the Power-Good configuration is '00' (after last supply reaches target), LDO_VPOS, CP_VNEG, and LDO_OREF all need to be enabled.

Table 9. Power-Good Flag Configuration

POWER-GOOD FLAG CONFIGURATION BITS	FLAG PIN INFORMATION DURING START-UP	FLAG PIN INFORMATION DURING SHUTDOWN
00	Power-Good bit set to '1' after last supply reaches target	Power-Good bit set to '0' after first supply falls below target
01	Power-Good bit set to '1' after LDO_VPOS reaches target	Power-Good bit set to '0' after LDO_VPOS falls below target
10	Power-Good bit set to '1' after CP_VNEG reaches target	Power-Good bit set to '0' after CP_VNEG falls below target
11	Power-Good bit set to '1' after LDO_OREF reaches target	Power-Good bit set to '0' after LDO_OREF falls below target

8.3.10 OTP_SEL Pin

The OTP selection pin is dedicated for selection between two different default setups. Setting this pin to VBATT or GND selects the OTP from where the default setup is loaded. Note that this selection applies only for the backlight and LCD configuration registers (registers from 0x05h to 0x12h).

8.3.11 Thermal Shutdown

The LM3631 has Thermal Shutdown protection which shuts down the backlight, all bias voltage outputs and enters standby mode when the die temperature reaches or exceeds 140°C (typ.). When the die temperature falls below 120°C (typ.), the LM3631 comes out of standby. The I^2C interface remains active during a Thermal Shutdown event. If a TSD fault occurs, TMPFLT fault is set — the fault is cleared by an I^2C write '1' to TMPFLT bit or by setting LCD_EN high.

8.3.12 Undervoltage Lockout

The LM3631 has an undervoltage lockout feature (UVLO), which indicates of the device operation at low input voltages. If the supply voltage V_{IN} is below the UVLO threshold, a UVLO fault is set. UVLO fault is cleared by an I^2C write '1' to UVLO bit. UVLO does not shut down the outputs.

UVLO rising threshold is 2.6 V (typ.), and UVLO falling threshold is 2.5 V (typ.).

8.4 Device Functional Modes

8.4.1 Modes of Operation

Shutdown: The LM3631 is in shutdown when nRST pin is low.

Standby: After nRST pin is set high, and V_{IN} is over UVLO limit, the LM3631 goes into Standby mode. Before entering Standby mode, references and bias currents are enabled (bias delay typically 200 µs), and registers are read from OTP (EPROM read delay typically 700 µs). In Standby mode references and bias currents are enabled, and I^2C writes are allowed. LCD powers, and backlight are disabled.

Normal mode: When LCD_EN is set to high (pin or bit), the start-up sequence is started. During the start-up sequence LDO_CONT, LCD Boost, and LCD bias powers are started. If the LDO_CONT is disabled, the start-up sequence goes directly to LCD Boost start-up.

- LDO_CONT start-up: LDO_CONT is enabled. Programmable delay of 0 to 200 ms.
- LCD Boost start-up: LCD Boost is enabled. Waits until Boost output voltage is reached 90% of target value.
- LCD bias start-up enables, sequentially, LDO_VPOS, CP_VNEG, and LDO_OREF according to start-up delay settings.

After the LCD bias start-up has completed, the LM3631 enters backlight start-up mode if BL_EN bit is set to '1', and the PWM brightness value is different than 0. Even if the backlight is not enabled, LCD powers remains active. If the backlight is enabled, and BL_EN bit is set to '0' or PWM brightness value is set to 0, backlight is disabled. LCD powers remains active.

If LCD_EN is set to '0', the LM3631 shuts down backlight and bias powers and enters Standby mode. During power down the backlight is shut down first if it was enabled. After backlight shutdown is completed, the device enters LCD Bias shutdown. In LCD bias shutdown LDO_VPOS, CP_VNEG, and LDO_OREF are shut down sequentially according to shutdown delay settings. After the LDO_VPOS, CP_VNEG, and LDO_OREF shutdown sequence is complete, LCD Boost and LDO_CONT (if it was enabled) are shut down. LDO_CONT is shut down after adjustable delay (0 to 200 ms). Once LDO_CONT has shut down, the LM3631 enters Standby mode.

In a fault situation (thermal, backlight boost short circuit, LDO_OREF overcurrent, VPOS overcurrent, or CP short circuit), the device starts the shutdown sequence and enters Standby mode.

Device Functional Modes (continued)

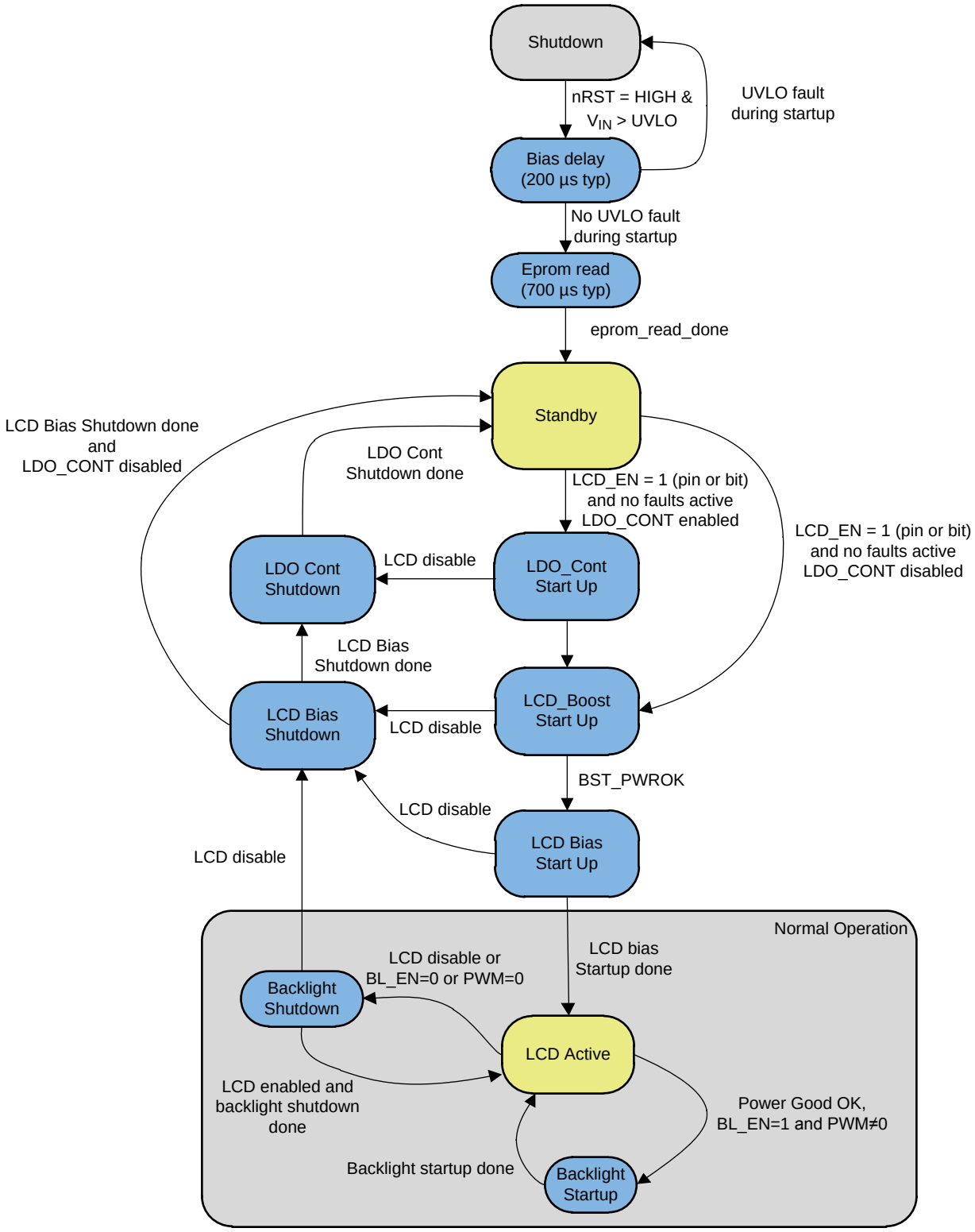


Figure 51. Modes of Operations

8.5 Programming

8.5.1 I²C-Compatible Serial Bus Interface

8.5.1.1 Interface Bus Overview

The I²C-compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the IC's connected to the bus. The two interface lines are the Serial Data Line (SDA) and the Serial Clock Line (SCL). These lines should be connected to a positive supply via a pull-up resistor and remain HIGH even when the bus is idle.

Every device on the bus is assigned a unique address and acts as either a Master or a Slave, depending whether it generates or receives the serial clock (SCL).

8.5.1.2 Data Transactions

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

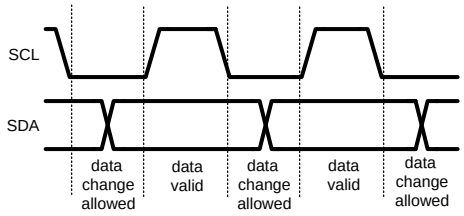


Figure 52. Data Validity

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software), and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow. The following sections provide further details of this process.

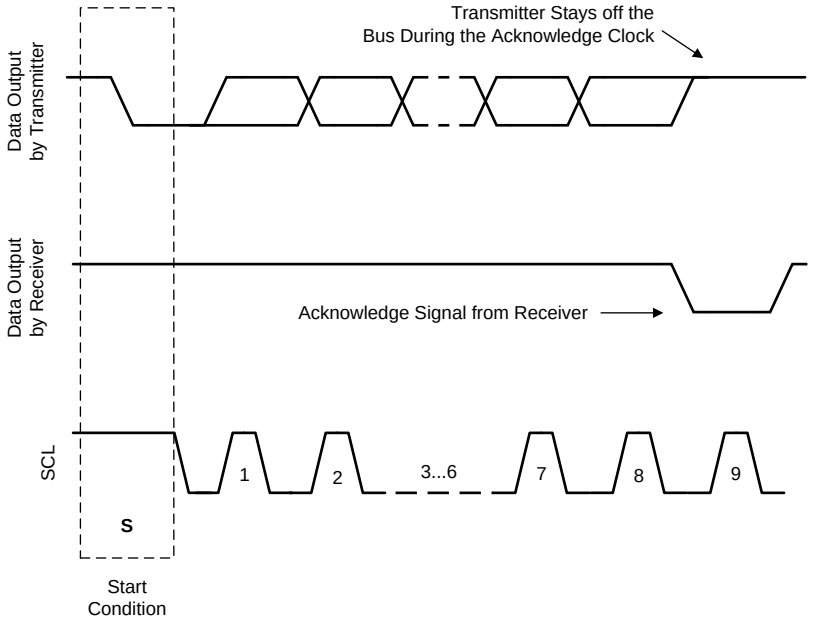


Figure 53. Acknowledge Signal

Programming (continued)

The Master device on the bus always generates the Start and Stop Conditions (control codes). After a Start Condition is generated, the bus is considered busy, and it retains this status until a certain time after a Stop Condition is generated. A high-to-low transition of the data line (SDA) while the clock (SCL) is high indicates a Start Condition. A low-to-high transition of the SDA line while the SCL is high indicates a Stop Condition.

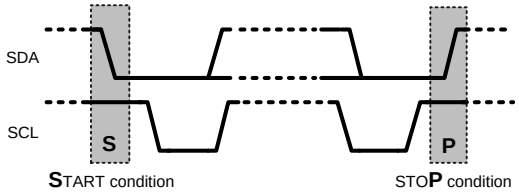


Figure 54. Start and Stop Conditions

In addition to the first Start Condition, a repeated Start Condition can be generated in the middle of a transaction. This allows another device to be accessed, or a register read cycle.

8.5.1.3 Acknowledge Cycle

The Acknowledge Cycle consists of two signals: the acknowledge clock pulse the master sends with each byte transferred, and the acknowledge signal sent by the receiving device.

The master generates the acknowledge clock pulse on the ninth clock pulse of the byte transfer. The transmitter releases the SDA line (permits it to go high) to allow the receiver to send the acknowledge signal. The receiver must pull down the SDA line during the acknowledge clock pulse and ensure that SDA remains low during the high period of the clock pulse, thus signaling the correct reception of the last data byte and its readiness to receive the next byte.

8.5.1.4 Acknowledge After Every Byte Rule

The master generates an acknowledge clock pulse after each byte transfer. The receiver sends an acknowledge signal after every byte received.

There is one exception to the “acknowledge after every byte” rule. When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (“negative acknowledge”) the last byte clocked out of the slave. This “negative acknowledge” still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

8.5.1.5 Addressing Transfer Formats

Each device on the bus has a unique slave address. The LM3631 operates as a slave device with the 7-bit address. If an 8-bit address is used for programming, the 8th bit is '1' for read and '0' for write. The 7-bit address for the LM3631 is 0x29.

Before any data is transmitted, the master transmits the address of the slave being addressed. The slave device should send an acknowledge signal on the SDA line, once it recognizes its address. The slave address is the first seven bits after a Start Condition. The direction of the data transfer (R/W) depends on the bit sent after the slave address — the eighth bit.

When the slave address is sent, each device in the system compares this slave address with its own. If there is a match, the device considers itself addressed and sends an acknowledge signal. Depending upon the state of the R/W bit (1:read, 0:write), the device acts as a transmitter or a receiver.

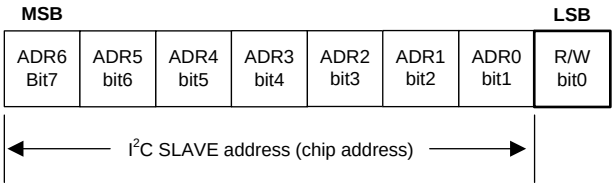


Figure 55. I²C Device Address

Programming (continued)

Control Register Write Cycle

- Master device generates start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master sends data byte to be written to the addressed register.
- Slave sends acknowledge signal.
- If master sends further data bytes the control register address is incremented by one after acknowledge signal.
- Write cycle ends when the master creates stop condition.

Control Register Read Cycle

- Master device generates a start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w = 0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal
- Master device generates repeated start condition.
- Master sends the slave address (7 bits) and the data direction bit (r/w = 1).
- Slave sends acknowledge signal if the slave address is correct.
- Slave sends data byte from addressed register.
- If the master device sends acknowledge signal, the control register address is incremented by one. Slave device sends data byte from addressed register.
- Read cycle ends when the master does not generate acknowledge signal after data byte and generates stop condition.

Table 10. I^2C Data Read/Write(1)

	ADDRESS MODE
Data Read	<Start Condition> <Slave Address><r/w =0>[Ack] <Register Addr>[Ack] <Repeated Start Condition> <Slave Address><r/w = 1>[Ack] [Register Data]<Ack or NAck> ...additional reads from subsequent register address possible <Stop Condition>
Data Write	<Start Condition> <Slave Address><r/w = 0>[Ack] <Register Addr>[Ack] <Register Data>[Ack] ...additional writes to subsequent register address possible <Stop Condition>

(1) < > = Data from master, [ ] = Data from slave

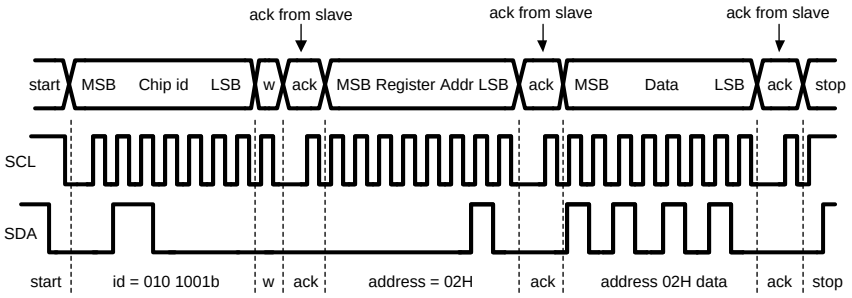


Figure 56. Register Write Format

When a READ function is to be accomplished, a WRITE function must precede the READ function, as show in the Read Cycle waveform.

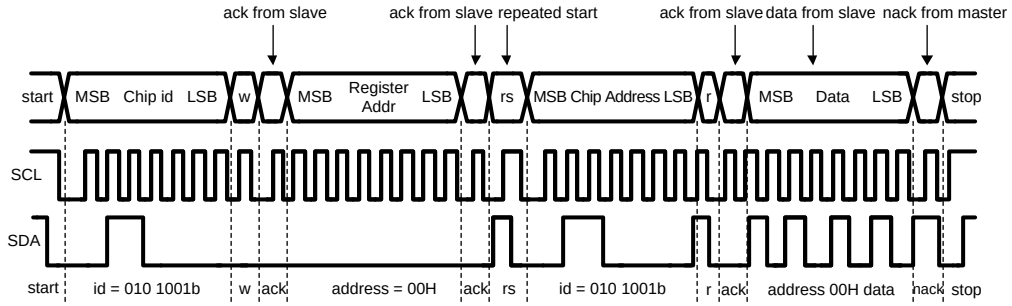


Figure 57. Register Read Format

NOTE

w = write (SDA = 0), r = read (SDA = 1), ack = acknowledge (SDA pulled down by either master or slave), rs = repeated start id = 7-bit chip address

8.6 Register Maps

Table 11. Device Control Register (0x00)

[Bit 7]	[Bit 6]	[Bit 5]	[Bit 4]	[Bit 3]	[Bit 2]	[Bit 1] LCD_EN	[Bit 0] BL_EN
Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	0 = LCD disabled 1 = LCD enabled	0 = Backlight disabled 1 = Backlight enabled

Table 12. LED Brightness Register LSB (0x01)

[Bit 7]	[Bit 6]	[Bit 5]	[Bit 4]	[Bit 3]	[Bits 2:0] Brightness LSB
Not Used	Not Used	Not Used	Not Used	Not Used	BRT[2:0]. Lower 3 bits (LSB's) of brightness code. Concatenated with brightness bits in Register 0x02 (MSB).

Table 13. LED Brightness Register MSB (0x02)

[Bits 7:0] Brightness MSB
BRT[10:3]. Upper 8 bits (MSB's) of brightness code. Concatenated with brightness bits in Register 0x01 (LSB).

Table 14. Faults Register (0x03)

[Bit 7] BL_SCFLT	[Bit 6] TMPFLT	[Bit 5] BL_OCPFLT	[Bit 4] BL_OVPFLT	[Bit 3] LCD_OVPFLT	[Bit 2] LDO_OREF_FLT	[Bit 1] LDO_VPOS_FLT	[Bit 0] UVLO FLAG
0 = normal 1 = backlight short circuit condition	0 = normal 1 = device has hit thermal shutdown threshold	0 = normal 1 = fault, backlight boost current limit reached	0 = normal 1 = fault, backlight boost overvoltage protection limit reached	0 = normal 1 = fault, LCD boost overvoltage protection limit reached	0 = normal 1 = fault, LDO_OREF short circuit condition	0 = normal 1 = fault, LDO_VPOS short circuit condition	0 = normal 1 = UVLO event

Table 15. Faults and Power-Good Register (0x04)

[Bit 7]	[Bit 6]	[Bit 5]	[Bit 4]	[Bit 3] NEG_CP_SC	[Bit 2] NEG_CP_OVP	[Bit 1] LDO_CONT_FLT	[Bit 0] PG_FLAG
Not Used	Not Used	Not Used	Not Used	0 = normal 1 = fault, negative chargepump short circuit condition	0 = normal 1 = fault, negative chargepump overvoltage protection limit reached	0 = normal 1 = fault, LDO Controller current limit reached	Power-Good flag

Table 16. Backlight Configuration (Auto Frequency Threshold) Register 1 (0x05)

[Bits 7:0] AUTO_FREQ_THRES
LED current threshold value. When the Auto Frequency Select Mode Bit is '1' (Bit[3] in register 0x07), the 8 bit code in this register (AUTOFREQ_THRESH) is compared against the MSB's of the I^2C Brightness code (BRT [10:3]), and this comparison is used to determine whether the device operates in Low Frequency or High Frequency Mode. 1. When BRT[10:3] > AUTOFREQ_THRESH[7:0] , the Boost Frequency Select Bit is automatically set to '1' forcing the device into High Frequency Mode. 2. When BRT[10:3] ≤ AUTOFREQ_THRESH[7:0], the Boost Frequency Select Bit automatically set to '0' and the device operates in Low Frequency Mode.

Table 17. Backlight Configuration Register 2 (0x06)

[Bit 7]	[Bit 6]	[Bit 5] LINEAR_MAPPER	[Bit 4]	[Bit 3] STRING_MODE	[Bit 2] INDUCTOR	[Bits 1:0] PEAK_CURR_LIM
Not Used	Not Used	0= Exponential mapping in use 1 = Linear mapping in use	Not Used	0 = Both LED strings enabled 1 = Only LED string 1 enabled	0 = Inductor typical value = 22 µH 1 = Inductor typical value = 10 µH	00 = 600 mA 01 = 700 mA 10 = 800 mA 11 = 900 mA

Table 18. Backlight Configuration Register 3 (0x07)

[Bits 7:6] SEL_I	[Bits 5:4] SEL_P	[Bit 3] BL_AUTOFRQ	[Bits 2:1] BL_BST_OVP	[Bit 0] BL_BST_FREQ
Backlight boost compensator adjustment. Select value according to number of LEDs in LED string.	Backlight boost compensator adjustment. Select value according to inductor	0 = Manual frequency mode 1 = Auto frequency mode	Backlight Boost OVP target 00 = 17 V 01 = 21 V 10 = 25 V 11 = 29 V	Backlight Boost frequency 0 = 500 kHz 1 = 1 MHz

Table 19. Backlight Configuration Register 4 (0x08)

[Bit 7] PWM_EDGE_DET_SEL	[Bit 6] PWM POLARITY	[Bits 5:4] HYSTERESIS	[Bits 3:2] BRT_MODE	[Bit 1] EN__ADV_SLOPE	[Bit 0] DISABLE_DITHER
PWM edge detection selection 0 = PWM measured from rising edge 1 = PWM measured from falling edge	0 = PWM active polarity LOW 1 = PWM active polarity HIGH	PWM input hysteresis selection (change in 11-bit brightness) 00 = 0.05% shift causes change 01 = 0.1% shift causes change 10 = 0.2% shift causes change 11 = 0.4% shift causes change	Brightness mode selection 00 = I^2C register used for brightness control 01 = PWM input duty cycle used for brightness control 10 = I^2C code multiplied with PWM duty cycle before sloping 11 = Sloped I^2C brightness code multiplied with PWM duty cycle	0 = Advanced slope disabled 1 = Advanced slope enabled	0 = Dither enabled 1 = Dither disabled

Table 20. Backlight Configuration Register 5 (0x09)

[Bits 7:4] SLOPE	[Bits 3:0] DITHER_FREQ_SEL
0000 = Slope function disabled, immediate brightness change 0001 = 1 ms 0010 = 2 ms 0011 = 5 ms 0100 = 10 ms 0101 = 20 ms 0110 = 50 ms 0111 = 100 ms 1000 = 250 ms 1001 = 500 ms 1010 = 750 ms 1011 = 1000 ms 1100 = 1500 ms 1101 = 2000 ms 1110 = 3000 ms 1111 = 4000 ms	Dithering frequency selection 0000 = 62.5 kHz 0001 = 31.3 kHz 0010 = 15.6 kHz 0011 = 7.8 kHz 0100 = 3.9 kHz 0101 = 1.95 kHz 0110 = 977 Hz 0111 = 488 Hz 1000 = 244 Hz 1001 = 122 Hz

Table 21. LCD Configuration Register 1 (0x0A)

[Bit 7]	[Bit 6] LDO_CONT_SD_PULLDN	[Bit 5] LDO_OREF_SD_PULLDN	[Bit 4] CP_VNEG_SD_PULLUP	[Bit 3] LDO_VPOS_SD_PULLDN	[Bit 2] LDO_VPOS_EN	[Bit 1] CP_VNEG_EN	[Bit 0] LDO_OREF_EN
Not Used	0 = LDO_CONT pull-down resistor disabled 1 = LDO_CONT pull-down resistor enabled	0 = LDO_OREF pull-down resistor disabled 1 = LDO_OREF pull-down resistor enabled	0 = CP_VNEG pull-up resistor disabled 1 = CP_VNEG pull-up resistor enabled	0 = LDO_VPOS pull-down resistor disabled 1 = LDO_VPOS pull-down resistor enabled	0 = LDO_VPOS disabled 1 = LDO_VPOS enabled	0 = CP_VNEG disabled 1 = CP_VNEG enabled	0 = LDO_OREF disabled 1 = LDO_OREF enabled

Table 22. LCD Configuration Register 2 (LDO_CONT) (0x0B)

[Bit 7]	[Bits 6:4] LDO_CONT_SU_DELAY	[Bits 3:1] LDO_CONT_SD_DELAY	[Bit 0] LDO_CONT_EN
Not Used	LDO_CONT start-up delay 000 = 0 ms 001 = 2 ms 010 = 5 ms 011 = 10 ms 100 = 20 ms 101 = 50 ms 110 = 100 ms 111 = 200 ms	LDO_CONT shutdown delay 000 = 0 ms 001 = 2 ms 010 = 5 ms 011 = 10 ms 100 = 20 ms 101 = 50 ms 110 = 100 ms 111 = 200 ms	0 = LDO_CONT disabled 1 = LDO_CONT enabled

Table 23. LCD Configuration Register 3 (0x0C)

[Bits 7:6] LDO_CONT_VOUT	[Bits 5:0] LCD_BST_OUT
LDO_CONT output voltage 00 = 1.8 V 01 = 2.3 V 10 = 2.8 V 11 = 3.3 V	LCD Boost output voltage 000 000 = 4.50 V 000 001 = 4.55 V 000 010 = 4.60 V 000 011 = 4.65 V 000 100 = 4.70 V ... 010 111 = 5.65 V 011 000 = 5.70 V 011 001 = 5.75 V ... 100 001 = 6.15 V 100 010 = 6.20 V 100 011 = 6.25 V 100 100 = 6.30 V 100 101 = 6.35 V

Table 24. LCD Configuration Register 4 (LDO_VPOS) (0x0D)

[Bit 7]	[Bit 6]	[Bits 5:0] LDO_VPOS_TARGET
Not Used	Not Used	000 000 = 4.00 V 000 001 = 4.05 V 000 010 = 4.10 V 000 011 = 4.15 V 000 100 = 4.20 V ... 011 011 = 5.35 V 011 100 = 5.40 V 011 101 = 5.45 V ... 100 100 = 5.80 V 100 101 = 5.85 V 100 110 = 5.90 V 100 111 = 5.95 V 101 000 = 6.00 V (6.00V is the maximum level regardless of the adjustment level above value '101 000')

Table 25. LCD Configuration Register 5 (CP_VNEG) (0x0E)

[Bit 7]	[Bit 6]	[Bits 5:0] CP_VNEG_TARGET
Not Used	Not Used	000 000 = –4.00 V 000 001 = –4.05 V 000 010 = –4.10 V 000 011 = –4.15 V 000 100 = –4.20 V ... 011 011 = –5.35 V 011 100 = –5.40 V 011 101 = –5.45 V ... 100 100 = –5.80 V 100 101 = –5.85 V 100 110 = –5.90 V 100 111 = –5.95 V 101 000 = –6.00 V (–6.00V is the maximum level regardless of the adjustment level above value '101 000')

Table 26. LCD Configuration Register 6 (LDO_OREF) (0x0F)

[Bit 7]	[Bit 6]	[Bits 5:0] LDO_OREF_TARGET
Not Used	Not Used	000 000 = 4.00 V 000 001 = 4.05 V 000 010 = 4.10 V 000 011 = 4.15 V 000 100 = 4.20 V ... 011 011 = 5.35 V 011 100 = 5.40 V 011 101 = 5.45 V ... 100 100 = 5.80 V 100 101 = 5.85 V 100 110 = 5.90 V 100 111 = 5.95 V 101 000 = 6.00 V (6.00V is the maximum level regardless of the adjustment level above value '101 000')

Table 27. LCD Configuration Register 7 (LDO_VPOS Sequence Control) (0x10)

[Bits 7:4] LDO_VPOS START-UP DELAY	[Bits 3:0] LDO_VPOS SHUTDOWN DELAY
0000 = 0.0 ms	0000 = 0.0 ms
0001 = 1.0 ms	0001 = 1.0 ms
0010 = 2.0 ms	0010 = 2.0 ms
0011 = 3.0 ms	0011 = 3.0 ms
0100 = 4.0 ms	0100 = 4.0 ms
0101 = 5.0 ms	0101 = 5.0 ms
0110 = 6.0 ms	0110 = 6.0 ms
0111 = 7.0 ms	0111 = 7.0 ms
1000 = 8.0 ms	1000 = 8.0 ms
1001 = 9.0 ms	1001 = 9.0 ms
1010 = 10.0 ms	1010 = 10.0 ms
1011 = 11.0 ms	1011 = 11.0 ms
1100 = 12.0 ms	1100 = 12.0 ms
1101 = 13.0 ms	1101 = 13.0 ms
1110 =14.0 ms	1110 =14.0 ms
1111 = 15.0 ms	1111 = 15.0 ms

Table 28. LCD Configuration Register 8 (CP_VNEG Sequence Control) (0x11)

[Bits 7:4] CP_VNEG START-UP DELAY (ms)	[Bits 3:0] CP_VNEG SHUTDOWN DELAY (ms)
0000 = 0.0 ms	0000 = 0.0 ms
0001 = 1.0 ms	0001 = 1.0 ms
0010 = 2.0 ms	0010 = 2.0 ms
0011 = 3.0 ms	0011 = 3.0 ms
0100 = 4.0 ms	0100 = 4.0 ms
0101 = 5.0 ms	0101 = 5.0 ms
0110 = 6.0 ms	0110 = 6.0 ms
0111 = 7.0 ms	0111 = 7.0 ms
1000 = 8.0 ms	1000 = 8.0 ms
1001 = 9.0 ms	1001 = 9.0 ms
1010 = 10.0 ms	1010 = 10.0 ms
1011 = 11.0 ms	1011 = 11.0 ms
1100 = 12.0 ms	1100 = 12.0 ms
1101 = 13.0 ms	1101 = 13.0 ms
1110 =14.0 ms	1110 =14.0 ms
1111 = 15.0 ms	1111 = 15.0 ms

Table 29. LCD Configuration Register 9 (LDO_OREF Sequence Control) (0x12)

[Bits 7:4] LDO_OREF START-UP DELAY	[Bits 3:0] LDO_OREF SHUTDOWN DELAY
0000 = 0.0 ms	0000 = 0.0 ms
0001 = 1.0 ms	0001 = 1.0 ms
0010 = 2.0 ms	0010 = 2.0 ms
0011 = 3.0 ms	0011 = 3.0 ms
0100 = 4.0 ms	0100 = 4.0 ms
0101 = 5.0 ms	0101 = 5.0 ms
0110 = 6.0 ms	0110 = 6.0 ms
0111 = 7.0 ms	0111 = 7.0 ms
1000 = 8.0 ms	1000 = 8.0 ms
1001 = 9.0 ms	1001 = 9.0 ms
1010 = 10.0 ms	1010 = 10.0 ms
1011 = 11.0 ms	1011 = 11.0 ms
1100 = 12.0 ms	1100 = 12.0 ms
1101 = 13.0 ms	1101 = 13.0 ms
1110 =14.0 ms	1110 =14.0 ms
1111 = 15.0 ms	1111 = 15.0 ms

Table 30. FLAG Configuration Register (0x13)

[Bit 7]	[Bit 6]	[Bit 5]	[Bit 4] FLAG_PIN_POLARITY	[Bits 3:2] PG_FLAG_CTRL	[Bits 1:0] PG_FLAG_CONFIG
Not Used	Not Used	Not Used	0 =FLAG pin active polarity LOW 1 = FLAG pin active polarity HIGH	00 = Power-Good set after last supply reaches target 01 = Power-Good set after LDO_VPOS 10 = Power-Good set after CP_VNEG 11 = Power-Good set after LDO_OREF	00 = FLAG disabled, no flag indication 01 = Power-Good state, selectable with PG_FLAG_CTRL bits 10 = Backlight ON state 11 = Fault state

Table 31. BOOT/RESET Register (0x14)

[Bit 7:0] BOOT
Write FFh to set all I^2C registers to RESET value

Table 32. Revision Register (0x16)

[Bit 7:6] DIE TRACEABILITY	[Bit 5:3] OTP REVISION	[Bit 2:0] DEVICE REVISION
Die Traceability Information	Device OTP Revision Information	Device Revision Information

9 Application and Implementation

9.1 Application Information

The LM3631 integrates an LCD backlight driver and LCD positive and negative bias voltage supplies into a single device. The backlight boost converter generates the high voltage required for the LEDs. The LM3631 can drive one or two LED strings with 4 to 8 white LEDs per string. Positive and negative bias voltages are post-regulated from the LCD bias boost output voltage. In addition, for the LCD bias voltages, the device has two programmable LDO regulator outputs which can be used to the power display controller, the LCD gamma reference, or any additional peripherals within output-current capability.

LDC bias voltages can be used without the backlight. Pulling LCD_EN high starts the LCD bias boost regulator. Once the LCD bias boost regulator has started up all voltage outputs can be enabled individually. The LM3631 can also be programmed to enable any voltage outputs automatically per a preset start-up sequence. The backlight cannot be enabled until enabled bias voltages have settled.

9.2 Typical Application

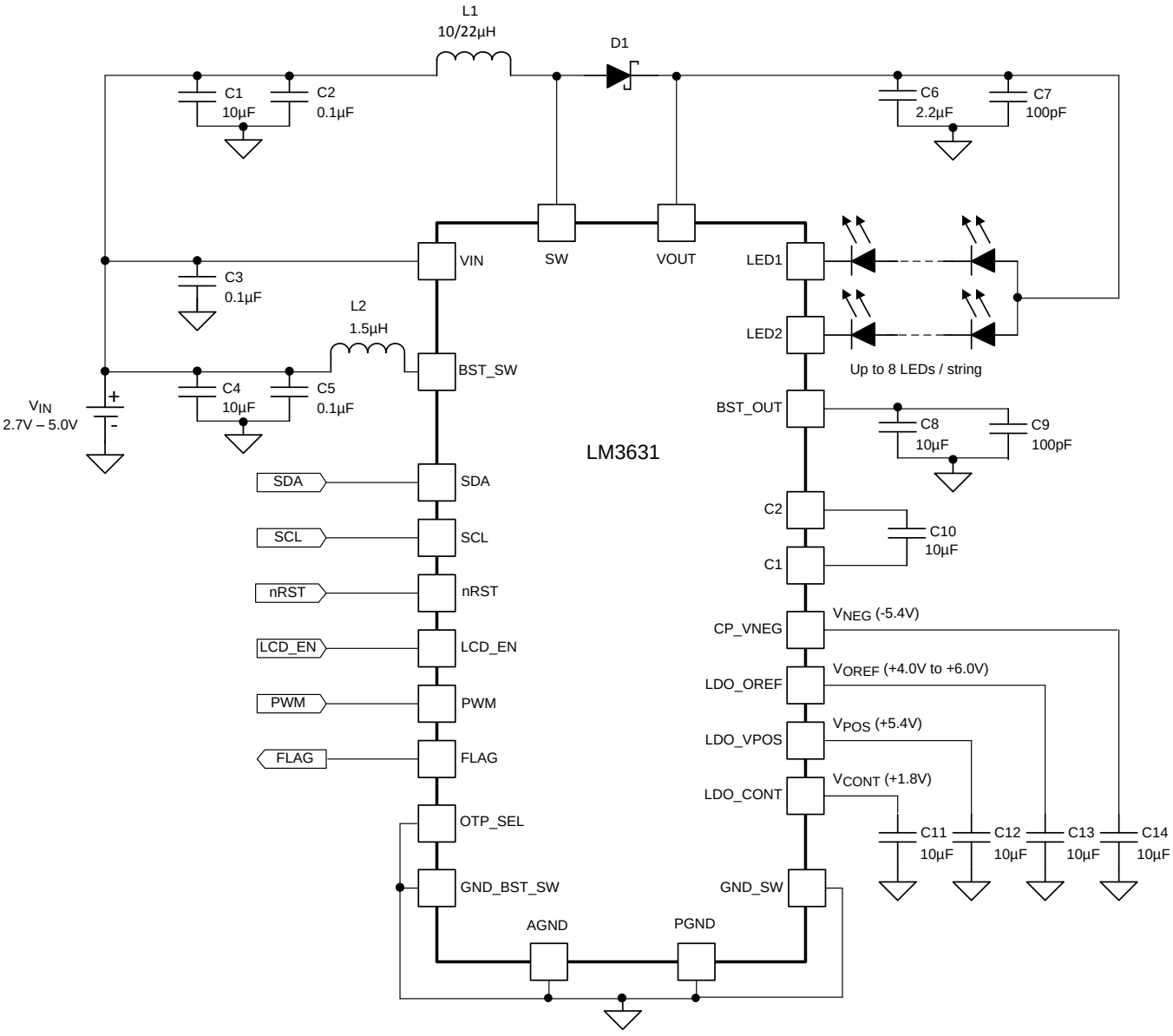


Figure 58. Typical Application Schematic

Typical Application (continued)

9.2.1 Design Requirements

Example requirements based on default register values (OTP_SEL = 1):

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	2.7 V to 4.5 V (Single Li-Ion cell battery)
Brightness Control	I^2C Register
LED Configuration	2 parallel, 6 series
LED Current	max 25 mA / string
Backlight Boost maximum voltage	28 V
Backlight boost SW frequency	1MHz
Backlight Boost inductor	10-µH, 900-mA saturation current
LCD boost output voltage	5.9 V
V_{NEG} output voltage	–5.4 V
V_{POS} output voltage	5.4 V
V_{OREF} output voltage	5.6 V
V_{CONT} output voltage	1.8 V
LCD Boost inductor	1.5-µH, 1-A saturation current

9.2.2 Detailed Design Procedure

9.2.2.1 External Components

Table 33 shows examples of external components for the LM3631. Small 100-pF ceramic capacitors parallel with boost-converter-output capacitors are optional and are used to reduce high-frequency noise generated by the boost converters. Boost-converter dual-output capacitors can be replaced with a single capacitor of higher output capacitance as long as the minimum effective capacitance requirement is met. DC bias effect of the ceramic capacitors must be taken into consideration when choosing the output capacitors. This is especially true for the high output-voltage backlight-boost converter.

Table 33. Recommended External Components

DESIGNATOR (Figure 58)	DESCRIPTION	VALUE	EXAMPLE	NOTE
C1, C4, C8, C10, C11, C12, C13, C14	Ceramic capacitor	10 µF, 10V or 16V	EMK107BBJ106MA-T	
C2, C3, C5	Ceramic capacitor	0.1 µF, 10V	GRM188R71H104KA93D	
C6	Ceramic capacitor	2.2 µF, 35V or 50V	C2012X5R1H225K	
C7, C9	Ceramic capacitor	100 pF, 50V	06035A101JAT2A	Optional, only for HF interference reduction.
L1	Inductor	22 or 10 µH, 900mA	VLF403210MT-100M or 1235AS-H-220M	
L2	Inductor	1.5 µH	DFE252010R-H-1R5M	
D1	Schottky diode	40V, 200mA	NSR0240P2T5G	

9.2.2.2 Inductor Selection

Both of the LM3631 boost converters are internally compensated. The compensation parameters of the LCD bias boost converter are fixed and set for a 1.5-µH inductor. The backlight boost converter has a selection bit to choose between 10-µH or 22-µH inductors. The inductor typical inductance is selected with the INDUCTOR bit (Register 0x06, bit 2). Effective inductance of the inductors should be ±20%.

There are two main considerations when choosing an inductor: the inductor should not saturate, and the inductor current ripple should be small enough to achieve the desired output voltage ripple. Different saturation current rating specifications are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C. However, ratings at the maximum ambient temperature of application should be requested from the manufacturer. The saturation current should be greater than the sum of the maximum load current and the worst-case average-to-peak inductor current. The equation below shows the worst case conditions.

$$I_{SAT} > \frac{I_{OUTMAX}}{D'} + I_{RIPPLE}$$

$$\text{Where } I_{RIPPLE} = \frac{(V_{OUT} - V_{IN})}{(2 \times L \times f)} \times \frac{V_{IN}}{V_{OUT}}$$

$$\text{Where } D = \frac{(V_{OUT} - V_{IN})}{V_{OUT}} \quad \text{and } D' = (1 - D)$$

where

- I_{RIPPLE} = peak inductor current
- I_{OUTMAX} = maximum load current
- V_{IN} = minimum input voltage in application
- L = minimum inductor value including worst case tolerances
- f = minimum switching frequency
- V_{OUT} = output voltage (7)

As a result the inductor should be selected according to the I_{SAT}. A more conservative and recommended approach is to choose an inductor that has a saturation current rating greater than the maximum current limit. The inductor's resistance should be kept small for good efficiency.

See detailed information in "Understanding Boost Power Stages in Switch Mode Power Supplies" http://focus.ti.com/lit/an/slva061/slva061.pdf. "Power Stage Designer™ Tools" can be used for the boost calculation: http://www.ti.com/tool/powerstage-designer.

9.2.2.3 Boost Output Capacitor Selection

Two 2.2-µF capacitors are recommended for the backlight boost converter output capacitors. A single 2.2-µF capacitor can be used for reducing solution size as long as the effective output capacitance is higher than 1 µF. A high-quality ceramic type X5R or X7R is recommended. Voltage rating must be greater than the maximum output voltage that is used.

For the LCD-bias-boost output two 10-µF capacitors are recommended. A high-quality ceramic type X5R or X7R is recommended. Voltage rating must be greater than the maximum output voltage that is used.

The DC-bias effect of the capacitors must be taken into consideration when selecting the output capacitors. The effective capacitance of a ceramic capacitor can drop down to less than 10% with maximum rated DC bias voltage depending on capacitor type. Note that with a same voltage applied, the capacitors with higher voltage rating suffer less from the DC-bias effect than capacitors with lower voltage rating.

9.2.2.4 Backlight Boost Diode Selection

A Schottky diode should be used for the output diode. Peak repetitive current should be greater than inductor peak current to ensure reliable operation. Average current rating should be greater than the maximum output current. Reverse breakdown voltage of the Schottky diode should be significantly larger than the maximum output voltage.

9.2.2.5 Charge Pump Capacitor Selection

Voltage ratings for the flying capacitor and output capacitor must be higher than the maximum output voltage. Ceramic X5R/X7R capacitors are recommended. 10-V voltage rating and 10 µF capacitors are recommended for both.

9.2.2.6 LDO Output Capacitor Selection

Voltage ratings for the LDO output capacitors must be higher than the maximum output voltage. Ceramic X5R/X7R capacitors are recommended. 10-V voltage rating and 10-µF capacitors are recommended for all.

9.2.3 Application Curves

Figure 59 and Figure 60 show typical backlight start-up and shutdown curves using the LCD_EN pin control.

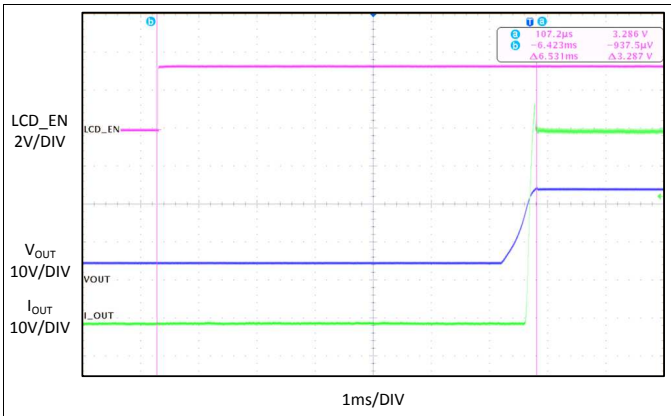


Figure 59. Backlight Start-up with LCD_EN Pin Control

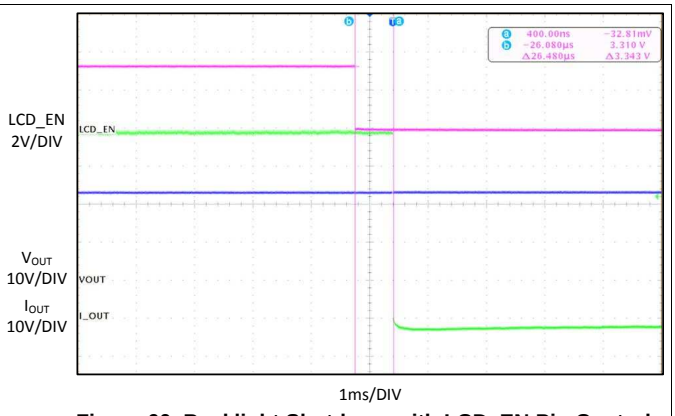


Figure 60. Backlight Shutdown with LCD_EN Pin Control

Figure 61 and Figure 62 show the default start-up and shutdown waveforms with OTP_SEL = GND. LDO_CONT pulldown is disabled by default causing V_{CONT} to float after shutdown.

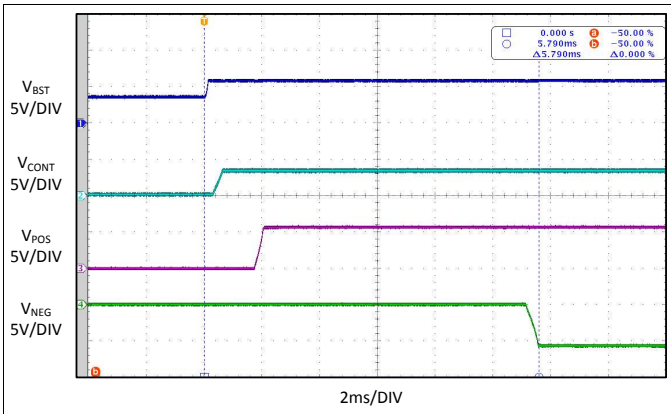


Figure 61. Default LCD Bias Startup, OTP_SEL = GND.

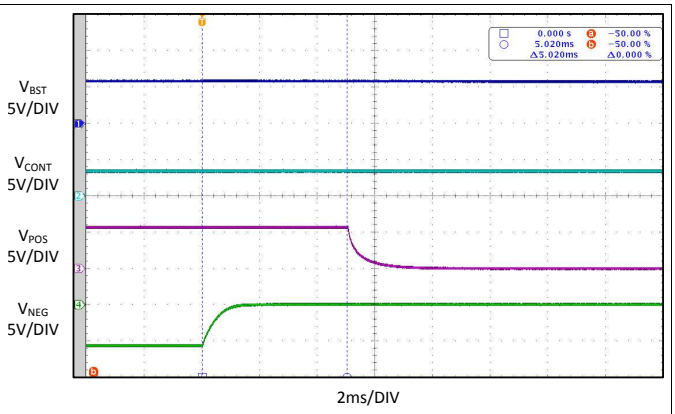


Figure 62. Default LCD Bias Shutdown, OTP_SEL = GND.

10 Power Supply Recommendations

The LM3631 is designed to operate from an input voltage supply range between 2.7 V and 5 V. This input supply must be well regulated and capable to supply the required input current. If the input supply is located far from the LM3631 additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

11 Layout

11.1 Layout Guidelines

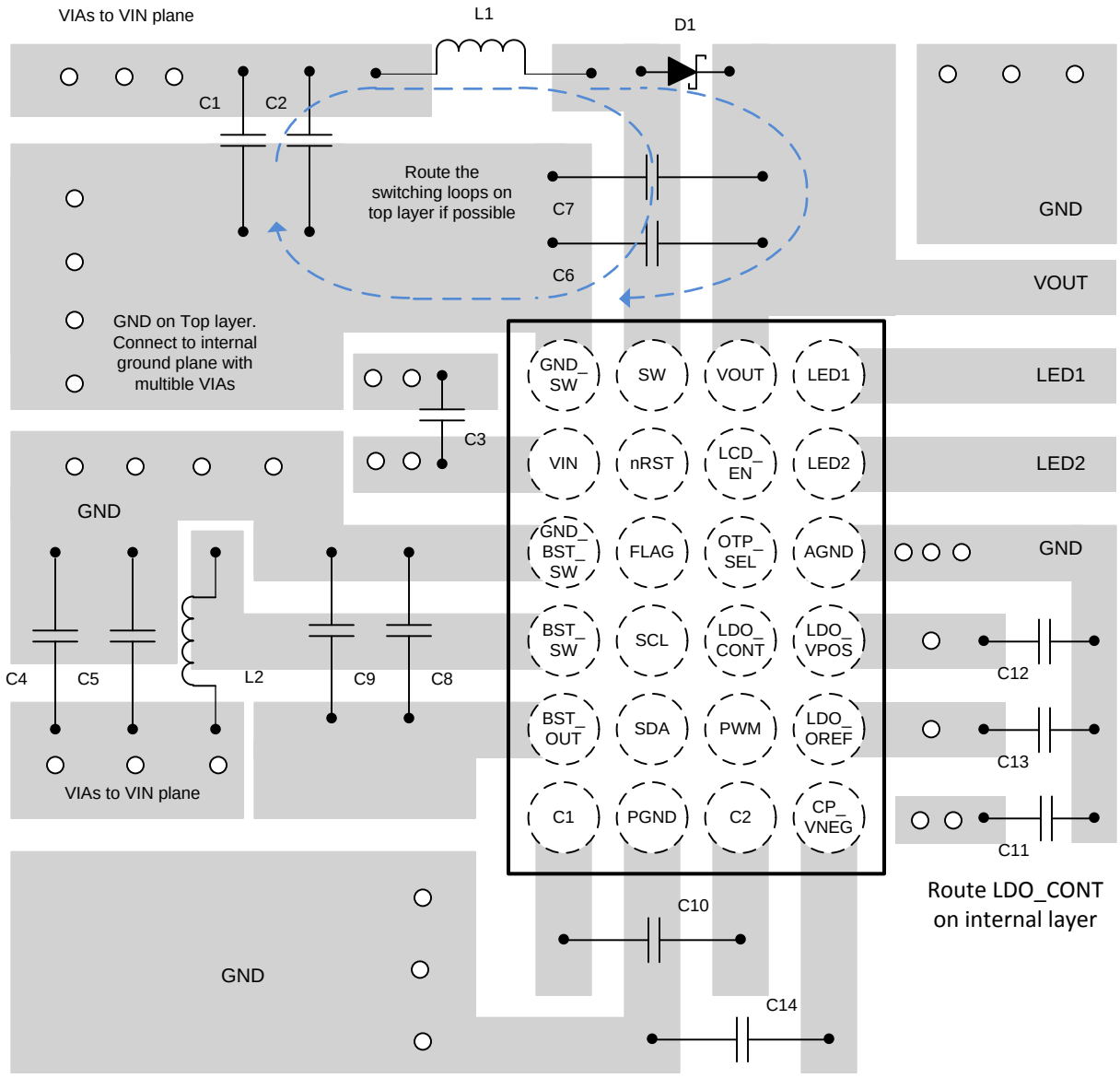
- Place the boost converters output capacitors as close to the output voltage and GND pins as possible.
- Minimize the boost converter switching loops by placing the input capacitors and inductors close to GND and switch pins.
- If possible, route the switching loops on top layer only. For best efficiency, try to minimize copper on the

Layout Guidelines (continued)

switch node to minimize switch pin parasitic capacitance while preserving adequate routing width.

- VIN input voltage pin needs to be bypassed to ground with a low-ESR bypass capacitor. Place the capacitor as close to VIN pin as possible
- Place the output capacitors of the LDOs as close to output pins as possible. Also place the charge pump flying capacitor and output capacitor close to respective pins.
- Route the internal pins on the second layer. Use offset micro vias to go from top layer to mid layer1. Avoid routing the signal traces directly under the switching loops of the boost converters.

11.2 Layout Example



12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM3631YFFR	Active	Production	DSBGA (YFF) | 24	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	LM3631
LM3631YFFR.A	Active	Production	DSBGA (YFF) | 24	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	LM3631

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

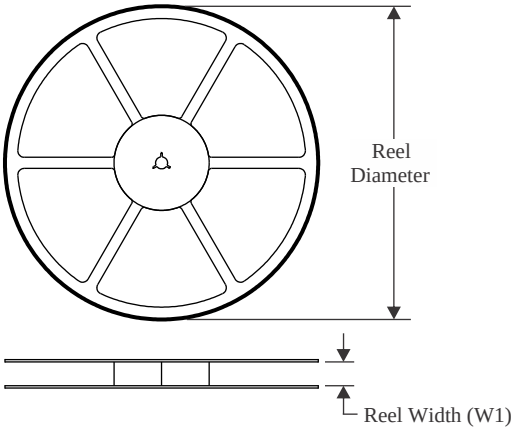
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

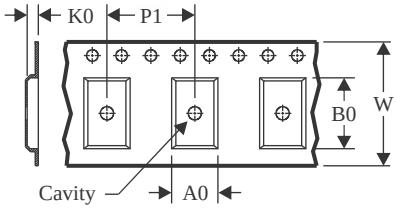
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

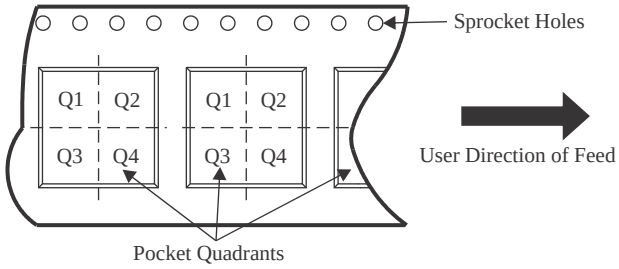


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

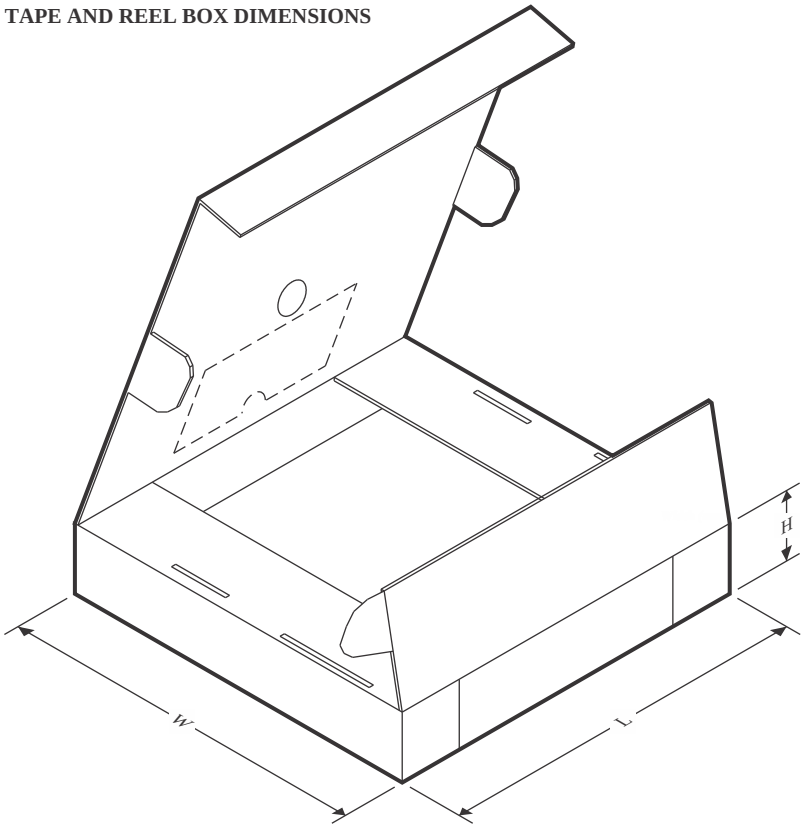
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3631YFFR	DSBGA	YFF	24	3000	180.0	8.4	2.1	2.76	0.81	4.0	8.0	Q1

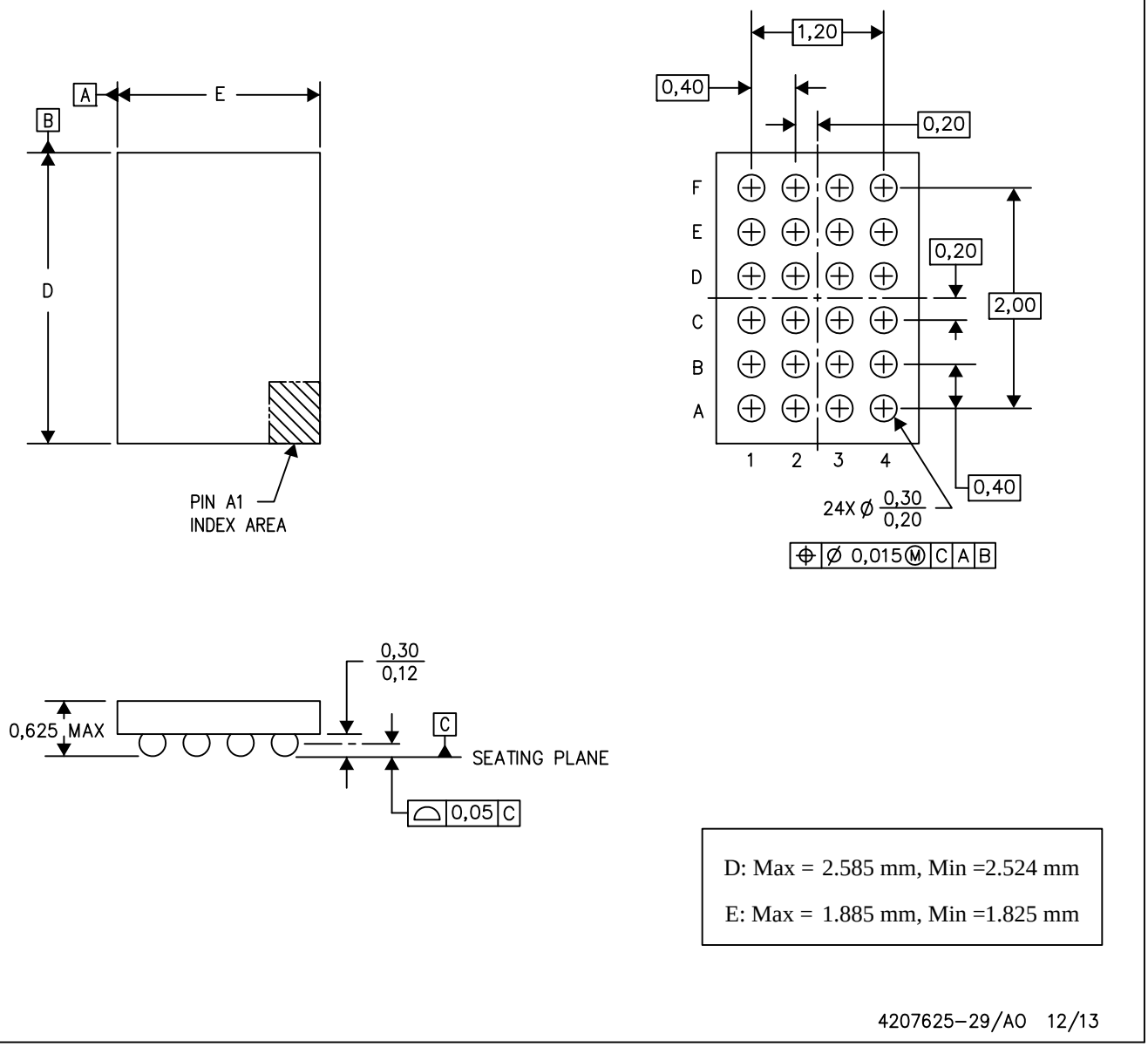
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3631YFFR	DSBGA	YFF	24	3000	182.0	182.0	20.0

YFF (R–XBGA–N24) DIE–SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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Last updated 10/2025