LM4855 Boomer® Audio Power Amplifier Series Integrated Audio Amplifier System

Check for Samples: LM4855

FEATURES

- **1.1W (Typ) Output Power with 8Ω Mono BTL Load**
- **115mW (Typ) Output Power with Stereo 32Ω BTL Loads**
- **SPI Programmable 32 Step Digital Volume Control**
- **Eight Distinct Output Modes**
- **DSBGA and WQFN Surface Mount Packaging**
- **"Click and Pop" Suppression Circuitry**
- **Thermal Shutdown Protection**
- **Low Shutdown Current (0.1uA, Typ)**

KEY SPECIFICATIONS

- **THD+N at 1kHz, 1.1W into 8Ω BTL: 1.0% (Typ)**
- **THD+N at 1kHz, 115mW into 32Ω BTL: 0.5% (Typ)**
- **Single Supply Operation: 2.6 to 5.0V**

APPLICATIONS

- **Moblie Phones**
- **PDAs**

DESCRIPTION

The LM4855 is an audio power amplifier system capable of delivering 1.1W (typ) of continuous average power into a mono 8Ω bridged-tied load (BTL) with 1% THD+N and 115mW (typ) per channel of continuous average power into stereo 32Ω BTL loads with 0.5% THD+N, using a 5V power supply.

The LM4855 features a 32 step digital volume control and eight distinct output modes. The digital volume control and output modes are programmed through a three-wire SPI serial control interface, that allows flexibility in routing and mixing audio channels.

The LM4855 is designed for cellular phone, PDA, and other portable handheld applications. It delivers high quality output power from a surface-mount package and requires only six external components.

The industry leading DSBGA package only utilizes 2mm x 2.3mm of PCB space, making the LM4855 the most space efficient audio sub system available today.

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Typical Application

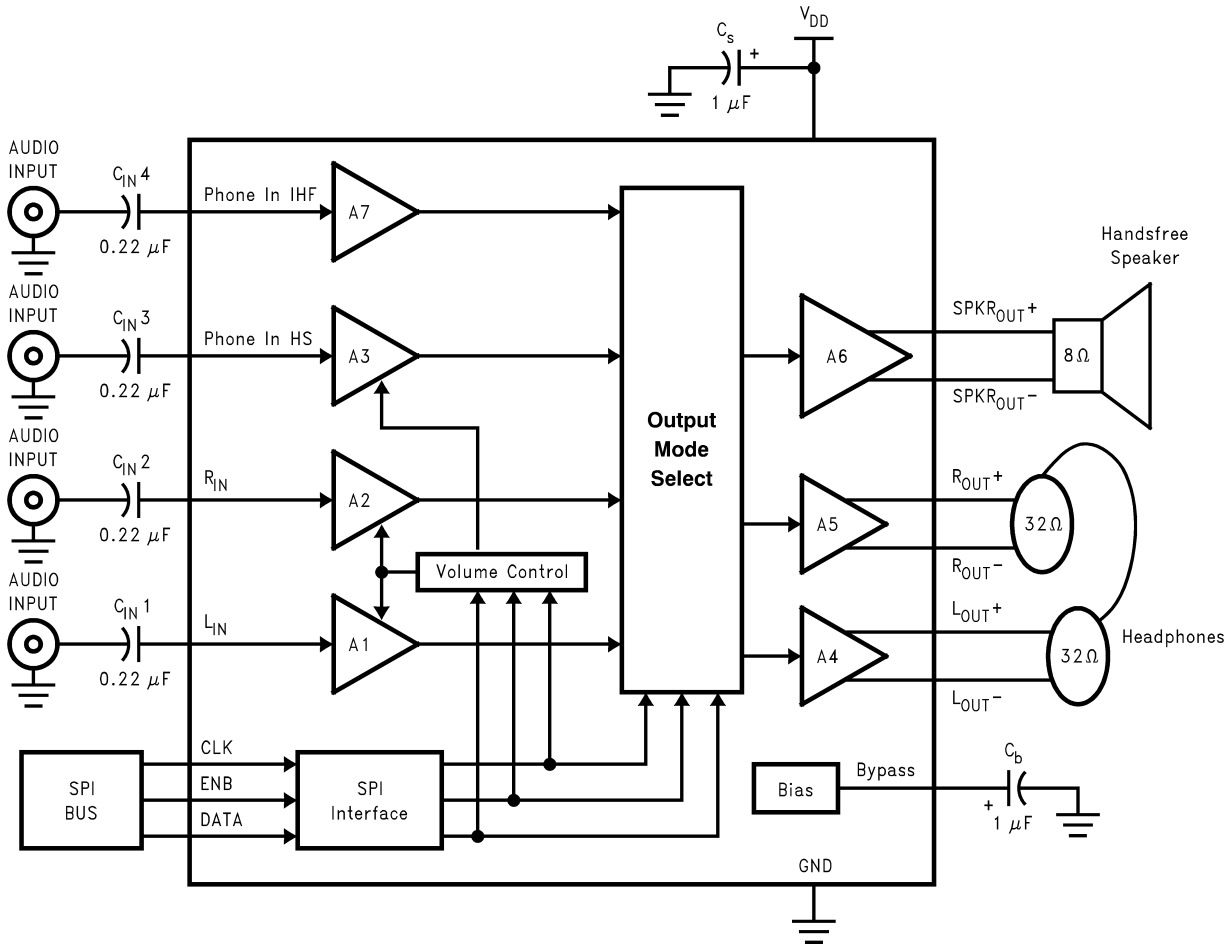

Figure 1. Typical Audio Amplifier Application Circuit

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Connection Diagrams

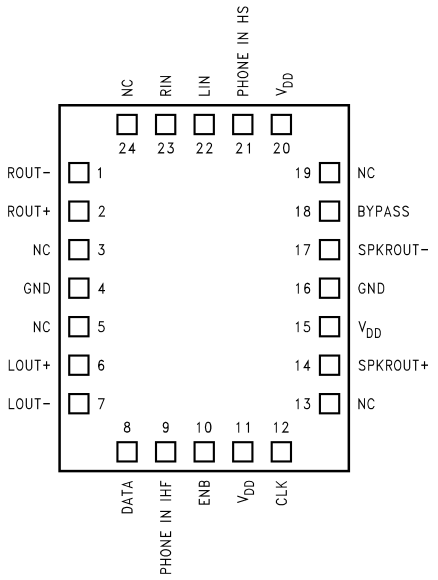

Figure 2. WQFN Package Top View
See Package Number NHW0024A
for Exposed-DAP WQFN

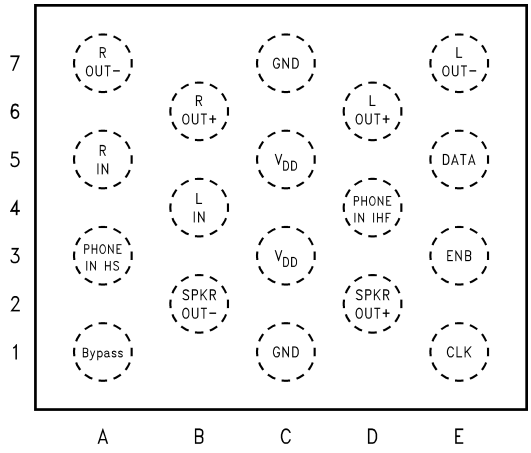

Figure 3. Top View (Bump-Side Down)
See Package Number YZR0018AAA

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage		6.0V
Storage Temperature		−65°C to +150°C
ESD Susceptibility[3]		2.0kV
ESD Machine model[4]		200V
Junction Temperature (T_J)		150°C
Solder Information	Vapor Phase (60 sec.)	215°C
	Infrared (15 sec.)	220°C
Thermal Resistance	θ_{JA} (typ) - NHW0024A	42°C/W
	θ_{JC} (typ) - NHW0024A	3.0°C/W
	θ_{JA} (typ) - YZR0018AAA	48°C/W[5]
	θ_{JC} (typ) - YZR0018AAA	23°C/W[5]

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human body model, 100pF discharged through a 1.5kΩ resistor.
(4) Machine Model ESD test is covered by specification EIAJ IC-121-1981. A 200pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (resistance of discharge path must be under 50Ω).
(5) The given θ_{JA} and θ_{JC} are for an LM4855 mounted on a demonstration board with a $4in^2$ area of 1oz printed circuit board copper ground plane.

Operating Ratings[1]

Temperature Range	−40°C to 85°C
Supply Voltage V_{DD}	$2.6V \le V_{DD} \le 5.0V$

(1) Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

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5V Electrical Characteristics[1][2]

The following specifications apply for V_{DD}= 5.0V, T_A= 25°C unless otherwise specified.

Symbol	Parameter	Conditions	LM4855		Units (Limits)
			Typical[3]	Limits[4]	
I_{DD}	Supply Current	Output mode 1 V_{IN} = 0V; No loads	5.7	8	mA (max)
		Output mode 1 V_{IN} = 0V; Loaded (Fig.1)	6.7	9	mA (max)
		Output modes 2, 3, 4, 5, 6, 7 V_{IN} = 0V; No loads	7.5	11	mA (max)
		Output modes 2, 3, 4, 5, 6, 7 V_{IN} = 0V; Loaded (Fig. 1)	8.5	12	mA (max)
I_{SD}	Shutdown Current	Output mode 0	0.1	2.0	µA (max)
V_{OS}	Output Offset Voltage	V_{IN} = 0V	5.0	40	mV (max)
P_O	Output Power	$SPKR_{OUT}$; R_L = 4Ω THD+N = 1%; f = 1kHz, LM4855LQ	1.5		W
		$SPKR_{OUT}$; R_L = 8Ω THD+N = 1%; f = 1kHz	1.1	0.8	W (min)
		R_{OUT} and L_{OUT}; R_L = 32Ω THD+N = 0.5%; f = 1kHz	115	70	mW (min)
THD+N	Total Harmonic Distortion Plus Noise	$SPKR_{OUT}$ f = 20Hz to 20kHZ P_{OUT} = 400mW; R_L = 8Ω	0.5		%
		R_{OUT} and L_{OUT} f = 20Hz to 20kHZ P_{OUT} = 50mW; R_L = 32Ω	0.5		%
N_{OUT}	Output Noise	A-weighted[5]	29		µV
PSRR	Power Supply Rejection Ratio $SPKR_{OUT}$	V_{RIPPLE} = 200mV_{PP}; f = 217Hz, C_B = 1.0µF All audio inputs terminated into 50Ω; Output referred Gain (BTL) = 12dB Output Mode 1, 3, 5, 7	57	54	dB (min)
	Power Supply Rejection Ratio $R_{OUT}$and L_{OUT}	V_{RIPPLE} = 200mV_{PP}; f = 217Hz, C_B = 1.0µF All audio inputs terminated into 50Ω; Output referred Maximum gain setting			
		Output Mode 2, 3	62	59	dB (min)
		Output Mode 4, 5	57	54	dB (min)
		Output Mode 6, 7	54	51	dB (min)
V_{IH}	Logic High Input Voltage			1.4 V_{DD}	V (min) V (max)
V_{IL}	Logic Low Input Voltage			0.4 GND	V (max) V (min)

(1) Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to the ground pin, unless otherwise specified.
(3) Typical specifications are specified at +25°C and represent the most likely parametric norm.
(4) Tested limits are ensured to AOQL (Average Outgoing Quality Level).
(5) Please refer to the Output Noise vs Output Mode table in the Typical Performance Characteristics section for more details.

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5V Electrical Characteristics[1][2] (continued)

The following specifications apply for V_{DD}= 5.0V, T_A= 25°C unless otherwise specified.

Symbol	Parameter	Conditions	LM4855		Units (Limits)
			Typical[3]	Limits[4]	
	Digital Volume Range (R_{IN} and L_{IN})	Input referred minimum gain	-34.5	-35.1 -33.9	dB (min) dB (max)
		Input referred maximum gain	12.0	11.4 12.6	dB (min) dB (max)
	Digital Volume Stepsize		1.5		dB
	Digital Volume Stepsize Error		±0.1	±0.6	dB (max)
	Phone_In_IHF Volume	BTL gain from Phone_In _IHF to $SPKR_{OUT}$	12	11.4 12.6	dB (min) dB (max)
	Phone _In_IHF Mute Attenuation	Output Mode 2, 4, 6	80	72	dB (min)
	Phone_In_IHF Input Impedance		20	15 25	kΩ (min) kΩ (max)
	Phone_In_HS Input Impedance	Maximum gain setting	50	37.5 62.5	kΩ (min) kΩ (max)
		Mininum gain setting	100	75 125	kΩ (min) kΩ (max)
	R_{IN} and L_{IN} Input Impedance	Maximum gain setting	33.5	25 42	kΩ (min) kΩ (max)
		Mininum gain setting	100	75 125	kΩ (min) kΩ (max)
t_{SD}	Thermal Shutdown Temperature		170	150	°C (min)
t_{ES}	Enable Setup Time (ENB)			20	ns (min)
t_{EH}	Enable Hold Time (ENB)			20	ns (min)
t_{EL}	Enable Low Time (ENB)			30	ns (min)
t_{DS}	Data Setup Time (DATA)			20	ns (min)
t_{DH}	Data Hold Time (DATA)			20	ns (min)
t_{CS}	Clock Setup Time (CLK)			20	ns (min)
t_{CH}	Clock Logic High Time (CLK)			50	ns (min)
t_{CL}	Clock Logic Low Time (CLK)			50	ns (min)
f_{CLK}	Clock Frequency			DC 10	(min) MHz (max)

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3V Electrical Characteristics[1][2]

The following specifications apply for V_{DD}= 3.0V, T_A= 25°C unless otherwise specified.

Symbol	Parameter	Conditions	LM4855		Units (Limits)
			Typical [3]	Limits [4]	
I_{DD}	Supply Current	Output mode 1 V_{IN} = 0V; No loads	4.5	7	mA (max)
		Output mode 1 V_{IN} = 0V; Loaded (Fig.1)	5.0	8	mA (max)
		Output modes 2, 3, 4, 5, 6, 7 V_{IN} = 0V; No loads	6.5	10	mA (max)
		Output modes 2, 3, 4, 5, 6, 7 V_{IN} = 0V; Loaded (Fig. 1)	7	11	mA (max)
I_{SD}	Shutdown Current	Output mode 0	0.1	2.0	µA (max)
V_{OS}	Output Offset Voltage	V_{IN} = 0V	5.0	40	mV (max)
P_O	Output Power	$SPKR_{OUT}$; R_L = 4Ω THD+N = 1%; f = 1kHz, LM4855LQ	430		mW
		$SPKR_{OUT}$; R_L = 8Ω THD+N = 1%; f = 1kHz	340	300	mW (min)
		R_{OUT} and L_{OUT}; R_L = 32Ω THD+N = 0.5%; f = 1kHz	25	20	mW (min)
THD+N	Total Harmonic Distortion Plus Noise	$SPKR_{OUT}$ f = 20Hz to 20kHZ P_{OUT} = 250mW; R_L = 8Ω	0.5		%
		R_{OUT} and L_{OUT} f = 20Hz to 20kHZ P_{OUT} = 20mW; R_L = 32Ω	0.5		%
N_{OUT}	Output Noise	A-weighted [5]	29		µV
PSRR	Power Supply Rejection Ratio $SPKR_{OUT}$	V_{RIPPLE} = 200mV_{PP}; f = 217Hz, C_B = 1.0µF All audio inputs terminated into 50Ω; Output referred Gain (BTL) = 12dB Output Mode 1, 3, 5, 7	58	55	dB (min)
	Power Supply Rejection Ratio $R_{OUT}$and L_{OUT}	V_{RIPPLE} = 200mV_{PP}; f = 217Hz, C_B = 1.0µF All audio inputs terminated into 50Ω; Output referred Maximum gain setting			
		Output Mode 2, 3	63	60	dB (min)
		Output Mode 4, 5	58	55	dB (min)
		Output Mode 6, 7	55	52	dB (min)
V_{IH}	Logic High Input Voltage			1.4 V_{DD}	V (min) V (max)
V_{IL}	Logic Low Input Voltage			0.4 GND	V (max) V (min)

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.
(2) All voltages are measured with respect to the ground pin, unless otherwise specified.
(3) Typical specifications are specified at +25°C and represent the most likely parametric norm.
(4) Tested limits are ensured to AOQL (Average Outgoing Quality Level).
(5) Please refer to the Output Noise vs Output Mode table in the Typical Performance Characteristics section for more details.

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3V Electrical Characteristics[1][2] (continued)

The following specifications apply for V_{DD}= 3.0V, T_A= 25°C unless otherwise specified.

Symbol	Parameter	Conditions	LM4855		Units (Limits)
			Typical (3)	Limits (4)	
	Digital Volume Range (R_{IN} and L_{IN})	Input referred minimum gain	-34.5	-35.1 -33.9	dB (min) dB (max)
		Input referred maximum gain	12.0	11.4 12.6	dB (min) dB (max)
	Digital Volume Stepsize		1.5		dB
	Digital Volume Stepsize Error		±0.1	±0.6	dB (max)
	Phone_In_IHF Volume	BTL gain from Phone_In _IHF to $SPKR_{OUT}$	12	11.4 12.6	dB (min) dB (max)
	Phone _In_IHF Mute Attenuation	Output Mode 2, 4, 6	80	72	dB (min)
	Phone_In_IHF Input Impedance		20	15 25	kΩ (min) kΩ (max)
	Phone_In_HS Input Impedance	Maximum gain setting	50	37.5 62.5	kΩ (min) kΩ (max)
		Mininum gain setting	100	75 125	kΩ (min) kΩ (max)
	R_{IN} and L_{IN} Input Impedance	Maximum gain setting	33.5	25 42	kΩ (min) kΩ (max)
		Mininum gain setting	100	75 125	kΩ (min) kΩ (max)
t_{SD}	Thermal Shutdown Temperature		170	150	°C (min)
t_{ES}	Enable Setup Time (ENB)			20	ns (min)
t_{EH}	Enable Hold Time (ENB)			20	ns (min)
t_{EL}	Enable Low Time (ENB)			30	ns (min)
t_{DS}	Data Setup Time (DATA)			20	ns (min)
t_{DH}	Data Hold Time (DATA)			20	ns (min)
t_{CS}	Clock Setup Time (CLK)			20	ns (min)
t_{CH}	Clock Logic High Time (CLK)			50	ns (min)
t_{CL}	Clock Logic Low Time (CLK)			50	ns (min)
f_{CLK}	Clock Frequency			DC 10	(min) MHz (max)

External Components Description

Components		Functional Description
1.	C_{IN}	This is the input coupling capacitor. It blocks the DC voltage and couples the input signal to the amplifier's input terminals. C_{IN} also creates a highpass filter with the internal resistor R_i (Input Impedance) at $f_c = 1/(2\pi R_i C_{IN})$.
2.	C_S	This is the supply bypass capacitor. It filters the supply voltage applied to the V_{DD} pin and helps maintain the LM4855's PSRR.
3.	C_B	This is the BYPASS pin capacitor. It filters the V_{DD} / 2 voltage and helps maintain the LM4855's PSRR.

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Typical Performance Characteristics

THD+N vs Frequency LM4855LQ

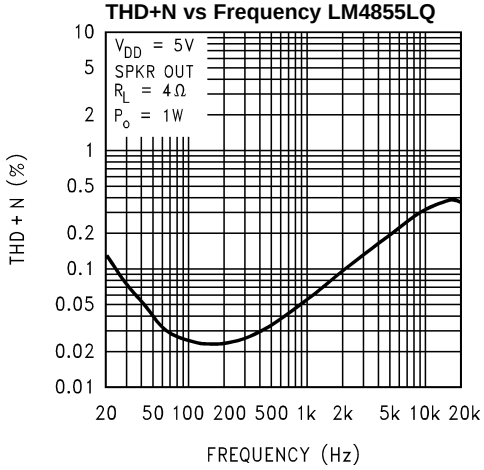

Figure 4.

THD+N vs Frequency LM4855LQ

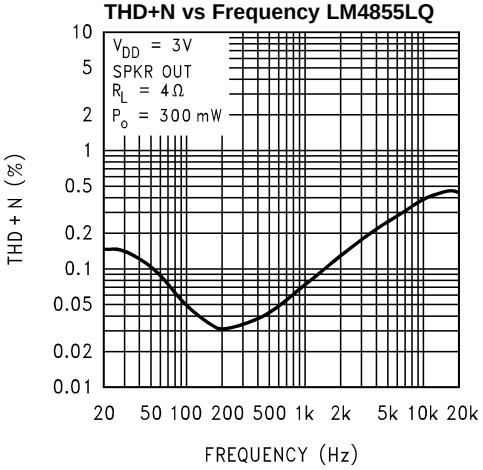

Figure 5.

THD+N vs Frequency

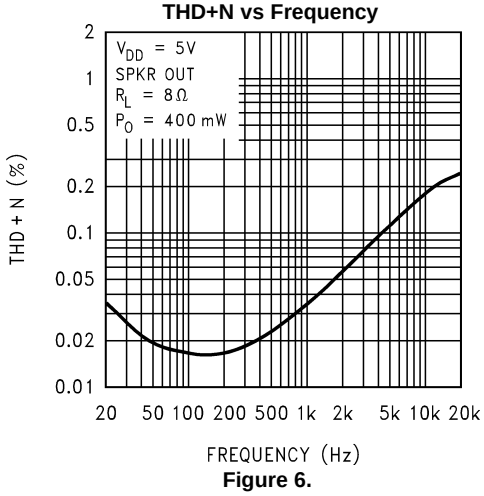

Figure 6.

THD+N vs Frequency

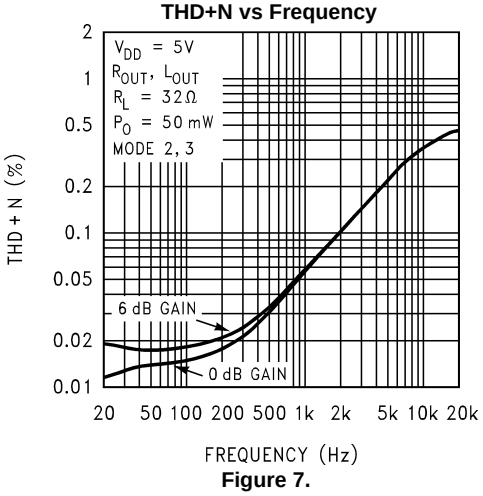

Figure 7.

THD+N vs Frequency

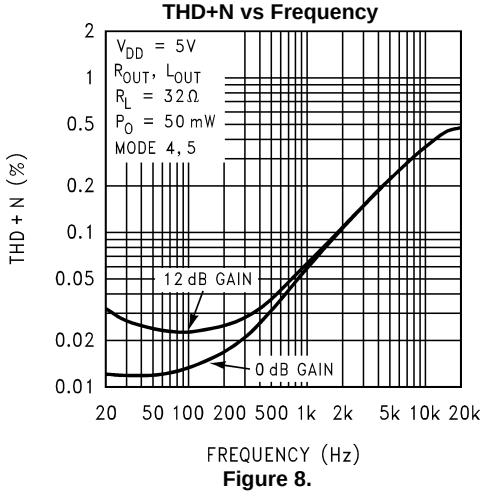

Figure 8.

THD+N vs Frequency

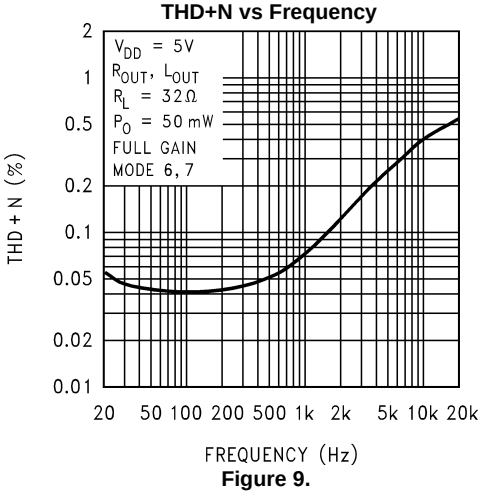

Figure 9.

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Typical Performance Characteristics (continued)

THD+N vs Frequency

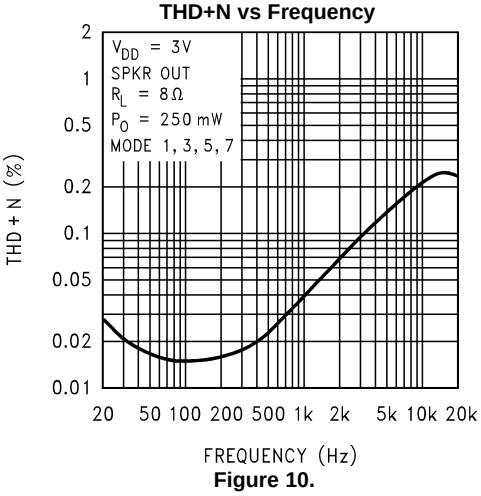

Figure 10.

THD+N vs Frequency

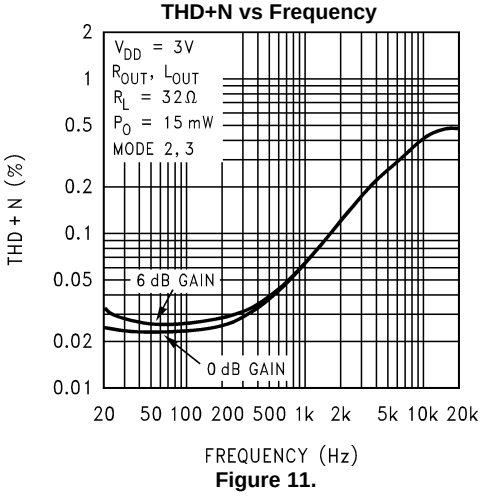

Figure 11.

THD+N vs Frequency

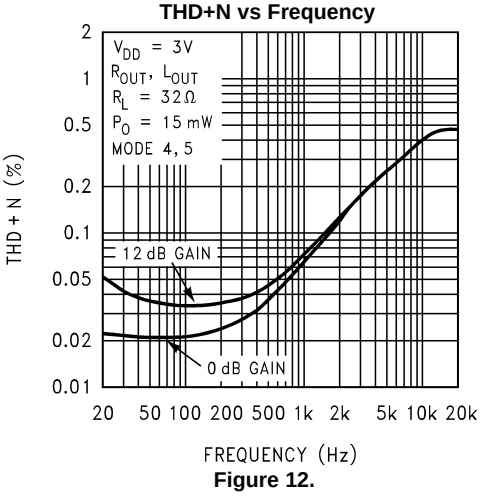

Figure 12.

THD+N vs Frequency

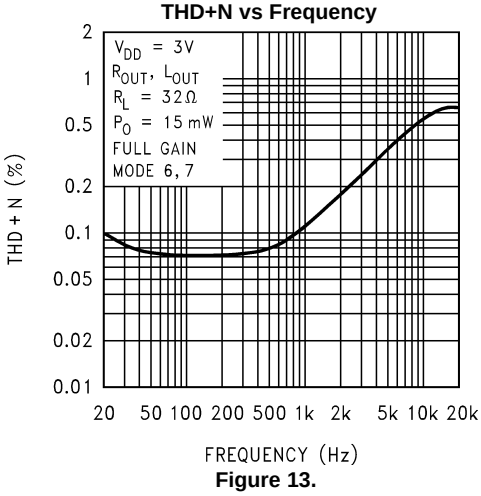

Figure 13.

THD+N vs Output Power LM4855LQ

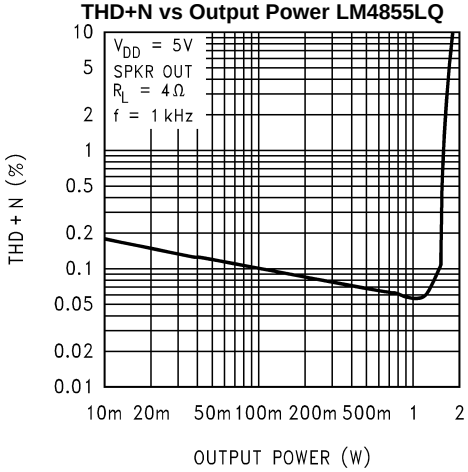

Figure 14.

THD+N vs Output Power LM4855LQ

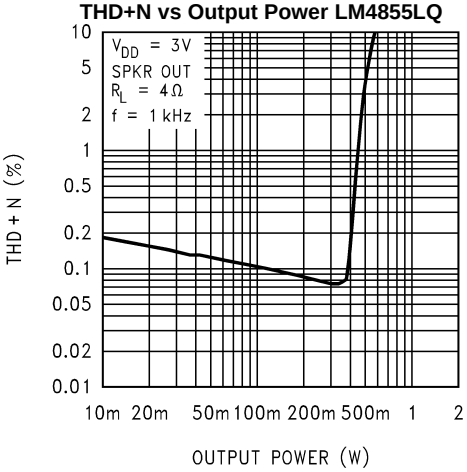

Figure 15.

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Typical Performance Characteristics (continued)

THD+N vs Output Power

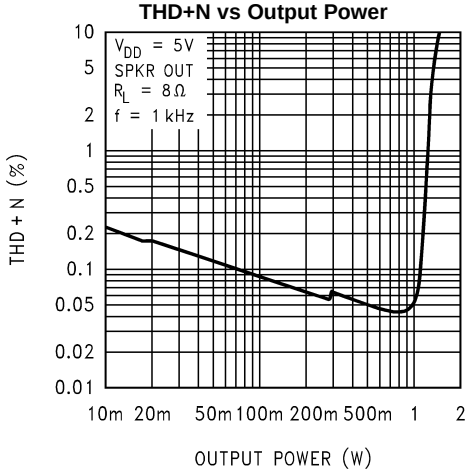

Figure 16.

THD+N vs Output Power

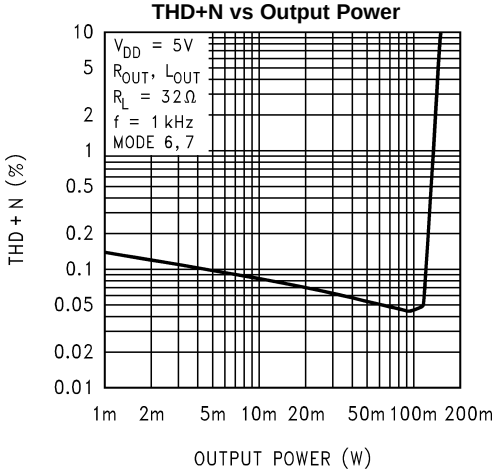

Figure 17.

THD+N vs Output Power

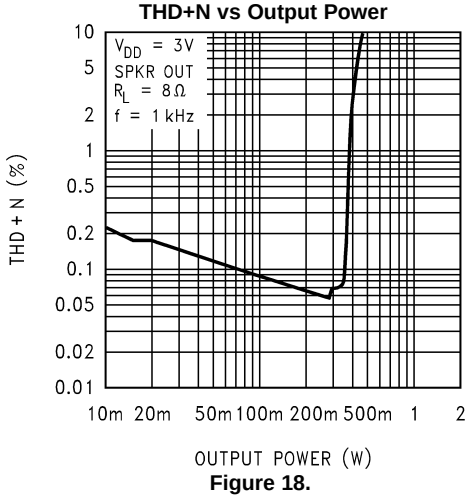

Figure 18.

THD+N vs Output Power

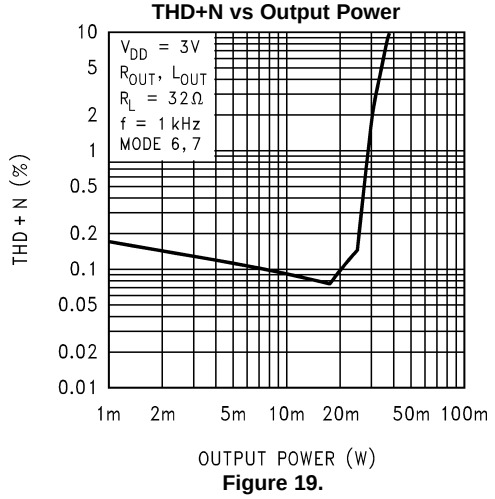

Figure 19.

Power Supply Rejection Ratio

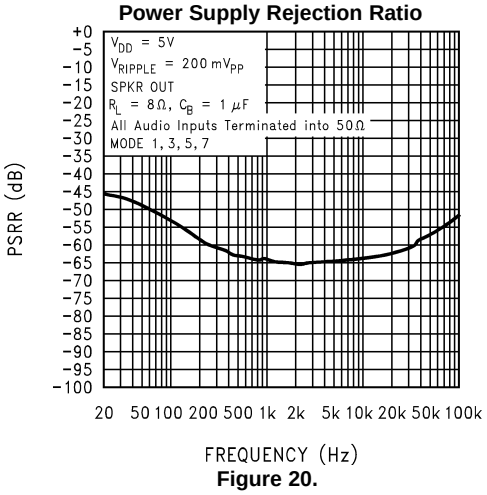

Figure 20.

Power Supply Rejection Ratio

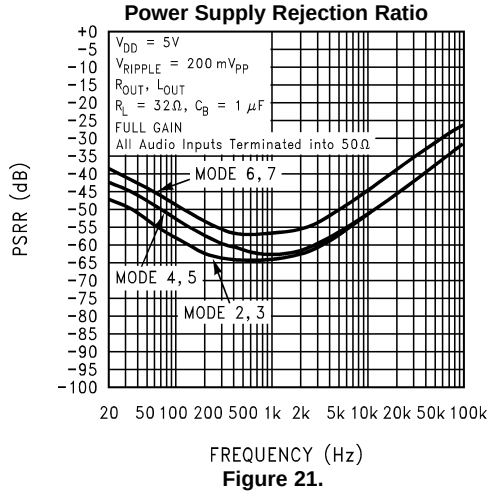

Figure 21.

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Typical Performance Characteristics (continued)

Power Supply Rejection Ratio

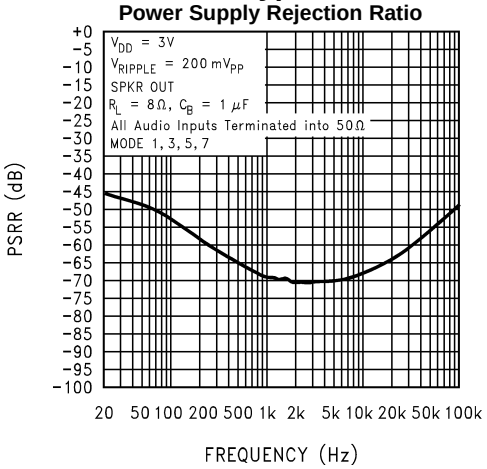

Figure 22.

Power Supply Rejection Ratio

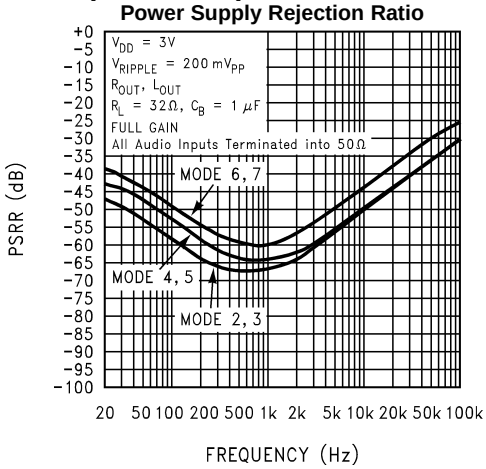

Figure 23.

Power Supply Rejection Ratio

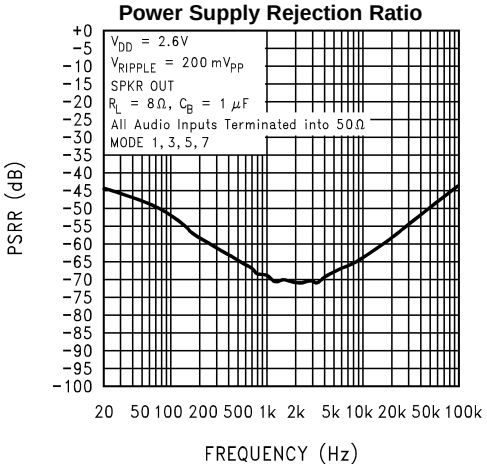

Figure 24.

Power Supply Rejection Ratio

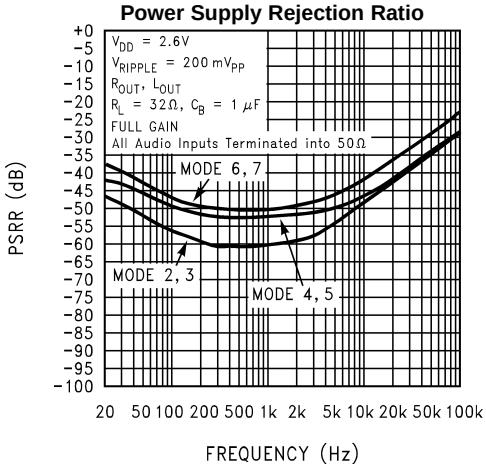

Figure 25.

Output Power vs Supply Voltage

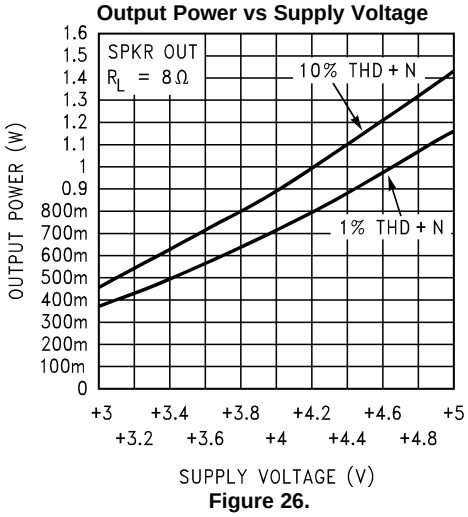

Figure 26.

Output Power vs Supply Voltage

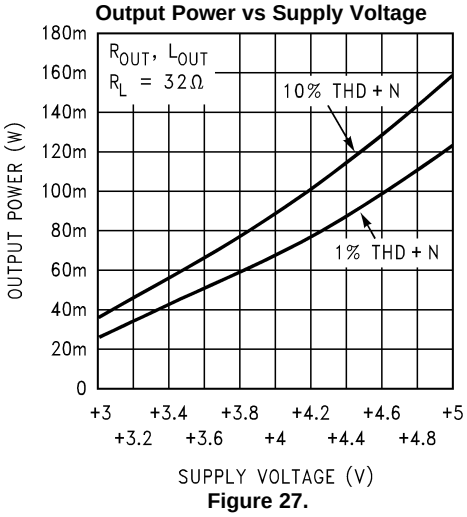

Figure 27.

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Typical Performance Characteristics (continued)

Output Power vs Load Resistance

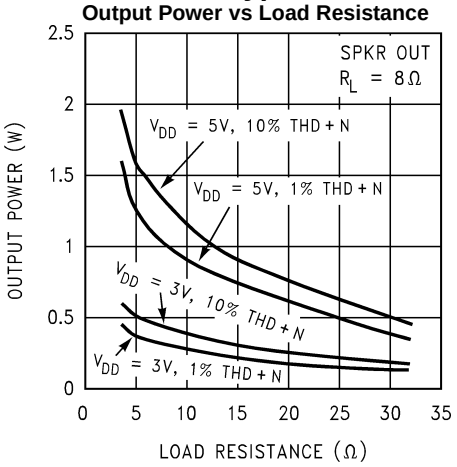

Figure 28.

Output Power vs Load Resistance

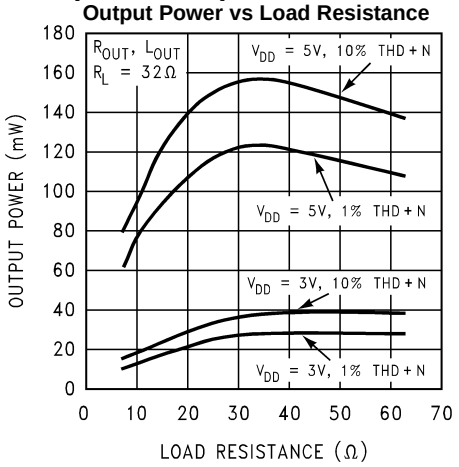

Figure 29.

Power Dissipation vs Output Power

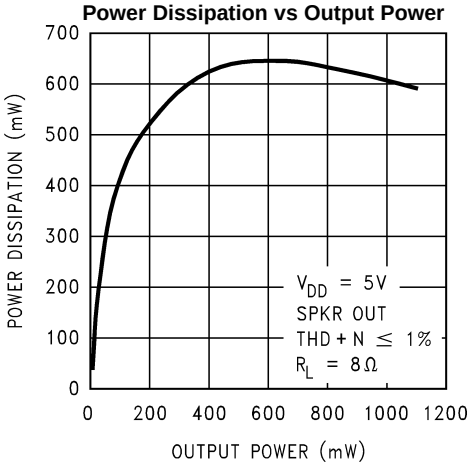

Figure 30.

Power Dissipation vs Output Power

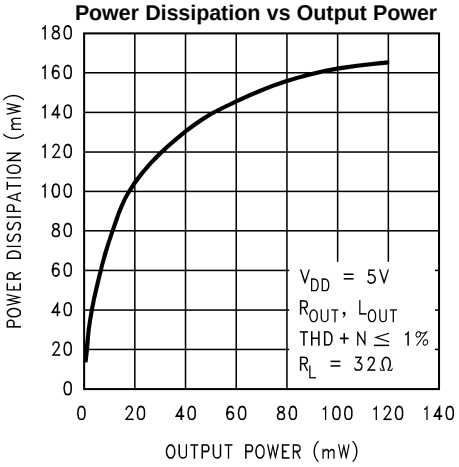

Figure 31.

Supply Current vs Supply Voltage

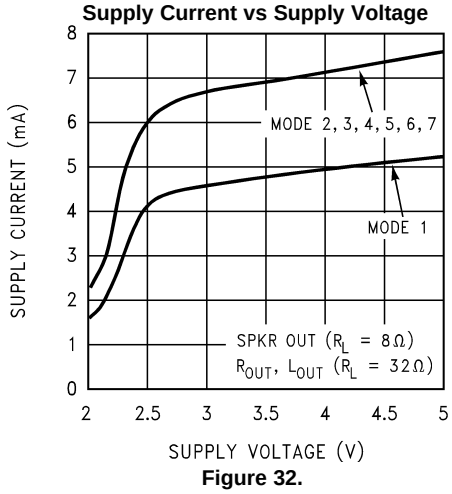

Figure 32.

Channel Separation

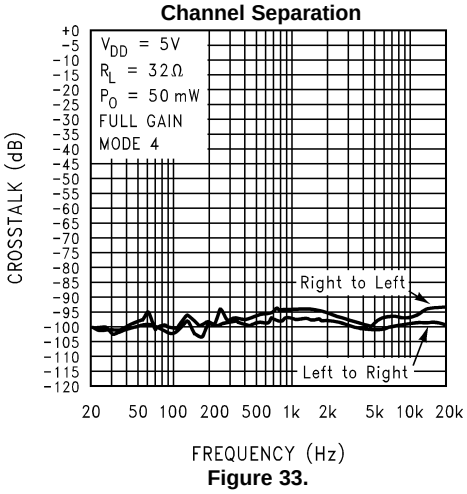

Figure 33.

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Typical Performance Characteristics (continued)

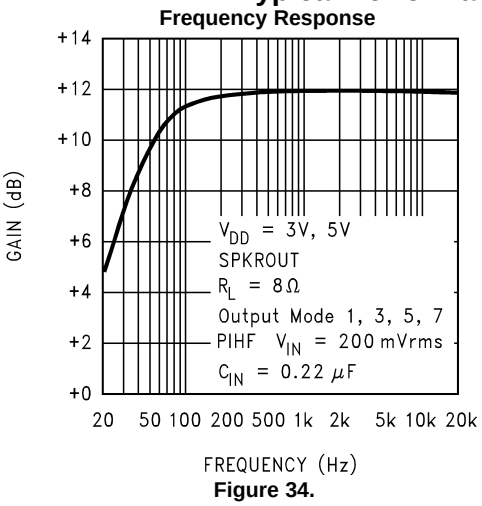

Figure 34.

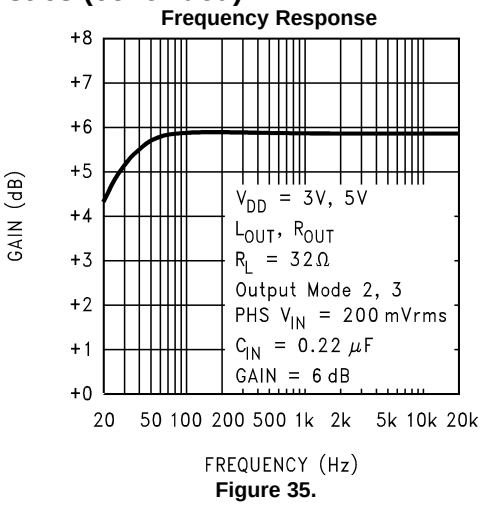

Figure 35.

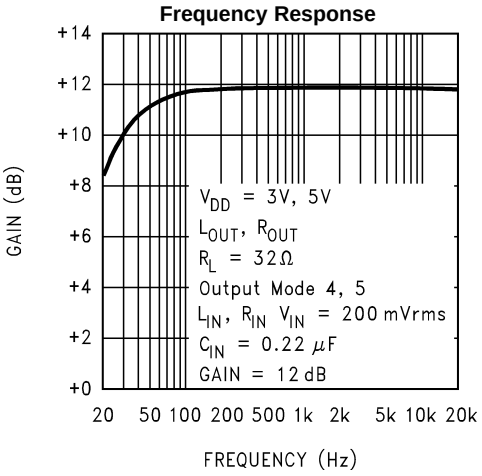

Figure 36.

Table 1. Output Noise vs Output Mode (V_{DD} = 3V, 5V)[1][2][3]

Output Mode	SPKROUT Output Noise (µV)	LOUT/ROUT Output Noise (µV)
1	29	X
2	X	28 (G1 = 0dB) 31 (G1 = 6dB)
3	29	28 (G1 = 0dB) 31 (G1 = 6dB)
4	X	28 (G2 = 0dB) 38 (G2 = 12dB)
5	29	28(G2 = 0dB) 38 (G2 = 12dB)
6	X	38 (G2 = 0dB) 41 (G1 = 0dB) 48 (G1 = 6dB)
7	29	38 (G2 = 0dB) 41 (G1 = 0dB) 48 (G1 = 6dB)

(1) G1 = gain from P_{HS} to LOUT/ROUT
(2) G2 = gain from LIN/RIN to LOUT/ROUT
(3) A - weighted filter used

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APPLICATION INFORMATION

SPI PIN DESCRIPTION

DATA: This is the serial data input pin.

CLK: This is the clock input pin.

ENB: This is the SPI enable pin and is active-high.

SPI OPERATION DESCRIPTION

The serial data bits are organized into a field which contains 8 bits of data defined by Table 2. The Data 0 to Data 2 bits determine the output mode of the LM4855 as shown in Table 3. The Data 3 to Data 7 bits determine the volume level setting as illustrated by Table 4. For each SPI transfer, the data bits are written to the DATA pin with the least significant bit (LSB) first. All serial data are sampled at the rising edge of the CLK signal. Once all the data bits have been sampled, ENB transitions from logic-high to logic-low to complete the SPI sequence. All 8 bits must be received before any data latch can occur. Any excess CLK and DATA transitions will be ignored after the eighth rising clock edge has occurred. For any data sequence longer than 8 bits, only the first 8 bits will get loaded into the shift register and the rest of the bits will be disregarded.

Table 2. Bit Allocation

Data 0	Mode Select
Data 1	Mode Select
Data 2	Mode Select
Data 3	Volume Control
Data 4	Volume Control
Data 5	Volume Control
Data 6	Volume Control
Data 7	Volume Control

Table 3. Output Mode Selection(1)

Output Mode #	Data 2	Data 1	Data 0	$SPKR_{OUT}$	R_{OUT}	L_{OUT}
0	0	0	0	SD	SD	SD
1	0	0	1	12dB x P_{IHF}	SD	SD
2	0	1	0	MUTE	G1 x P_{HS}	G1 x P_{HS}
3	0	1	1	12dB x P_{IHF}	G1 x P_{HS}	G1 x P_{HS}
4	1	0	0	MUTE	G2 x R	G2 x L
5	1	0	1	12dB x P_{IHF}	G2 x R	G2 x L
6	1	1	0	MUTE	(G1 x P_{HS}) + (G2 x R)	(G1 x P_{HS}) + (G2 x L)
7	1	1	1	12dB x P_{IHF}	(G1 x P_{HS}) + (G2 x R)	(G1 x P_{HS}) + (G2 x L)

(1) R = Rin
L = Lin
P_{IHF} = Phone_In_IHF
P_{HS} = Phone_In_HS
SD = Shutdown Mode
MUTE = Mute Mode
G1 = gain from P_{HS} to LOUT/ROUT
G2 = gain from LIN/ RIN to LOUT/ROUT
Default Mode upon device power-up is Output Mode 0

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Table 4. Volume Control Settings

Gain (dB)		Data 7	Data 6	Data 5	Data 4	Data 3
G2	G1					
R_{IN}, L_{IN} to R_{OUT}, L_{OUT}	Phone_In_HS to R_{OUT}, L_{OUT}					
-34.5	-40.5	0	0	0	0	0
-33.0	-39.0	0	0	0	0	1
-31.5	-37.5	0	0	0	1	0
-30.0	-360	0	0	0	1	1
-28.5	-34.5	0	0	1	0	0
-27.0	-33.0	0	0	1	0	1
-25.5	-31.5	0	0	1	1	0
-24.0	-30.0	0	0	1	1	1
-22.5	-28.5	0	1	0	0	0
-21.0	-27.0	0	1	0	0	1
-19.5	-25.5	0	1	0	1	0
-18.0	-24.0	0	1	0	1	1
-16.5	-22.5	0	1	1	0	0
-15.0	-21.0	0	1	1	0	1
-13.5	-19.5	0	1	1	1	0
-12.0	-18.0	0	1	1	1	1
-10.5	-16.5	1	0	0	0	0
-9.0	-15.0	1	0	0	0	1
-7.5	-13.5	1	0	0	1	0
-6.0	-12.0	1	0	0	1	1
-4.5	-10.5	1	0	1	0	0
-3.0	-9.0	1	0	1	0	1
-1.5	-7.5	1	0	1	1	0
0.0	-6.0	1	0	1	1	1
1.5	-4.5	1	1	0	0	0
3.0	-3.0	1	1	0	0	1
4.5	-1.5	1	1	0	1	0
6.0	0	1	1	0	1	1
7.5	1.5	1	1	1	0	0
9.0	3.0	1	1	1	0	1
10.5	4.5	1	1	1	1	0
12.0	6.0	1	1	1	1	1

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SPI OPERATIONAL REQUIREMENTS

1. The data bits are transmitted with the LSB first.

2. The maximum clock rate is 10MHz for the CLK pin.

3. CLK must remain logic-high for at least 50ns (t_{CH}) after the rising edge of CLK, and CLK must remain logic-low for at least 50ns (t_{CL}) after the falling edge of CLK.

4. The serial data bits are sampled at the rising edge of CLK. Any transition on DATA must occur at least 20ns (t_{DS}) before the rising edge of CLK. Also, any transition on DATA must occur at least 20ns (t_{DH}) after the rising edge of CLK and stabilize before the next rising edge of CLK.

5. ENB should be logic-high only during serial data transmission.

6. ENB must be logic-high at least 20ns (t_{ES}) before the first rising edge of CLK, and ENB has to remain logic-high at least 20ns (t_{EH}) after the eighth rising edge of CLK.

7. If ENB remains logic-low for more than 10ns before all 8 bits are transmitted then the data latch will be aborted.

8. If ENB is logic-high for more than 8 CLK pulses then only the first 8 data bits will be latched and activated when ENB transitions to logic-low.

9. ENB must remain logic-low for at least 30ns (t_{EL}) to latch in the data.

10. Coincidental rising or falling edges of CLK and ENB are not allowed. If CLK is to be held logic-high after the data transmission, the falling edge of CLK must occur at least 20ns (t_{CS}) before ENB transitions to logic-high for the next set of data.

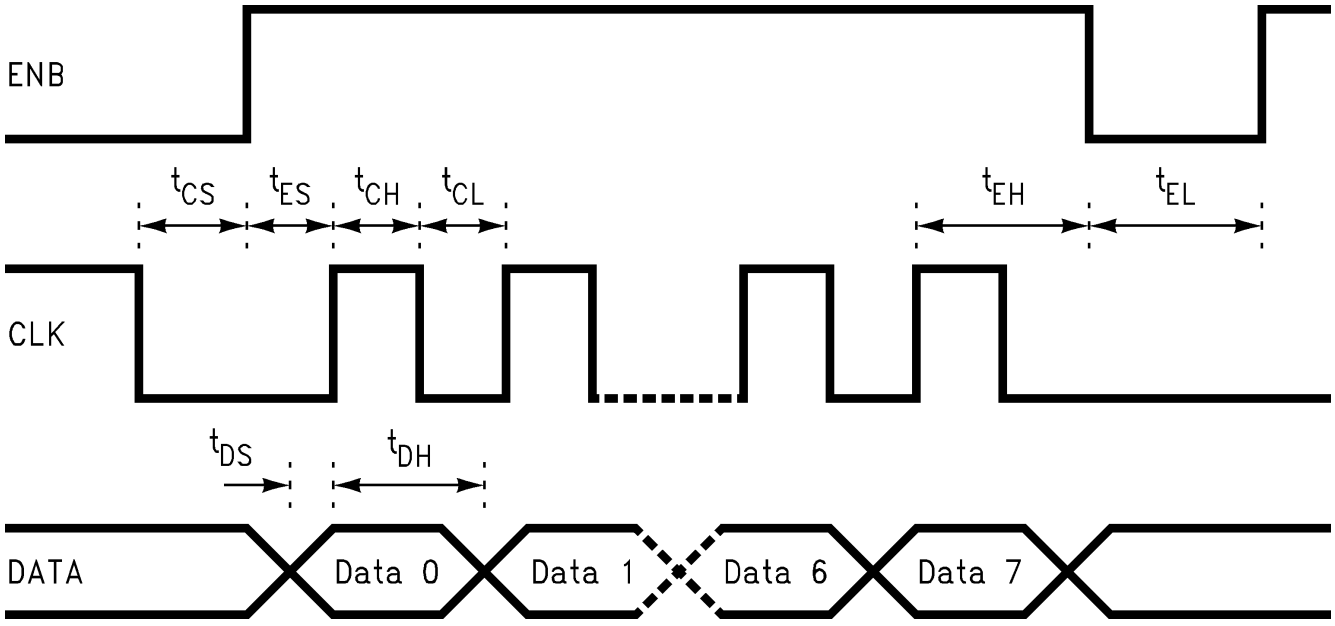

Figure 37. SPI Timing Diagram

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EXPOSED-DAP MOUNTING CONSIDERATIONS

The LM4855's exposed-DAP (die attach paddle) package (NHW) provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper area heatsink, copper traces, ground plane, and finally, surrounding air. The result is a low voltage audio power amplifier that produces 1.1W dissipation in a 8Ω load at ≤ 1% THD+N. This high power is achieved through careful consideration of necessary thermal design. Failing to optimize thermal design may compromise the LM4855's high power performance and activate unwanted, though necessary, thermal shutdown protection.

The NHW package must have its DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad is then, ideally, connected to a large plane of continuous unbroken copper. This plane forms a thermal mass, heat sink, and radiation area. Place the heat sink area on either outside plane in the case of a two-sided or multi-layer PCB. (The heat sink area can also be placed on an inner layer of a multi-layer board. The thermal resistance, however, will be higher.) Connect the DAP copper pad to the inner layer or backside copper heat sink area with 6 (3 X 2) (NHW) vias. The via diameter should be 0.012in - 0.013in with a 1.27mm pitch. Ensure efficient thermal conductivity by plugging and tenting the vias with plating and solder mask, respectively.

Best thermal performance is achieved with the largest practical copper heat sink area. If the heatsink and amplifier share the same PCB layer, a nominal 2.5in^2 (min) area is necessary for 5V operation with a 4Ω load. Heatsink areas not placed on the same PCB layer as the LM4855 should be 5in^2 (min) for the same supply voltage and load resistance. The last two area recommendations apply for 25°C ambient temperature. Increase the area to compensate for ambient temperatures above 25°C. In all circumstances and under all conditions, the junction temperature must be held below 150°C to prevent activating the LM4855's thermal shutdown protection. Further detailed and specific information concerning PCB layout and fabrication and mounting an NHW (WQFN) is found in TI's AN1187.

PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING 3Ω AND 4Ω LOADS

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example, 0.1Ω trace resistance reduces the output power dissipated by a 4Ω load from 1.7W to 1.6W. The problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

BRIDGE CONFIGURATION EXPLANATION

As shown in Figure 1, the LM4855 consists of three pairs of output amplifier blocks (A4-A6). A4, A5, and A6 consist of bridged-tied amplifier pairs that drive LOUT, ROUT, and SPKROUT respectively. The LM4855 drives a load, such as a speaker, connected between outputs, SPKROUT+ and SPKROUT-. In the amplifier block A6, the output of the amplifier that drives SPKROUT- serves as the input to the unity gain inverting amplifier that drives SPKROUT+.

This results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between SPKROUT- and SPKROUT+ and driven differentially (commonly referred to as 'bridge mode'). This results in a differential or BTL gain of:

$$A_{VD} = 2(R_f/R_i) = 2 \quad (1)$$

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Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. Theoretically, this produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited and that the output signal is not clipped.

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing SPKROUT- and SPKROUT+ outputs at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a typical single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier.

A direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation. The LM4855 has a pair of bridged-tied amplifiers driving a handsfree speaker, SPKROUT. The maximum internal power dissipation operating in the bridge mode is twice that of a single-ended amplifier. From Equation (2), assuming a 5V power supply and an 8Ω load, the maximum SPKROUT power dissipation is 634mW.

$$P_{DMAX\text{-}SPKROUT} = 4(V_{DD})^2/(2\pi^2 R_L)\text{: Bridge Mode} \quad (2)$$

The LM4855 also has 2 pairs of bridged-tied amplifiers driving stereo headphones, ROUT and LOUT. The maximum internal power dissipation for ROUT and LOUT is given by equation (3) and (4). From Equations (3) and (4), assuming a 5V power supply and a 32Ω load, the maximum power dissipation for LOUT and ROUT is 158mW, or 316mW total.

$$P_{DMAX\text{-}LOUT} = 4(V_{DD})^2/(2\pi^2 R_L)\text{: Bridge Mode} \quad (3)$$

$$P_{DMAX\text{-}ROUT} = 4(V_{DD})^2/(2\pi^2 R_L)\text{: Bridge Mode} \quad (4)$$

The maximum internal power dissipation of the LM4855 occurs when all 3 amplifiers pairs are simultaneously on; and is given by Equation (5).

$$P_{DMAX\text{-}TOTAL} = P_{DMAX\text{-}SPKROUT} + P_{DMAX\text{-}LOUT} + P_{DMAX\text{-}ROUT} \quad (5)$$

The maximum power dissipation point given by Equation (5) must not exceed the power dissipation given by Equation (6):

$$P_{DMAX}' = (T_{JMAX} - T_A)/\theta_{JA} \quad (6)$$

The LM4855's TJMAX = 150°C. In the YZR package, the LM4855's θ_{JA} is 48°C/W. In the NHW package soldered to a DAP pad that expands to a copper area of 2.5in^2 on a PCB, the LM4855's θ_{JA} is 42°C/W. At any given ambient temperature T_A, use Equation (6) to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation (6) and substituting $P_{DMAX\text{-}TOTAL}$ for P_{DMAX}' results in Equation (7). This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the LM4855's maximum junction temperature.

$$T_A = T_{JMAX} - P_{DMAX\text{-}TOTAL}\theta_{JA} \quad (7)$$

For a typical application with a 5V power supply and an 8Ω load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 104°C for the YZR package.

$$T_{JMAX} = P_{DMAX\text{-}TOTAL}\,\theta_{JA} + T_A \quad (8)$$

Equation (8) gives the maximum junction temperature T_{JMAX}. If the result violates the LM4855's 150°C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases. If the result of Equation (5) is greater than that of Equation (6), then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce θ_{JA}. The heat sink can be created using additional

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copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. External, solder attached SMT heatsinks such as the Thermalloy 7106D can also improve power dissipation. When adding a heat sink, the θ_{JA} is the sum of θ_{JC}, θ_{CS}, and θ_{SA}. (θ_{JC} is the junction-to-case thermal impedance, θ_{CS} is the case-to-sink thermal impedance, and θ_{SA} is the sink-to-ambient thermal impedance.) Refer to the Typical Performance Characteristics curves for power dissipation information at lower output power levels.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10µF in parallel with a 0.1µF filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0µF tantalum bypass capacitance connected between the LM4855's supply pins and ground. Keep the length of leads and traces that connect capacitors between the LM4855's power supply pin and ground as short as possible. Connecting a 1µF capacitor, C_B, between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR. The PSRR improvements increase as the bypass pin capacitor value increases. Too large, however, increases turn-on time and can compromise the amplifier's click and pop performance. The selection of bypass capacitor values, especially C_B, depends on desired PSRR requirements, click and pop performance (as explained in the section Selecting External Components) system cost, and size constraints.

SELECTING EXTERNAL COMPONENTS

Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitor (C_i in Figure 1). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using large input capacitor.

The internal input resistor (R_i) and the input capacitor (C_i) produce a high pass filter cutoff frequency that is found using Equation (9).

$$f_c = 1 / (2\pi R_i C_i) \quad (9)$$

As an example when using a speaker with a low frequency limit of 150Hz, C_i, using Equation (9) is 0.063µF. The 0.22µF C_i shown in Figure 1 allows the LM4855 to drive high efficiency, full range speaker whose response extends below 40Hz.

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Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to value of C_B, the capacitor connected to the BYPASS pin. Since C_B determines how fast the LM4855 settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the LM4855's outputs ramp to their quiescent DC voltage (nominally $V_{DD}/2$), the smaller the turn-on pop. Choosing C_B equal to 1.0µF along with a small value of C_i (in the range of 0.1µF to 0.39µF), produces a click-less and pop-less shutdown function. As discussed above, choosing C_i no larger than necessary for the desired bandwidth helps minimize clicks and pops. C_B's value should be in the range of 5 times to 7 times the value of C_i. This ensures that output transients are eliminated when power is first applied or the LM4855 resumes operation after shutdown.

Demonstration Board Layout

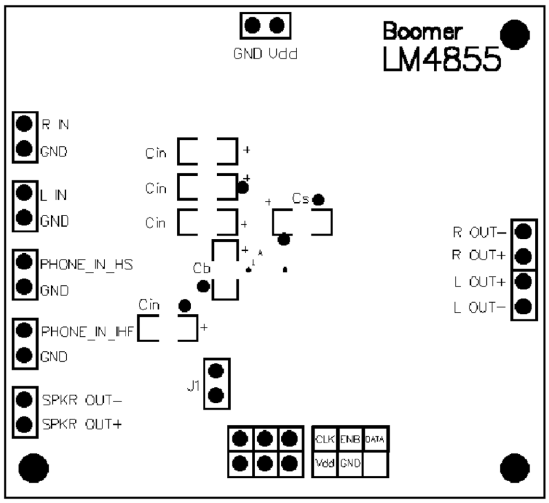

Figure 38. Recommended YZR PC Board Layout: Top Silkscreen

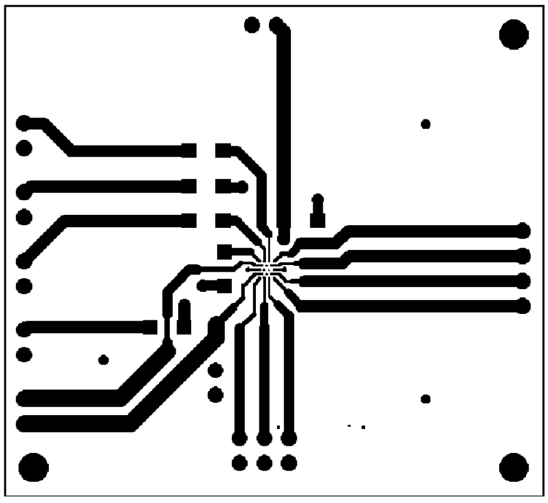

Figure 39. Recommended YZR PC Board Layout: Top Layer

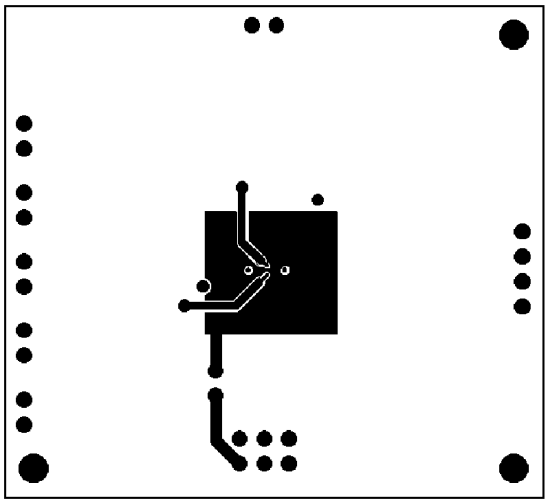

Figure 40. Recommended YZR PC Board Layout: Middle Layer

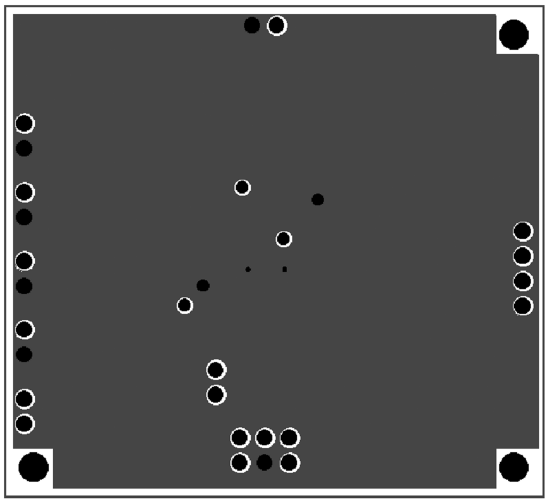

Figure 41. Recommended YZR PC Board Layout: Bottom Layer

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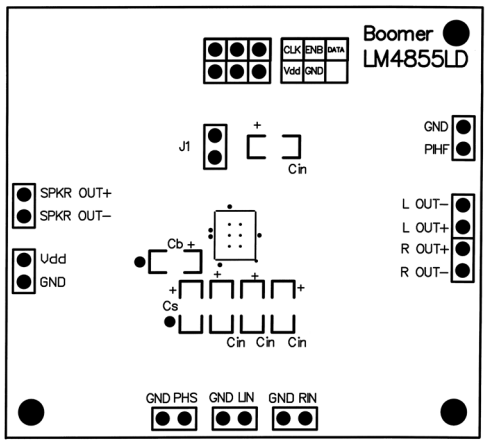

Figure 42. Recommended NHW PC Board Layout: Top Silkcreen Layer

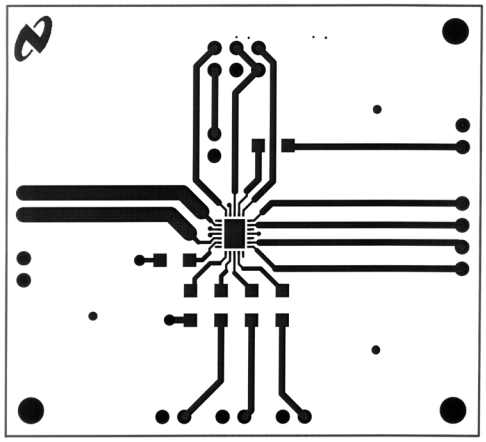

Figure 43. Recommended NHW PC Board Layout: Top Layer

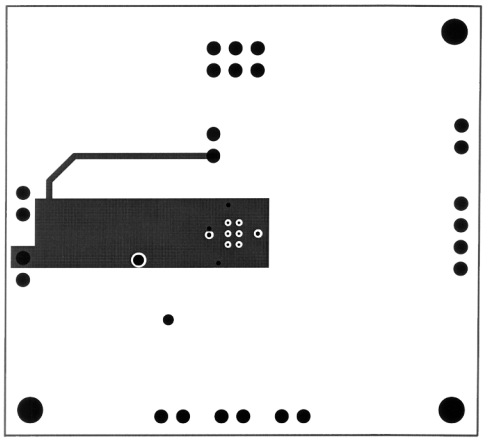

Figure 44. Recommended NHW PC Board Layout: Inner Layer 1

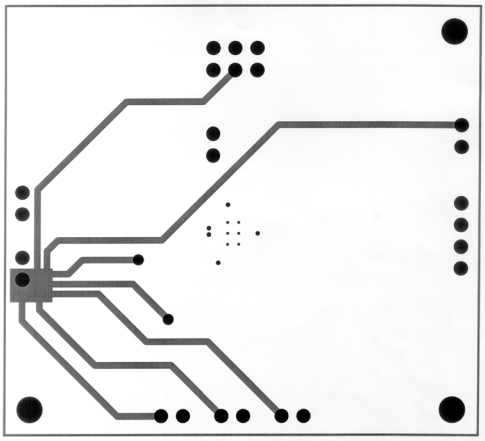

Figure 45. Recommended NHW PC Board Layout: Inner Layer 2

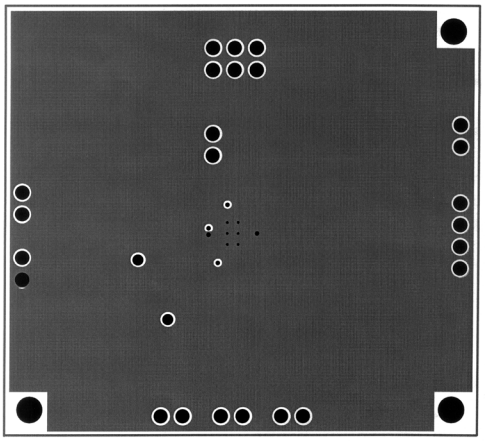

Figure 46. Recommended NHW PC Board Layout: Bottom Layer

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REVISION HISTORY

Changes from Revision B (May 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	21

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM4855LQ/NOPB	Active	Production	WQFN (NHW) | 24	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L4855LQ
LM4855LQ/NOPB.A	Active	Production	WQFN (NHW) | 24	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L4855LQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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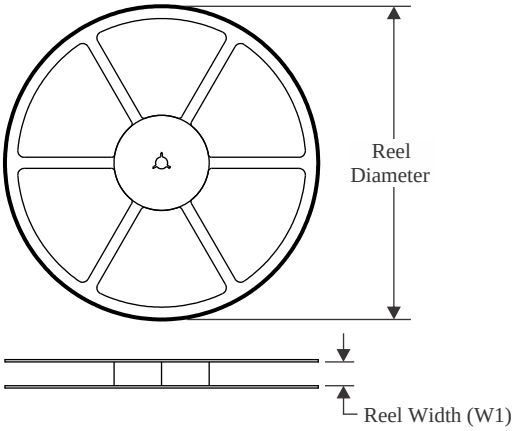
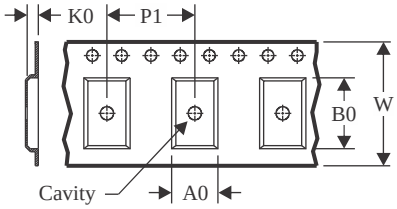
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

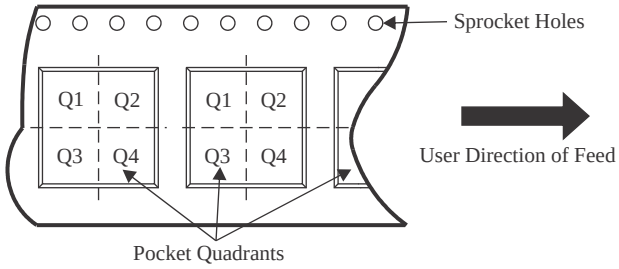


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

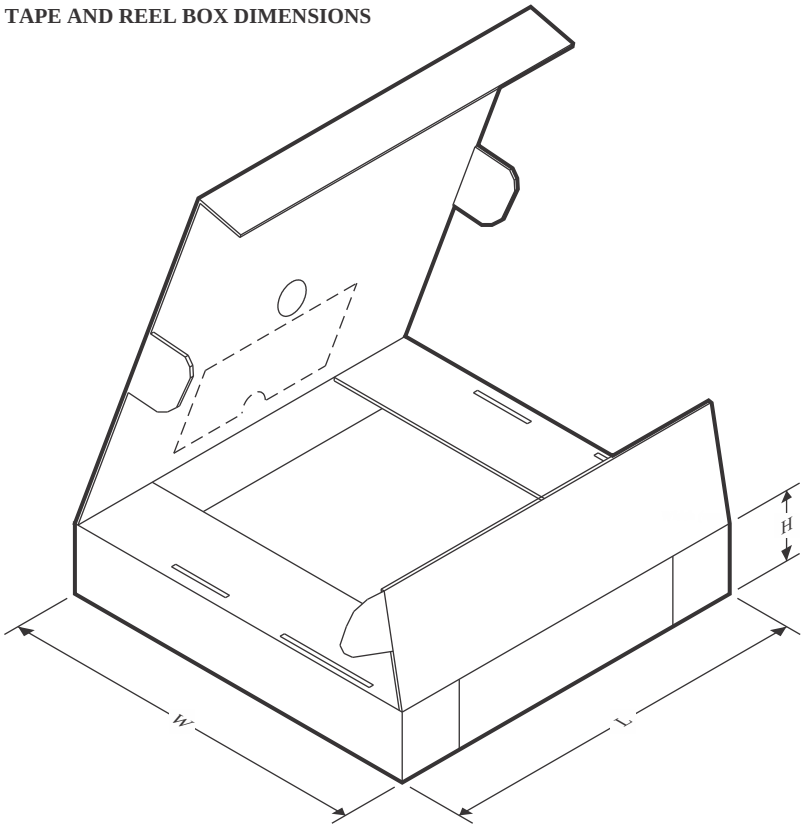
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4855LQ/NOPB	WQFN	NHW	24	1000	177.8	12.4	4.3	5.3	1.3	8.0	12.0	Q1

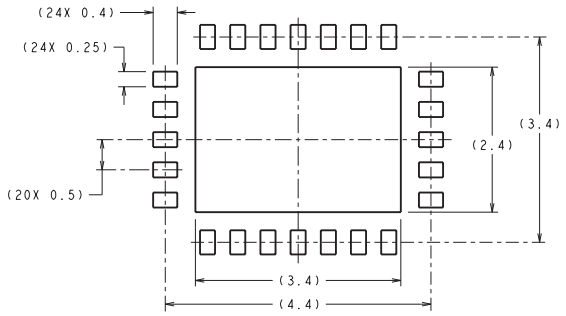
TAPE AND REEL BOX DIMENSIONS



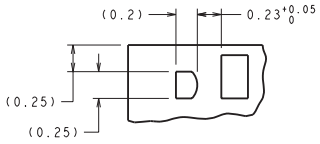
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4855LQ/NOPB	WQFN	NHW	24	1000	208.0	191.0	35.0

NHW0024B

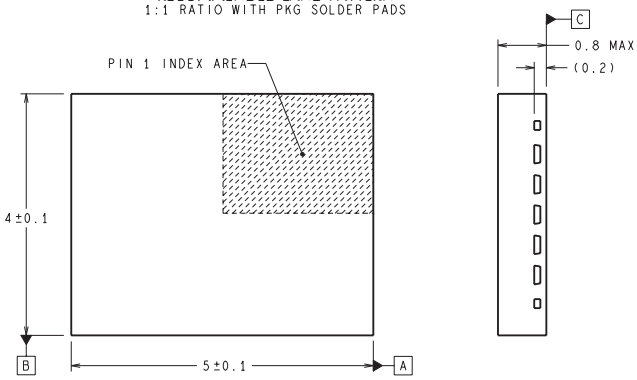


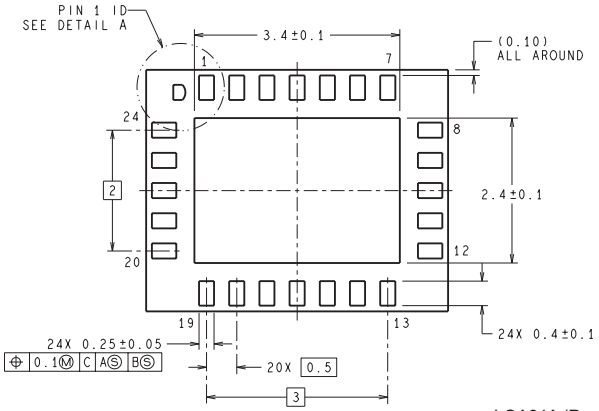
RECOMMENDED LAND PATTERN
1:1 RATIO WITH PKG SOLDER PADS



DETAIL A

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY





LQA24A (Rev B)

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