LM4863 Boomer® Audio Power Amplifier Series Dual 2.2W Audio Amplifier Plus Stereo Headphone Function

Check for Samples: LM4863

FEATURES

- **Stereo Headphone Amplifier Mode**
- **"Click and Pop" Suppression Circuitry**
- **Unity-Gain Stable**
- **Thermal Shutdown Protection Circuitry**
- **SOIC, TSSOP, exposed-DAP TSSOP, and WQFN packages**

KEY SPECIFICATIONS

- **PO at 1% THD+N**
  - **LM4863LQ, 3Ω, 4Ω loads: 2.5W(typ), 2.2W(typ)**
  - **LM4863MTE, 3Ω, 4Ω loads: 2.5W(typ), 2.2W(typ)**
  - **LM4863MTE, 8Ω load: 1.1W(typ)**
  - **LM4863, 8Ω: 1.1W(typ)**
- **Single-ended mode THD+N at 75mW into 32Ω: 0.5%(max)**
- **Shutdown current: 0.7μA(typ)**
- **Supply voltage range: 2.0V to 5.5V**

APPLICATIONS

- **Multimedia Monitors**
- **Portable and Desktop Computers**
- **Portable Televisions**

DESCRIPTION

The LM4863 is a dual bridge-connected audio power amplifier which, when connected to a 5V supply, will deliver 2.2W to a 4Ω load or 2.5W to a 3Ω load with less than 1.0% THD+N (see Notes below). In addition, the headphone input pin allows the amplifiers to operate in single-ended mode when driving stereo headphones.

Boomer audio power amplifiers were designed specifically to provide high quality output power from a surface mount package while requiring few external components. To simplify audio system design, the LM4863 combines dual bridge speaker amplifiers and stereo headphone amplifiers on one chip.

The LM4863 features an externally controlled, low-power consumption shutdown mode, a stereo headphone amplifier mode, and thermal shutdown protection. It also utilizes circuitry to reduce "clicks and pops" during device turn-on.

NOTE

An LM4863MTE or LM4863LQ that has been properly mounted to a circuit board will deliver 2.2W into 4Ω. The other package options for the LM4863 will deliver 1.1W into 8Ω. See Application Information for further information concerning the LM4863MTE and LM4863LQ.

NOTE

An LM4863MTE or LM4863LQ that has been properly mounted to a circuit board and forced-air cooled will deliver 2.5W into 3Ω.

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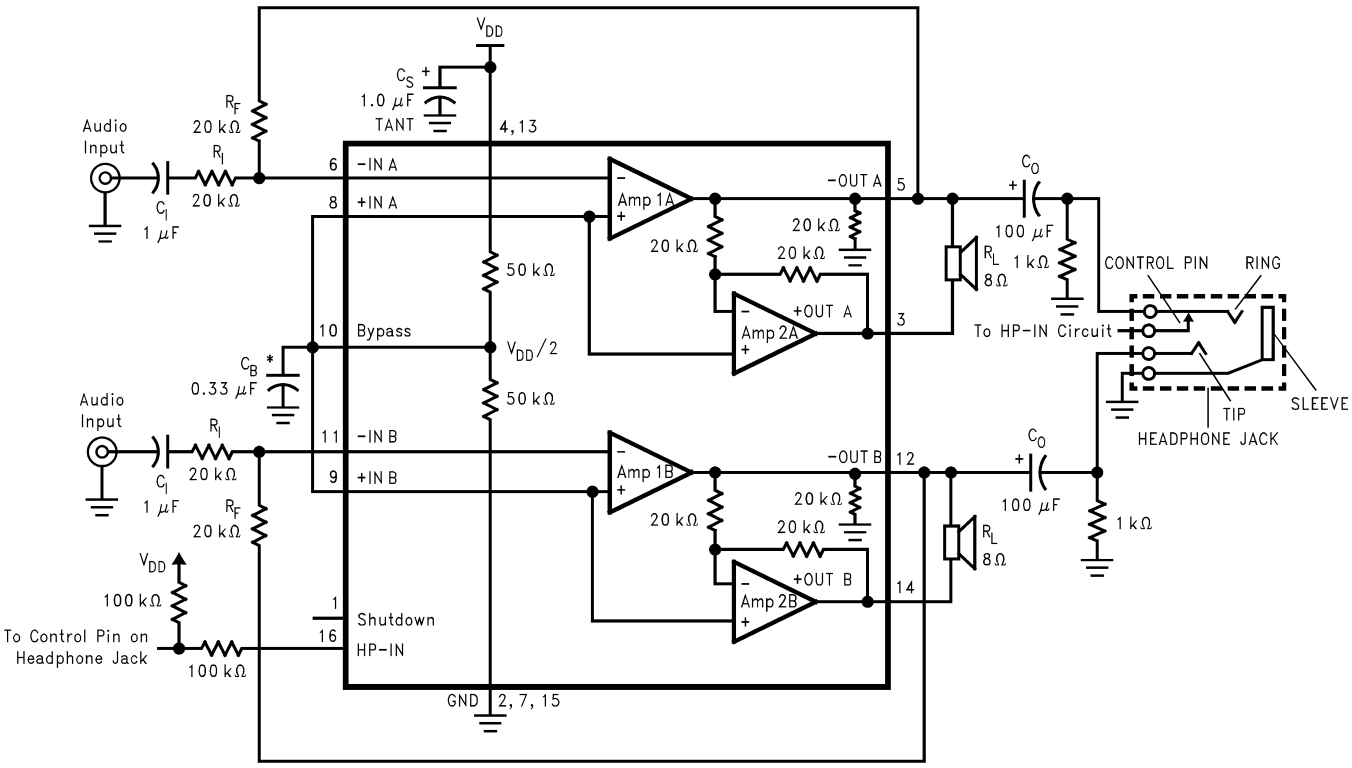
Typical Application



Note: Pin out shown for SOIC package. Refer to Connection Diagrams for the pinout of the TSSOP, Exposed-DAP TSSOP, and Exposed-DAP WQFN packages.

Connection Diagrams

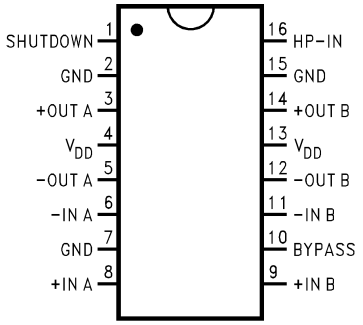


Figure 1. 16-Pin SOIC - Top View
See Package Number DW0016B

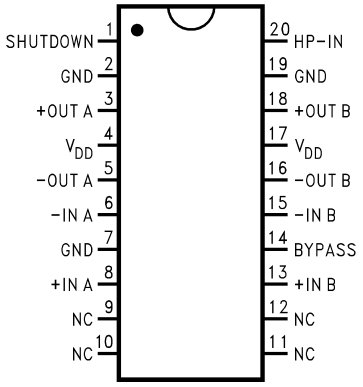


Figure 2. 20-Pin TSSOP - Top View
See Package Number PW0020A

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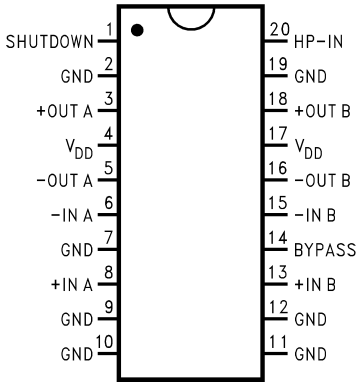

Figure 3. 20-Pin Exposed-DAP TSSOP - Top View See Package Number PWP0020A

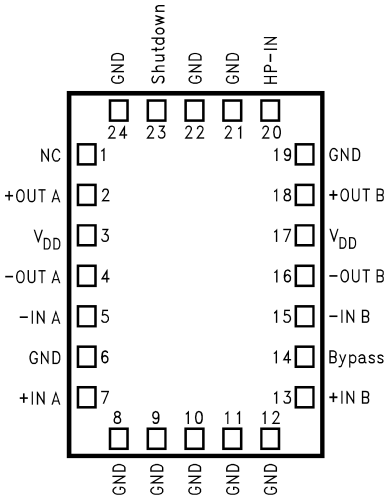

Figure 4. 24-Pin Exposed-DAP WQFN - Top View See Package Number NHW0024A

Not recommended for new designs. Contact TI Audio Marketing.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)(2)

Supply Voltage			6.0V
Storage Temperature			−65°C to +150°C
Input Voltage			−0.3V to V_{DD} +0.3V
Power Dissipation (3)			Internally limited
ESD Susceptibility (4)			2000V
ESD Susceptibility (5)			200V
Junction Temperature			150°C
Solder Information	Small Outline Package	Vapor Phase (60 sec.)	215°C
		Infrared (15 sec.)	220°C
Thermal Resistance	θ_{JC} (typ)—DW0016B		20°C/W
	θ_{JA} (typ)—DW0016B		80°C/W
	θ_{JC} (typ)—DW0020A		20°C/W
	θ_{JA} (typ)—DW0020A		80°C/W
	θ_{JC} (typ)—PWP0020A		2°C/W
	θ_{JA} (typ)—PWP0020A		41°C/W (6)
	θ_{JA} (typ)—PWP0020A		51°C/W (7)
	θ_{JA} (typ)—PWP0020A		90°C/W (8)
	θ_{JC} (typ)—NHW0024A		3.0°C/W
	θ_{JA} (typ)—NHW0024A		42°C/W (9)

(1) Not recommended for new designs. Contact Texas Insturments Audio Marketing.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The maximum power dissipation is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A and must be derated at elevated temperatures. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$. For the LM4863, T_{JMAX} = 150°C. For the θ_{JA}s for different packages, please see Application Informationor the Absolute Maximum Ratings section.
(4) Human body model, 100 pF discharged through a 1.5kΩ resistor.
(5) Machine model, 220pF – 240pF discharged through all pins.
(6) The given θ_{JA} is for an LM4863 packaged in an PWP0020A with the exposed−DAP soldered to an exposed $2in^2$ area of 1oz printed circuit board copper.
(7) The given θ_{JA} is for an LM4863 packaged in an PWP0020A with the exposed−DAP soldered to an exposed $1in^2$ area of 1oz printed circuit board copper.
(8) The given θ_{JA} is for an LM4863 packaged in an PWP0020A with the exposed-DAP not soldered to printed circuit board copper.
(9) The given θ_{JA} is for an LM4863 packaged in an NHW0024A with the exposed−DAP soldered to an exposed $2in^2$ area of 1oz printed circuit board copper.

Operating Ratings

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	−40°C ≤ T_A ≤ 85°C
Supply Voltage		2.0V ≤ V_{DD} ≤ 5.5V

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Electrical Characteristics for Entire IC (1)(2)

The following specifications apply for V_{DD}= 5V unless otherwise noted. Limits apply for T_A= 25°C.

Symbol	Parameter	Conditions	LM4863		Units (Limits)
			Typical (3)	Limit (4)	
V_{DD}	Supply Voltage			2	V (min)
				5.5	V (max)
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A (5), HP-IN = 0V	11.5	20	mA (max)
				6	mA (min)
		V_{IN} = 0V, I_O = 0A (5), HP-IN = 4V	5.8		mA
I_{SD}	Shutdown Current	V_{DD} applied to the SHUTDOWN pin	0.7	2	µA (max)
V_{IH}	Headphone High Input Voltage			4	V (min)
V_{IL}	Headphone Low Input Voltage			0.8	V (max)

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not specify specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not specified for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) All voltages are measured with respect to the ground (GND) pins unless otherwise specified.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to TI's AOQL (Average Outgoing Quality Level).
(5) The quiescent power supply current depends on the offset voltage when a practical load is connected to the amplifier.

Electrical Characteristics for Bridged-Mode Operation (1)(2)

The following specifications apply for V_{DD}= 5V unless otherwise specified. Limits apply for T_A= 25°C.

Symbol	Parameter	Conditions	LM4863		Units (Limits)
			Typical (3)	Limit (4)	
V_{OS}	Output Offset Voltage	V_{IN} = 0V	5	50	mV (max)
P_O	Output Power (5)	THD+N = 1%, f = 1kHz (6)			
		LM4863MTE, R_L = 3Ω	2.5		W
		LM4863LQ, R_L = 3Ω	2.5		W
		LM4863MTE, R_L = 4Ω	2.2		W
		LM4863LQ, R_L = 4Ω	2.2		W
		LM4863, R_L = 8Ω	1.1	1.0	W (min)
		THD+N = 10%, f = 1kHz (6)			
		LM4863MTE, R_L = 3Ω	3.2		W
		LM4863LQ, R_L = 3Ω	3.2		W
		LM4863MTE, R_L = 4Ω	2.7		W
		LM4863LQ, R_L = 4Ω	2.7		W
		LM4863, R_L = 8Ω	1.5		W
		THD+N = 1%, f = 1kHz, R_L = 32Ω	0.34		W
THD+N	Total Harmonic Distortion+Noise	20Hz ≤ f ≤ 20kHz, A_{VD} = 2	0.3 0.3		%
		LM4863MTE, R_L = 4Ω, P_O = 2W			
		LM4863LQ, R_L = 4Ω, P_O = 2W			
		LM4863, R_L = 8Ω, P_O = 1W	0.3		%
PSRR	Power Supply Rejection Ratio	V_{DD} = 5V, V_{RIPPLE} = 200mV_{RMS}, R_L = 8Ω, C_B = 1.0µF	67		dB

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not specify specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not specified for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) All voltages are measured with respect to the ground (GND) pins unless otherwise specified.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to TI's AOQL (Average Outgoing Quality Level).
(5) Output power is measured at the device terminals.
(6) When driving 3Ω or 4Ω and operating on a 5V supply, the LM4863LQ and LM4863MTE must be mounted to the circuit board that has a minimum of 2.5in^2 of exposed, uninterrupted copper area connected to the WQFN package's exposed DAP.

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Electrical Characteristics for Bridged-Mode Operation (1)(2) (continued)

The following specifications apply for V_{DD}= 5V unless otherwise specified. Limits apply for T_A= 25°C.

Symbol	Parameter	Conditions	LM4863		Units (Limits)
			Typical (3)	Limit (4)	
X_{TALK}	Channel Separation	f = 1kHz, C_B = 1.0μF	90		dB
SNR	Signal To Noise Ratio	V_{DD} = 5V, P_O = 1.1W, R_L = 8Ω	98		dB

Electrical Characteristics for Single-Ended Operation (1)(2)

The following specifications apply for V_{DD}= 5V unless otherwise specified. Limits apply for T_A= 25°C.

Symbol	Parameter	Conditions	LM4863		Units (Limits)
			Typical (3)	Limit (4)	
V_{OS}	Output Offset Voltage	V_{IN} = 0V	5	50	mV (max)
P_O	Output Power	THD+N = 0.5%, f = 1kHz, R_L = 32Ω	85	75	mW (min)
		THD+N = 1%, f = 1kHz, R_L = 8Ω	340		mW
		THD+N = 10%, f = 1kHz, R_L = 8Ω	440		mW
THD+N	Total Harmonic Distortion+Noise	A_V = −1, P_O = 75mW, 20Hz ≤ f ≤ 20kHz, R_L = 32Ω	0.2		%
PSRR	Power Supply Rejection Ratio	C_B = 1.0μF, V_{RIPPLE} = 200mV $_{RMS}$, f = 1kHz	52		dB
X_{TALK}	Channel Separation	f = 1kHz, C_B = 1.0μF	60		dB
SNR	Signal To Noise Ratio	V_{DD} = 5V, P_O = 340mW, R_L = 8Ω	95		dB

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not specify specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not specified for parameters where no limit is given, however, the typical value is a good indication of device performance.

(2) The maximum power dissipation is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A and must be derated at elevated temperatures. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$. For the LM4863, T_{JMAX} = 150°C. For the θ_{JA}s for different packages, please see Application Informationor the Absolute Maximum Ratings section.

(3) Typicals are measured at 25°C and represent the parametric norm.

(4) Limits are specified to TI's AOQL (Average Outgoing Quality Level).

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Typical Performance Characteristics- PWP Specific Characteristics

LM4863MTE THD+N vs Output Power

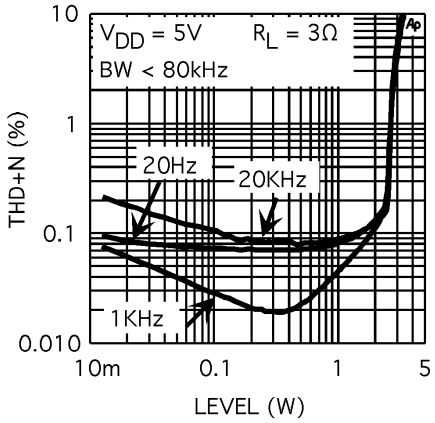


Figure 5.

LM4863MTE THD+N vs Frequency

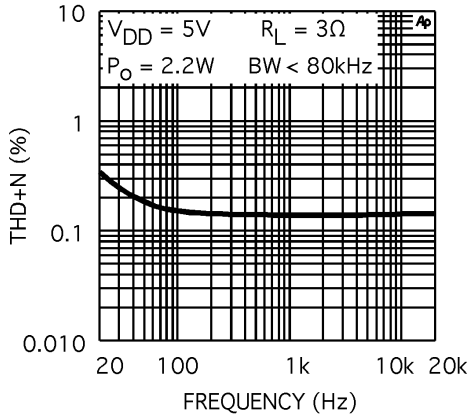


Figure 6.

LM4863MTE THD+N vs Output Power

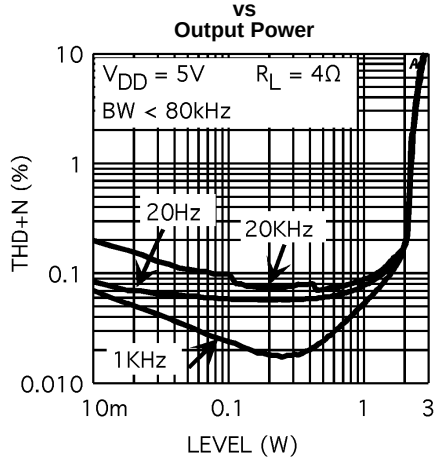


Figure 7.

LM4863MTE THD+N vs Frequency

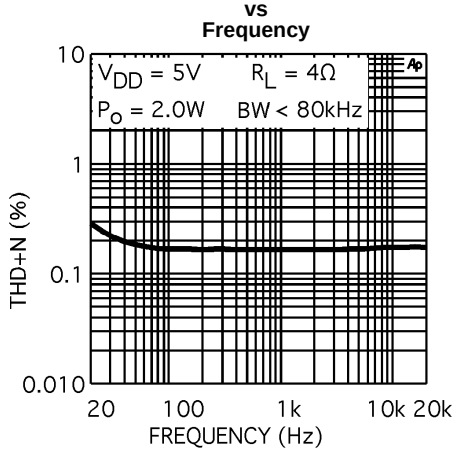


Figure 8.

LM4863MTE Power Dissipation vs Power Output

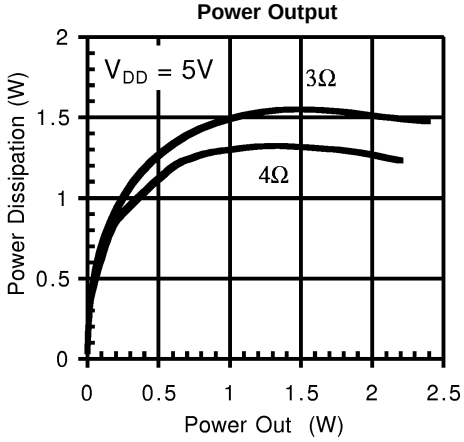


Figure 9.

LM4863MTE Power Derating Curve

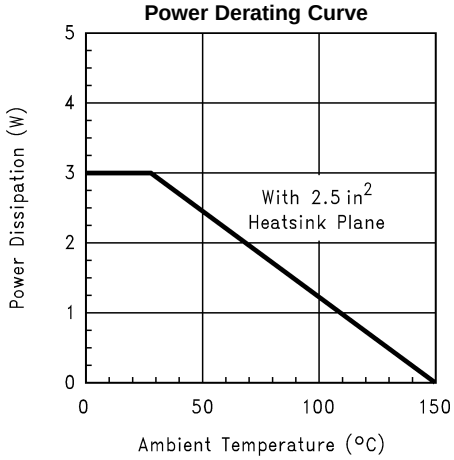
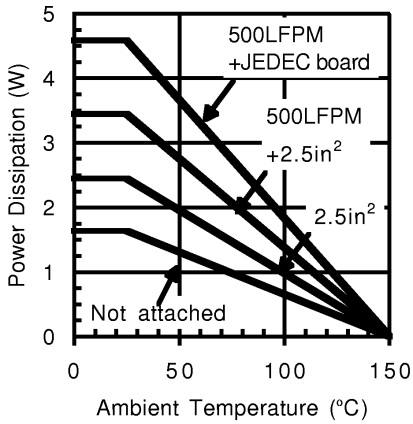


Figure 10.

Typical Performance Characteristics- PWP Specific Characteristics (continued)

LM4863MTE
Power Derating Curve



This curve shows the LM4863MTE's thermal dissipation ability at different ambient temperatures given these conditions: 500LFPM + JEDEC board: The part is soldered to a 1S2P 20-lead exposed-DAP TSSOP test board with 500 linear feet per minute of forced-air flow across it. Board information - copper dimensions: 74x74mm, copper coverage: 100% (buried layer) and 12% (top/bottom layers), 16 vias under the exposed-DAP. 500LFPM + 2.5in^2: The part is soldered to a 2.5in^2, 1 oz. copper plane with 500 linear feet per minute of forced-air flow across it. 2.5in^2: The part is soldered to a 2.5in^2, 1oz. copper plane. Not Attached: The part is not soldered down and is not forced-air cooled.

Figure 11.

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Non-PWP Specific Characteristics

THD+N vs Frequency

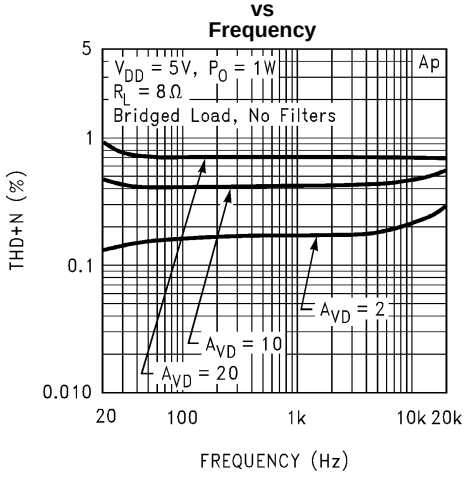

Figure 12.

THD+N vs Frequency

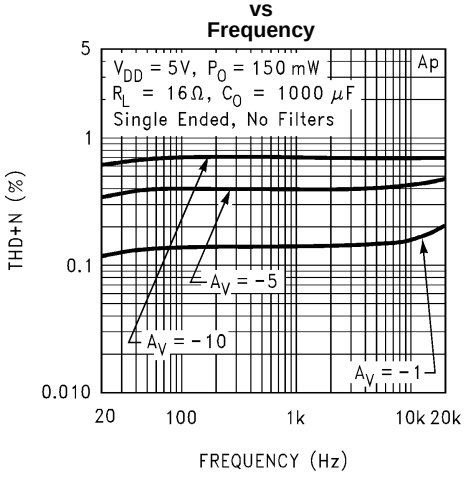

Figure 13.

THD+N vs Frequency

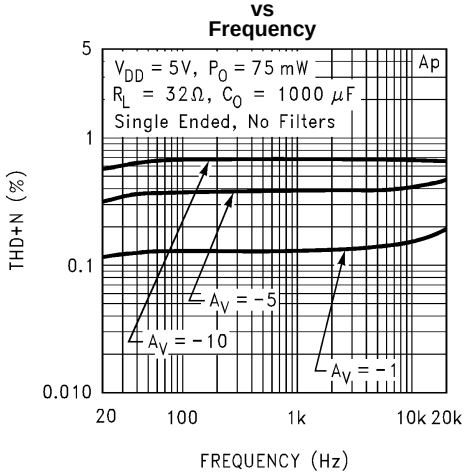

Figure 14.

THD+N vs Output Power

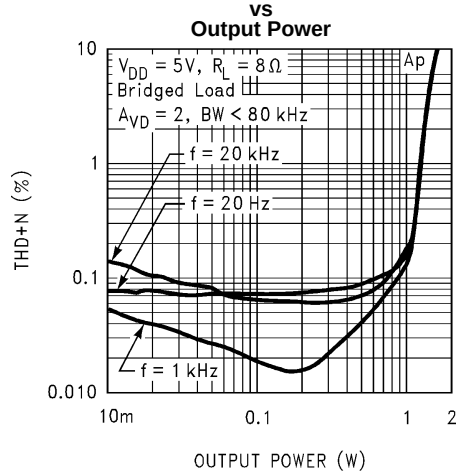

Figure 15.

THD+N vs Output Power

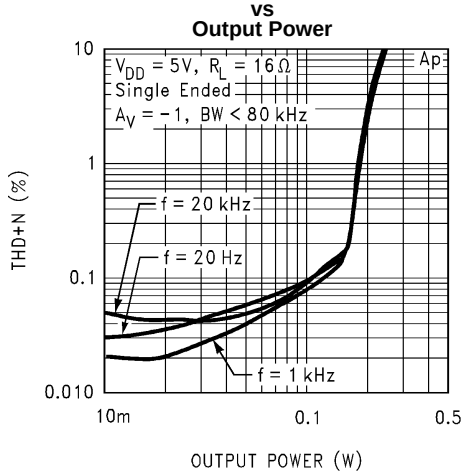

Figure 16.

THD+N vs Output Power

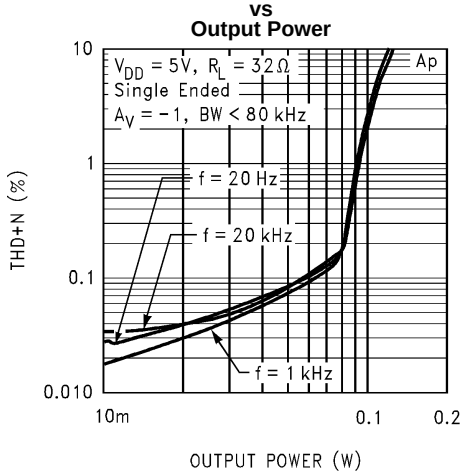

Figure 17.

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Non-PWP Specific Characteristics (continued)

THD+N vs Output Power

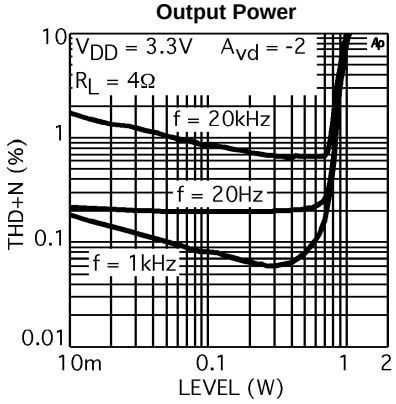

Figure 18.

THD+N vs Frequency

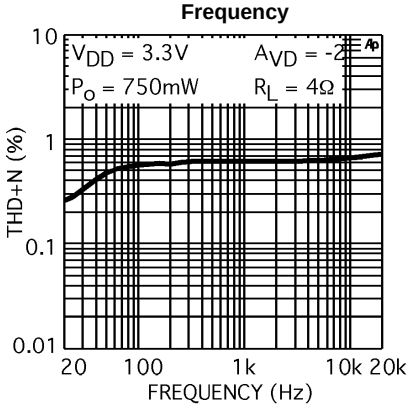

Figure 19.

THD+N vs Output Power

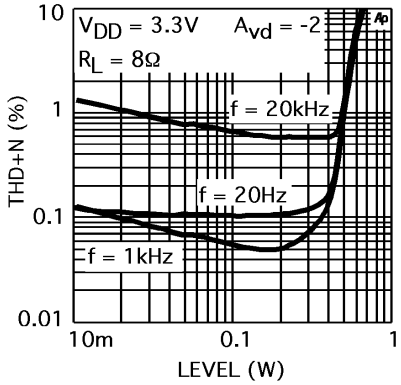

Figure 20.

THD+N vs Frequency

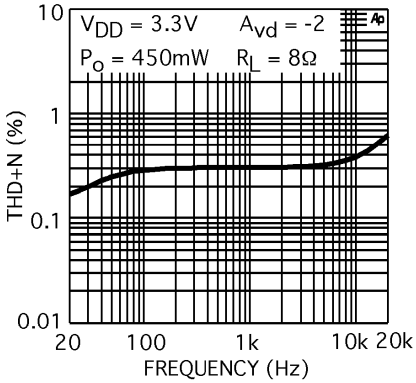

Figure 21.

Output Power vs Load Resistance

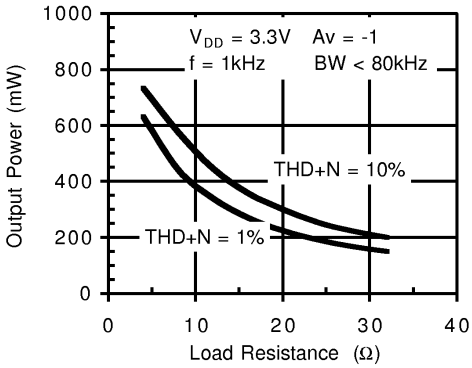

Figure 22.

Power Dissipation vs Supply Voltage

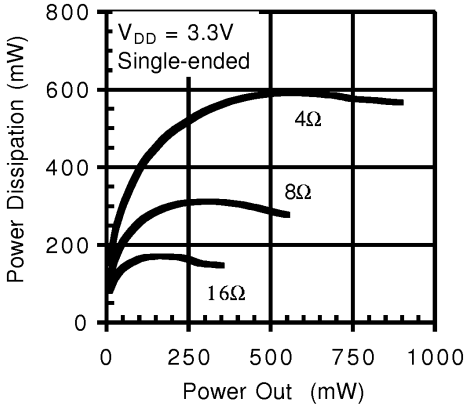

Figure 23.

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Non-PWP Specific Characteristics (continued)

Output Power vs Supply Voltage

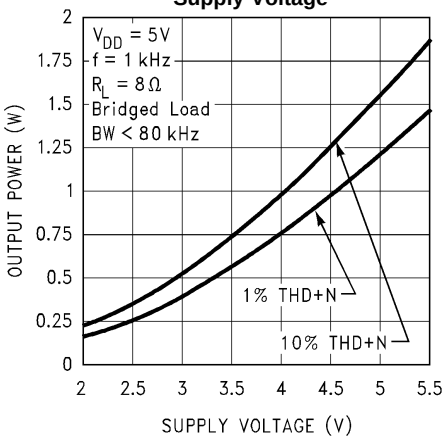

Figure 24.

Output Power vs Supply Voltage

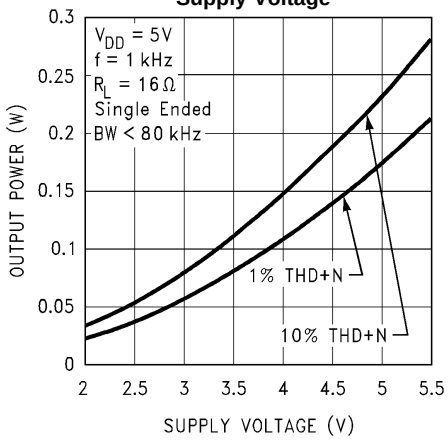

Figure 25.

Output Power vs Supply Voltage

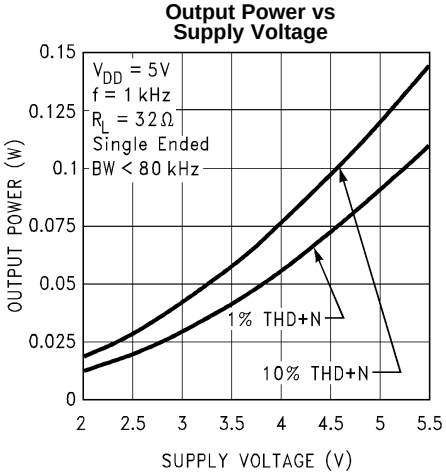

Figure 26.

Output Power vs Load Resistance

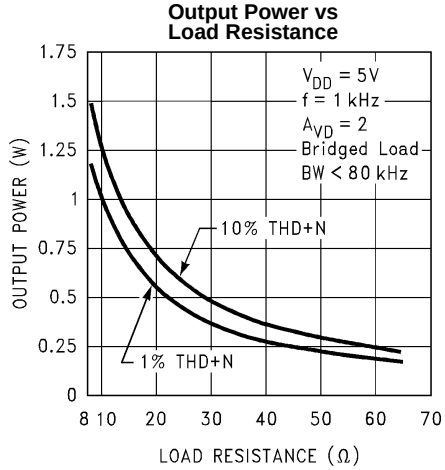

Figure 27.

Output Power vs Load Resistance

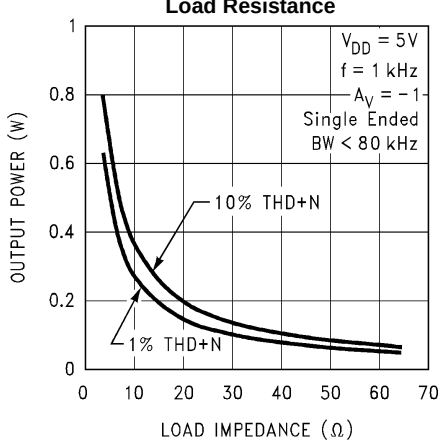

Figure 28.

Power Dissipation vs Output Power

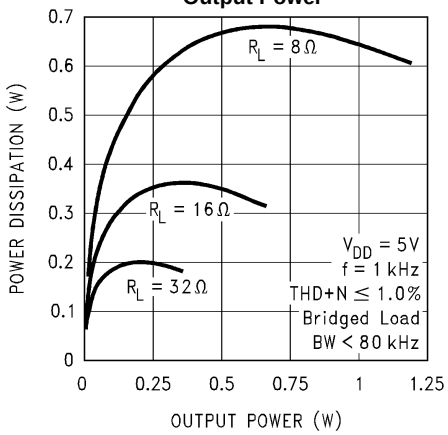

Figure 29.

Non-PWP Specific Characteristics (continued)

Dropout Voltage vs Supply Voltage

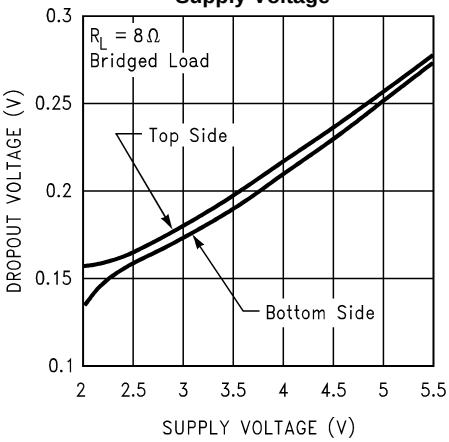

Figure 30.

Power Derating Curve

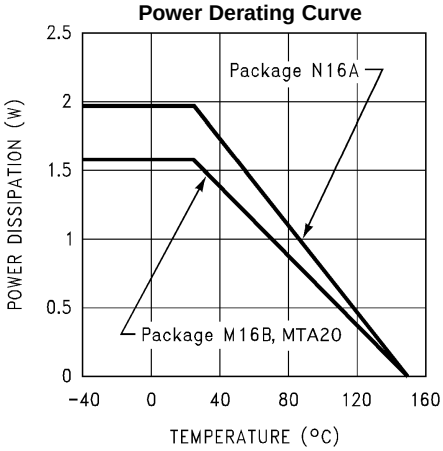

Figure 31.

Power Dissipation vs Output Power

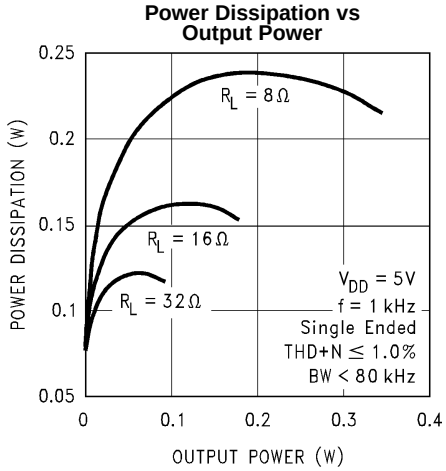

Figure 32.

Noise Floor

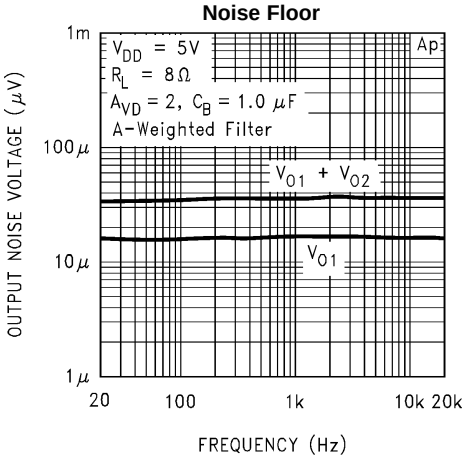

Figure 33.

Channel Separation

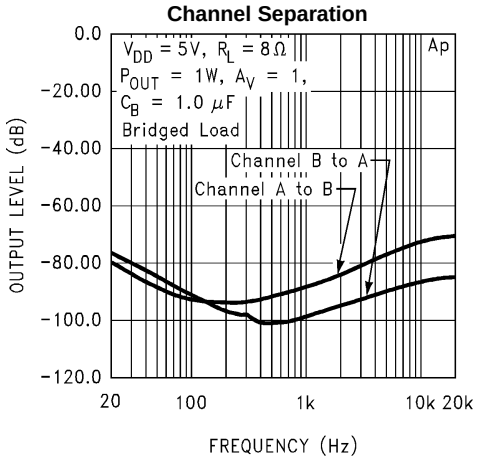

Figure 34.

Channel Separation

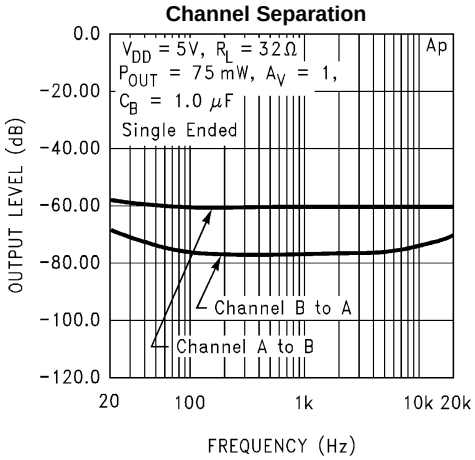

Figure 35.

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Non-PWP Specific Characteristics (continued)

Power Supply Rejection Ratio

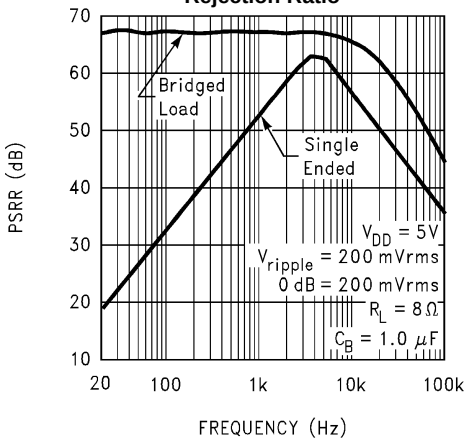

Figure 36.

Open Loop Frequency Response

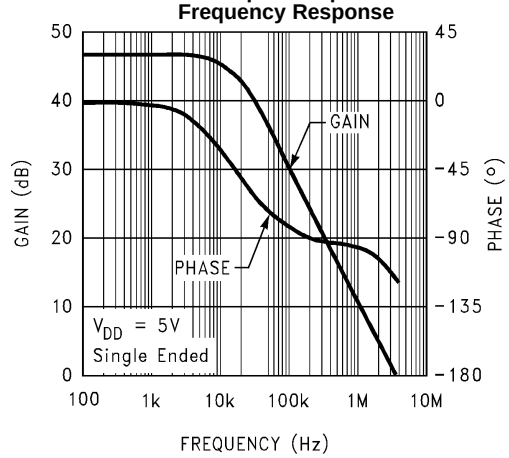

Figure 37.

Supply Current vs Supply Voltage

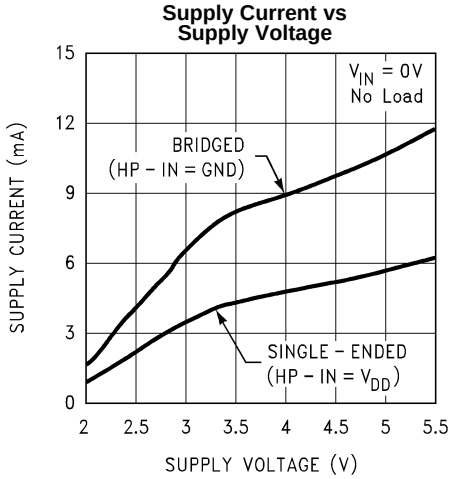

Figure 38.

External Components Description

(Refer to Figure 39.)

Components		Functional Description
1.	R_i	The Inverting input resistance, along with R_f, set the closed-loop gain. R_i, along with C_i, form a high pass filter with $f_c = 1/(2\pi R_i C_i)$.
2.	C_i	The input coupling capacitor blocks DC voltage at the amplifier's input terminals. C_i, along with R_i, create a highpass filter with $f_c = 1/(2\pi R_i C_i)$. Refer to SELECTING PROPER EXTERNAL COMPONENTS, for an explanation of determining the value of C_i.
3.	R_f	The feedback resistance, along with R_i, set the closed-loop gain.
4.	C_S	The supply bypass capacitor. Refer to POWER SUPPLY BYPASSING for information about properly placing, and selecting the value of, this capacitor.
5.	C_B	The capacitor, C_B, filters the half-supply voltage present on the BYPASS pin. Refer to SELECTING PROPER EXTERNAL COMPONENTS section for information concerning proper placement and selecting C_B's value.

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APPLICATION INFORMATION

EXPOSED-DAP PACKAGE PCB MOUNTING CONSIDERATIONS

The LM4863's exposed-DAP (die attach paddle) packages (PWP and NHW) provide a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane and, finally, surrounding air. The result is a low voltage audio power amplifier that produces 2.2W at ≤ 1% THD with a 4Ω load. This high power is achieved through careful consideration of necessary thermal design. Failing to optimize thermal design may compromise the LM4863's high power performance and activate unwanted, though necessary, thermal shutdown protection.

The PWP and NHW packages must have their DAPs soldered to a copper pad on the PCB. The DAP's PCB copper pad is connected to a large plane of continuous unbroken copper. This plane forms a thermal mass and heat sink and radiation area. Place the heat sink area on either outside plane in the case of a two-sided PCB, or on an inner layer of a board with more than two layers. Connect the DAP copper pad to the inner layer or backside copper heat sink area with 32(4x8) (PWP) or 6(3x2) (NHW) vias. The via diameter should be 0.012in - 0.013in with a 1.27mm pitch. Ensure efficient thermal conductivity by plating-through and solder-filling the vias.

Best thermal performance is achieved with the largest practical copper heat sink area. If the heatsink and amplifier share the same PCB layer, a nominal 2.5in^2 (min) area is necessary for 5V operation with a 4Ω load. Heatsink areas not placed on the same PCB layer as the LM4863 should be 5in^2 (min) for the same supply voltage and load resistance. The last two area recommendations apply for 25°c ambient temperature. Increase the area to compensate for ambient temperatures above 25°c. In systems using cooling fans, the LM4863MTE can take advantage of forced air cooling. With an air flow rate of 450 linear-feet per minute and a 2.5in^2 exposed copper or 5.0in^2 inner layer copper plane heatsink, the LM4863MTE can continuously drive a 3Ω load to full power. The LM4863LQ achieves the same output power level without forced air cooling. In all circumstances and conditions, the junction temperature must be held below 150°C to prevent activating the LM4863's thermal shutdown protection. The LM4863's power de-rating curve, Figure 31, in Non-PWP Specific Characteristics shows the maximum power dissipation versus temperature. Example PCB layouts for the exposed-DAP TSSOP and WQFN packages are shown in RECOMMENDED PRINTED CIRCUIT BOARD LAYOUT. Further detailed and specific information concerning PCB layout, fabrication, and mounting an WQFN package is available from Texas Instruments' package Engineering Group. When contacting them, ask for "Preliminary Application Note for the Assembly of the WQFN Package on a Printed Circuit Board, Revision A dated 7/14/00."

PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING 3Ω AND 4Ω LOADS

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example, 0.1Ω trace resistance reduces the output power dissipated by a 4Ω load from 2.1W to 2.0W. This problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

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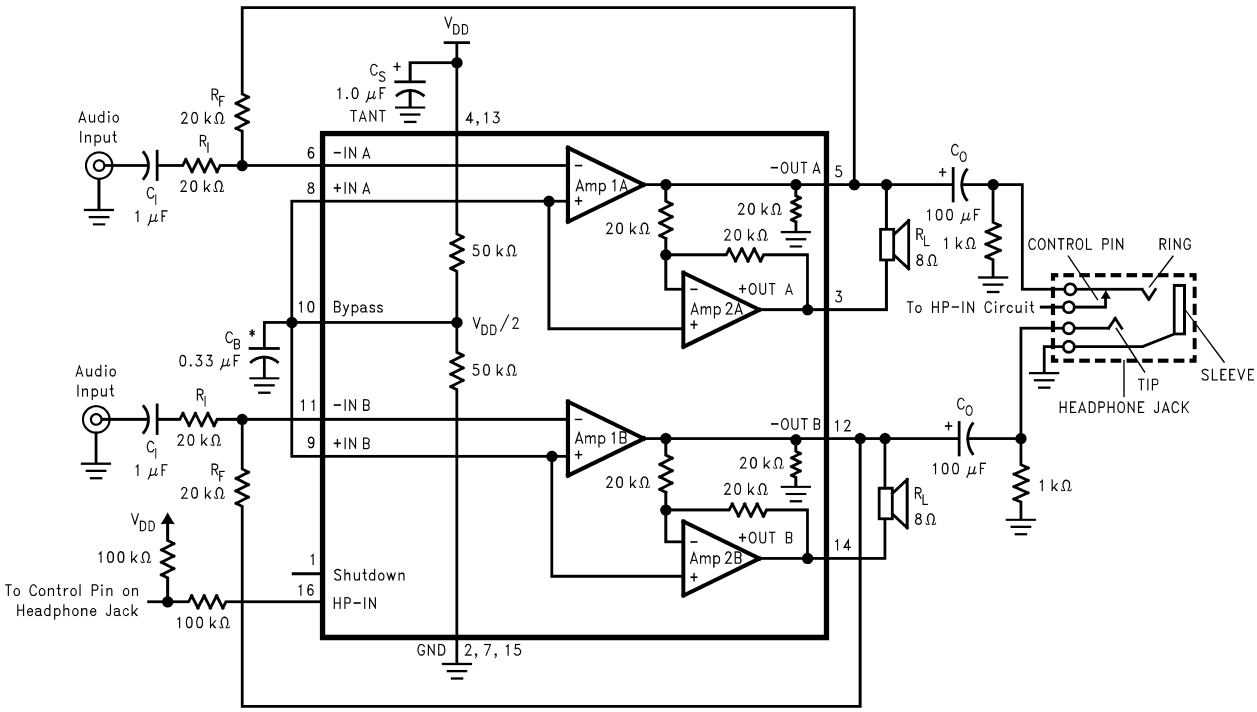

* Refer to SELECTING PROPER EXTERNAL COMPONENTS, for a detailed discussion of C_B size.
Pin out shown for the SOIC package. Refer to Connection Diagrams for the pinout of the TSSOP, Exposed-DAP TSSOP, and Exposed-DAP WQFN packages.

Figure 39. Typical Audio Amplifier Application Circuit

BRIDGE CONFIGURATION EXPLANATION

As shown in Figure 39, the LM4863 consists of two pairs of operational amplifiers, forming a two-channel (channel A and channel B) stereo amplifier. (Though the following discusses channel A, it applies equally to channel B.) External resistors R_f and R_i set the closed-loop gain of Amp1A, whereas two internal 20kΩ resistors set Amp2A's gain at -1. The LM4863 drives a load, such as a speaker, connected between the two amplifier outputs, -OUTA and +OUTA.

Figure 39 shows that Amp1A's output serves as Amp2A's input. This results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between -OUTA and +OUTA and driven differentially (commonly referred to as "bridge mode"). This results in a differential gain of

$$A_{VD} = 2 \times (R_f / R_i) \quad (1)$$

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. This produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or that the output signal is not clipped. To ensure minimum output signal clipping when choosing an amplifier's closed-loop gain, refer to AUDIO POWER AMPLIFIER DESIGN.

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing channel A's and channel B's outputs at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

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POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier. Equation 2 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load

$$P_{DMAX} = (V_{DD})^2 / (2\pi^2 R_L) \text{ Single-Ended} \quad (2)$$

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation for the same conditions.

The LM4863 has two operational amplifiers per channel. The maximum internal power dissipation per channel operating in the bridge mode is four times that of a single-ended amplifier. From Equation 3, assuming a 5V power supply and an 4Ω load, the maximum single channel power dissipation is 1.27W or 2.54W for stereo operation.

$$P_{DMAX} = 4 \times (V_{DD})^2 / (2\pi^2 R_L) \text{ Bridge Mode} \quad (3)$$

The LM4973's power dissipation is twice that given by Equation 2 or Equation 3 when operating in the single-ended mode or bridge mode, respectively. Twice the maximum power dissipation point given by Equation 3 must not exceed the power dissipation given by Equation 4:

$$P_{DMAX}' = (T_{JMAX} - T_A) / \theta_{JA} \quad (4)$$

The LM4863's T_{JMAX} = 150°C. In the NHW (WQFN) package soldered to a DAP pad that expands to a copper area of $5in^2$ on a PCB, the LM4863's θ_{JA} is 20°C/W. In the PWP package soldered to a DAP pad that expands to a copper area of $2in^2$ on a PCB , the LM4863's θ_{JA} is 41°C/W. At any given ambient temperature $T_{J\backslash A}$, use Equation 4 to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation 4 and substituting PDMAX for PDMAX' results in Equation 5. This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the LM4863's maximum junction temperature.

$$T_A = T_{JMAX} - 2 \times P_{DMAX}\, \theta_{JA} \quad (5)$$

For a typical application with a 5V power supply and an 4Ω load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 99°C for the WQFN package and 45°C for the PWP package.

$$T_{JMAX} = P_{DMAX}\, \theta_{JA} + T_A \quad (6)$$

Equation 6 gives the maximum junction temperature T_{JMAX}. If the result violates the LM4863's 150°C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases.

If the result of Equation 5 is greater than that of Equation 6, then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce θ_{JA}. The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. External, solder attached SMT heatsinks such as the Thermalloy 7106D can also improve power dissipation. When adding a heat sink, the θ_{JA} is the sum of θ_{JC}, θ_{CS}, and θ_{SA}. (θ_{JC} is the junction−to−case thermal impedance, $_{CS}$ is the case−to−sink thermal impedance, and $\theta_{SA}$is the sink−to−ambient thermal impedance.) Refer to Typical Performance Characteristics for power dissipation information at lower output power levels.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10µF in parallel with a 0.1µF filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0µF tantalum bypass capacitance connected between the LM4863's supply pins and ground. Do not substitute a ceramic capacitor for the tantalum. Doing so may cause oscillation in the output signal. Keep the length of leads and traces that connect capacitors between the LM4863's power supply pin and ground as short as possible. Connecting a 1µF capacitor, C_B, between the

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BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR. The PSRR improvements increase as the bypass pin capacitor value increases. Too large, however, increases turn-on time and can compromise amplifier's click and pop performance. The selection of bypass capacitor values, especially C_B, depends on desired PSRR requirements, click and pop performance (as explained in SELECTING PROPER EXTERNAL COMPONENTS, system cost, and size constraints.

MICRO-POWER SHUTDOWN

The voltage applied to the SHUTDOWN pin controls the LM4863's shutdown function. Activate micro-power shutdown by applying V_{DD} to the SHUTDOWN pin. When active, the LM4863's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. The logic threshold is typically $V_{DD}/2$. The low 0.7µA typical shutdown current is achieved by applying a voltage that is as near as V_{DD} as possible to the SHUTDOWN pin. A voltage thrat is less than V_{DD} may increase the shutdown current.

There are a few ways to control the micro-power shutdown. These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When using a switch, connect an external 10kΩ pull-up resistor between the SHUTDOWN pin and V_{DD}. Connect the switch between the SHUTDOWN pin and ground. Select normal amplifier operation by closing the switch. Opening the switch connects the SHUTDOWN pin to V_{DD} through the pull-up resistor, activating micro-power shutdown. The switch and resistor ensure that the SHUTDOWN pin will not float. This prevents unwanted state changes. In a system with a microprocessor or a microcontroller, use a digital output to apply the control voltage to the SHUTDOWN pin. Driving the SHUTDOWN pin with active circuitry eliminates the pull up resistor.

Table 1. Logic level truth table for SHUTDOWN and HP-IN Operation

SHUTDOWN	HP-IN PIN	OPERATIONAL MODE
Low	logic Low	Bridged amplifiers
Low	logic High	Single-Ended amplifiers
High	logic Low	Micro-power Shutdown
High	logic High	Micro-power Shutdown

HP-IN FUNCTION

Applying a voltage between 4V and V_{DD} to the LM4863's HP-IN headphone control pin turns off Amp2A and Amp2B, muting a bridged-connected load. Quiescent current consumption is reduced when the IC is in this single-ended mode.

Figure 40 shows the implementation of the LM4863's headphone control function. With no headphones connected to the headphone jack, the R1-R2 voltage divider sets the voltage applied to the HP-IN pin (pin 16) at approximately 50mV. This 50mV enables Amp1B and Amp2B, placing the LM4863's in bridged mode operation. The output coupling capacitor blocks the amplifier's half-supply DC voltage, protecting the headphones.

While the LM4863 operates in bridged mode, the DC potential across the load is essentially 0V. The HP-IN threshold is set at 4V. Therefore, even in an ideal situation, the output swing cannot cause a false single-ended trigger. Connecting headphones to the headphone jack disconnects the headphone jack contact pin from -OUTA and allows R1 to pull the HP Sense pin up to V_{DD}. This enables the headphone function, turns off Amp2A and Amp2B, and mutes the bridged speaker. The amplifier then drives the headphones, whose impedance is in parallel with resistor R2 and R3. These resistors have negligible effect on the LM4863's output drive capability since the typical impedance of headphones is 32Ω.

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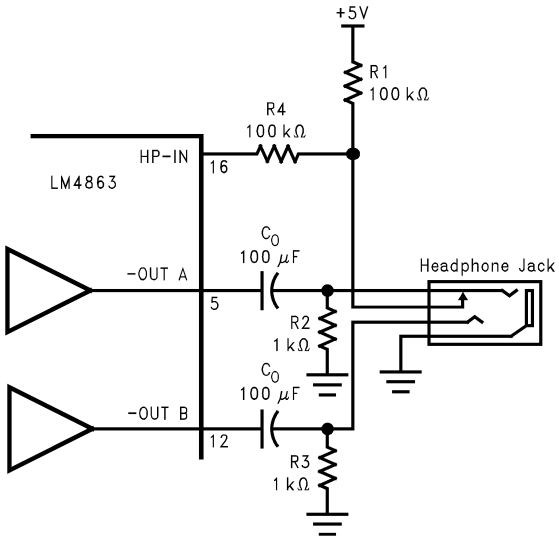

Figure 40. Headphone Circuit

Figure 40 also shows the suggested headphone jack electrical connections. The jack is designed to mate with a three-wire plug. The plug's tip and ring should each carry one of the two stereo output signals, whereas the sleeve should carry the ground return. A headphone jack with one control pin contact is sufficient to drive the HP-IN pin when connecting headphones.

A microprocessor or a switch can replace the headphone jack contact pin. When a microprocessor or switch applies a voltage greater than 4V to the HP-IN pin, a bridge-connected speaker is muted and Amp1A and Amp2A drive a pair of headphones.

SELECTING PROPER EXTERNAL COMPONENTS

Optimizing the LM4863's performance requires properly selecting external components. Though the LM4863 operates well when using external components with wide tolerances, best performance is achieved by optimizing component values.

The LM4863 is unity-gain stable, giving a designer maximum design flexibility. The gain should be set to no more than a given application requires. This allows the amplifier to achieve minimum THD+N and maximum signal-to-noise ratio. These parameters are compromised as the closed-loop gain increases. However, low gain demands input signals with greater voltage swings to achieve maximum output power. Fortunately, many signal sources such as audio CODECs have outputs of $1V_{RMS}$ ($2.83V_{P-P}$). Please refer to AUDIO POWER AMPLIFIER DESIGN for more information on selecting the proper gain.

Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitor (C_i in Figure 39). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using large input capacitor.

Besides effecting system cost and size, C_i has an affect on the LM4863's click and pop performance. When the supply voltage is first applied, a transient (pop) is created as the charge on the input capacitor changes from zero to a quiescent state. The magnitude of the pop is directly proportional to the input capacitor's size. Higher value capacitors need more time to reach a quiescent DC voltage (usually $V_{DD}/2$) when charged with a fixed current. The amplifier's output charges the input capacitor through the feedback resistor, R_f. Thus, pops can be minimized by selecting an input capacitor value that is no higher than necessary to meet the desired -3dB frequency.

A shown in Figure 39, the input resistor (R_I) and the input capacitor, C_I produce a −3dB high pass filter cutoff frequency that is found using Equation 7.

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$$f_{-3\,dB} = \frac{1}{2\pi R_{IN} C_I} \tag{7}$$

As an example when using a speaker with a low frequency limit of 150Hz, C_I, using Equation 4, is 0.063µF. The 1.0µF C_I shown in Figure 39 allows the LM4863 to drive high efficiency, full range speaker whose response extends below 30Hz.

Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to value of C_B, the capacitor connected to the BYPASS pin. Since C_B determines how fast the LM4863 settles to quiescent operation, its value is critical when minimizing turn−on pops. The slower the LM4863's outputs ramp to their quiescent DC voltage (nominally 1/2 V_{DD}), the smaller the turn−on pop. Choosing C_B equal to 1.0µF along with a small value of C_i (in the range of 0.1µF to 0.39µF), produces a click-less and pop-less shutdown function. As discussed above, choosing C_i no larger than necessary for the desired bandwidth helps minimize clicks and pops.

OPTIMIZING CLICK AND POP REDUCTION PERFORMANCE

The LM4863 contains circuitry to minimize turn-on and shutdown transients or "clicks and pop". For this discussion, turn-on refers to either applying the power supply voltage or when the shutdown mode is deactivated. While the power supply is ramping to its final value, the LM4863's internal amplifiers are configured as unity gain buffers. An internal current source changes the voltage of the BYPASS pin in a controlled, linear manner. Ideally, the input and outputs track the voltage applied to the BYPASS pin. The gain of the internal amplifiers remains unity until the voltage on the bypass pin reaches 1/2 V_{DD}. As soon as the voltage on the BYPASS pin is stable, the device becomes fully operational. Although the bypass pin current cannot be modified, changing the size of C_B alters the device's turn-on time and the magnitude of "clicks and pops". Increasing the value of C_B reduces the magnitude of turn-on pops. However, this presents a tradeoff: as the size of C_B increases, the turn-on time increases. There is a linear relationship between the size of C_B and the turn-on time. Here are some typical turn-on times for various values of C_B:

C_B	T_{ON}
0.01µF	20 ms
0.1µF	200 ms
0.22µF	440 ms
0.47µF	940 ms
1.0µF	2 Sec

In order eliminate "clicks and pops", all capacitors must be discharged before turn-on. Rapidly switching V_{DD} may not allow the capacitors to fully discharge, which may cause "clicks and pops". In a single-ended configuration, the output is coupled to the load by C_{OUT}. This capacitor usually has a high value. C_{OUT} discharges through internal 20kΩ resistors. Depending on the size of C_{OUT}, the discharge time constant can be relatively large. To reduce transients in single-ended mode, an external 1kΩ - 5kΩ resistor can be placed in parallel with the internal 20kΩ resistor. The tradeoff for using this resistor is increased quiescent current.

NO LOAD STABILITY

The LM4863 may exhibit low level oscillation when the load resistance is greater than 10kΩ. This oscillation only occurs as the output signal swings near the supply voltages. Prevent this oscillation by connecting a 5kΩ between the output pins and ground.

AUDIO POWER AMPLIFIER DESIGN

Audio Amplifier Design: Driving 1W into an 8Ω Load

The following are the desired operational parameters:

Power Output:	1Wrms
Load Impedance:	8Ω
Input Level:	1Vrms
Input Impedance:	20kΩ

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Bandwidth:	100Hz−20 kHz ± 0.25 dB

The design begins by specifying the minimum supply voltage necessary to obtain the specified output power. One way to find the minimum supply voltage is to use Figure 24, Figure 25, and Figure 26 in Typical Performance Characteristics. Another way, usingEquation 4, is to calculate the peak output voltage necessary to achieve the desired output power for a given load impedance. To account for the amplifier's dropout voltage, two additional voltages, based on Figure 30 in Typical Performance Characteristics, must be added to the result obtained by Equation 8. The result in Equation 8.

$$V_{opeak} = \sqrt{(2R_LP_O)} \tag{8}$$

$$V_{DD} \geq (V_{OUTPEAK} + (V_{ODTOP} + V_{ODBOT})) \tag{9}$$

Figure 24 for an 8Ω load indicates a minimum supply voltage of 4.6V. This is easily met by the commonly used 5V supply voltage. The additional voltage creates the benefit of headroom, allowing the LM4863 to produce peak output power in excess of 1W without clipping or other audible distortion. The choice of supply voltage must also not create a situation that violates maximum power dissipation as explained above in POWER DISSIPATION.

After satisfying the LM4863's power dissipation requirements, the minimum differential gain is found using Equation 10.

$$A_{VD} \geq \sqrt{(P_OR_L)}/(V_{IN}) = V_{orms}/V_{inrms} \tag{10}$$

Thus, a minimum gain of 2.83 allows the LM4863's to reach full output swing and maintain low noise and THD+N performance. For this example, let A_{VD} = 3.

The amplifier's overall gain is set using the input (R_i) and feedback (R_f) resistors. With the desired input impedance set at 20kΩ, the feedback resistor is found using Equation 11.

$$R_f/R_i = A_{VD}/2 \tag{11}$$

The value of R_f is 30kΩ.

The last step in this design example is setting the amplifier's −3dB frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one−fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the ±0.25dB desired limit. The results are an

$$f_L = 100Hz/5 = 20Hz \tag{12}$$

and an

$$F_H = 20kHz \times 5 = 100kHz \tag{13}$$

As mentioned in SELECTING PROPER EXTERNAL COMPONENTS, R_i and C_i create a highpass filter that sets the amplifier's lower bandpass frequency limit. Find the coupling capacitor's value usingEquation 14.

$$C_i \geq \frac{1}{2\pi R_i f_c} \tag{14}$$

the result is

$$1/(2\pi*20k\Omega*20Hz) = 0.398\mu F \tag{15}$$

Use a 0.39µF capacitor, the closest standard value.

The product of the desired high frequency cutoff (100kHz in this example) and the differential gain, A_{VD}, determines the upper passband response limit. With A_{VD} = 3 and f_H = 100kHz, the closed-loop gain bandwidth product (GBWP) is 300kHz. This is less than the LM4863's 3.5MHz GBWP. With this margin, the amplifier can be used in designs that require more differential gain while avoiding performance-restricting bandwidth limitations.

RECOMMENDED PRINTED CIRCUIT BOARD LAYOUT

Figure 41 through Figure 44 show the recommended two-layer PC board layout that is optimized for the 20-pin PWP-packaged LM4863 and associated external components. Figures 7 through 11 show the recommended four-layer PC board layout that is optimized for the 24-pin NHW-packaged LM4863 and associated external components. These circuits are designed for use with an external 5V supply and 4Ω speakers.

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These circuit boards are easy to use. Apply 5V and ground to the board's V_{DD} and GND pads, respectively. Connect 4Ω speakers between the board's -OUTA and +OUTA and OUTB and +OUTB pads.

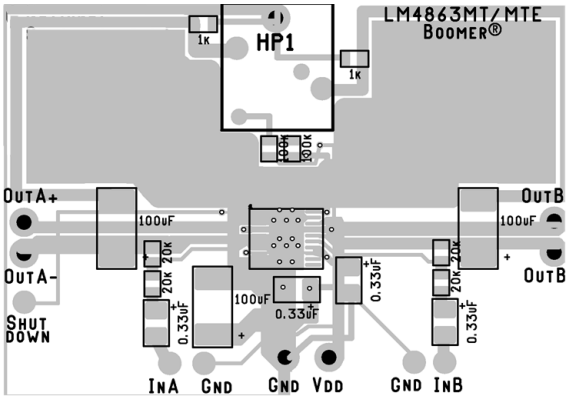

Figure 41. PWP PC board layout: all layers superimposed

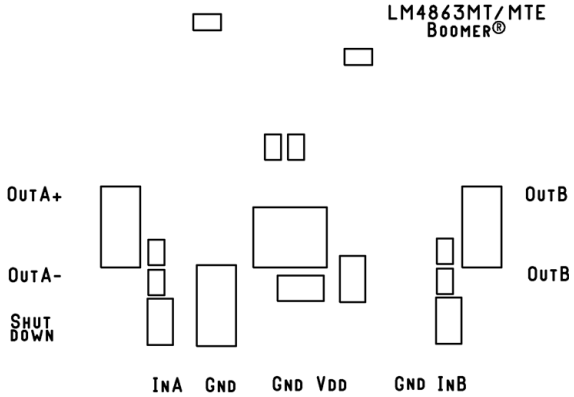

Figure 42. PWP PC board layout: Component-side Silkscreen

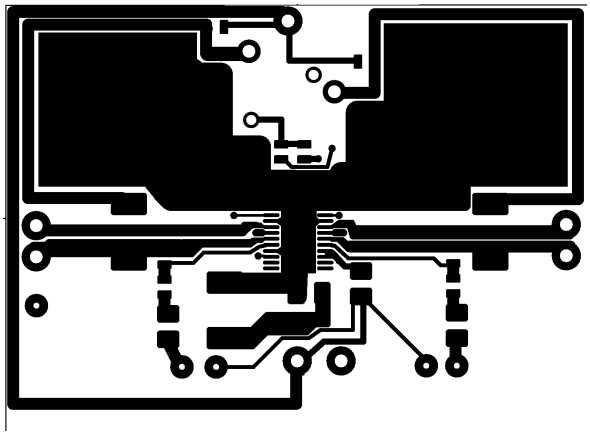

Figure 43. Recommended PWP PC board layout: Component-side layout

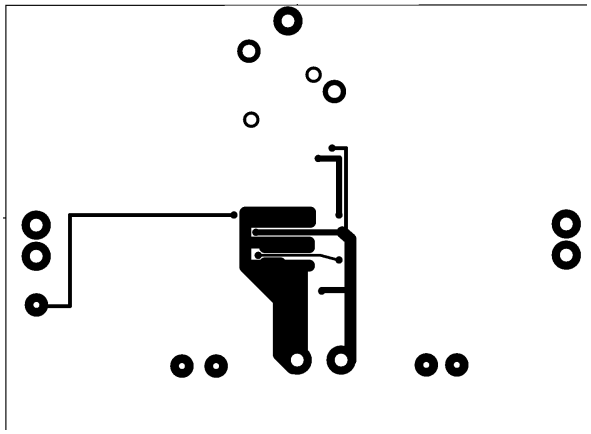

Figure 44. Recommended PWP PC board layout: bottom-side layout

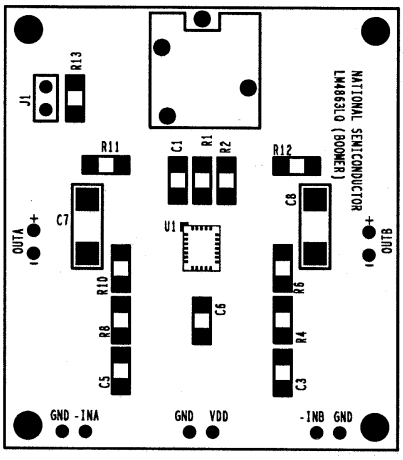

Figure 45. Recommended NHW PC board layout: Component-side Silkscreen

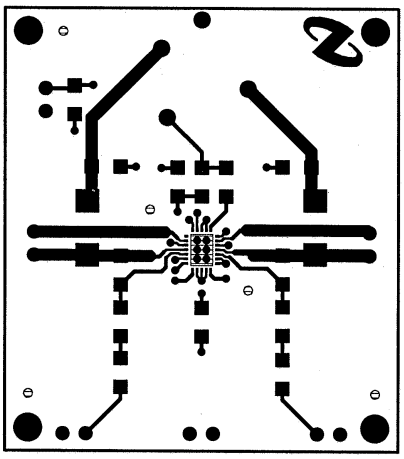

Figure 46. Recommended NHW PC board layout: Component-side layout

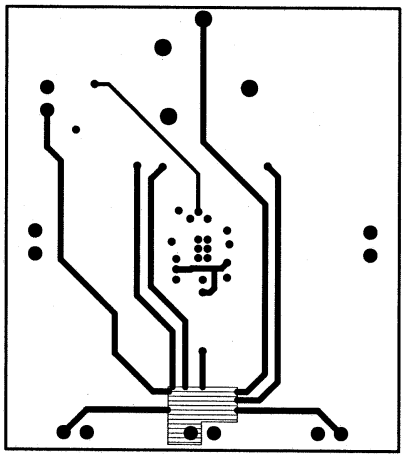

Figure 48. Recommended NHW PC board layout: lower inner-layer layout

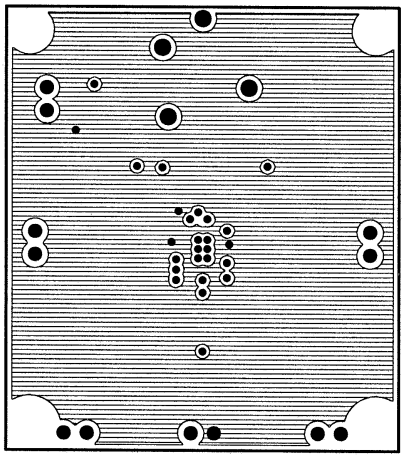

Figure 47. Recommended NHW PC board layout: upper inner-layer layout

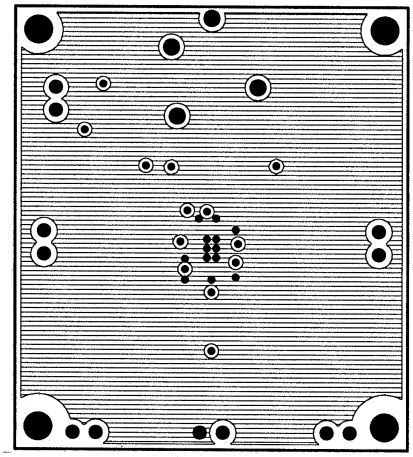

Figure 49. Recommended NHW PC board layout: bottom-side layout

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REVISION HISTORY

Rev	Date	Description
1.1	10/30/06	Removed all references to the 16–lead plastic-PDIP package.
F	5/2/2013	Changed layout of National Data Sheet to TI format

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM4863LQ/NOPB	Active	Production	WQFN (NHW) | 24	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L4863
LM4863LQ/NOPB.A	Active	Production	WQFN (NHW) | 24	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	L4863

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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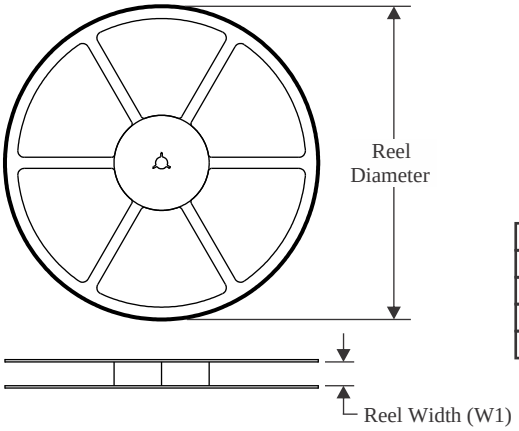
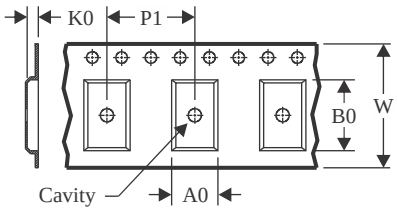
TAPE AND REEL INFORMATION

REEL DIMENSIONS

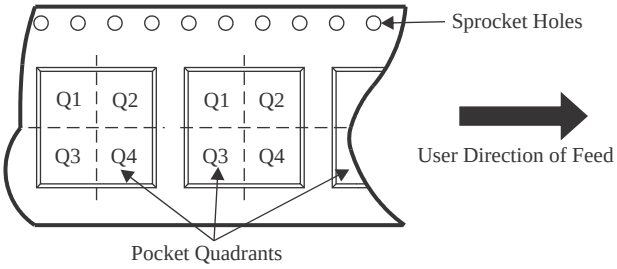


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

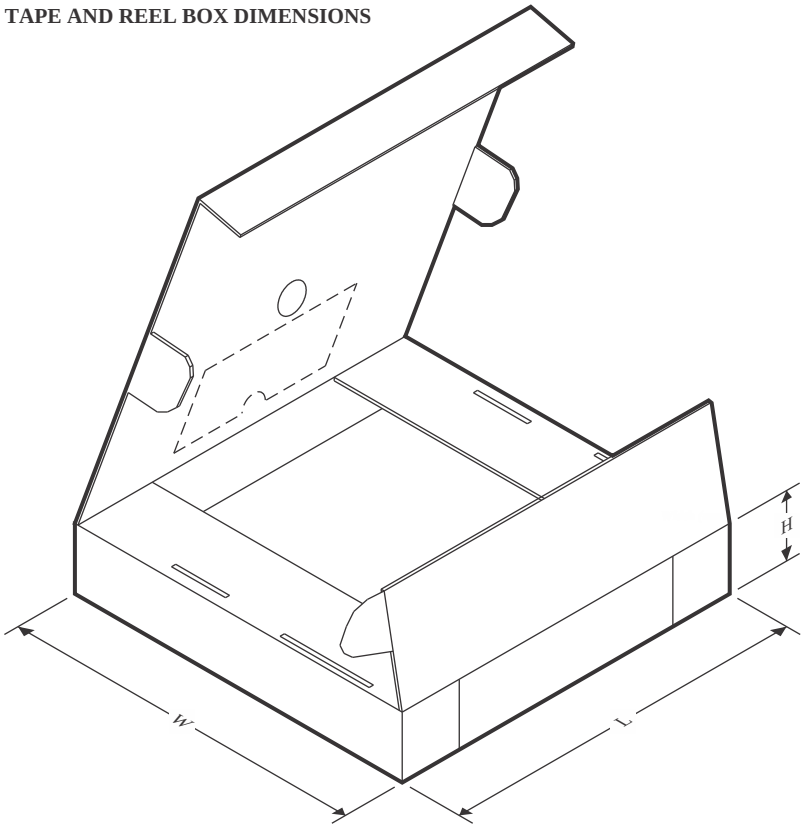
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4863LQ/NOPB	WQFN	NHW	24	1000	177.8	12.4	4.3	5.3	1.3	8.0	12.0	Q1

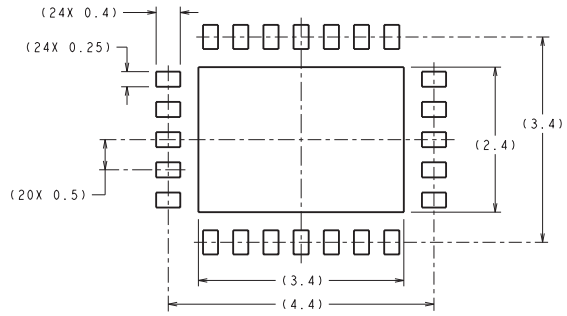
TAPE AND REEL BOX DIMENSIONS



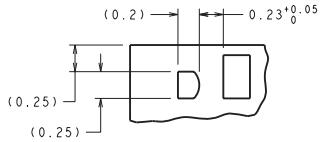
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4863LQ/NOPB	WQFN	NHW	24	1000	208.0	191.0	35.0

NHW0024B

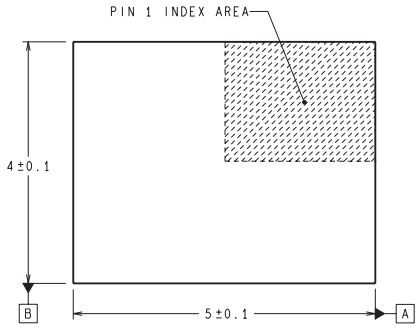


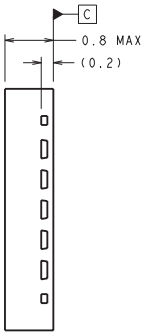
RECOMMENDED LAND PATTERN
1:1 RATIO WITH PKG SOLDER PADS

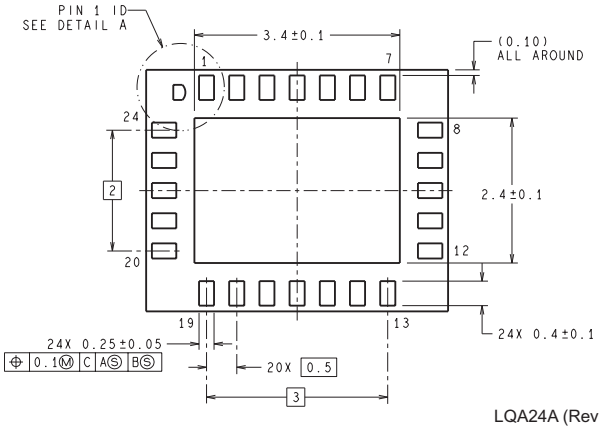


DETAIL A

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY







LQA24A (Rev B)

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