LM4881 Boomer® Audio Power Amplifier Series Dual 200 mW Headphone Amplifier with Shutdown Mode

Check for Samples: LM4881

FEATURES

- **VSSOP Surface Mount Packaging**
- **Unity-gain Stable**
- **External Gain Configuration Capability**
- **Thermal Shutdown Protection Circuitry**
- **No Bootstrap Capacitors, or Snubber Circuits are Necessary**

APPLICATIONS

- **Headphone Amplifier**
- **Personal Computers**
- **Microphone Preamplifier**

KEY SPECIFICATIONS

- **THD+N at 1kHz at 125mW Continuous Average Output Power into 8Ω 0.1% (max)**
- **THD+N at 1kHz at 75mW Continuous 0.02% (typ)**
- **Output Power at 10% THD+N at 1kHz into 8Ω 300 mW (typ)**
- **Shutdown Current 0.7μA (typ)**
- **Supply Voltage Range 2.7V to 5.5 V**

DESCRIPTION

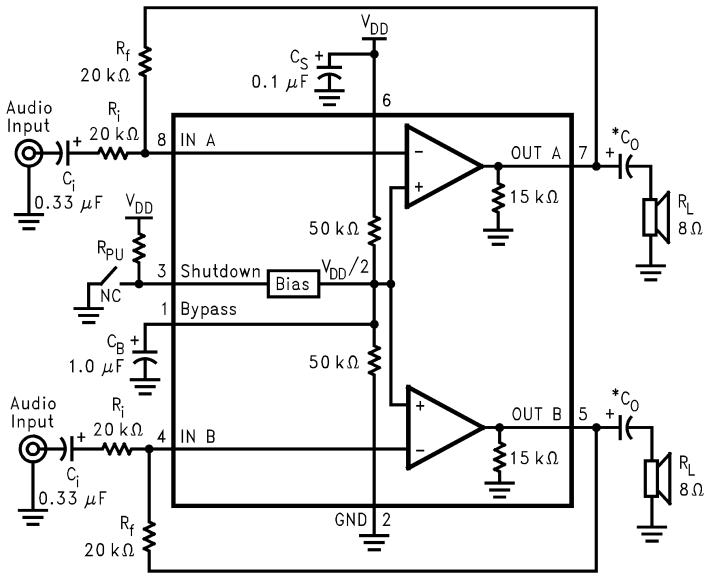
The LM4881 is a dual audio power amplifier capable of delivering 200mW of continuous average power into an 8Ω load with 0.1% THD+N from a 5V power supply.

Boomer™ audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components using surface mount packaging. Since the LM4881 does not require bootstrap capacitors or snubber networks, it is optimally suited for low-power portable systems.

The LM4881 features an externally controlled, low power consumption shutdown mode which is virtually clickless and popless, as well as an internal thermal shutdown protection mechanism.

The unity-gain stable LM4881 can be configured by external gain-setting resistors.

Typical Application



*Refer to Application Information for information concerning proper selection of the input and output coupling capacitors.

Figure 1. Typical Audio Amplifier Application Circuit

Connection Diagrams

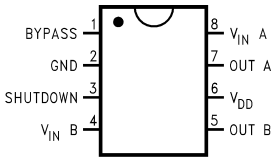


Figure 2. VSSOP Package
Top View
See Package Number DGK0008A

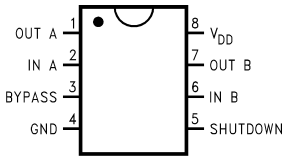


Figure 3. SOIC and PDIP Package
Top View
See Package Number D0008A, or P0008E

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage			6.0V
Storage Temperature			−65°C to +150°C
Input Voltage			−0.3V to V_{DD} + 0.3V
Power Dissipation[3]			Internally limited
ESD Susceptibility[4]			2000V
ESD Susceptibility[5]			200V
Junction Temperature			150°C
Soldering Information	Small Outline Package	Vapor Phase (60 seconds)	215°C
		Infrared (15 seconds)	220°C
Thermal Resistance		θ_{JC} (VSSOP)	56°C/W
		θ_{JA} (VSSOP)	210°C/W
		θ_{JC} (SOIC)	35°C/W
		θ_{JA} (SOIC)	170°C/W
		θ_{JC} (PDIP)	37°C/W
		θ_{JA} (PDIP)	107°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$. For the LM4881, T_{JMAX} = 150°C, and the typical junction-to-ambient thermal resistance, when board mounted, is 210°C/W for the VSSOP Package and 107°C/W for package P0008E.
(4) Human body model, 100 pF discharged through a 1.5 kΩ resistor.
(5) Machine Model, 220 pF–240 pF discharged through all pins.

Operating Ratings

Temperature Range $T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le 85°C$
Supply Voltage	$2.7V \le V_{DD} \le 5.5V$

Electrical Characteristics[1][2]

The following specifications apply for V_{DD} = 5V unless otherwise specified. Limits apply for T_A = 25C.

Symbol	Parameter	Conditions	LM4881		Units (Limits)
			Typ[3]	Limit[4]	
V_{DD}	Power Supply Voltage			2.7	V (min)
				5.5	V (max)
I_{DD}	Quiescent Current	V_{IN} = 0V, I_O = 0A	3.6	6.0	mA (max)
I_{SD}	Shutdown Current	$V_{PIN1} = V_{DD}$	0.7	5	µA (max)
V_{OS}	Offset Voltage	V_{IN} = 0V	5	50	mV (max)

(1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Limits are specified to TI's AOQL (Average Outgoing Quality Level).

Electrical Characteristics[1][2] (continued)

The following specifications apply for V_{DD} = 5V unless otherwise specified. Limits apply for T_A = 25C.

Symbol	Parameter	Conditions	LM4881		Units (Limits)
			Typ[3]	Limit[4]	
P_O	Output Power	THD = 0.1% (max); f = 1 kHz;			
		R_L = 8Ω	200	125	mW (min)
		R_L = 16Ω	150		mW
		R_L = 32Ω	85		mW
		THD + N = 10%; f = 1 kHz;			
		R_L = 8Ω	300		mW
		R_L = 16Ω	200		mW
		R_L = 32Ω	110		mW
THD+N	Total Harmonic Distortion + Noise	R_L = 16Ω, P_O = 120 mWrms;	0.025		%
		R_L = 32Ω, P_O = 75 mWrms; f = 1 kHz	0.02		%
PSRR		C_B = 1.0 µF, V_{RIPPLE} = 200 mVrms, f = 120Hz	50		dB
I_{DD}	Quiescent Current	V_{IN} = 0V, I_O = 0A	1.1		mA
I_{SD}	Shutdown Current	V_{PIN1} = V_{DD}	0.7		µA
V_{OS}	Offset Voltage	V_{IN} = 0V	5		mV
P_O	Output Power	THD = 1% (max); f = 1 kHz;			
		R_L = 8Ω	70		mW
		R_L= 16Ω	65		mW
		R_L = 32Ω	30		mW
		THD + N = 10%; f = 1 kHz;			
		R_L = 8Ω	95		mW
		R_L = 16Ω	65		mW
		R_L = 32Ω	35		mW
THD+N	Total Harmonic Distortion + Noise	R_L = 16Ω, P_O = 60 mWrms;	0.2		%
		R_L = 32Ω, P_O = 25 mWrms; f = 1 kHz	0.03		%
PSRR	Power Supply Rejection Ratio	C_B = 1.0 µF, V_{RIPPLE} = 200 mVrms, f = 100 Hz	50		dB

External Components Description

(Figure 1)

Components	Functional Description
1. R_i	Inverting input resistance which sets the closed-loop gain in conjuction with R_f. This resistor also forms a high pass filter with C_i at $f_c = 1 / (2\pi R_i C_i)$.
2. C_i	Input coupling capacitor which blocks the DC voltage at the amplifier's input terminals. Also creates a highpass filter with R_i at $f_c = 1 / (2\pi R_i C_i)$. Refer to the section, Proper Selection of External Components, for an explanation of how to determine the value of C_i.
3. R_f	Feedback resistance which sets closed-loop gain in conjuction with R_i.
4. C_S	Supply bypass capacitor which provides power supply filtering. Refer to the Application Information section for proper placement and selection of the supply bypass capacitor.
5. C_B	Bypass pin capacitor which provides half-supply filtering. Refer to the section, Proper Selection of External Components, for information concerning proper placement and selection of C_B.
6. C_O	Output coupling capacitor which blocks the DC voltage at the amplifier's output. Forms a high pass filter with R_L at $f_O = 1/(2\pi R_L C_O)$

Typical Performance Characteristics

THD+N vs Frequency

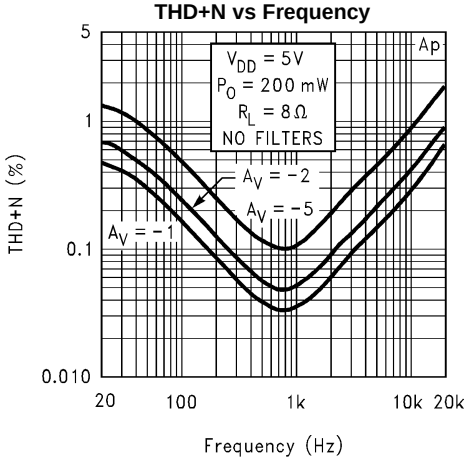


Figure 4.

THD+N vs Frequency

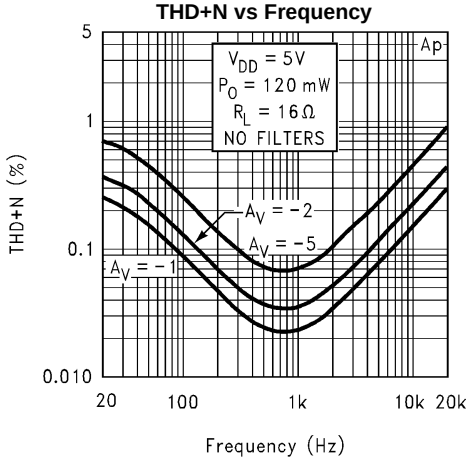


Figure 5.

THD+N vs Frequency

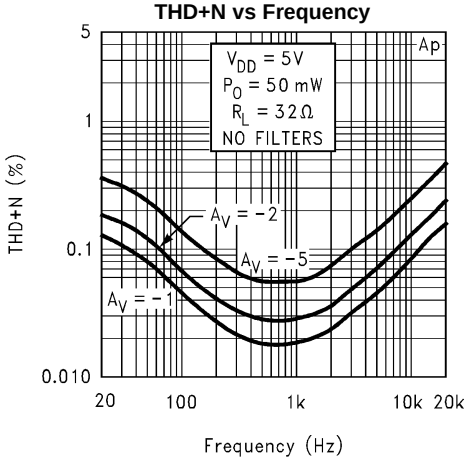


Figure 6.

THD+N vs Frequency

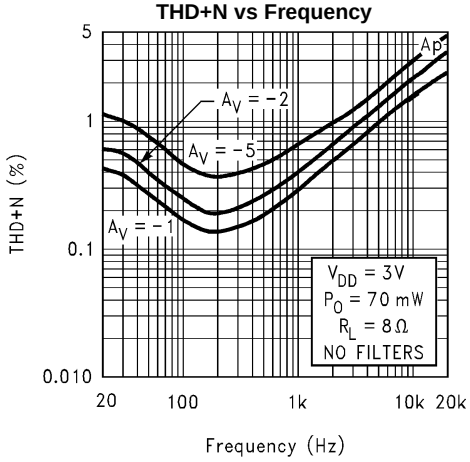


Figure 7.

THD+N vs Frequency

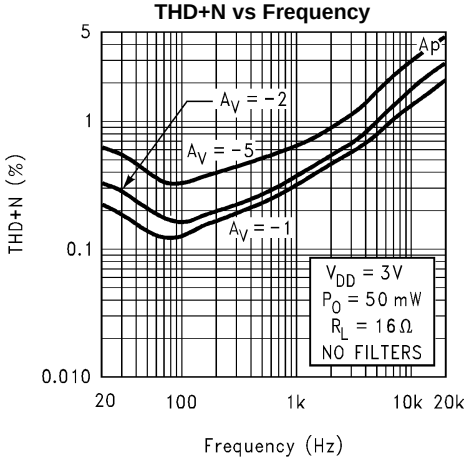


Figure 8.

THD+N vs Frequency

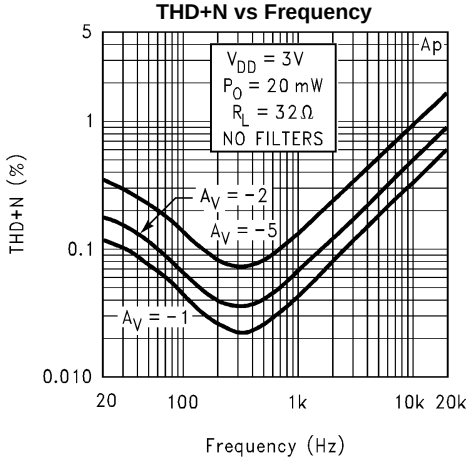


Figure 9.

Typical Performance Characteristics (continued)

THD+N vs Output Power

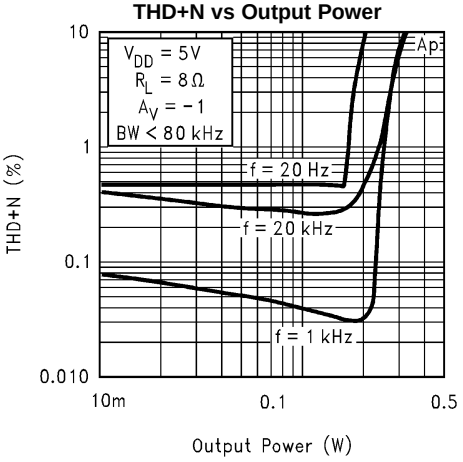


Figure 10.

THD+N vs Output Power

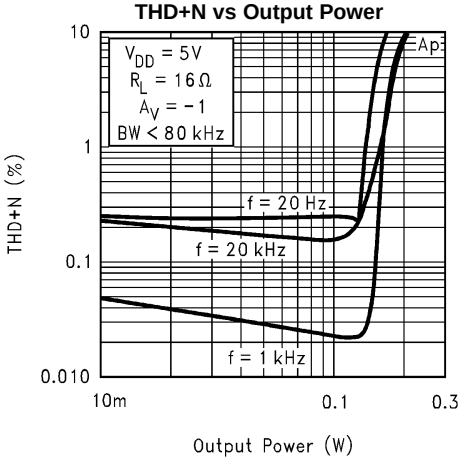


Figure 11.

THD+N vs Output Power

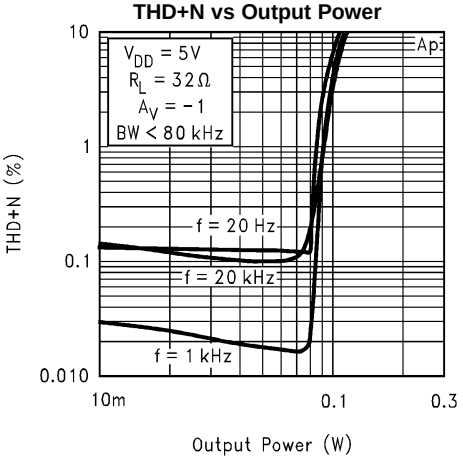


Figure 12.

THD+N vs Output Power

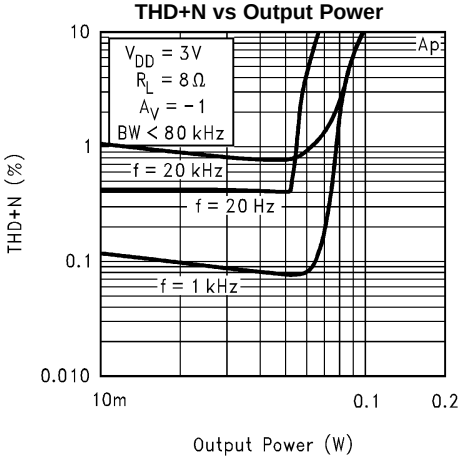


Figure 13.

THD+N vs Output Power

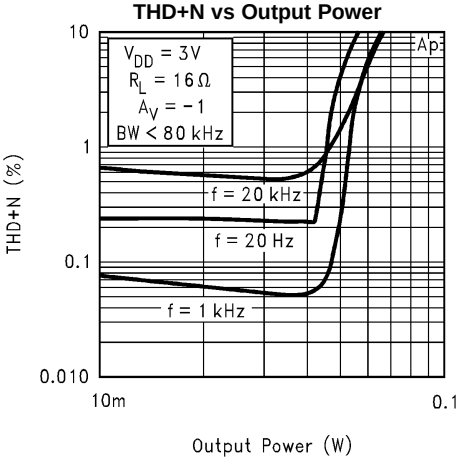


Figure 14.

THD+N vs Output Power

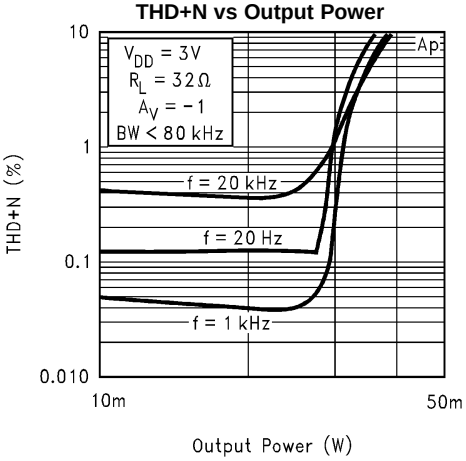


Figure 15.

Typical Performance Characteristics (continued)

Output Power vs Supply Voltage

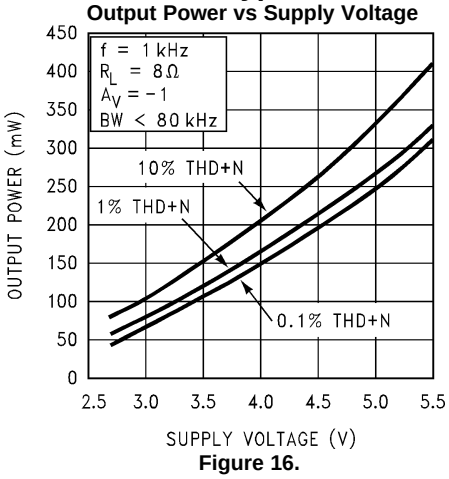


Figure 16.

Output Power vs Supply Voltage

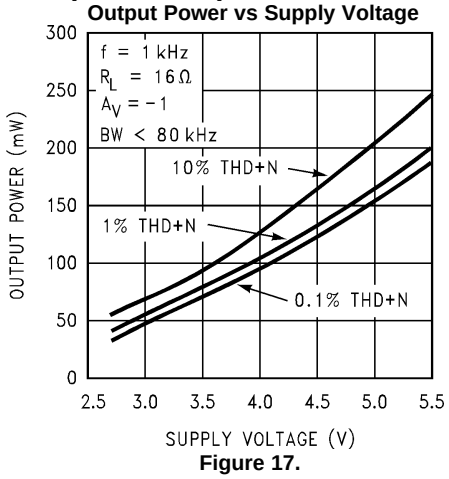


Figure 17.

Output Power vs Supply Voltage

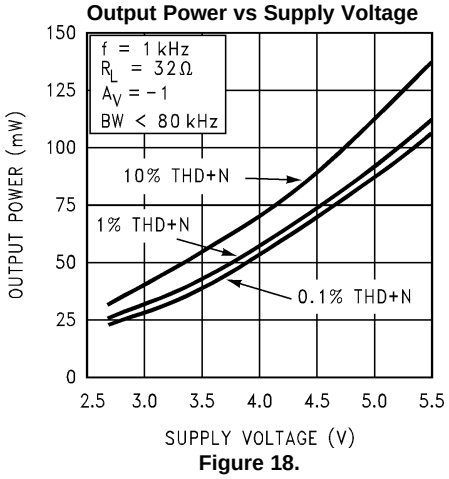


Figure 18.

Power Dissipation vs Output Power

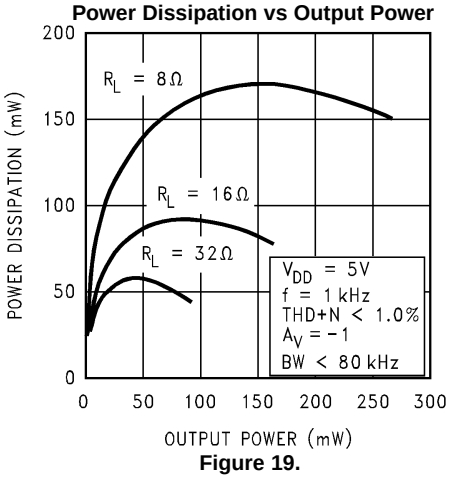


Figure 19.

Output Power vs Load Resistance

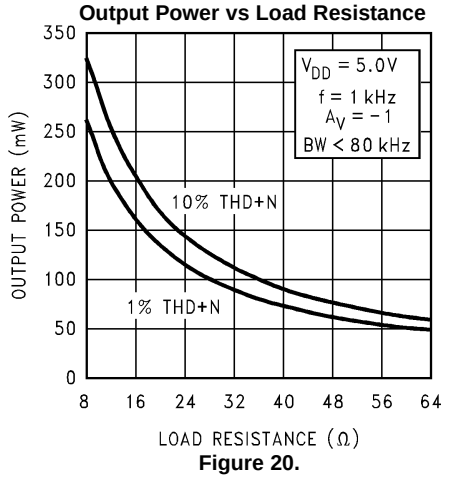


Figure 20.

Output Power vs Load Resistance

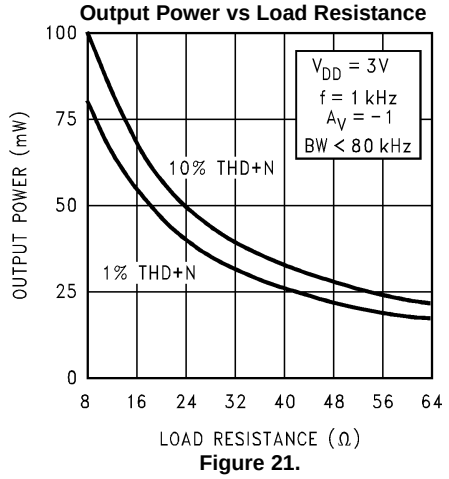


Figure 21.

Typical Performance Characteristics (continued)

Power Dissipation vs Output Power

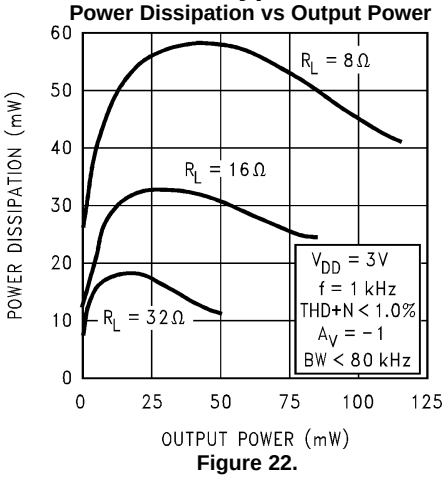


Figure 22.

Clipping Voltage vs Supply Voltage

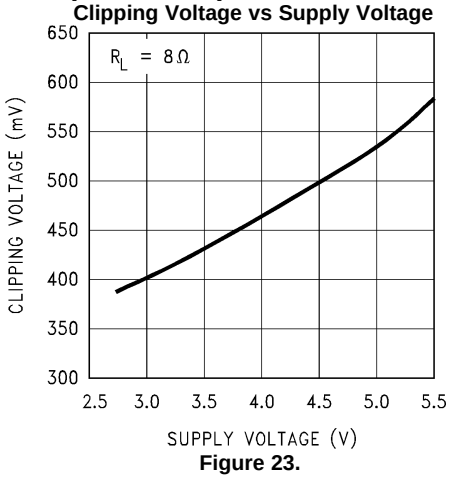


Figure 23.

Clipping Voltage vs Supply Voltage

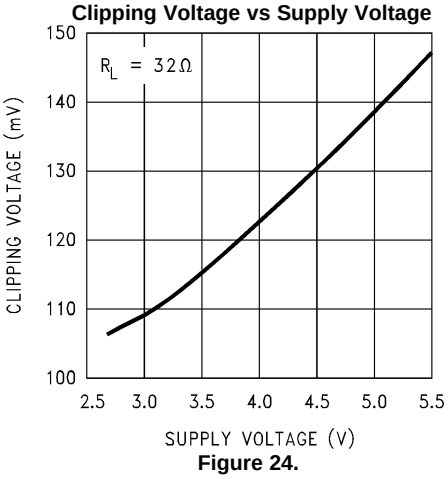


Figure 24.

Channel Separation

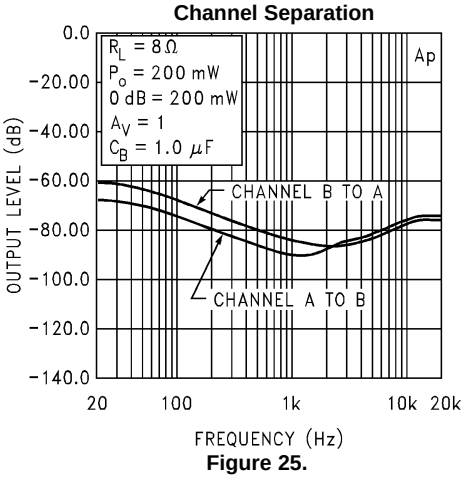


Figure 25.

Output Attenuation in Shutdown Mode

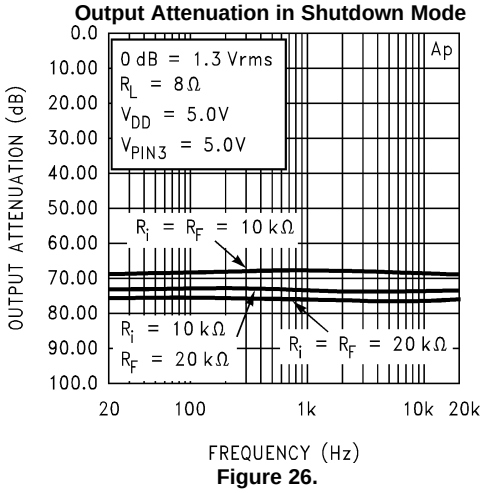


Figure 26.

Supply Current vs Supply Voltage

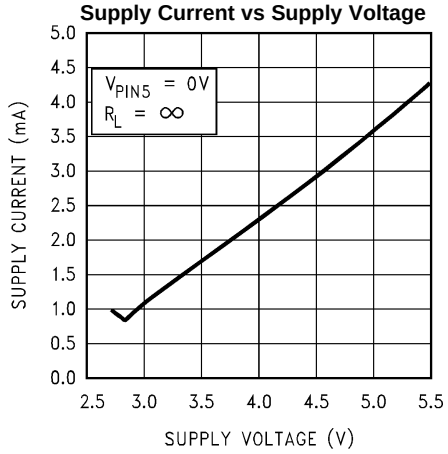


Figure 27.

Typical Performance Characteristics (continued)

Power Supply Rejection Ratio

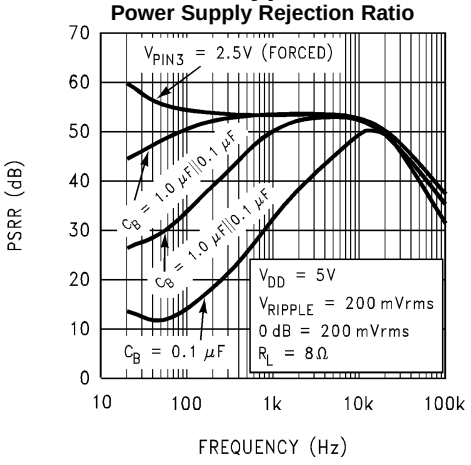


Figure 28.

Open Loop Frequency Response

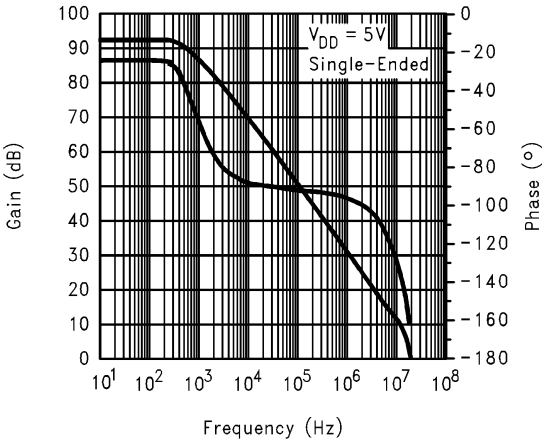


Figure 29.

Noise Floor

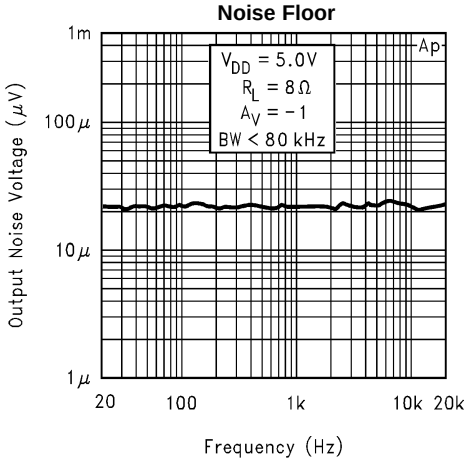


Figure 30.

Frequency Response vs Output Capacitor Size

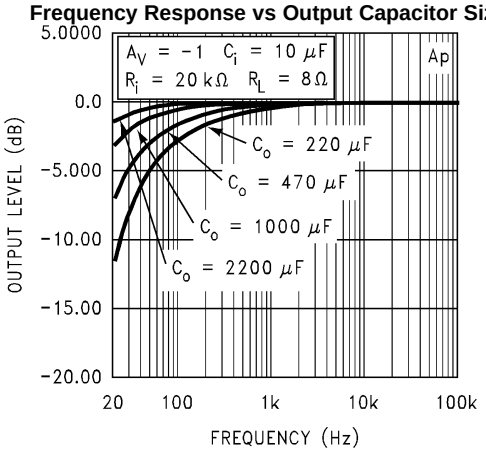


Figure 31.

Frequency Response vs Output Capacitor Size

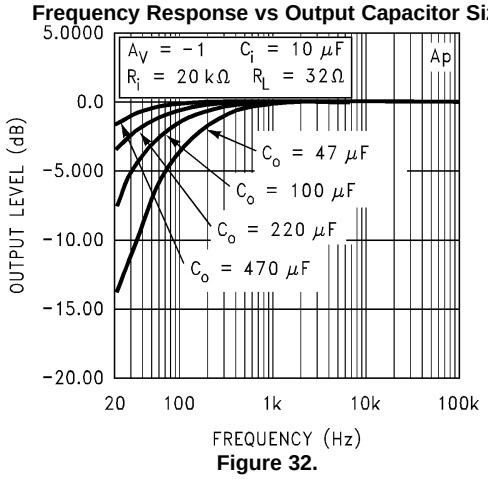


Figure 32.

Frequency Response vs Output Capacitor Size

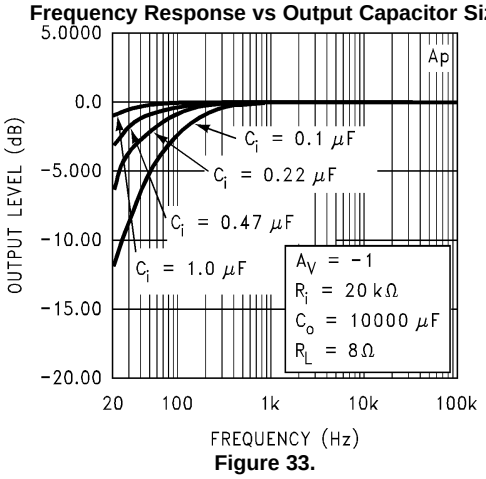


Figure 33.

Typical Performance Characteristics (continued)

Typical Application Frequency Response

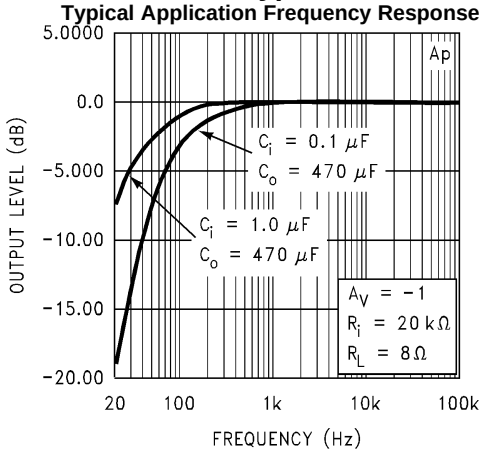


Figure 34.

Typical Application Frequency Response

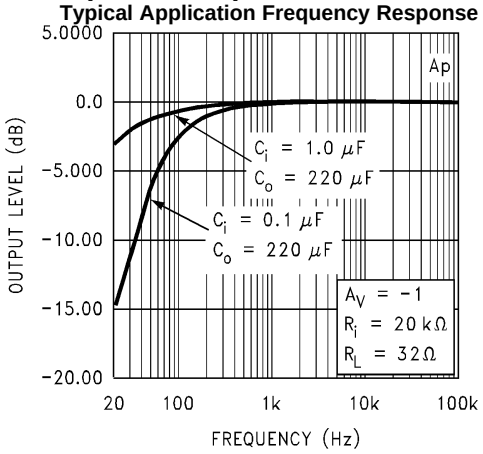


Figure 35.

Power Derating Curve

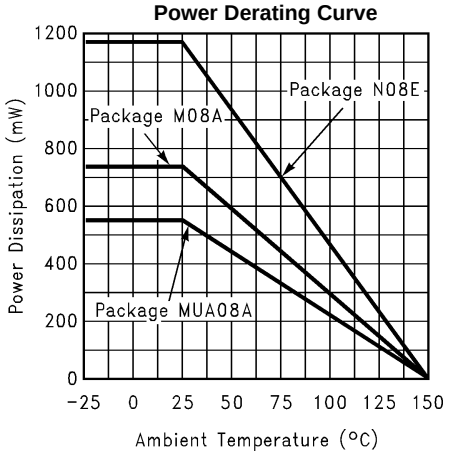


Figure 36.

APPLICATION INFORMATION

SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the LM4881 contains a shutdown pin to externally turn off the amplifier's bias circuitry. This shutdown feature turns the amplifier off when a logic high is placed on the shutdown pin. The trigger point between a logic low and logic high level is typically half supply. It is best to switch between ground and supply to provide maximum device performance. By switching the shutdown pin to the V_{DD}, the LM4881 supply current draw will be minimized in idle mode. While the device will be disabled with shutdown pin voltages less than V_{DD}, the idle current may be greater than the typical value of 0.7 µA. In either case, the shutdown pin should be tied to a definite voltage because leaving the pin floating may result in an unwanted shutdown condition. In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry which provides a quick, smooth transition into shutdown. Another solution is to use a single-pole, single-throw switch in conjunction with an external pull-up resistor. When the switch is closed, the shutdown pin is connected to ground and enables the amplifier. If the switch is open, then the external pull-up resistor will disable the LM4881. This scheme ensures that the shutdown pin will not float which will prevent unwanted state changes.

POWER DISSIPATION

Power dissipation is a major concern when using any power amplifier and must be thoroughly understood to ensure a successful design. Equation 1 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2 / (2\pi^2 R_L) \quad (1)$$

Since the LM4881 has two operational amplifiers in one package, the maximum internal power dissipation point is twice that of the number which results from Equation 1. Even with the large internal power dissipation, the LM4881 does not require heat sinking over a large range of ambient temperature. From Equation 1, assuming a 5V power supply and an 8Ω load, the maximum power dissipation point is 158 mW per amplifier. Thus the maximum package dissipation point is 317 mW. The maximum power dissipation point obtained must not be greater than the power dissipation that results from Equation 2:

$$P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA} \quad (2)$$

For package DGK0008A, θ_{JA} = 230°C/W, and for package D0008A, θ_{JA} = 170°C/W, and for package P0008E, θ_{JA} = 107°C/W. T_{JMAX} = 150°C for the LM4881. Depending on the ambient temperature, T_A, of the system surroundings, Equation 2 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 1 is greater than that of Equation 2, then either the supply voltage must be decreased, the load impedance increased or T_A reduced. For the typical application of a 5V power supply, with an 8Ω load, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 96°C provided that device operation is around the maximum power dissipation point. Power dissipation is a function of output power and thus, if typical operation is not around the maximum power dissipation point, the ambient temperature may be increased accordingly. Refer to the Typical Performance Characteristics curves for power dissipation information for lower output powers.

POWER SUPPLY BYPASSING

As with any power amplifer, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. As displayed in the Typical Performance Characteristics section, the effect of a larger half supply bypass capacitor is improved low frequency PSRR due to increased half-supply stability. Typical applications employ a 5V regulator with 10 µF and a 0.1 µF bypass capacitors which aid in supply stability, but do not eliminate the need for bypassing the supply nodes of the LM4881. The selection of bypass capacitors, especially C_B, is thus dependent upon desired low frequency PSRR, click and pop performance as explained in Proper Selection of External Components system cost, and size constraints.

PROPER SELECTION OF EXTERNAL COMPONENTS

Selection of external components when using integrated power amplifiers is critical to optimize device and system performance. While the LM4881 is tolerant of external component combinations, consideration to component values must be used to maximize overall system quality.

The LM4881 is unity gain stable and this gives a designer maximum system flexibility. The LM4881 should be used in low gain configurations to minimize THD+N values, and maximum the signal-to-noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1 Vrms are available from sources such as audio codecs. Please refer to the section, Audio Power Amplifier Design, for a more complete explanation of proper gain selection.

Besides gain, one of the major considerations is the closed loop bandwidth of the amplifier. To a large extent, the bandwidth is dicated by the choice of external components shown in Figure 1. Both the input coupling capacitor, C_i, and the output coupling capacitor, C_o, form first order high pass filters which limit low frequency response. These values should be chosen based on needed frequency response for a few distinct reasons.

Selection of Input and Output Capacitor Size

Large input and output capacitors are both expensive and space hungry for portable designs. Clearly a certain sized capacitor is needed to couple in low frequencies without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150 Hz. Thus using large input and output capacitors may not increase system performance.

In addition to system cost and size, click and pop performance is effected by the size of the input coupling capacitor, C_i. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally 1/2 V_{DD}). This charge comes from the output via the feedback and is apt to create pops upon device enable. Thus, by minimizing the capacitor size based on necessary low frequency response, turn on pops can be minimized.

Besides minimizing the input and output capacitor sizes, careful consideration should be paid to the bypass capacitor value. Bypass capacitor C_B is the most critical component to minimize turn on pops since it determines how fast the LM4881 turns on. The slower the LM4881's outputs ramp to their quiescent DC voltage (nominally 1/2 V_{DD}), the smaller the turn on pop. Thus choosing C_B equal to 1.0 µF along with a small value of C_i (in the range of 0.1 µF to 0.39 µF), the shutdown function should be virtually clickless and popless. While the device will function properly, (no oscillations or motorboating), with C_B equal to 0.1 µF, the device will be much more susceptible to turn on clicks and pops. Thus, a value of C_B equal to 0.1 µF or larger is recommended in all but the most cost sensitive designs.

AUDIO POWER AMPLIFIER DESIGN

Design a Dual 200mW/8Ω Audio Amplifier

Given:	
Power Output	200 mWrms
Load Impedance	8Ω
Input Level	1 Vrms (max)
Input Impedance	20 kΩ
Bandwidth	100 Hz–20 kHz ± 0.50 dB

A designer must first determine the needed supply rail to obtain the specified output power. Calculating the required supply rail involves knowing two parameters, V_{OPEAK} and also the dropout voltage. The latter is typically 530 mV and can be found from the graphs in the Typical Performance Characteristics. V_{OPEAK} can be determined from Equation 3.

$$V_{opeak} = \sqrt{(2R_L P_O)} \tag{3}$$

For 200 mW of output power into an 8Ω load, the required V_{OPEAK} is 1.79 volts. A minimum supply rail of 2.32V results from adding V_{OPEAK} and V_{OD}. Since 5V is a standard supply voltage in most applications, it is chosen for the supply rail. Extra supply voltage creates headroom that allows the LM4881 to reproduce peaks in excess of 200 mW without clipping the signal. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the Power Dissipation section. Remember that the maximum power dissipation point from Equation 1 must be multiplied by two since there are two independent amplifiers inside the package.

Once the power dissipation equations have been addressed, the required gain can be determined from Equation 4.

$$A_V \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (4)$$

$$A_V = R_f/R_i \quad (5)$$

From Equation 4, the minimum gain is: $A_V = 1.26$

Since the desired input impedance was 20 kΩ, and with a gain of 1.26, a value of 27 kΩ is designated for R_f, assuming 5% tolerance resistors. This combination results in a nominal gain of 1.35. The final design step is to address the bandwidth requirements which must be stated as a pair of −3 dB frequency points. Five times away from a −3 dB point is 0.17 dB down from passband response assuming a single pole roll-off. As stated in the External Components Description section, both R_i in conjunction with C_i, and C_o with R_L, create first order highpass filters. Thus to obtain the desired frequency low response of 100 Hz within ±0.5 dB, both poles must be taken into consideration. The combination of two single order filters at the same frequency forms a second order response. This results in a signal which is down 0.34 dB at five times away from the single order filter −3 dB point. Thus, a frequency of 20 Hz is used in the following equations to ensure that the response is better than 0.5 dB down at 100 Hz.

$$C_i \geq 1 / (2\pi * 20\ k\Omega * 20\ Hz) = 0.397\ \mu F;\ use\ 0.39\ \mu F. \quad (6)$$

$$C_o \geq 1 / (2\pi * 8\Omega * 20\ Hz) = 995\ \mu F;\ use\ 1000\ \mu F. \quad (7)$$

The high frequency pole is determined by the product of the desired high frequency pole, f_H, and the closed-loop gain, A_V. With a closed-loop gain of 1.35 and f_H = 100 kHz, the resulting GBWP = 135 kHz which is much smaller than the LM4881 GBWP of 18 MHz. This figure displays that if a designer has a need to design an amplifier with a higher gain, the LM4881 can still be used without running into bandwidth limitations.

REVISION HISTORY

Changes from Revision C (May 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	13

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM4881M/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM48 81M
LM4881M/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM48 81M
LM4881MM/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	Z81
LM4881MM/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	Z81
LM4881MX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM48 81M
LM4881MX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	LM48 81M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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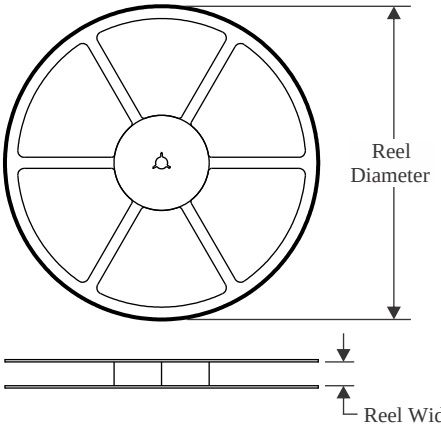
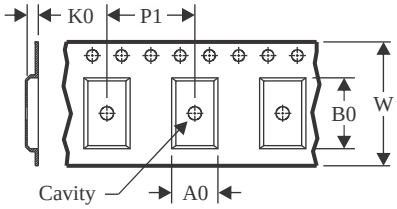
TAPE AND REEL INFORMATION

REEL DIMENSIONS

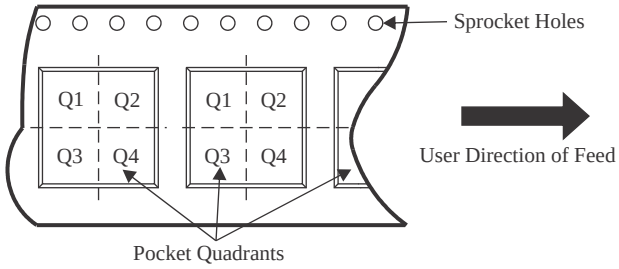


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

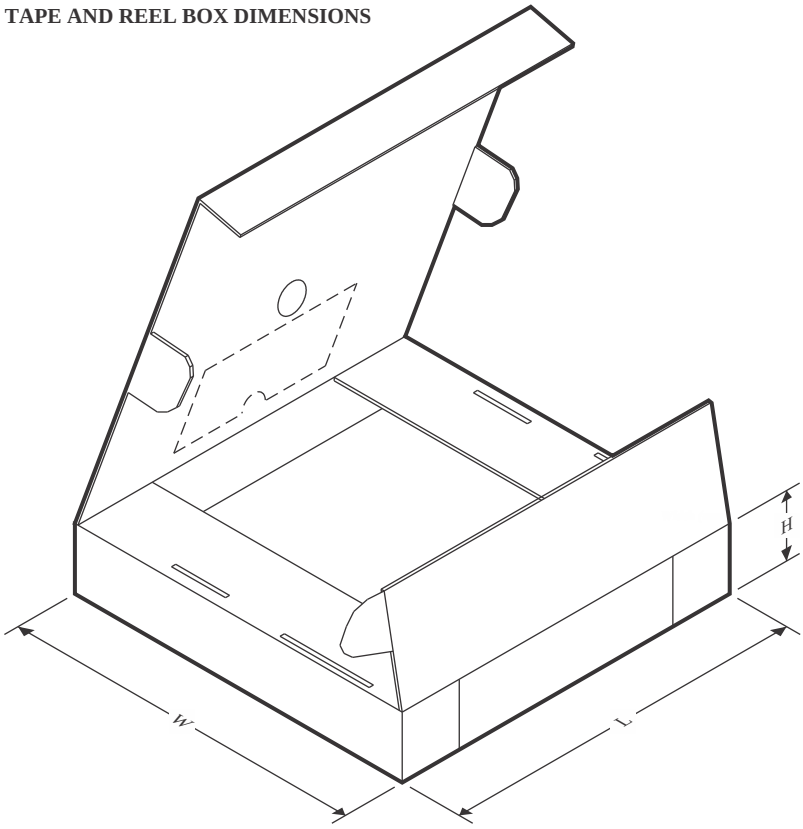
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4881MM/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM4881MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

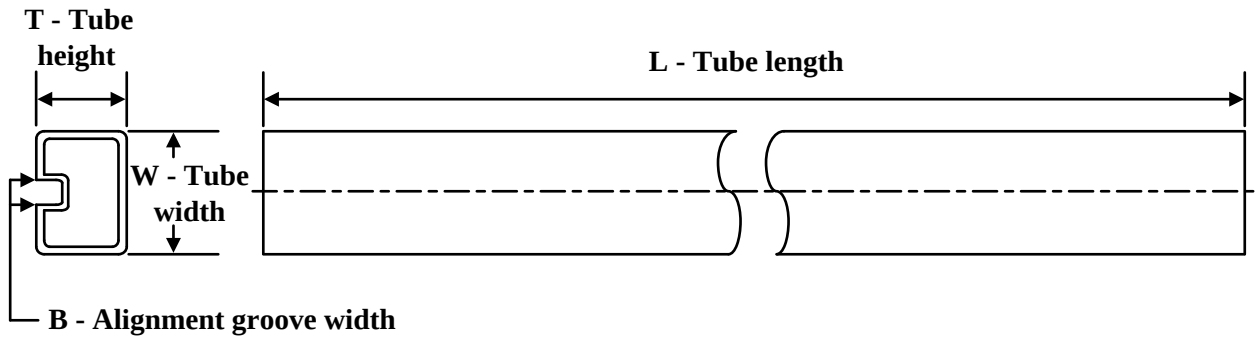
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4881MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM4881MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

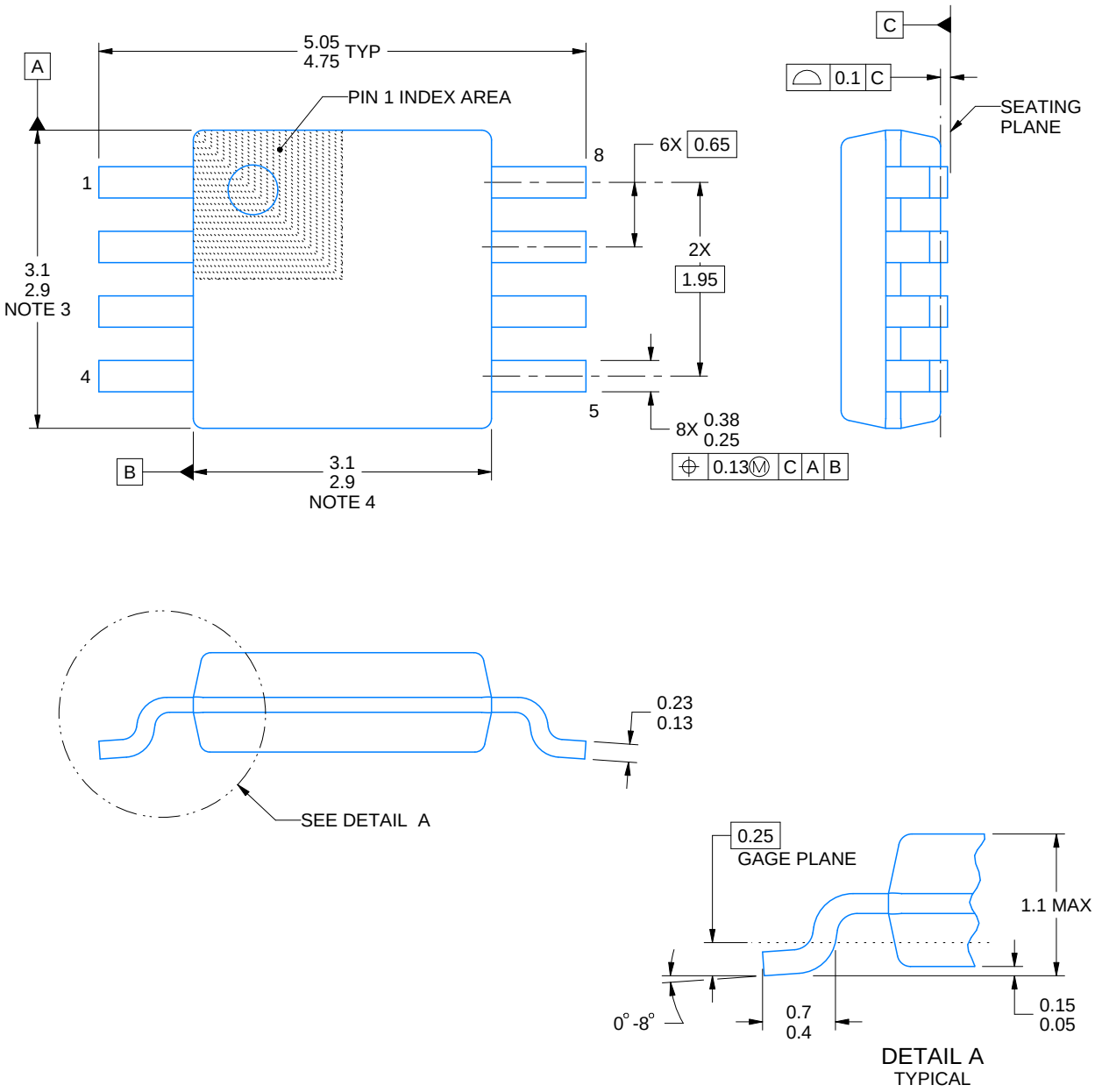
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM4881M/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM4881M/NOPB.A	D	SOIC	8	95	495	8	4064	3.05

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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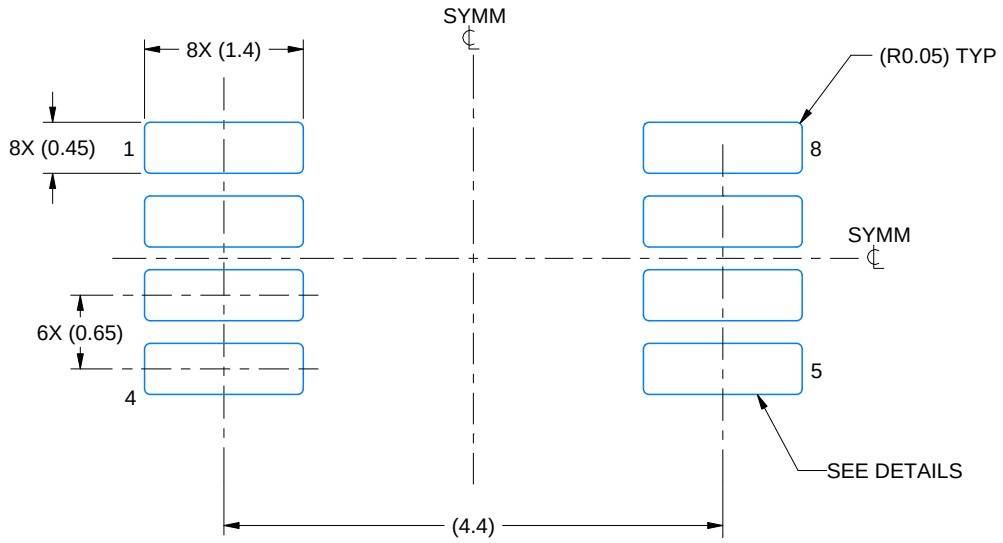
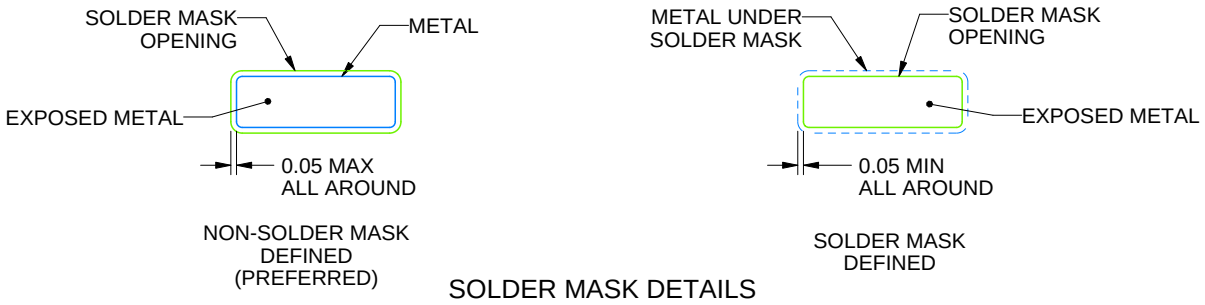
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

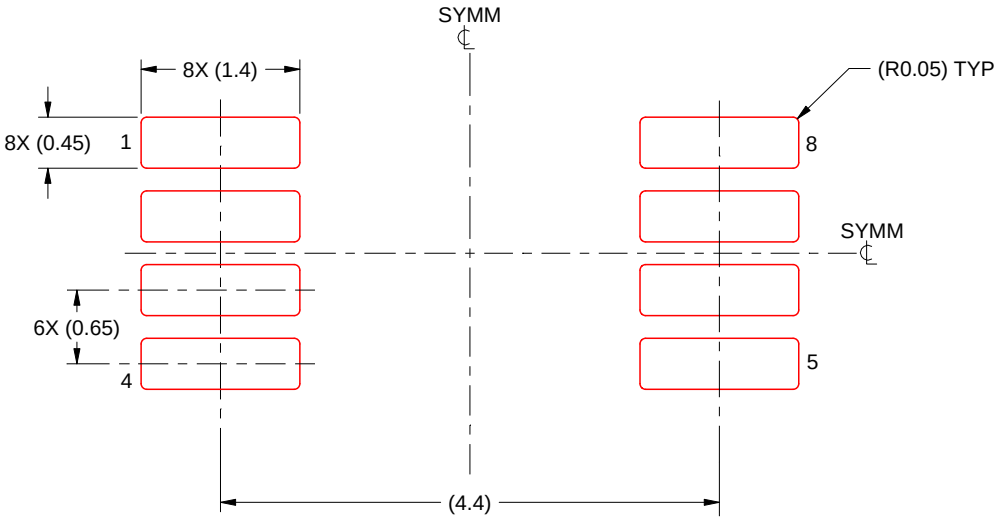


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

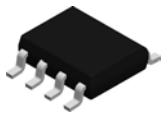


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

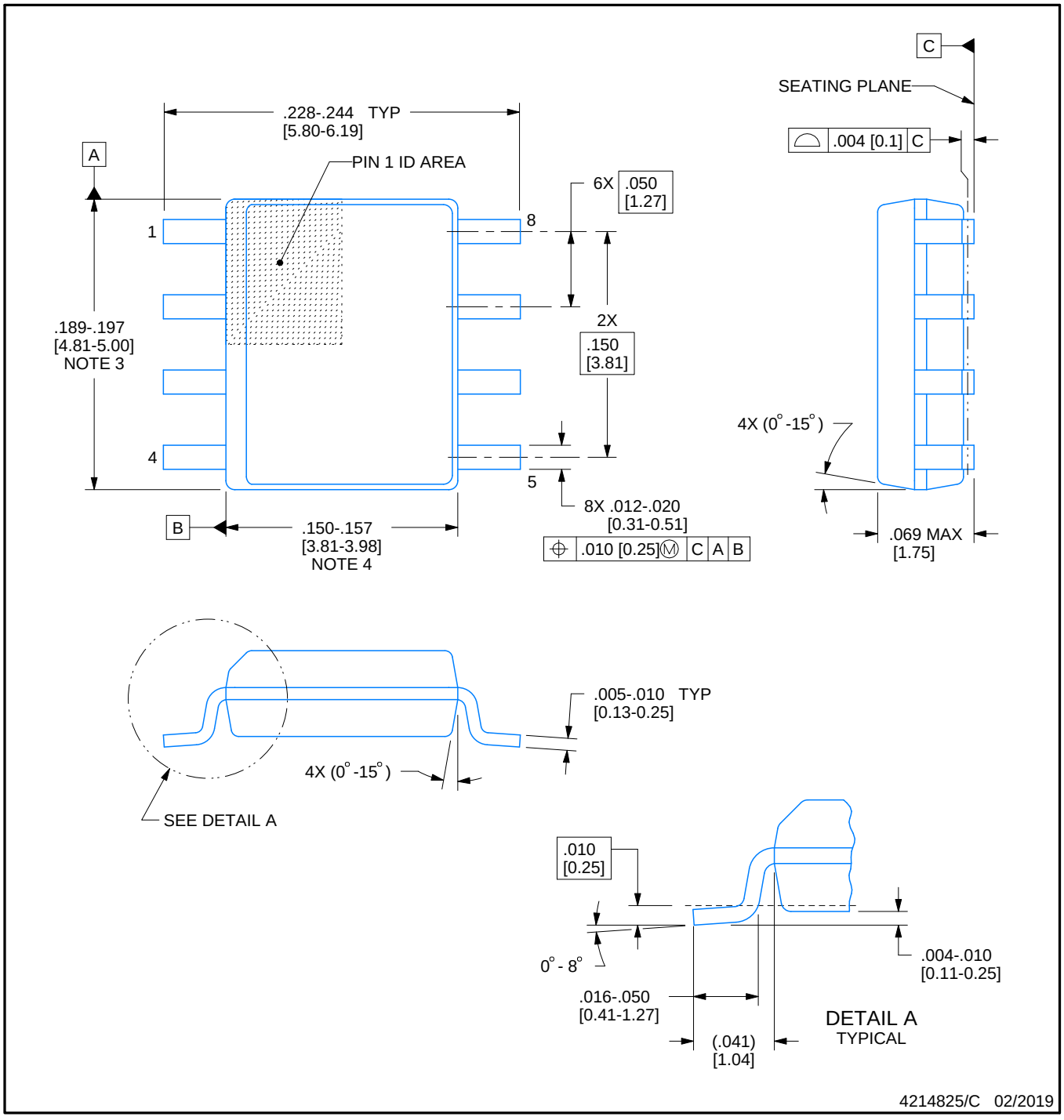


PACKAGE OUTLINE

D0008A

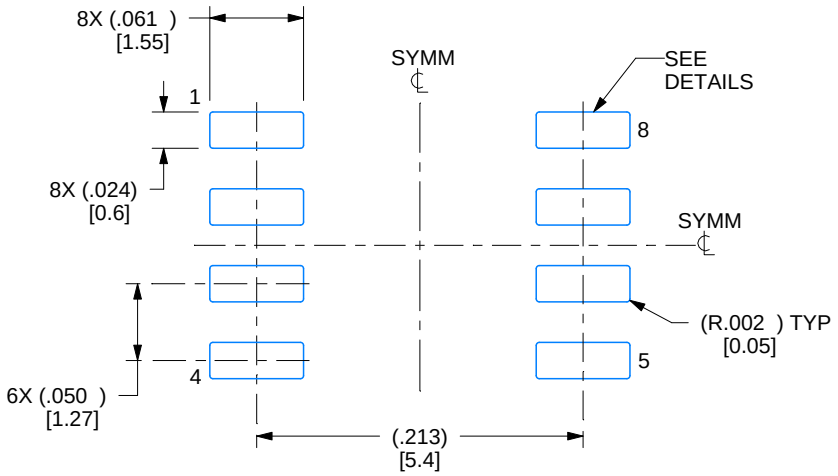
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

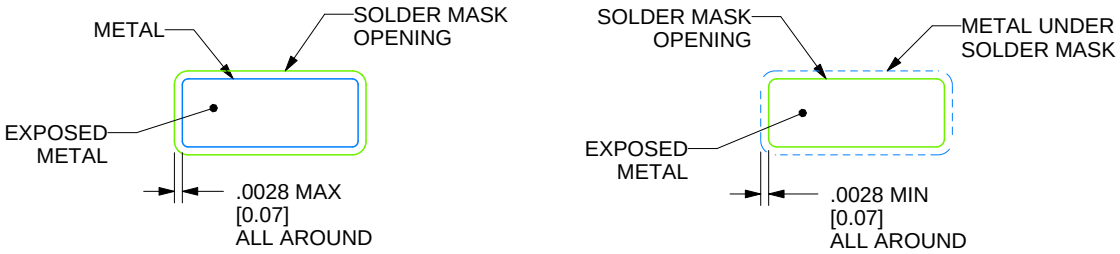


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

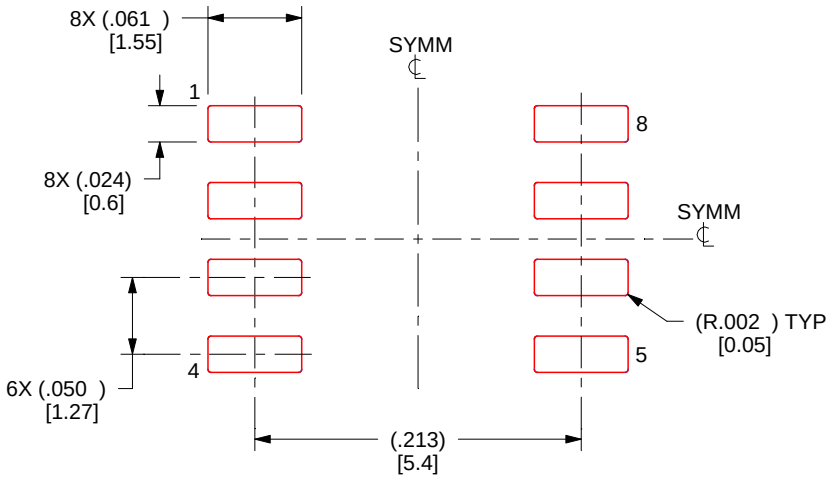
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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