

# LM48824 Boomer® Audio Power Amplifier Series **Class G Headphone Amplifier** with I<sup>2</sup>C Volume Control

Check for Samples: [LM48824](#)

## FEATURES

- **Class G Power Savings**
- **Ground Referenced Headphone Outputs – Eliminates Output Coupling Capacitors**
- **Common-Mode Sense**
- **I<sup>2</sup>C Volume and Mode Control**
- **High Output Impedance in Shutdown**
- **Differential Inputs**
- **Advanced Click-and-Pop Suppression**
- **Low Supply Current**
- **Low THD Mode Option**

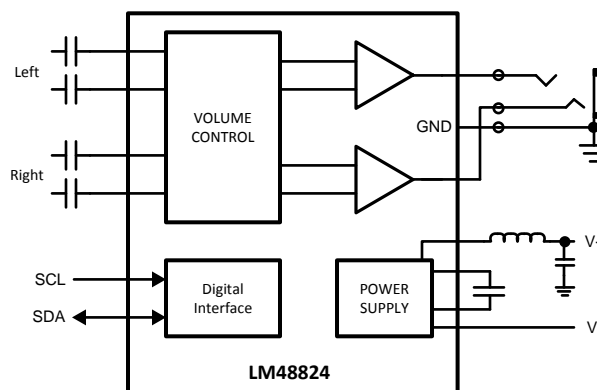
## APPLICATIONS

- **Mobile Phones, PDAs, MP3 Players**
- **Portable Electronic Devices, Notebook PCs**

## KEY SPECIFICATIONS

- **Quiescent Power Supply Current at 3.6V: 0.9mA (typ)**
- **Output Power/Channel at V<sub>DD</sub> = 3.6V (R<sub>L</sub> = 16Ω, THD+N ≤ 1%): 37 mW (Typ)**
- **Output Power/Channel at V<sub>DD</sub> = 3.6V (R<sub>L</sub> = 32Ω, THD+N ≤ 1%): 29 mW (Typ)**
- **PSRR at 217Hz: 100 dB (Typ)**
- **Shutdown Current: 2.5 μA (Typ)**

## Simplified Block Diagram



## DESCRIPTION

The LM48824 is a Class G, ground-referenced stereo headphone amplifier designed for portable devices. The LM48824 features TI's ground-referenced architecture, which eliminates the large DC blocking capacitors required by traditional headphone amplifiers, saving board space and minimizing system cost.

The LM48824 takes advantage of TI's patent-pending Class G architecture offering power savings compared to a traditional Class AB headphone amplifier. Additionally, output noise is improved by common-mode sensing that corrects for any differences between the amplifier ground and the potential at the headphone return terminal, minimizing noise created by any ground mismatches.

A high output impedance mode allows the LM48824's outputs to be driven by an external source without degrading the signal. Other features include flexible power supply requirements, differential inputs for improved noise rejection, a low power (2.5μA) shutdown mode, and a 32-step I<sup>2</sup>C volume control with mute function.

The LM48824's superior click and pop suppression eliminates audible transients on power-up/down and during shutdown. The LM48824 is available in an ultra-small 16-bump, 0.4mm pitch DSBGA package (1.69mm x 1.69mm)



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Typical Application

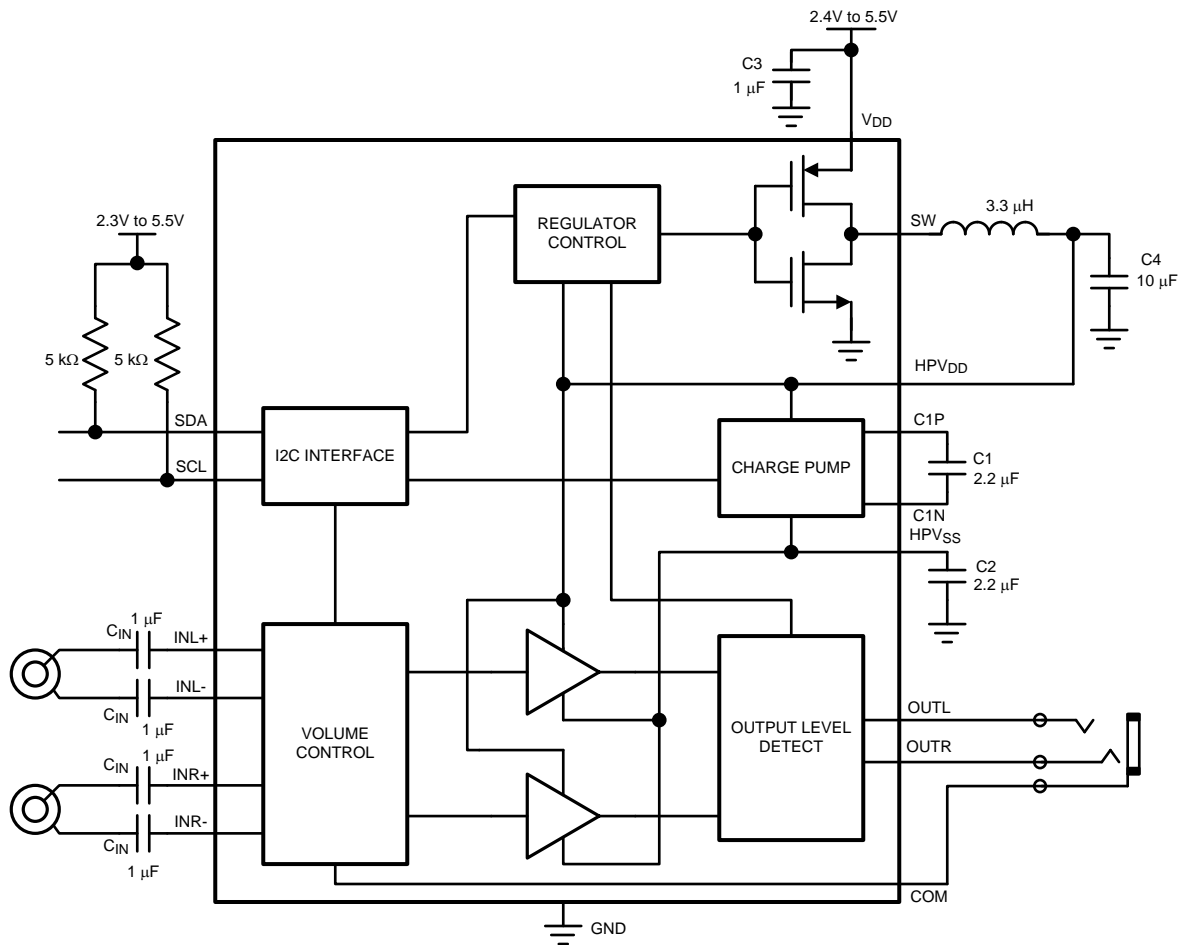
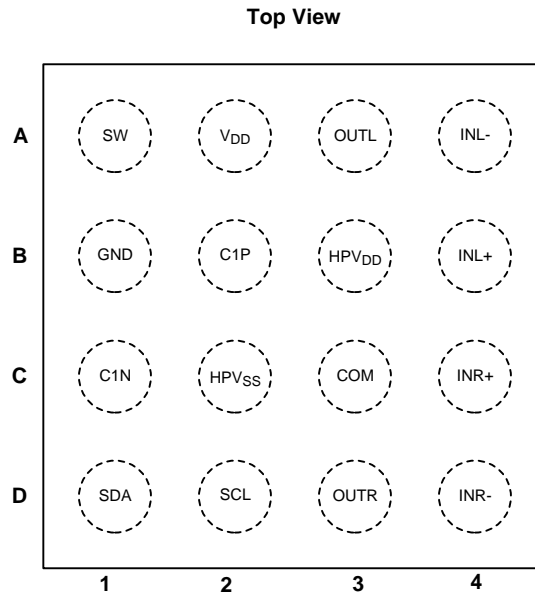


Figure 1. Typical Audio Amplifier Application Circuit

## Connection Diagram



**Figure 2.**  
**DSBGA Package (1.7mm x 1.7mm x 0.6mm)**  
**See Package Number YFQ0016DDA**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings<sup>(1)(2)(3)(4)</sup>

|                                  |                              |                                 |
|----------------------------------|------------------------------|---------------------------------|
| Supply Voltage <sup>(1)</sup>    |                              | 6V                              |
| Storage Temperature              |                              | -65°C to +150°C                 |
| Input Voltage                    |                              | -0.3V to V <sub>DD</sub> + 0.3V |
| Power Dissipation <sup>(5)</sup> |                              | Internally Limited              |
| ESD Rating <sup>(6)</sup>        |                              | 2000V                           |
| ESD Rating <sup>(7)</sup>        |                              | 200V                            |
| ESD Rating <sup>(8)</sup>        |                              | 500V                            |
| Junction Temperature             |                              | 150°C                           |
| Soldering Information            | Vapor Phase (60 sec.)        | 215°C                           |
|                                  | Infrared (15 sec.)           | 220°C                           |
| Thermal Resistance               | θ <sub>JA</sub> (YFQ0016DDA) | 60°C/W                          |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) The Electrical Characteristics tables list specified specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (3) Soldering Information: See [AN-1112](#) "Micro SMD Wafer Level Chip Scale package"
- (4) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (5) The maximum power dissipation must be derated at elevated temperatures and is dictated by T<sub>JMAX</sub>, θ<sub>JA</sub>, and the ambient temperature, T<sub>A</sub>. The maximum allowable power dissipation is P<sub>DMAX</sub> = (T<sub>JMAX</sub> - T<sub>A</sub>) / θ<sub>JA</sub> or the number given in Absolute Maximum Ratings, whichever is lower.
- (6) Human body model, applicable std. JESD22-A114C.
- (7) Machine model, applicable std. JESD22-A115-A.
- (8) Charged Device Model, applicable std. JESD22-C101-C.

## Operating Ratings

|   |   |
|---|---|
| Temperature Range ( $T_{MIN} \leq T_A \leq T_{MAX}$ ) | $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ |
| Supply Voltage ( $V_{DD}$ )                           | $2.4\text{V} \leq V_{DD} \leq 5.5\text{V}$              |

## Electrical Characteristics $V_{DD} = 3.6\text{V}^{(1)(2)}$

The following specifications apply for  $A_V = 0\text{dB}$ ,  $R_L = 32\Omega$ ,  $f = 1\text{kHz}$ , unless otherwise specified. Limits apply to  $T_A = 25^{\circ}\text{C}$ .

| Parameter     |                                | Test Conditions  | LM48824            |                      | Units (Limits)       |
|---------------|--------------------------------|--|--------------------|----------------------|----------------------|
|               |                                |  | Typ <sup>(3)</sup> | Limit <sup>(4)</sup> |                      |
| $I_{DD}$      | Quiescent Power Supply Current | $V_{IN} = 0\text{V}$ , both channels active, $R_L = \infty$  | 0.9                | 1.3                  | mA (max)             |
|               |                                | $R_L = \infty$ , Low THD mode  | 1.55               |                      | mA                   |
| $I_{DD(OP)}$  | Operating Power Supply Current | $P_O = 100\mu\text{W}$ , two channels in phase, 3dB Crest Factor, $R_L = 32\Omega + 15\Omega$                | 1.8                | 2.5                  | mA (max)             |
|               |                                | $P_O = 100\mu\text{W}$ , two channels in phase, 3dB Crest Factor, $R_L = 32\Omega + 15\Omega$ , Low THD mode | 2.2                |                      | mA                   |
|               |                                | $P_O = 500\mu\text{W}$ , two channels in phase, 3dB Crest Factor $R_L = 32\Omega + 15\Omega$                 | 3.1                | 3.8                  | mA (max)             |
|               |                                | $P_O = 500\mu\text{W}$ , two channels in phase, 3dB Crest Factor $R_L = 32\Omega + 15\Omega$ , Low THD mode  | 3.4                |                      | mA                   |
|               |                                | $P_O = 1\text{mW}$ , two channels in phase, 3dB Crest Factor, $R_L = 32\Omega + 15\Omega$                    | 4.1                | 4.9                  | mA (max)             |
|               |                                | $P_O = 1\text{mW}$ , two channels in phase, 3dB Crest Factor, $R_L = 32\Omega + 15\Omega$ , Low THD mode     | 4.4                |                      | mA                   |
| $I_{SD}$      | Shutdown Current               | Shutdown Enabled, $V_{SCL} = V_{SDA} = 1.8\text{V}$  | 2.5                | 3.9                  | $\mu\text{A}$ (max)  |
| $V_{OS}$      | Output Offset Voltage          | $V_{IN} = 0\text{V}$   | 0.15               | 0.65                 | mV (max)             |
| $T_{WU}$      | Wake Up Time                   | From Shutdown  | 2                  |                      | ms                   |
| $A_V$         | Gain                           | Minimum Gain Setting   | -59                | -58<br>-60           | dB (max)<br>dB (min) |
|               |                                | Maximum Gain Setting   | 4                  | 4.5<br>3.5           | dB (max)<br>dB (min) |
| $A_{V(MUTE)}$ | Mute Attenuation               |  | -110               |                      | dB                   |
| $R_{IN}$      | Input Resistance               | $A_V = 4\text{dB}$   | 24                 | 20                   | k $\Omega$ (min)     |
|               |                                | $A_V = -59\text{dB}$   | 64                 | 80                   | k $\Omega$ (max)     |
| $P_O$         | Output Power                   | $f = 1\text{kHz}$ , THD+N = 1%<br>Two channels in phase, $R_L = 16\Omega$                                    | 37                 | 30                   | mW (min)             |
|               |                                | $f = 1\text{kHz}$ , THD+N = 1%<br>Two channels in phase, $R_L = 32\Omega$                                    | 29                 | 23                   | mW (min)             |
| $V_O$         | Output Swing                   | THD+N = 1%, Two Channels in Phase  |                    |                      |                      |
|               |                                | $R_L = 16\Omega$   | 0.77               | 0.7                  | $V_{RMS}$ (min)      |
|               |                                | $R_L = 32\Omega$   | 0.96               | 0.86                 | $V_{RMS}$ (min)      |
|               |                                | $R_L = 32\Omega + 15\Omega$  | 1.05               |                      | $V_{RMS}$            |
|               |                                | $R_L = 10\text{k}\Omega$   | 1.3                | 1.1                  | $V_{RMS}$ (min)      |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
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- (4) Datasheet min/max specification limits are specified by test or statistical analysis.

**Electrical Characteristics  $V_{DD} = 3.6V^{(1)(2)}$  (continued)**

 The following specifications apply for  $A_V = 0dB$ ,  $R_L = 32\Omega$ ,  $f = 1kHz$ , unless otherwise specified. Limits apply to  $T_A = 25^\circ C$ .

| Parameter       |                                   | Test Conditions  | LM48824            |                      | Units (Limits)   |
|-----------------|-----------------------------------|--|--------------------|----------------------|------------------|
|                 |                                   |  | Typ <sup>(3)</sup> | Limit <sup>(4)</sup> |                  |
| THD+N           | Total Harmonic Distortion + Noise | f = 1kHz, Single Channel   |                    |                      |                  |
|                 |                                   | $V_O = 600mV_{RMS}$ , $R_L = 16\Omega$   | 0.05               |                      | %                |
|                 |                                   | $V_O = 600mV_{RMS}$ , $R_L = 16\Omega$ , Low THD Mode                          | 0.03               |                      | %                |
|                 |                                   | $V_O = 800mV_{RMS}$ , $R_L = 32\Omega$   | 0.035              |                      | %                |
|                 |                                   | $V_O = 800mV_{RMS}$ , $R_L = 32\Omega$ , Low THD Mode                          | 0.02               |                      | %                |
|                 |                                   | $V_O = 900mV_{RMS}$ , $R_L = 32\Omega + 15\Omega$                              | 0.027              | 0.04                 | %(max)           |
| PSRR            | Power Supply Rejection Ratio      | $V_{RIPPLE} = 200mV_{P-P}$ , Inputs AC GND, $C_{IN} = 1\mu F$ , input referred |                    |                      |                  |
|                 |                                   | $f_{RIPPLE} = 217Hz$   | 100                | 94                   | dB (min)         |
|                 |                                   | $f_{RIPPLE} = 1kHz$  | 100                |                      | dB               |
| CMRR            | Common Mode Rejection Ratio       | $V_{RIPPLE} = 1V_{P-P}$ , $f_{RIPPLE} = 217Hz$                                 | 60                 |                      | dB               |
| $X_{TALK}$      | Crosstalk                         | $R_L \geq 16\Omega$ , $P_O = 5mW$ , $f = 1kHz$                                 | 80                 | 70                   | dB (min)         |
|                 |                                   | $R_L \geq 10k\Omega$ , $V_{OUT} = 1V_{RMS}$ , $f = 1kHz$                       | 110                | 95                   | dB (min)         |
| SNR             | Signal-to-Noise Ratio             | $V_{OUT} = 1V_{RMS}$ , $f = 1kHz$  | 102                | 98                   | dB (min)         |
|                 |                                   | $V_{OUT} = 1V_{RMS}$ , $f = 1kHz$ , Low THD Mode                               | 105                |                      | dB               |
| $\epsilon_{OS}$ | Output Noise                      | $A_V = 4dB$ , A-Weighted Filter  | 8                  | 12                   | $\mu V$ (max)    |
|                 |                                   | $A_V = 4dB$ , A-weighted Filter, Low THD Mode                                  | 7                  |                      | $\mu V$          |
| $R_{OUT}$       | Output Impedance                  | Charge pump-only mode enabled  |                    |                      |                  |
|                 |                                   | f < 40kHz  | 43                 | 30                   | k $\Omega$ (min) |
|                 |                                   | f = 6MHz   |                    | 500                  | $\Omega$ (min)   |
|                 |                                   | f = 36MHz  |                    | 75                   | $\Omega$ (min)   |
| $C_L$           | Maximum Capacitive Load           | No Sustained Oscillations  |                    |                      |                  |
|                 |                                   | with 5 $\Omega$ series resistance  | 100                |                      | nF               |
|                 |                                   | with no series resistance  | 100                |                      | pF               |
| $V_{OUT}$       | Maximum Voltage Swing             | Voltage applied to amplifier outputs in charge pump-only mode                  | 1.1                | 1.0                  | $V_{RMS}$ (min)  |

## I<sup>2</sup>C Interface Characteristics $V_{DD} = 3.6V^{(1)(2)}$

The following specifications apply for  $A_V = 0dB$ ,  $R_L = 16\Omega$ ,  $f = 1kHz$ , unless otherwise specified. Limits apply to  $T_A = 25^\circ C$ .

| Parameter |                      | Test Conditions | LM48824            |                      | Units (Limits) |
|-----------|----------------------|-----------------|--------------------|----------------------|----------------|
|           |                      |                 | Typ <sup>(3)</sup> | Limit <sup>(4)</sup> |                |
| $t_1$     | SCL Period           |                 |                    | 2.5                  | $\mu s$ (min)  |
| $t_2$     | SDA Setup Time       |                 |                    | 250                  | ns (min)       |
| $t_3$     | SDA Stable Time      |                 |                    | 250                  | ns (min)       |
| $t_4$     | Start Condition Time |                 |                    | 250                  | ns (min)       |
| $t_5$     | Stop Condition Time  |                 |                    | 250                  | ns (min)       |
| $V_{IH}$  | Input High Voltage   |                 |                    | 1.2                  | V (min)        |
| $V_{IL}$  | Input Low Voltage    |                 |                    | 0.6                  | V (max)        |

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- (4) Datasheet min/max specification limits are specified by test or statistical analysis.

Typical Performance Characteristics

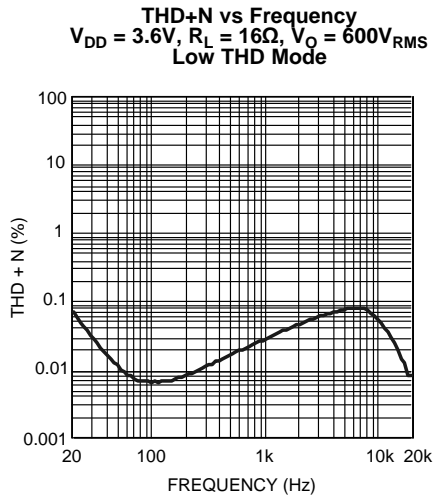


Figure 3.

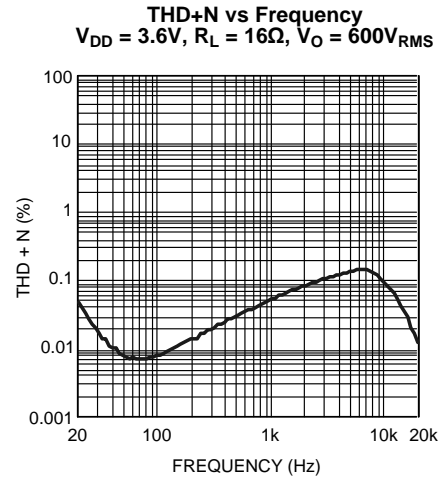


Figure 4.

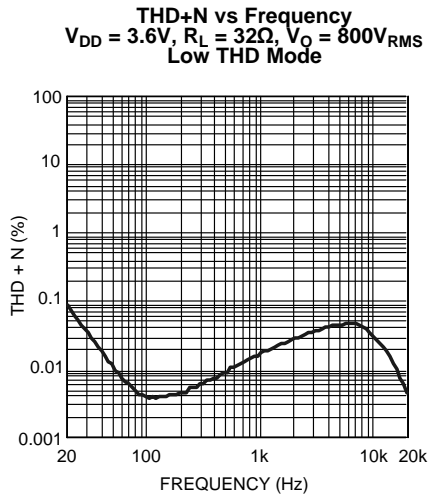


Figure 5.

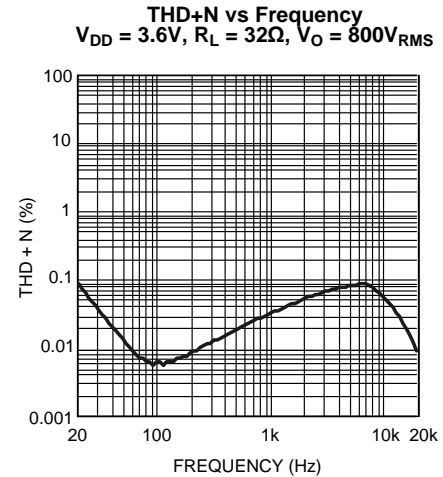


Figure 6.

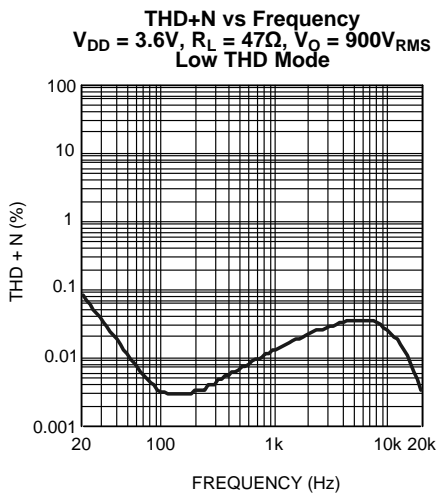


Figure 7.

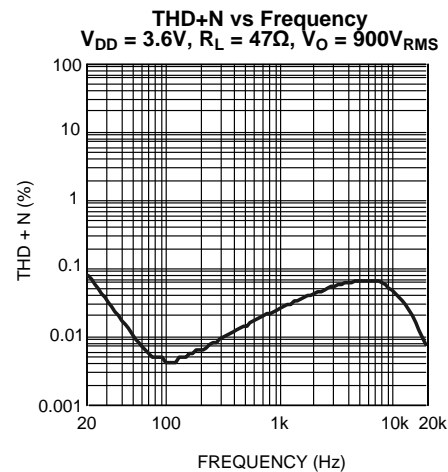
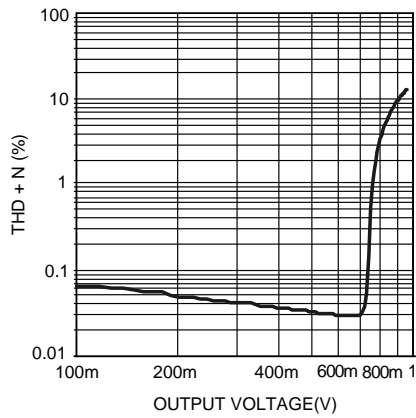


Figure 8.

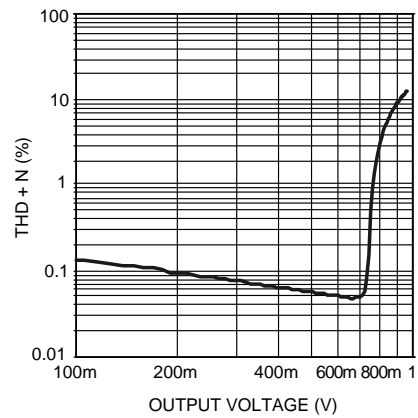
**Typical Performance Characteristics (continued)**

**THD+N vs Output Voltage**  
 $V_{DD} = 3.6V$ ,  $R_L = 16\Omega$ ,  $f = 1kHz$   
 Low THD Mode



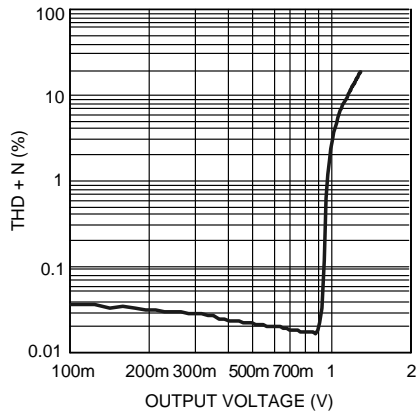
**Figure 9.**

**THD+N vs Output Voltage**  
 $V_{DD} = 3.6V$ ,  $R_L = 16\Omega$ ,  $f = 1kHz$



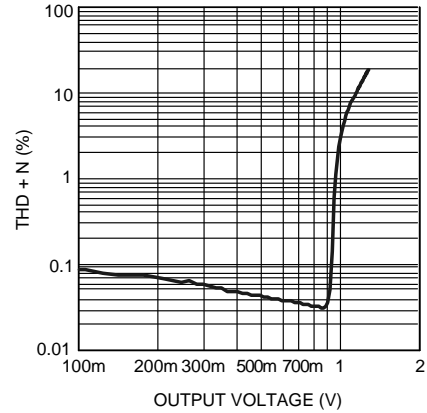
**Figure 10.**

**THD+N vs Output Voltage**  
 $V_{DD} = 3.6V$ ,  $R_L = 32\Omega$ ,  $f = 1kHz$   
 Low THD Mode



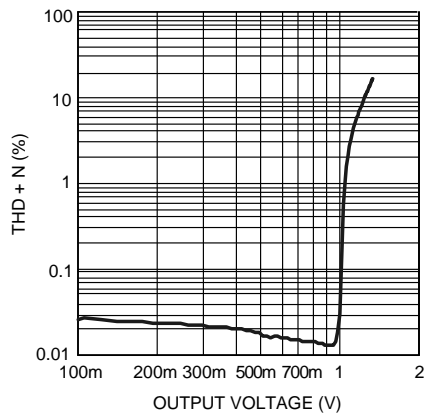
**Figure 11.**

**THD+N vs Output Voltage**  
 $V_{DD} = 3.6V$ ,  $R_L = 32\Omega$ ,  $f = 1kHz$



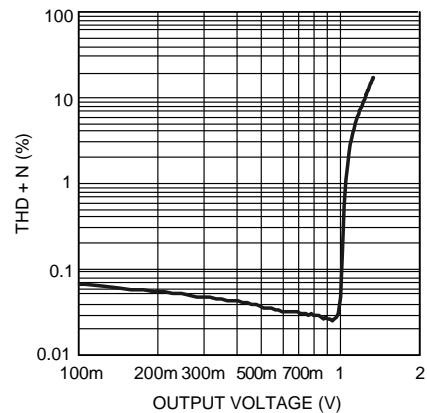
**Figure 12.**

**THD+N vs Output Voltage**  
 $V_{DD} = 3.6V$ ,  $R_L = 47\Omega$ ,  $f = 1kHz$   
 Low THD Mode



**Figure 13.**

**THD+N vs Output Voltage**  
 $V_{DD} = 3.6V$ ,  $R_L = 47\Omega$ ,  $f = 1kHz$



**Figure 14.**



Typical Performance Characteristics (continued)

THD+N vs Output Power  
 $V_{DD} = 3.6V$ ,  $R_L = 16\Omega$ ,  $f = 1kHz$   
 Low THD Mode

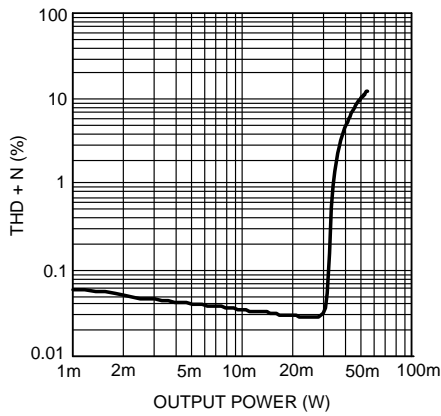


Figure 15.

THD+N vs Output Power  
 $V_{DD} = 3.6V$ ,  $R_L = 16\Omega$ ,  $f = 1kHz$

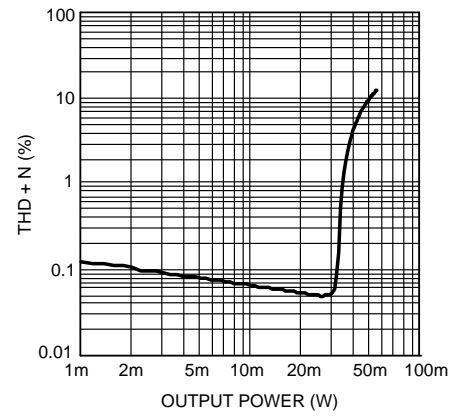


Figure 16.

THD+N vs Output Power  
 $V_{DD} = 3.6V$ ,  $R_L = 32\Omega$ ,  $f = 1kHz$   
 Low THD Mode

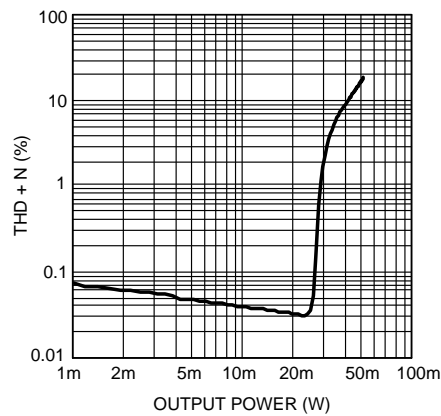


Figure 17.

THD+N vs Output Power  
 $V_{DD} = 3.6V$ ,  $R_L = 32\Omega$ ,  $f = 1kHz$

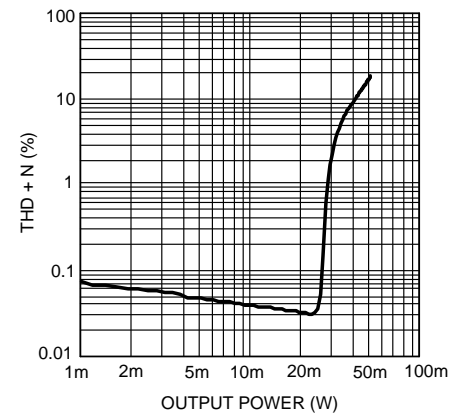


Figure 18.

Power Dissipation vs Output Power  
 $V_{DD} = 3.6V$ ,  $R_L = 16\Omega$ ,  $f = 1kHz$

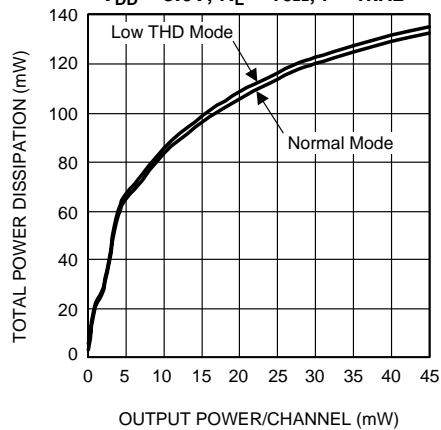


Figure 19.

Power Dissipation vs Output Power  
 $V_{DD} = 3.6V$ ,  $R_L = 32\Omega$ ,  $f = 1kHz$

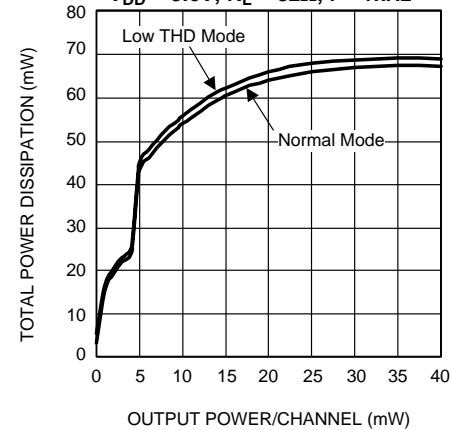


Figure 20.

**Typical Performance Characteristics (continued)**

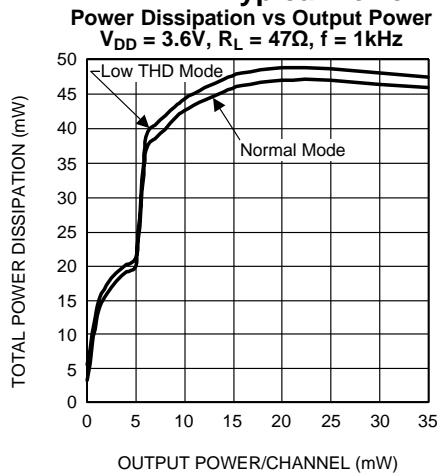


Figure 21.

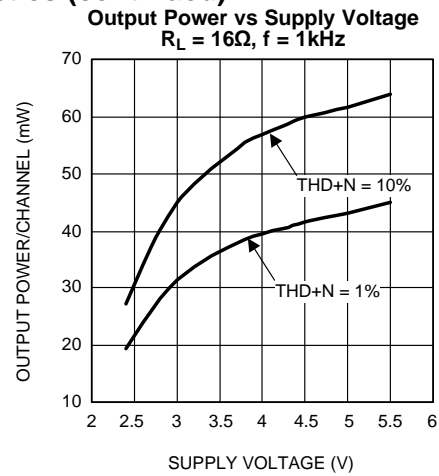


Figure 22.

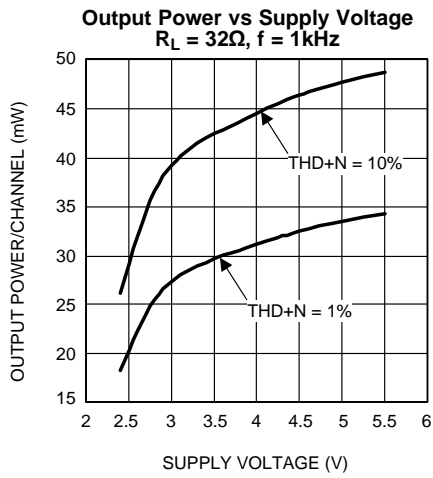


Figure 23.

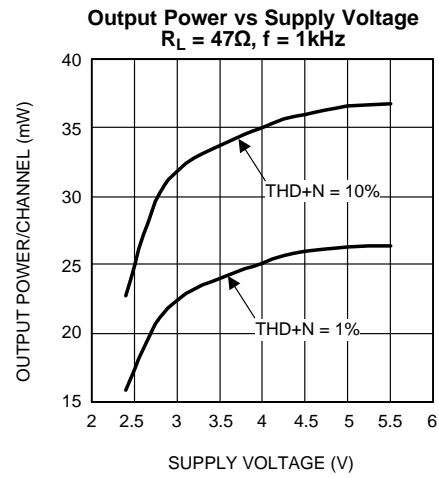


Figure 24.

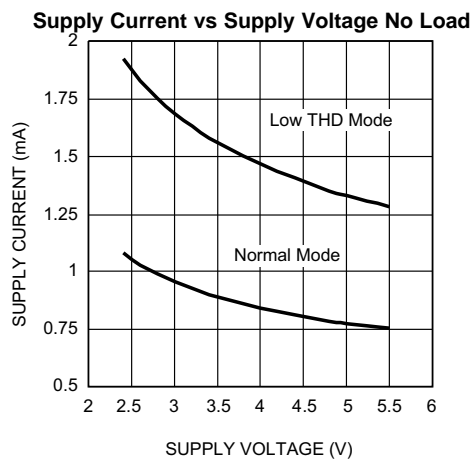


Figure 25.

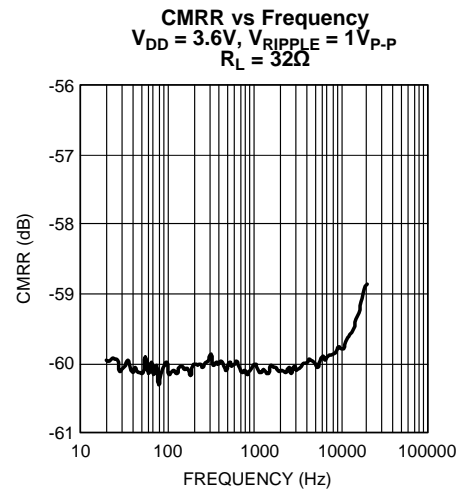
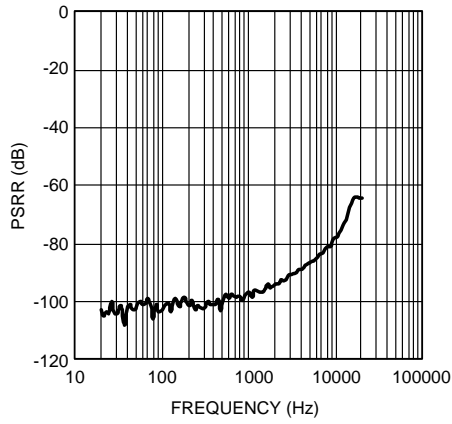


Figure 26.

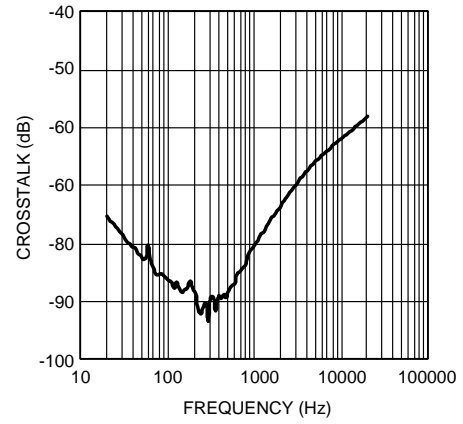
**Typical Performance Characteristics (continued)**

**PSRR vs Frequency**  
 $V_{DD} = 3.6V$ ,  $V_{RIPPLE} = 200V_{P-P}$   
 $R_L = 32\Omega$



**Figure 27.**

**Crosstalk vs Frequency**  
 $V_{DD} = 3.6V$ ,  $P_O = 5mW$   
 $R_L = 32\Omega$



**Figure 28.**

## APPLICATION INFORMATION

### I<sup>2</sup>C COMPATIBLE INTERFACE

The LM48824 is controlled through an I<sup>2</sup>C compatible serial interface that consists of a serial data line (SDA) and a serial clock (SCL). The clock line is uni-directional. The data line is bi-directional (open drain). The LM48824 and the master can communicate at clock rates up to 400kHz. Figure 29 shows the I<sup>2</sup>C interface timing diagram. Data on the SDA line must be stable during the HIGH period of SCL. The LM48824 is a transmit/receive slave-only device, reliant upon the master to generate the SCL signal. Each transmission sequence is framed by a START condition and a STOP condition (Figure 30). Each data word, device address and data, transmitted over the bus is 8 bits long and is always followed by an acknowledge pulse (Figure 31). The LM48824 device address is 1100000.

### I<sup>2</sup>C BUS FORMAT

The I<sup>2</sup>C bus format is shown in Figure 31. The START signal, the transition of SDA from HIGH to LOW while SCL is HIGH, is generated, alerting all devices on the bus that a device address is being written to the bus.

The 7-bit device address is written to the bus, most significant bit (MSB) first, followed by the  $\overline{R/W}$  bit ( $\overline{R/W} = 0$  indicates the master is writing to the LM48824,  $\overline{R/W} = 1$  indicates the master wants to read data from the LM48824). Data is latched into the device on the rising clock edge. Each address bit must be stable while SCL is HIGH. After the last address bit is transmitted, the master device releases SDA, during which time, an acknowledge clock pulse is generated by the slave device. If the LM48824 receives the correct address, the device pulls the SDA line low, generating an acknowledge bit (ACK).

Once the master device registers the ACK bit, the 8-bit register address word is sent. Each data bit should be stable while SCL is HIGH. After the 8-bit register address is sent, the LM48824 sends another ACK bit. Following the acknowledgment of the register address, the 8-bit register data word is sent. Each data bit should be stable while SCL is HIGH. After the 8-bit register data is sent, the LM48824 sends another ACK bit. Following the acknowledgement of the register data word, the master issues a STOP bit, allowing SDA to go high while SCL is high.

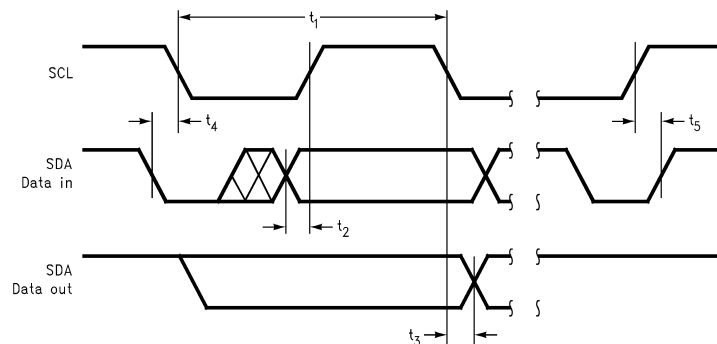


Figure 29. I<sup>2</sup>C Timing Diagram

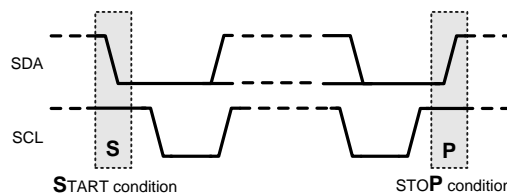


Figure 30. Start and Stop Diagram

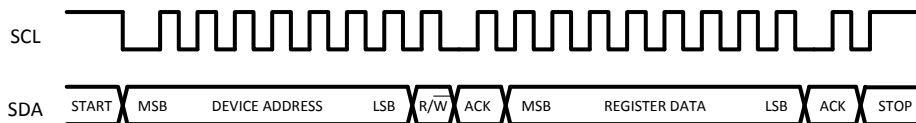


Figure 31. I<sup>2</sup>C Write Cycle

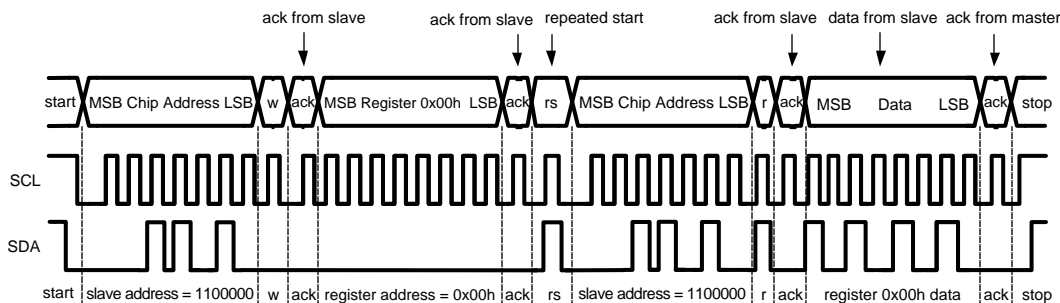


Figure 32. Example I<sup>2</sup>C Read Cycle

Table 1. Device Address

|                | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 (R/W) |
|----------------|----|----|----|----|----|----|----|----------|
| Device Address | 1  | 1  | 0  | 0  | 0  | 0  | 0  | X        |

Table 2. I<sup>2</sup>C Control Registers<sup>(1)</sup>

| Register Address | Register Name                  | B7     | B6     | B5   | B4   | B3      | B2   | B1    | B0    |
|------------------|--------------------------------|--------|--------|------|------|---------|------|-------|-------|
| 0x01h            | MODE CONTROL                   | HPL_EN | HPR_EN | 0    | 0    | 0       | 0    | THRM  | SHDN  |
| 0x02h            | VOLUME CONTROL                 | MUTE_L | MUTE_R | VOL4 | VOL3 | VOL2    | VOL1 | VOL0  | 0     |
| 0x03h            | OUTPUT CONTROL                 | 0      | 0      | 0    | 0    | LOW_THD | 0    | HiZ_L | HiZ_R |
| 0x04h            | DEVICE INFORMATION (Read-Only) | 0      | 1      | 0    | 0    | 0       | 0    | 0     | 0     |

(1) All registers default to 0 on initial power-up except SHDN, MUTE\_L, MUTE\_R bits default to 1 at power-up.

Table 3. Mode Control Register

| Bit | Name             | Value | Description                      |
|-----|------------------|-------|----------------------------------|
| B0  | SHDN             | 0     | Device enabled                   |
|     |                  | 1     | Device disabled                  |
| B1  | THRM (Read Only) | 0     | Thermal-protection inactive      |
|     |                  | 1     | Thermal-protection active        |
| B6  | HPR_EN           | 0     | Right channel amplifier disabled |
|     |                  | 1     | Right channel amplifier enabled  |
| B7  | HPL_EN           | 0     | Left channel amplifier disabled  |
|     |                  | 1     | Left channel amplifier enabled   |

**Table 4. Volume Control Register**

| Bit   | Name      | Value | Description  |
|-------|-----------|-------|--|
| B5:B1 | VOL4:VOL0 |       | These bits set the volume level. See <a href="#">Table 5</a> . |
| B6    | MUTE_R    | 0     | Right Channel Mute Disabled                                    |
|       |           | 1     | Right Channel Mute Enabled                                     |
| B7    | MUTE_L    | 0     | Left Channel Mute Disabled                                     |
|       |           | 1     | Left Channel Mute Enabled                                      |

**Table 5. Volume Control**

| Volume Step | VOL4 | VOL3 | VOL2 | VOL1 | VOL0 | HP Gain (dB) |
|-------------|------|------|------|------|------|--------------|
| 0           | 0    | 0    | 0    | 0    | 0    | -59          |
| 1           | 0    | 0    | 0    | 0    | 1    | -55          |
| 2           | 0    | 0    | 0    | 1    | 0    | -51          |
| 3           | 0    | 0    | 0    | 1    | 1    | -47          |
| 4           | 0    | 0    | 1    | 0    | 0    | -43          |
| 5           | 0    | 0    | 1    | 0    | 1    | -39          |
| 6           | 0    | 0    | 1    | 1    | 0    | -35          |
| 7           | 0    | 0    | 1    | 1    | 1    | -31          |
| 8           | 0    | 1    | 0    | 0    | 0    | -27          |
| 9           | 0    | 1    | 0    | 0    | 1    | -25          |
| 10          | 0    | 1    | 0    | 1    | 0    | -23          |
| 11          | 0    | 1    | 0    | 1    | 1    | -21          |
| 12          | 0    | 1    | 1    | 0    | 0    | -19          |
| 13          | 0    | 1    | 1    | 0    | 1    | -17          |
| 14          | 0    | 1    | 1    | 1    | 0    | -15          |
| 15          | 0    | 1    | 1    | 1    | 1    | -13          |
| 16          | 1    | 0    | 0    | 0    | 0    | -11          |
| 17          | 1    | 0    | 0    | 0    | 1    | -10          |
| 18          | 1    | 0    | 0    | 1    | 0    | -9           |
| 19          | 1    | 0    | 0    | 1    | 1    | -8           |
| 20          | 1    | 0    | 1    | 0    | 0    | -7           |
| 21          | 1    | 0    | 1    | 0    | 1    | -6           |
| 22          | 1    | 0    | 1    | 1    | 0    | -5           |
| 23          | 1    | 0    | 1    | 1    | 1    | -4           |
| 24          | 1    | 1    | 0    | 0    | 0    | -3           |
| 25          | 1    | 1    | 0    | 0    | 1    | -2           |
| 26          | 1    | 1    | 0    | 1    | 0    | -1           |
| 27          | 1    | 1    | 0    | 1    | 1    | 0            |
| 28          | 1    | 1    | 1    | 0    | 0    | 1            |
| 29          | 1    | 1    | 1    | 0    | 1    | 2            |
| 30          | 1    | 1    | 1    | 1    | 0    | 3            |
| 31          | 1    | 1    | 1    | 1    | 1    | 4            |

**Table 6. Output Control Register**

| Bit | Name    | Value | Description                                |
|-----|---------|-------|--|
| B0  | HiZ_R   | 0     | Right channel high impedance mode disabled |
|     |         | 1     | Right channel high impedance mode enabled  |
| B1  | HiZ_L   | 0     | Left channel high impedance mode disabled  |
|     |         | 1     | Left channel high impedance mode enabled   |
| B3  | LOW_THD | 0     | LOW_THD mode disabled                      |
|     |         | 1     | LOW_THD mode enabled, improves overall THD |

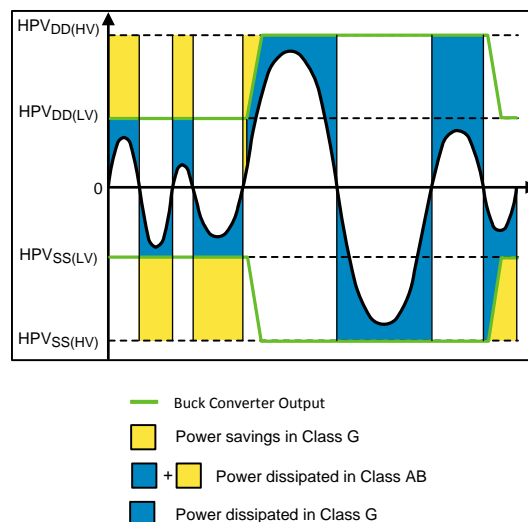
## GENERAL DEVICE FUNCTION

The LM48824 integrates a high efficiency step down (buck) DC-DC switching regulator with a ground reference headphone amplifier. The switching regulator delivers a constant voltage from an input voltage ranging from 2.4V to 5.5V. The switching regulator uses a voltage-mode architecture with synchronous rectification, improving efficiency and reducing component count.

The LM48824 headphone amplifier features TI's ground referenced architecture that eliminates the large DC-blocking capacitors required at the outputs of traditional single-ended headphone amplifiers. A low-noise inverting charge pump creates a negative supply (HPV<sub>SS</sub>) from the positive supply voltage (V<sub>DD</sub>). The headphone amplifiers operate from these bipolar supplies, with the amplifier outputs biased about GND. Because there is no DC component on the output signals, the large DC-blocking, AC coupling capacitors (typically 220µF) are not necessary, conserving board space, reducing system cost, and improving frequency response.

## CLASS G OPERATION

Class G is a modification of some other class of amplifier (normally Class B or Class AB) to increase efficiency and reduce power dissipation. Class G works off the fact that musical and voice signals have a high peak to mean ratio with most of the signal content at low levels. To decrease power dissipation, Class G has multiple voltage supplies. The LM48824 has two discrete voltage supplies at the output of the buck, 1.1V and 1.8V. When the output reached the threshold to switch to the higher voltage rails, the rails will switch from 1.1V to 1.8V. When the output falls below the required voltage rails for a set period of time, it will switch back to the lower rail until the next time the threshold is reached. Power dissipation is greatly reduced for typical musical or voice sources. The drawing below shows how a musical output may look. The green lines are the supply voltages at the output of the buck converter.



**Figure 33. Class G Operation**

## DIFFERENTIAL AMPLIFIER EXPLANATION

The LM48824 features a differential input stage, which offers improved noise rejection compared to a single-ended input amplifier. Because a differential input amplifier amplifies the difference between the two input signals, any component common to both signals is cancelled.

## SYNCHRONOUS RECTIFIER

The buck converter in the LM48824 uses an internal NFET synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relative low compared to the voltage drop across an ordinary rectifier diode and eliminating the need for the diode.

## CURRENT LIMITING

A current limit of the buck converter in the LM48824 allows the device to protect itself and external components during overload conditions.

## PFM OPERATION

During PFM(Pulse-Frequency Modulation) operation, if the output voltage of the buck converter is below the 'high' PFM comparator threshold, the PMOS power switch is turned on. It remains on until the output voltage reaches the 'high' PFM threshold or the peak current exceeds the  $I_{PFM}$  level set for PFM mode. The typical peak current in PFM mode is  $I_{PFM} = 112\text{mA} + V_{DD}/27\Omega$ .

Once the PMOS power switch is turned off, the NMOS power switch is turned on until the inductor current ramps to zero. When the NMOS zero-current condition is detected, the NMOS power switch is turned off. If the output voltage is below the 'high' PFM comparator threshold, the PMOS switch is again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the 'high' PFM threshold, the NMOS switch is turned on briefly to ramp the inductor current to zero and then both output switches are turned off and the part enters an extremely low power mode.

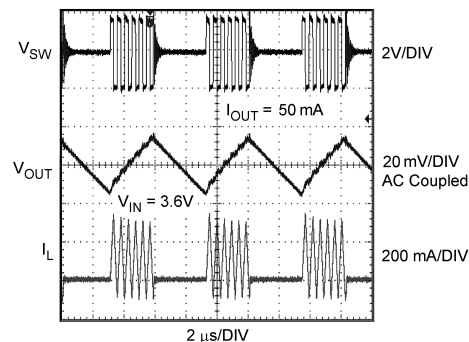


Figure 34. PFM Operation

## SOFT START

The buck converter has a soft-start circuit that limits in-rush current during start-up. During start-up the switch current limit is increased in steps. Soft start is activated only if global SHDN goes from 1 to 0 after  $V_{DD}$  reaches 2.7V. Soft start is implemented by increasing switch current limit in steps of 70mA, 140mA, 280mA, and 750mA (typical switch current limit). The start-up time thereby depends on the output capacitor and load current of the buck converter. Typical start-up times with a 10 $\mu\text{F}$  output capacitor and 150mA load is 280 $\mu\text{s}$  and with 5mA load is 240 $\mu\text{s}$ .



## COMMON-MODE SENSE

The LM48824 features a ground (common mode) sensing feature. In noisy applications, or where the headphone jack is used as a line out to other devices, noise pick up and ground imbalance can degrade audio quality. The LM48824 COM input senses and corrects any noise at the headphone return, or any ground imbalance between the headphone return and device ground, improving audio reproduction. Connect COM directly to the headphone return terminal of the headphone jack (Figure 35). No additional external components are required. Connect COM to GND if the common-mode sense feature is not in use.

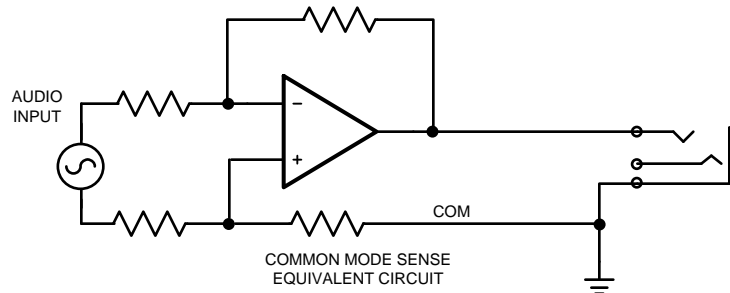


Figure 35. COM Connection

## SHUTDOWN FUNCTION

The LM48824 features individual amplifier shutdown control and a global device shutdown control.

Bit B0 (SHDN) of the MODE CONTROL register controls the global shutdown for the entire device. Set SHDN = 1 to put the device into current-saving shutdown mode, and set SHDN = 0 for normal operation. SHDN defaults to 1 at power-up.

Bit B7 (HPL\_EN) and Bit B6 (HPR\_EN) of the MODE CONTROL register (register address 0x01h) controls the left and right headphone amplifier shutdown respectively. Set HPL\_EN = 0 to set the left channel headphone amplifier to shutdown and set HPL\_EN = 1 to enable left channel operation. Set HPR\_EN = 0 to set the right channel headphone amplifier to shutdown and set HPR\_EN = 1 to enable right channel operation. The left and right channel amplifier shutdowns operate individually.

The LM48824 has a shutdown time of 3ms to complete the internal shutdown sequence. After SHDN is set to 1, any new I<sup>2</sup>C commands should only be sent after the 3ms shutdown time to ensure proper operation of the device.

## MUTE FUNCTION

The LM48824 features independent left and right channel mute functions.

Bit B7 (MUTE\_L) and Bit B6 (MUTE\_R) of the VOLUME CONTROL register (register address 0x02h) controls the mute function of the left and right channels respectively. Set MUTE\_L = 1 to mute the left channel and set the MUTE\_R = 1 to mute the right channel. Set MUTE\_L = 0 and MUTE\_R = 0 to disable mute on the respective channels. MUTE\_L and MUTE\_R defaults to 1 at power-up.

## LOW THD+N MODE

The LM48824 features a Low THD mode that reduces THD+N to improve audio quality. Set B3 (Low\_THD) of the OUTPUT CONTROL register (register address 0x03h) to 1 to enable the Low THD mode. There is a quiescent and operating current increase in Low THD mode. See [Electrical Characteristics](#) and [Typical Performance Characteristics](#) for reference.

## PROPER SELECTION OF EXTERNAL COMPONENTS

### INDUCTOR SELECTION

There are two main considerations when choosing an inductor; the inductor saturation current and the inductor current ripple should be small enough to achieve the desired output voltage ripple. Different saturation current rating specifications are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C, ratings at the maximum ambient temperature of application should be requested from the manufacturer. Shielded capacitors are preferred since these capacitors radiate less noise. Inductors with low DCR should also be considered to minimize the efficiency.

Inductor value involves trade-offs in performance. Larger inductors reduce inductor triple current, which typically means less output voltage ripple (for a given size of output capacitor).

### REGULATOR INPUT CAPACITOR SELECTION (C3)

A ceramic input capacitor of 1 $\mu$ F, 6.3V is sufficient for most applications. Place the input capacitor as close as possible to the V<sub>DD</sub> pin of the device. A larger value may be used for improved input voltage filtering. Use X7R or X5R types; do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603.

### REGULATOR OUTPUT CAPACITOR SELECTION (C4)

A low ESR ceramic output capacitor of 10 $\mu$ F, 6.3V is sufficient for most applications. Use X7R or X5R types; do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. DC bias characteristics vary from manufacturer to manufacturer and dc bias curves should be requested from them as part of the capacitor selection process.

### CHARGE PUMP CAPACITOR SELECTION

Use low ESR ceramic capacitors (less than 100m $\Omega$ ) for optimum performance.

### CHARGE PUMP FLYING CAPACITOR (C1)

The flying capacitor (C1) affects the load regulation and output impedance of the charge pump. A C1 value that is too low results in a loss of current drive, leading to a loss of amplifier headroom. A higher valued C1 improves load regulation and lowers charge pump output impedance to an extent. Above 2.2 $\mu$ F, the R<sub>DS(ON)</sub> of the charge pump switches and the ESR of C1 and C2 dominate the output impedance. A lower value capacitor can be used in systems with low maximum output power requirements.

### CHARGE PUMP HOLD CAPACITOR (C2)

The value and ESR of the hold capacitor (C2) directly affects the ripple on CPV<sub>SS</sub>. Increasing the value of C2 reduces output ripple. Decreasing the ESR of C2 reduces both output ripple and charge pump output impedance. A lower value capacitor can be used in systems with low maximum output power requirements.

### Amplifier Input Capacitor Selection

Input capacitors may be required for some applications, or when the audio source is single-ended. Input capacitors block the DC component of the audio signal, eliminating any conflict between the DC component of the audio source and the bias voltage of the LM48824. The input capacitors create a high-pass filter with the input resistors R<sub>IN</sub>. The -3dB point of the high-pass filter is found using the equation below.

$$f = 1 / 2\pi R_{IN} C_{IN} \quad (\text{Hz}) \quad (1)$$

Where the value of R<sub>IN</sub> is given in the [Electrical Characteristics VDD = 3.6V](#).

High-pass filtering the audio signal can be beneficial for some applications. When the LM48824 is using a single-ended source, power supply noise on the ground is seen as an input signal. Setting the high-pass filter point above the power supply noise frequencies, 217Hz in a GSM phone, for example, filters out the noise such that it is not amplified and heard on the output. Capacitors with a tolerance of 10% or better are recommended for impedance matching and improved CMRR and PSRR.

## SINGLE-ENDED AUDIO AMPLIFIER CONFIGURATION

The LM48824 is compatible with single-ended sources. Figure 36 shows the typical single-ended applications circuit. Input coupling capacitors are required for single-ended configuration.

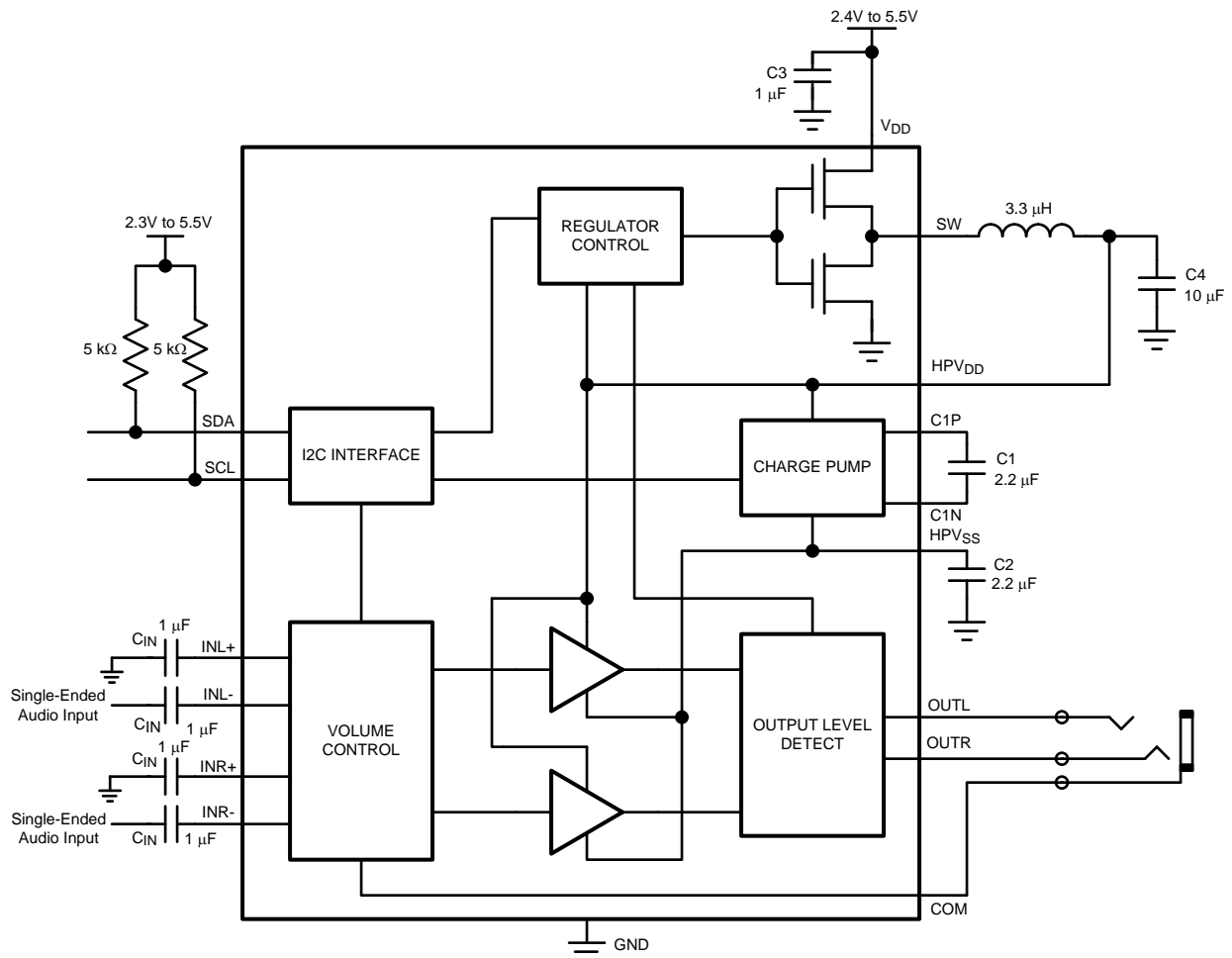


Figure 36. Single-Ended Input Configuration

## PCB LAYOUT CONFIGURATION

Table 7. LM48824TM Demoboard Bill of Materials

| Designator | Quantity | Description   |
|------------|----------|---|
| C1         | 1        | 10µF ±10% 16V 500Ω Tantalum Capacitor (B Case) AVX TPSB106K016R0500 |
| C2         | 1        | 1µF ±10% 16V X5R Ceramic Capacitor (603) Panasonic ECJ-1VB1C105K    |
| C3, C8, C9 | 3        | 2.2µF ±10% 10V X5R Ceramic Capacitor (603) Panasonic ECJ-1VB1A225K  |
| C4 – C7    | 4        | 1µF ±10% 16V X7R Ceramic Capacitor (1206) Panasonic ECJ-3YB1C105K   |
| R1, R2     | 2        | 5kΩ ±5% 1/10W Thick Film Resistor (603) Vishay CRCW06035R1KJNEA     |
| L1         | 1        | 3.3µH ± 30% 1.2A Inductor Murata LQM2MPN3R3NG0L                     |
| J1         | 1        | Stereo Headphone Jack   |
| J2         | 1        | 16-Pin Boardmount Socket 3M 8516-4500JL                             |
| JU1        | 1        | 3 Pin Header  |
| JU2        | 1        | 2 Pin Header  |
| LM4822TM   | 1        | LM48824TM (16-Bump microSMD)  |

Demoboard Schematic

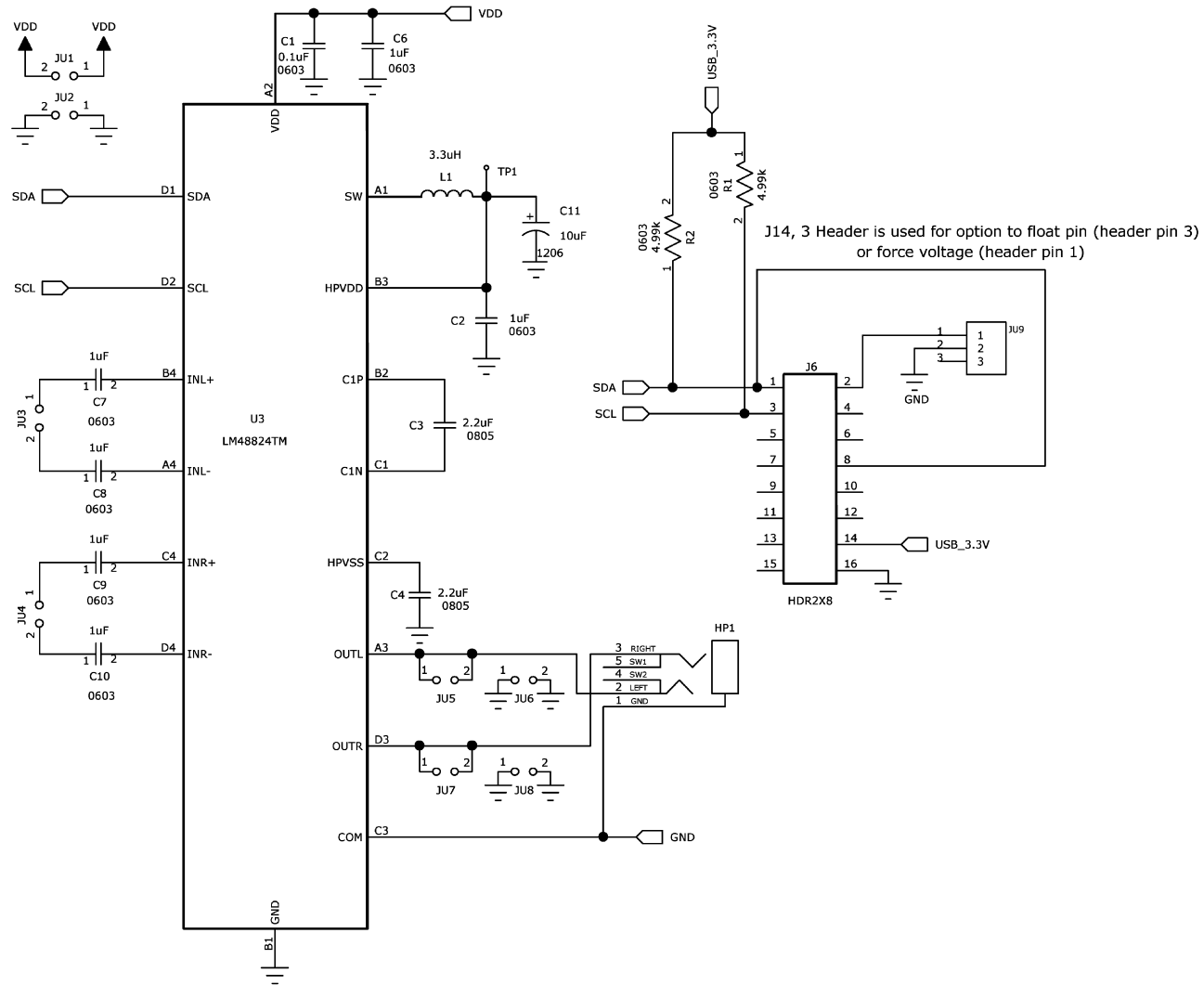


Figure 37. LM48824 Demoboard Schematic

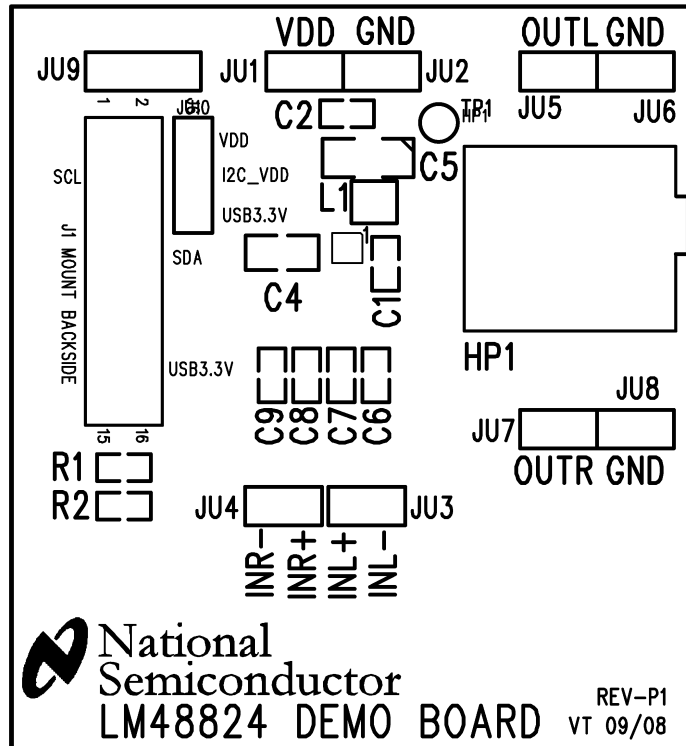


Figure 38. Top Silkscreen

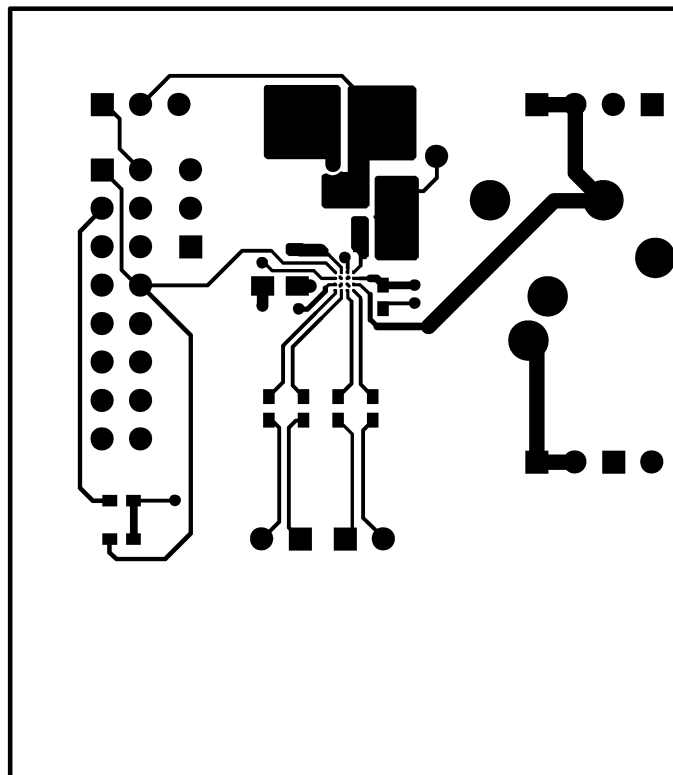


Figure 39. Top Layer

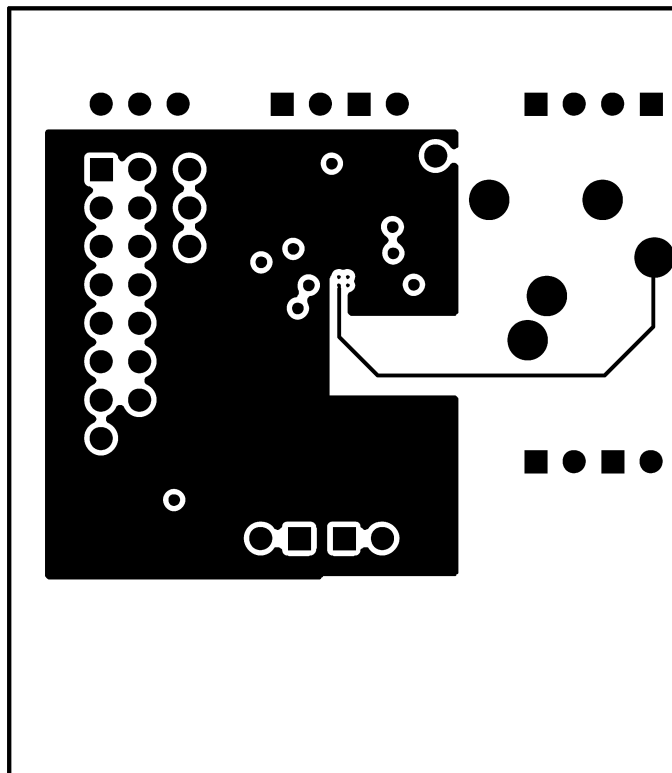


Figure 40. Layer 2 (GND)

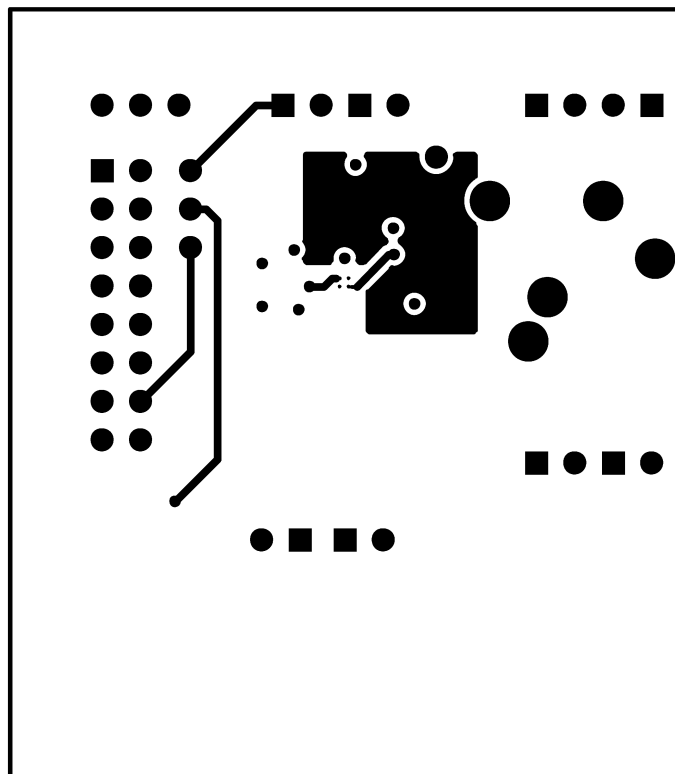


Figure 41. Layer 3 (VDD)

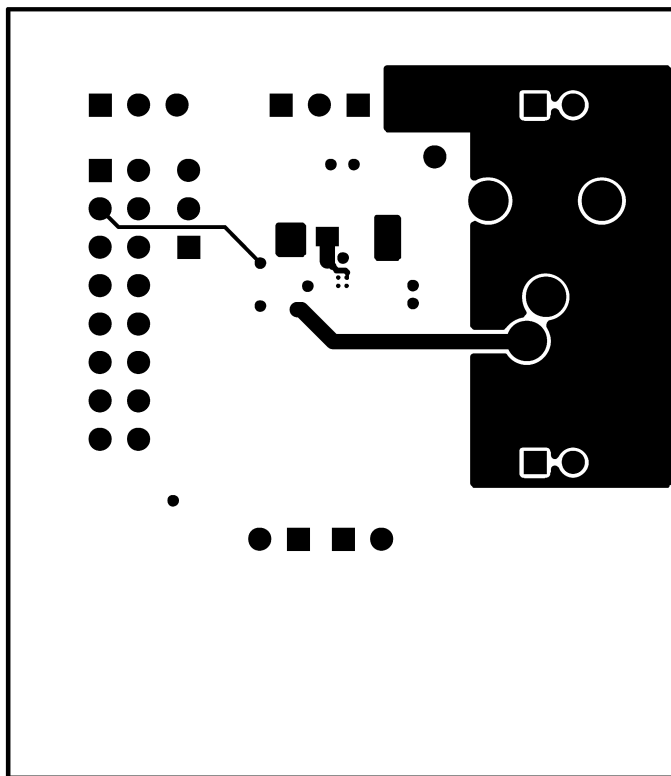


Figure 42. Bottom Layer

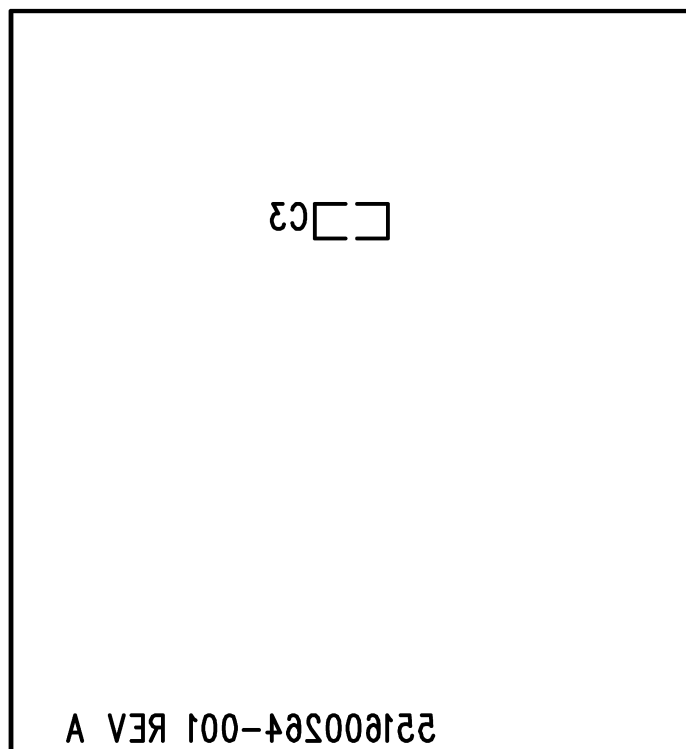


Figure 43. Bottom Silkscreen

### Revision History

| Rev  | Date       | Description   |
|------|------------|---|
| 1.0  | 08/06/09   | Initial released of the full datasheet.             |
| 1.01 | 08/31/09   | Text edits.   |
| D    | 05/02/2013 | Changed layout of National Data Sheet to TI format. |



**PACKAGING INFORMATION**

| Orderable part number           | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|---------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">LM48824TM/NOPB</a>  | Active        | Production           | DSBGA (YFQ)   16 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 85    | GL6                 |
| LM48824TM/NOPB.A                | Active        | Production           | DSBGA (YFQ)   16 | 250   SMALL T&R       | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 85    | GL6                 |
| <a href="#">LM48824TMX/NOPB</a> | Active        | Production           | DSBGA (YFQ)   16 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 85    | GL6                 |
| LM48824TMX/NOPB.A               | Active        | Production           | DSBGA (YFQ)   16 | 3000   LARGE T&R      | Yes         | SNAGCU                               | Level-1-260C-UNLIM                | -40 to 85    | GL6                 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

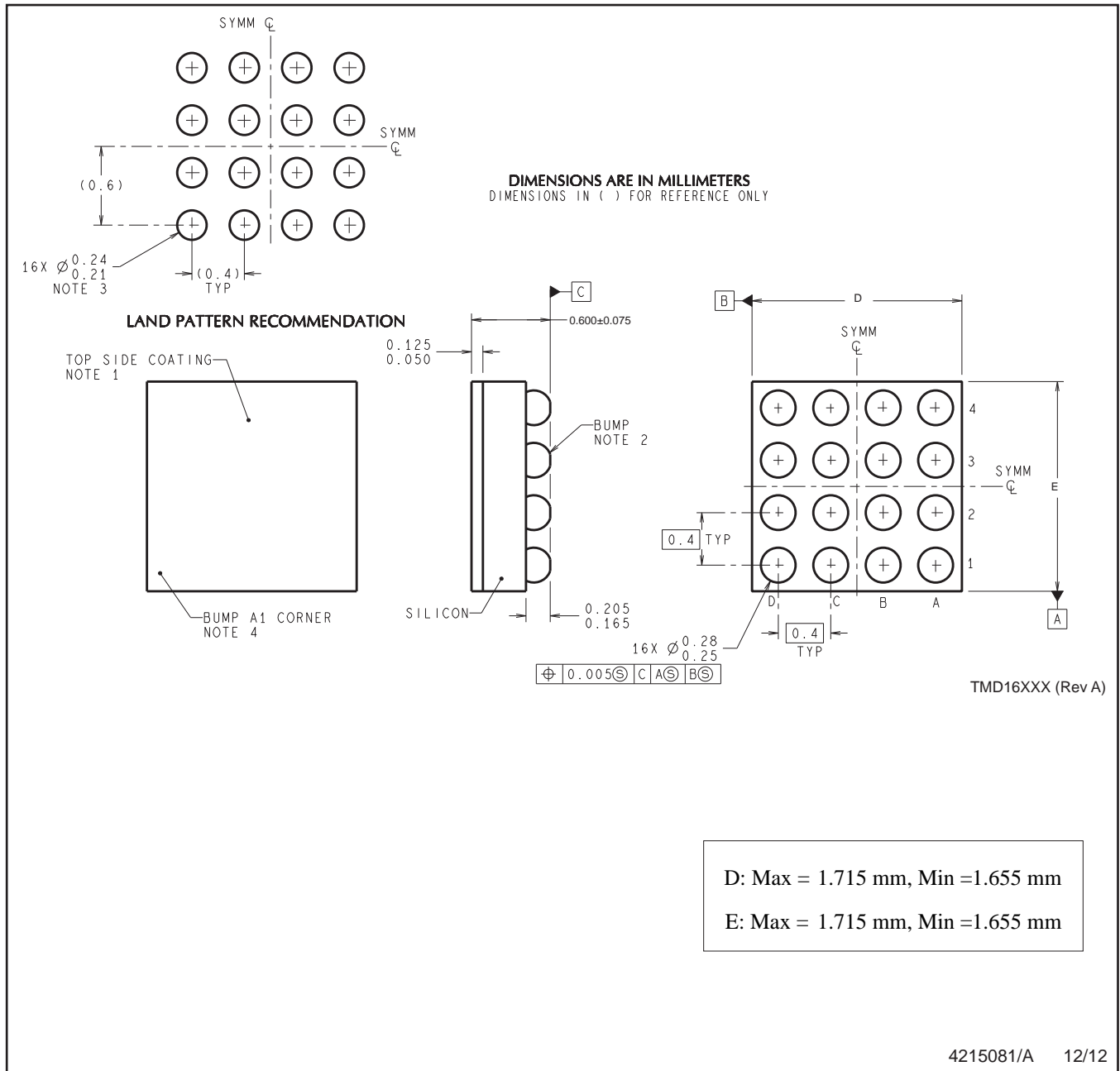
| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LM48824TM/NOPB  | DSBGA        | YFQ             | 16   | 250  | 178.0              | 8.4                | 1.85    | 2.01    | 0.76    | 4.0     | 8.0    | Q1            |
| LM48824TMX/NOPB | DSBGA        | YFQ             | 16   | 3000 | 178.0              | 8.4                | 1.85    | 2.01    | 0.76    | 4.0     | 8.0    | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LM48824TM/NOPB  | DSBGA        | YFQ             | 16   | 250  | 208.0       | 191.0      | 35.0        |
| LM48824TMX/NOPB | DSBGA        | YFQ             | 16   | 3000 | 208.0       | 191.0      | 35.0        |

YFQ0016



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  
B. This drawing is subject to change without notice.

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