LMC649x Dual and Quad, CMOS, Rail-to-Rail Input/Output Operational Amplifiers

1 Features

- Rail-to-rail input common-mode voltage range, specified over temperature
- Rail-to-rail output swing within 100mV of supply rail, 2kΩ load
- Can operate on standard 5V and 15V supplies
- Excellent CMRR and PSRR: 82dB
- Ultra-low input current: 150fA
- Low supply current (at V_S = 5V): 500µA/amplifier
- Low offset voltage drift: 1.0µV/°C

2 Applications

- Automotive transducer amplifier
- Pressure sensor
- Oxygen sensor
- Temperature sensor
- Speed sensor

3 Description

The LMC6492 and LMC6494 (LMC649x) amplifiers were specifically developed for single-supply applications that operate from −40°C to +125°C. This feature is an excellent choice for automotive systems because of the wide temperature range. A unique design topology enables the LMC649x common-mode voltage range to accommodate input signals beyond the rails. This eliminates non-linear output errors due to input signals exceeding a traditionally limited common-mode voltage range. The LMC649x signal range has a high CMRR of 82dB for excellent accuracy in noninverting circuit configurations.

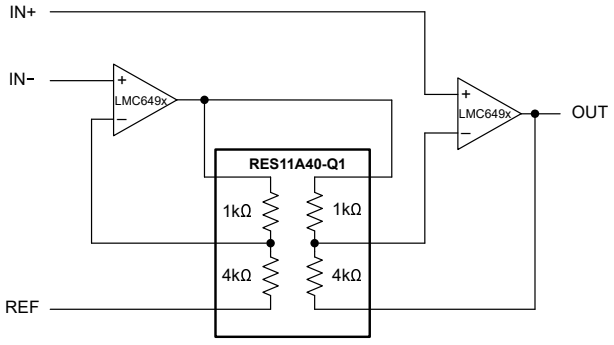
The LMC649x rail-to-rail input is complemented by rail-to-rail output swing. This configuration provides maximum dynamic signal range and is particularly important in 5V systems.

An ultra-low input current of 150fA and a 120dB open-loop gain provide high accuracy and direct interfacing with high-impedance sources.

Device Information

PART NUMBER	CHANNEL COUNT	PACKAGE(1)
LMC6492	Dual	D (SOIC, 8)
LMC6494	Quad	D (SOIC, 14)

(1) For more information, see Section 9.



Two-Op-Amp Instrumentation Amplifier Using the RES11A-Q1

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4 Pin Configuration and Functions

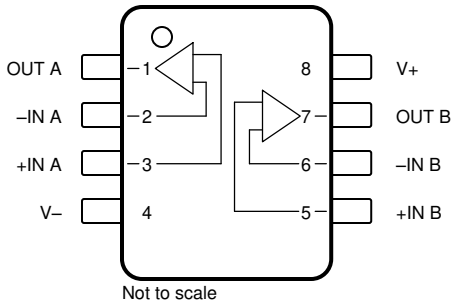


Figure 4-1. LMC6492: D Package, 8-Pin SOIC (Top View)

Table 4-1. Pin Functions: LMC6492

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	OUT A	Output	Output for amplifier A
2	−IN A	Input	Inverting input for amplifier A
3	+IN A	Input	Noninverting input for amplifier A
4	V–	Power	Negative supply voltage input
5	+IN B	Input	Noninverting input for amplifier B
6	−IN B	Input	Inverting input for amplifier B
7	OUT B	Output	Output for amplifier B
8	V+	Power	Positive supply voltage input

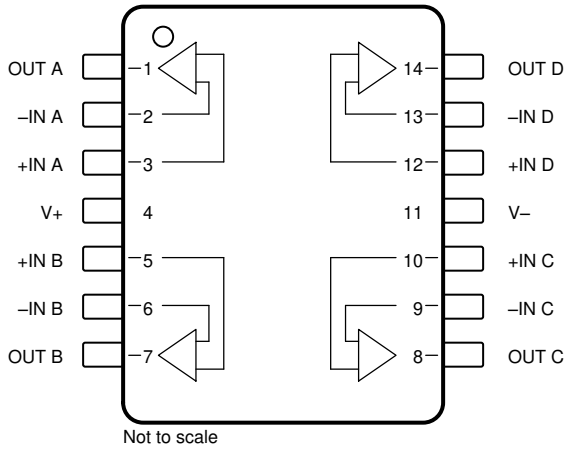


Figure 4-2. LMC6494: D Package, 14-Pin SOIC (Top View)

Table 4-2. Pin Functions: LMC6494

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	OUT A	Output	Output for amplifier A
2	−IN A	Input	Inverting input for amplifier A
3	+IN A	Input	Noninverting input for amplifier A
4	V+	Power	Positive supply voltage input
5	+IN B	Input	Noninverting input for amplifier B
6	−IN B	Input	Inverting input for amplifier B
7	OUT B	Output	Output for amplifier B
8	OUT C	Output	Output for amplifier C
9	−IN C	Input	Inverting input for amplifier C
10	+IN C	Input	Noninverting input for amplifier C
11	V–	Power	Negative supply voltage input
12	+IN C	Input	Inverting input for amplifier D
13	+IN C	Input	Noninverting input for amplifier D
14	OUT C	Output	Output for amplifier D

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted [1] [2]

		MIN	MAX	UNIT
	Differential input voltage		±Supply Voltage	
	Voltage at input/output pin	(V–) – 0.3	(V+) + 0.3	V
V_S	Supply voltage, V_S = (V+) – (V–)		16	V
	Current at input pin	–5	5	mA
	Current at output pin [3]	–30	30	mA
	Current at power supply pin		40	mA
	Lead temperature (soldering, 10 sec)		260	°C
T_{STG}	Storage temperature	–65	150	°C
T_J	Junction temperature [4]		150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) If military- or aerospace-specified devices are required, please contact the TI Sales Office or Distributors for availability and specifications.
(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30mA over a long term can adversely affect reliability.
(4) The maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly into a printed circuit board (PCB).

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	2.5		15.5	V
T_J	Junction temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRIC[1]		LMC6492 D (SOIC) 8 PINS	LMC6494 D (SOIC) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	128.9	83.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	68.6	42.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.4	42.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	19.7	7.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	71.6	42.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

at T_J = +25°C, V+ = 5V, V– = 0V, V_{CM} = V_{OUT} = V+ / 2, and R_L > 1MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC SPECS							
V_{OS}	Input offset voltage	LMC649xAE			±0.11	±3	mV
			T_A = –40°C to +125°C			±3.8	
		LMC649xBE			±0.11	±6	
			T_A = –40°C to +125°C			±6.8	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C			±1		µV/°C
I_B	Input bias current				±0.15		pA
		T_A = –40°C to +125°C				±200	
I_{OS}	Input offset current				±0.075		pA
		T_A = –40°C to +125°C				±100	
C_{IN}	Common-mode input capacitance				3		pF
R_{IN}	Input resistance				>10		TΩ
CMRR	Common-mode rejection ratio	LMC649xAE 0V ≤ V_{CM} ≤ 15V, V+ = 15V		65	82		dB
			T_A = –40°C to +125°C	60			
		LMC649xBE 0V ≤ V_{CM} ≤ 15V, V+ = 15V		63	82		
			T_A = –40°C to +125°C	58			
		LMC649xAE 0V ≤ V_{CM} ≤ 5V, V+ = 5V		65	82		
			T_A = –40°C to +125°C	60			
		LMC649xBE 0V ≤ V_{CM} ≤ 5V, V+ = 5V		63	82		
			T_A = –40°C to +125°C	58			
+PSRR	Positive power-supply rejection ratio	LMC649xAE 5V ≤ V+ ≤ 15V, V– = 0V, V_O = 2.5V		65	82		dB
			T_A = –40°C to +125°C	60			
		LMC649xBE 5V ≤ V+ ≤ 15V, V– = 0V, V_O = 2.5V		63	82		
			T_A = –40°C to +125°C	58			
–PSRR	Negative power-supply rejection ratio	LMC649xAE –5V ≤ V– ≤ –15V, V+ = 0V, V_O = –2.5V		65	82		dB
			T_A = –40°C to +125°C	60			
		LMC649xBE –5V ≤ V– ≤ –15V, V+ = 0V, V_O = –2.5V		63	82		
			T_A = –40°C to +125°C	58			
V_{CM}	Input common-mode voltage	V+ = 5V and 15V, for CMRR ≥ 50dB	Low		(V–) – 0.3	–0.25	V
			Low, T_A = –40°C to +125°C			0	
			High	(V+) + 0.25	(V+) + 0.3		
			High, T_A = –40°C to +125°C	V+			
A_V	Large-signal voltage gain	Sourcing, R_L = 2kΩ to 7.5V, V+ = 15V, 7.5V ≤ V_O ≤ 11.5V			300		V/mV
		Sinking, R_L = 2kΩ to 7.5V, V+ = 15V, 3.5V ≤ V_O ≤ 7.5V			40		

5.5 Electrical Characteristics (continued)

at T_J = +25°C, V+ = 5V, V– = 0V, V_{CM} = V_{OUT} = V+ / 2, and R_L > 1MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Voltage output swing	V+ = 5V, R_L = 2kΩ to V+ / 2	Swing high	4.8	4.9		V
			Swing high, T_A = –40°C to +125°C	4.7			
			Swing low		0.1	0.18	
			Swing low, T_A = –40°C to +125°C			0.24	
		V+ = 5V, R_L = 600Ω to V+ / 2	Swing high	4.5	4.7		
			Swing high, T_A = –40°C to +125°C	4.24			
			Swing low		0.3	0.5	
			Swing low, T_A = –40°C to +125°C			0.65	
		V+ = 15V, R_L = 2kΩ to V+ / 2	Swing high	14.4	14.7		
			Swing high, T_A = –40°C to +125°C	14.0			
			Swing low		0.16	0.35	
			Swing low, T_A = –40°C to +125°C			0.5	
		V+ = 15V, R_L = 600Ω to V+ / 2	Swing high	13.4	14.1		
			Swing high, T_A = –40°C to +125°C	13			
			Swing low		0.5	1.0	
			Swing low, T_A = –40°C to +125°C			1.5	
I_{SC}	Output short-circuit current	V+ = 5V, sourcing, V_O = 0V		16	25		mA
			T_A = –40°C to +125°C	10			
		V+ = 5V, sinking, V_O = 5V		11	22		
			T_A = –40°C to +125°C	8			
		V+ = 15V, sourcing, V_O = 0V		28	30		
			T_A = –40°C to +125°C	20			
		V+ = 15V, sinking, V_O = 5V[1]		30	30		
			T_A = –40°C to +125°C	22			
I_S	Supply current	Per amplifier, V+ = 5V, V_O = V+ / 2			0.5	0.875	mA
			T_A = –40°C to +125°C			1.05	
		Per amplifier, V+ = 15V, V_O = V+ / 2			0.65	0.975	
			T_A = –40°C to +125°C			1.15	

5.5 Electrical Characteristics (continued)

at T_J = +25°C, V+ = 5V, V– = 0V, V_{CM} = V_{OUT} = V+ / 2, and R_L > 1MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC SPECS							
SR	Slew rate(2)	V+ = 15V, connected as voltage follower with 10V step		0.7	1.3		V/µs
			T_A = –40°C to +125°C	0.5			
GBW	Gain bandwidth	V+ = 15V			1.5		MHz
Θ_m	Phase margin				50		Deg
G_m	Gain margin				15		dB
	Amp-to-amp isolation	Input referred V+ = 15V, R_L = 100kΩ to 7.5V, V_O = 12V_{PP}, f = 1kHz			150		dB
e_n	Input-referred voltage noise	f = 1kHz, V_{CM} = 1V			37		nV/√Hz
i_n	Input current noise density	f = 1kHz			0.06		pA/√Hz
THD	Total harmonic distortion	f = 1kHz, A_V = –2, R_L = 10kΩ, V_O = –4.1V_{PP}			0.01		%
		f = 10kHz, A_V = –2, R_L = 10kΩ, V_O = 8.5V_{PP}, V+ = 10V			0.01		

(1) Do not short circuit output to V+ when V+ is greater than 13V or reliability is adversely affected.
(2) Specification established from device population bench system measurements across multiple lots. Number specified is the slower of either the positive or negative slew rates.

5.6 Typical Characteristics

at V_S = +15V, single supply, and T_A = 25°C (unless otherwise specified)

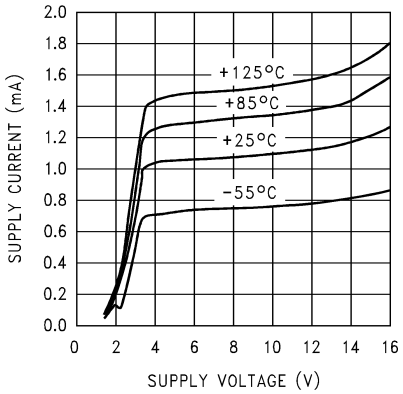


Figure 5-1. Supply Current vs Supply Voltage

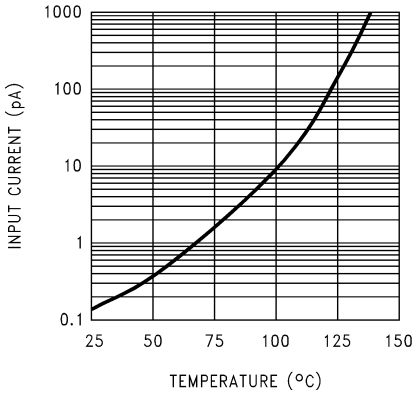


Figure 5-2. Input Current vs Temperature

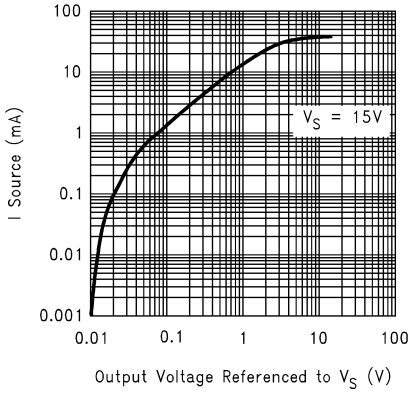


Figure 5-3. Sourcing Current vs Output Voltage

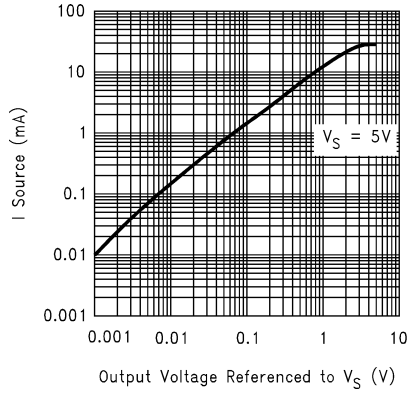


Figure 5-4. Sourcing Current vs Output Voltage

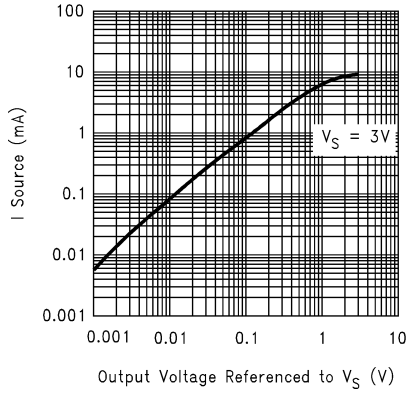


Figure 5-5. Sourcing Current vs Output Voltage

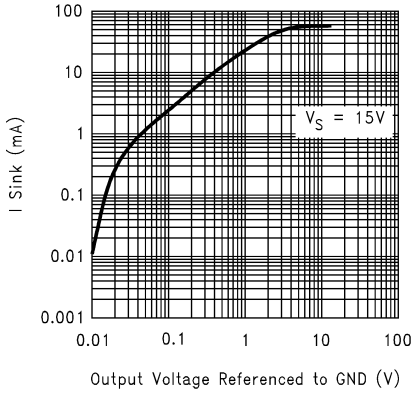


Figure 5-6. Sinking Current vs Output Voltage

5.6 Typical Characteristics (continued)

at V_S = +15V, single supply, and T_A = 25°C (unless otherwise specified)

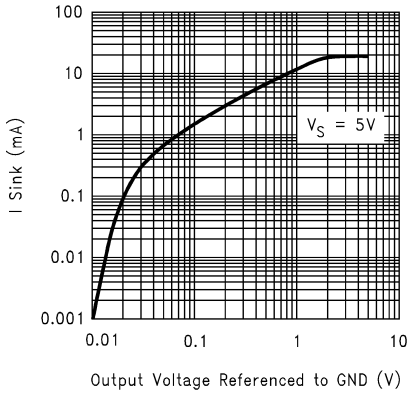


Figure 5-7. Sinking Current vs Output Voltage

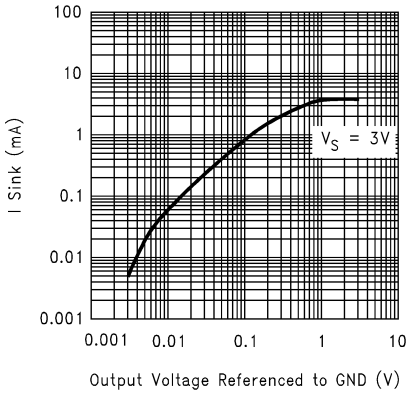


Figure 5-8. Sinking Current vs Output Voltage

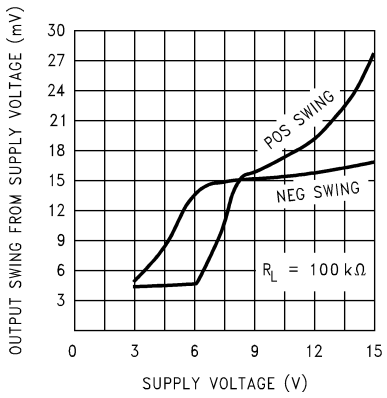


Figure 5-9. Output Voltage Swing vs Supply Voltage

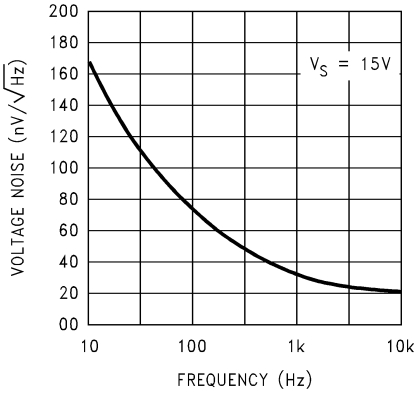


Figure 5-10. Input Voltage Noise vs Frequency

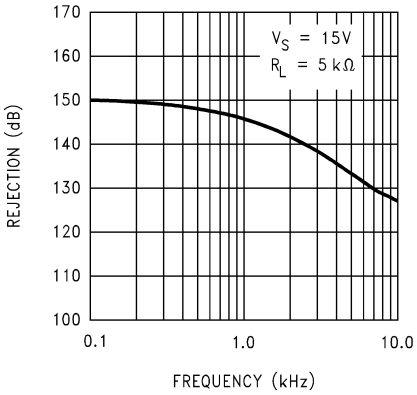


Figure 5-11. Crosstalk Rejection vs Frequency

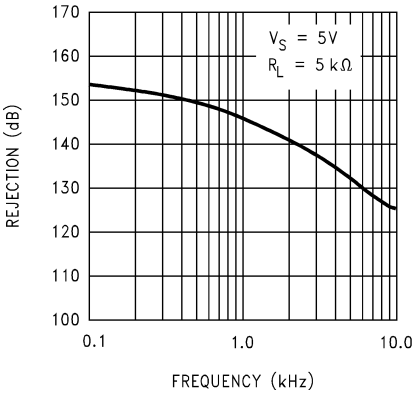


Figure 5-12. Crosstalk Rejection vs Frequency

5.6 Typical Characteristics (continued)

at V_S = +15V, single supply, and T_A = 25°C (unless otherwise specified)

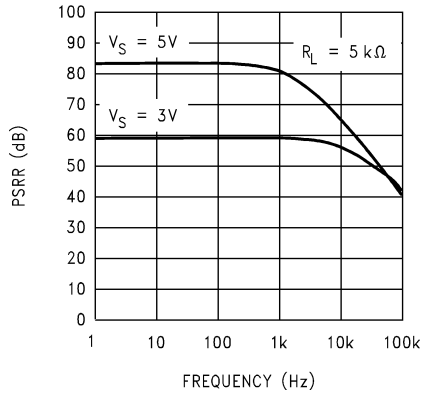


Figure 5-13. Positive PSRR vs Frequency

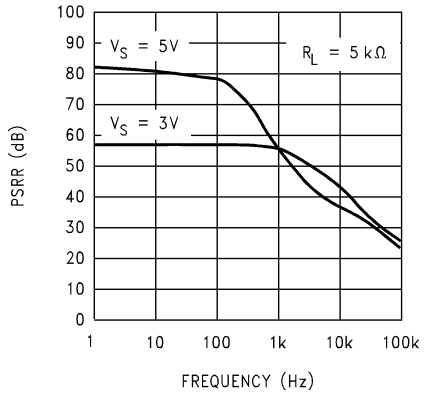


Figure 5-14. Negative PSRR vs Frequency

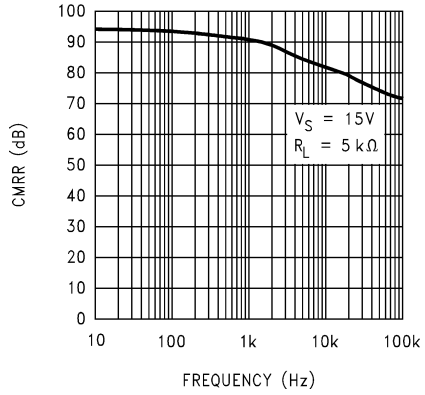


Figure 5-15. CMRR vs Frequency

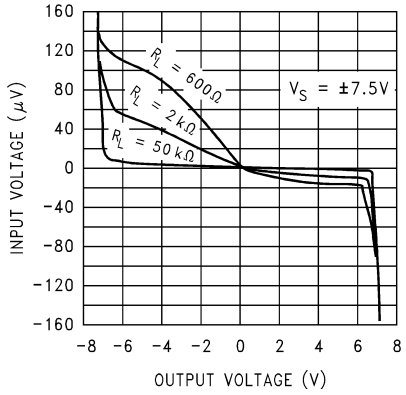


Figure 5-16. Input Voltage vs Output Voltage

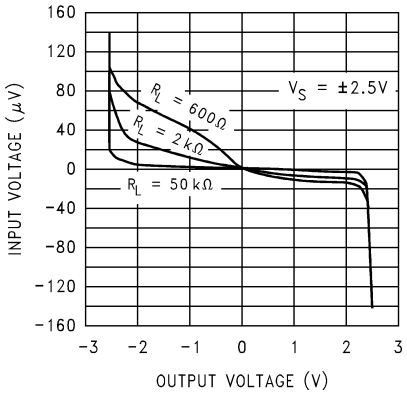


Figure 5-17. Input Voltage vs Output Voltage

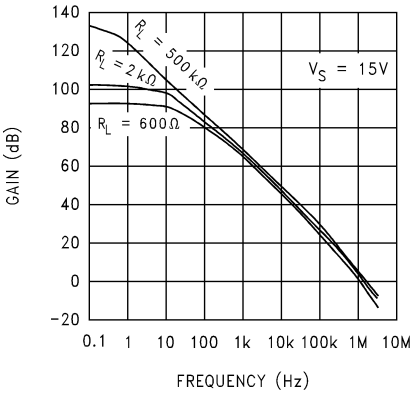


Figure 5-18. Open Loop Frequency Response

5.6 Typical Characteristics (continued)

at V_S = +15V, single supply, and T_A = 25°C (unless otherwise specified)

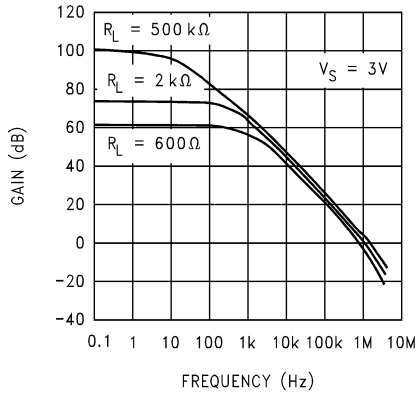


Figure 5-19. Open Loop Frequency Response

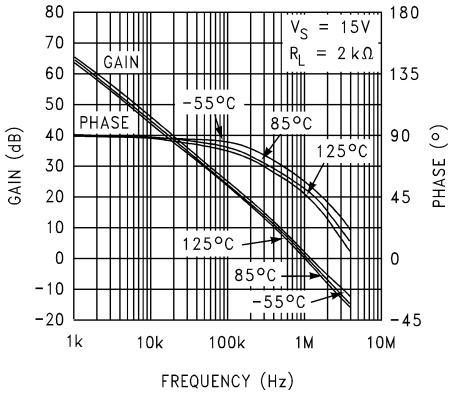


Figure 5-20. Open Loop Frequency Response vs Temperature

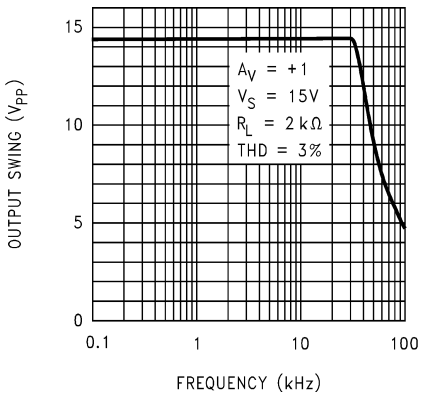


Figure 5-21. Maximum Output Swing vs Frequency

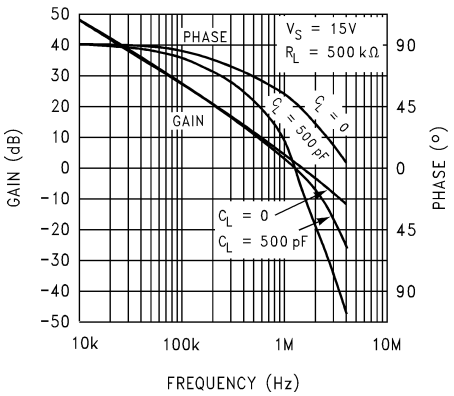


Figure 5-22. Gain and Phase vs Capacitive Load

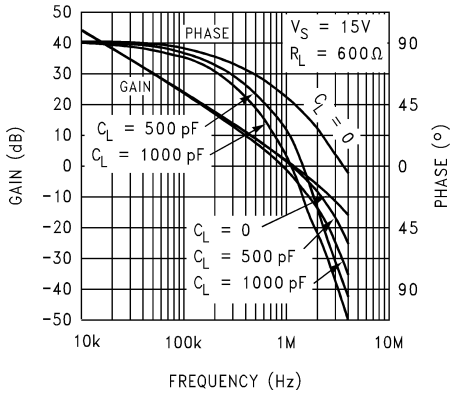


Figure 5-23. Gain and Phase vs Capacitive Load

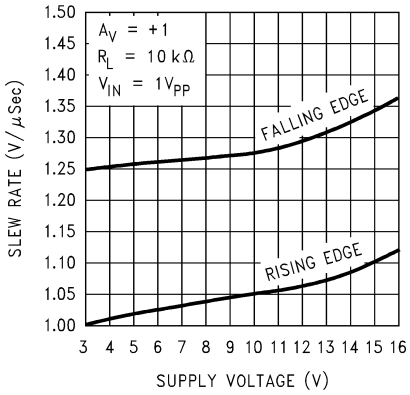


Figure 5-24. Slew Rate vs Supply Voltage

5.6 Typical Characteristics (continued)

at V_S = +15V, single supply, and T_A = 25°C (unless otherwise specified)

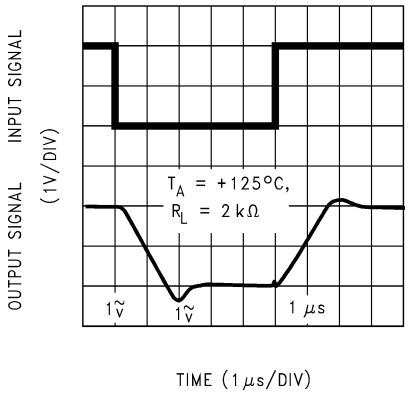


Figure 5-25. Non-Inverting Large Signal Pulse Response

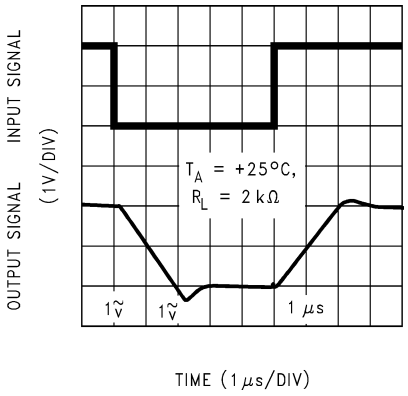


Figure 5-26. Non-Inverting Large Signal Pulse Response

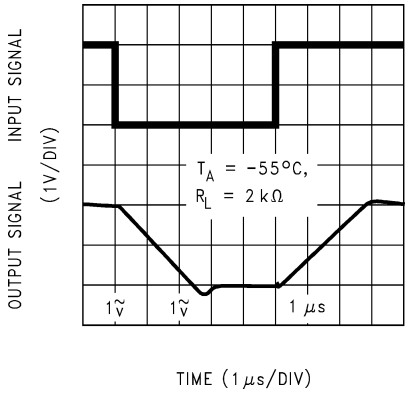


Figure 5-27. Non-Inverting Large Signal Pulse Response

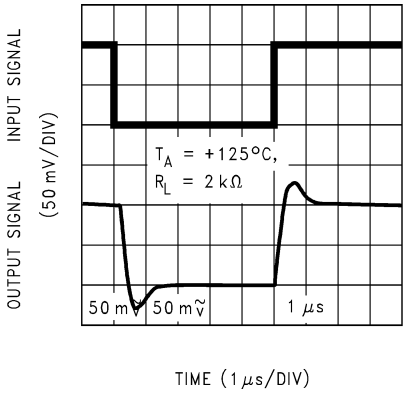


Figure 5-28. Non-Inverting Small Signal Pulse Response

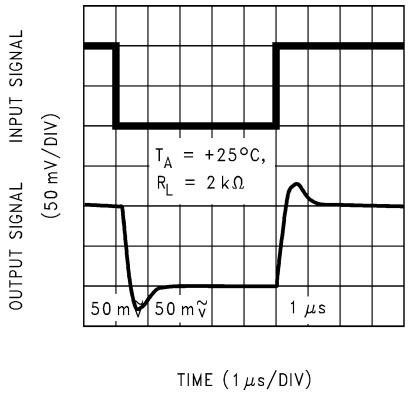


Figure 5-29. Non-Inverting Small Signal Pulse Response

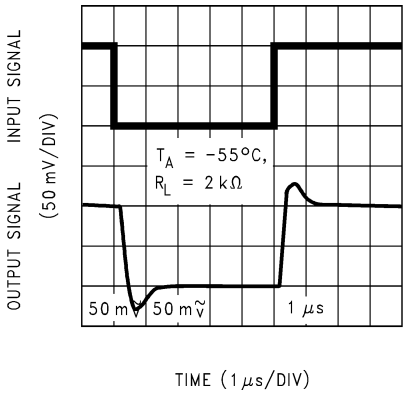


Figure 5-30. Non-Inverting Small Signal Pulse Response

5.6 Typical Characteristics (continued)

at V_S = +15V, single supply, and T_A = 25°C (unless otherwise specified)

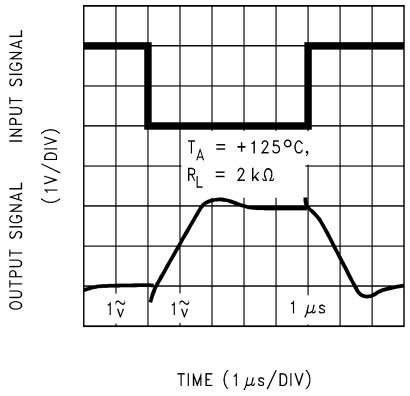


Figure 5-31. Inverting Large Signal Pulse Response

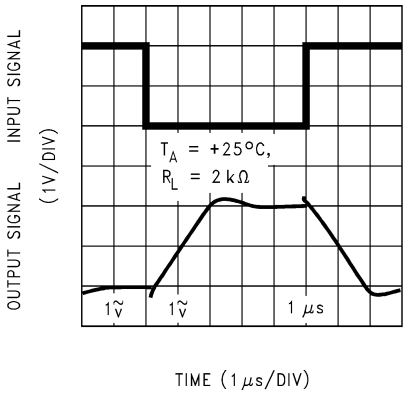


Figure 5-32. Inverting Large Signal Pulse Response

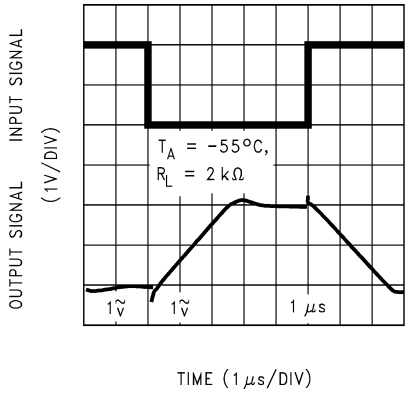


Figure 5-33. Inverting Large Signal Pulse Response

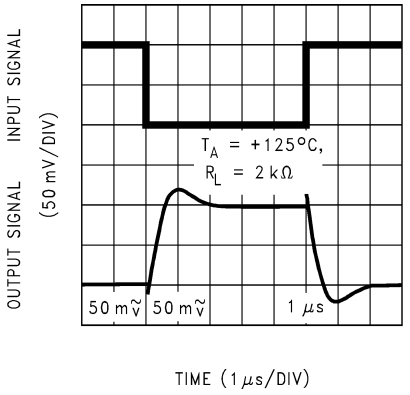


Figure 5-34. Inverting Small Signal Pulse Response

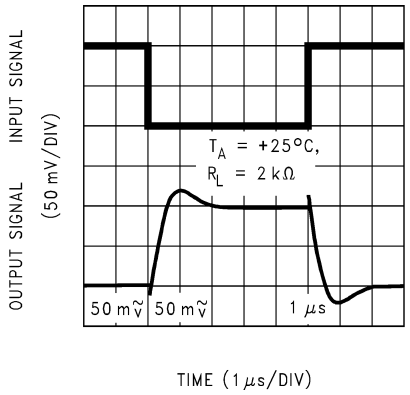


Figure 5-35. Inverting Small Signal Pulse Response

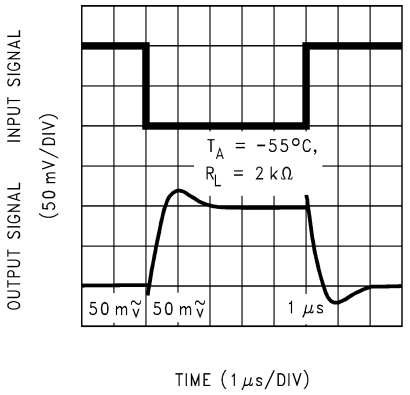


Figure 5-36. Inverting Small Signal Pulse Response

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

6.1.1 Input Common-Mode Voltage Range

Unlike Bi-FET amplifier designs, the LMC649x does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. Figure 6-1 shows an input voltage exceeding both supplies with no resulting phase inversion on the output.

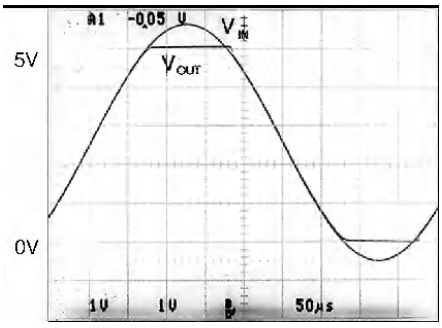


Figure 6-1. Input Voltage Signal Exceeds the LMC649x Power Supply Voltages With No Output Phase Inversion

The LMC649x is a true rail-to-rail input operational amplifier with an input common-mode range that extends beyond either supply rail. When the input common-mode voltage swings to about 3V from the positive rail, some dc specifications, namely offset voltage, can be slightly degraded. Figure 6-2 illustrates the input offset behavior across the entire common-mode range.

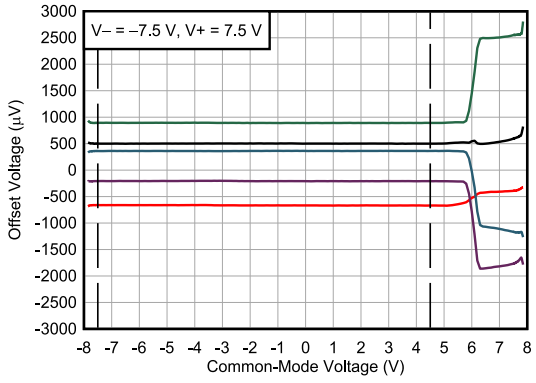


Figure 6-2. Input Offset Voltage vs Common-Mode Voltage

The absolute maximum input voltage is 300mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in Figure 6-3, can cause excessive current to flow in or out of the input pins possibly affecting reliability.

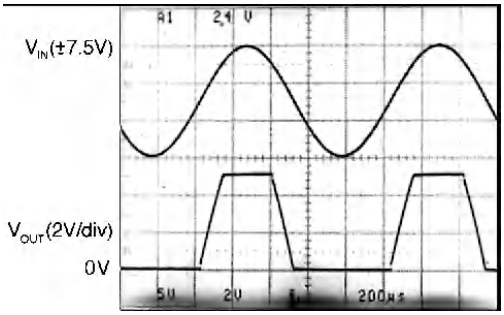


Figure 6-3. A ±7.5V Input Signal Greatly Exceeds the 5V Supply in Figure 6-3, Causing No Phase Inversion Due to R_I

Applications that exceed this rating must externally limit the maximum input current to ±5mA with an input resistor (R_I) as shown in Figure 6-4.

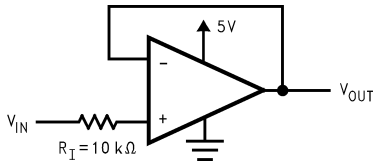


Figure 6-4. R_I Input Current Protection for Voltages Exceeding the Supply Voltages

6.1.2 Rail-to-Rail Output

The LMC649x output can swing to within a few hundred millivolts of either supply voltage. Using the specified output swing specifications, an approximate output resistance can be calculated for different sourcing and sinking conditions. Using the calculated output resistance, the maximum output voltage swing can be estimated as a function of load.

6.1.3 Compensating for Input Capacitance

Large values of feedback resistance are commonly used for amplifiers with ultra-low input current, such as the LMC649x.

Although the LMC649x is highly stable over a wide range of operating conditions, make sure that certain precautions are met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors with even small values of input capacitance (due to transducers, photodiodes, and circuit board parasitics) reduce phase margins.

When high input impedances are demanded, guarding of the LMC649x is suggested. Guarding input lines not only reduces leakage, but also lowers stray input capacitance. See Printed-Circuit-Board Layout for High Impedance Work.

The effect of input capacitance can be compensated by adding a capacitor, C_f, around the feedback resistors (as in Figure 6-1) so that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \quad (1)$$

or

$$R_1 C_{IN} \leq R_2 C_f \quad (2)$$

The exact value of C_{IN} is difficult to know; therefore, C_f can be experimentally adjusted so that the desired pulse response is achieved. See the LMC660 and LMC662 for a more detailed discussion on compensating for input capacitance.

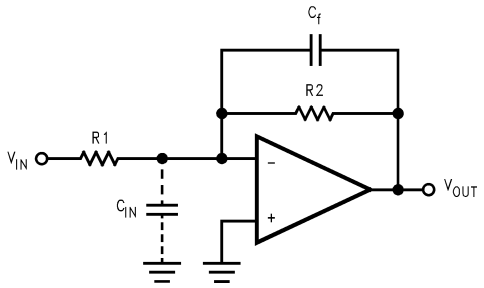


Figure 6-5. Canceling the Effect of Input Capacitance

6.1.4 Capacitive Load Tolerance

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominant pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see Typical Curves).

Direct capacitive loading reduces the phase margin of many op amps. A pole in the feedback loop is created by the combination of the op amp output impedance and the capacitive load. The open-loop output impedance of the LMC649x is shown in Figure 6-6. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in Figure 6-7.

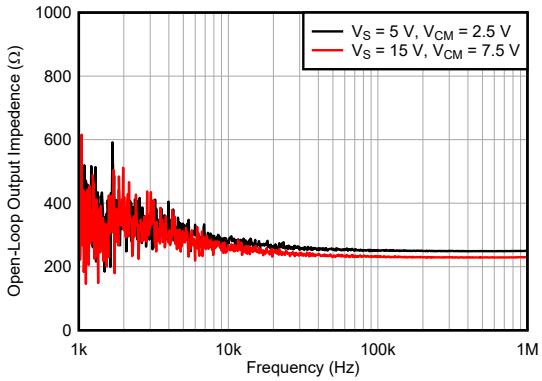


Figure 6-6. LMC649x Open-Loop Ouput Impedance

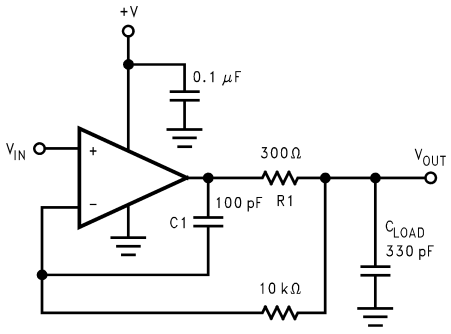
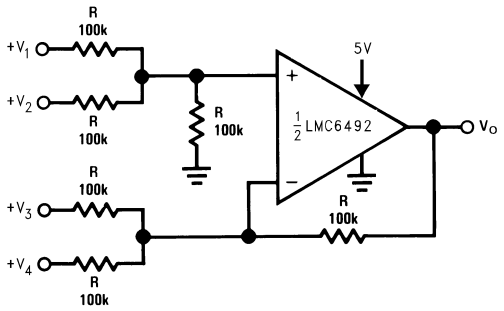


Figure 6-7. LMC649x Noninverting Amplifier, Compensated to Handle Capacitive Loads

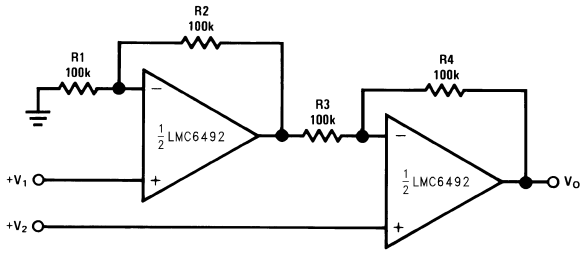
6.2 Typical Application

6.2.1 Application Circuits



Where: $V_0 = V_1 + V_2 - V_3 - V_4$
$(V_1 + V_2 \geq (V_3 + V_4)$ to keep $V_0 > 0V_{DC}$

Figure 6-8. DC Summing Amplifier ($V_{IN} \geq 0V_{DC}$ and $V_O \geq V_{DC}$



For

$$\frac{R1}{R2} = \frac{R4}{R3}$$

(CMRR depends on this resistor ratio match)

$$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$$

As shown: $V_O = 2(V_2 - V_1)$

Figure 6-9. High Input Z, DC Differential Amplifier

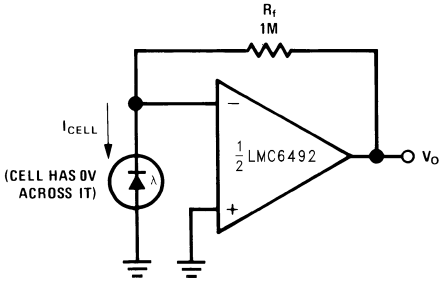
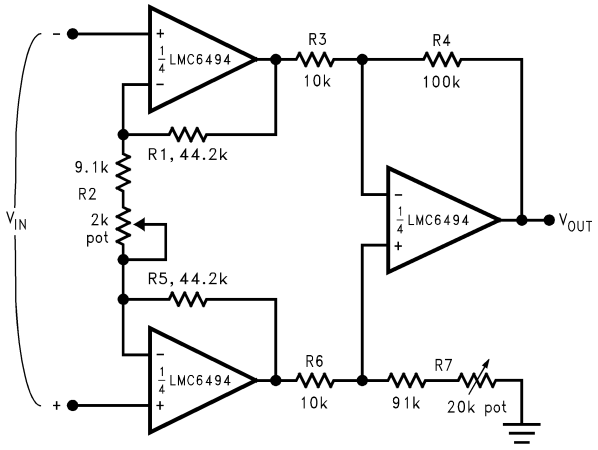


Figure 6-10. Photo Voltaic-Cell Amplifier



If R1 = R5, R3 = R6, and R4 = R7; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3}$$

$\therefore A_V \approx 100$ for circuit shown (R_2 = 9.3k).

Figure 6-11. Instrumentation Amplifier

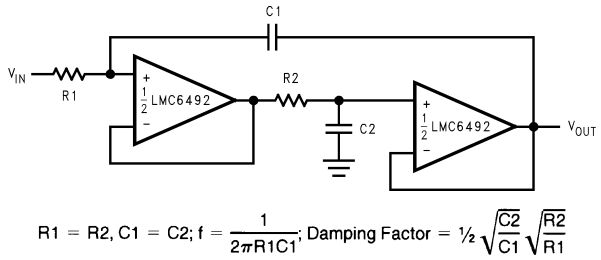


Figure 6-12. Rail-to-Rail Single Supply Low Pass Filter

This low-pass filter circuit can be used as an antialiasing filter with the same supply as the ADC. Filter designs can also take advantage of the LMC649x ultra-low input current. The ultra-low input current yields negligible offset error even when large value resistors are used. This configuration in turn allows the use of smaller-valued capacitors that take up less board space and cost less.

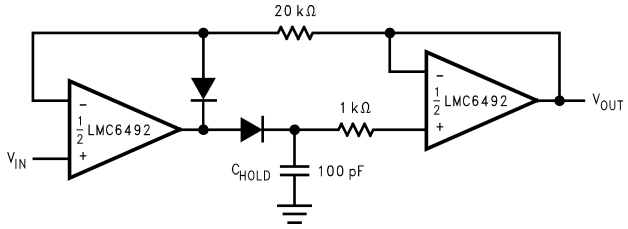
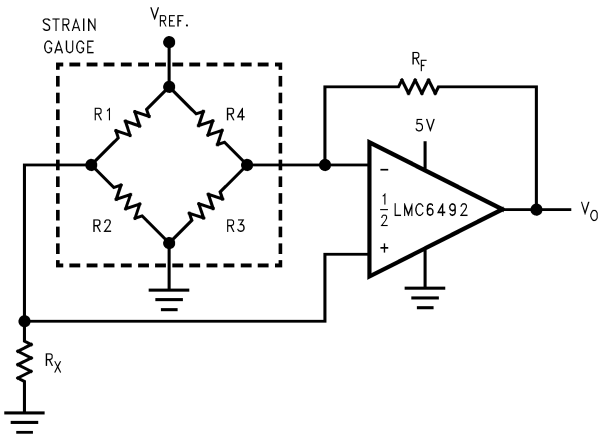


Figure 6-13. Low Voltage Peak Detector with Rail-to-Rail Peak Capture Range

Dielectric absorption and leakage is minimized by using a polystyrene or polypropylene hold capacitor. The droop rate is primarily determined by the value of C_{HOLD} and diode leakage current. Select low-leakage current diodes to minimize drooping.



$R_f = Rx$

$R_f >> R1, R2, R3, \text{ and } R4$

$$V_O = \left(\frac{R2}{R1 + R2} - \frac{R3}{R4 + R3}\right)\frac{R_f\,(R3 + R4)}{R3\,R4}V_{REF}$$

Figure 6-14. Pressure Sensor

In a manifold absolute pressure sensor application, a strain gauge is mounted on the intake manifold in the engine unit. Manifold pressure causes the sensing resistors, R1, R2, R3 and R4 to change. The resistors change in a way such that R2 and R4 increase by the same amount R1 and R3 decrease. This causes a differential voltage between the input of the amplifier. The gain of the amplifier is adjusted by R_f.

6.3 Layout

6.3.1 Layout Guidelines

6.3.1.1 Printed Circuit Board Layout For High-Impedance Work

Any circuit that operates with less than 1000pA of leakage current requires special layout of the printed circuit board (PCB). To take advantage of the ultra-low bias current of the LMC649x, typically 150fA, an excellent layout is required. Fortunately, the techniques to obtain low leakages are quite simple. First, do not ignore the surface leakage of the PCB. Even though this leakage can sometimes appear acceptably low, under conditions of high humidity or dust or contamination, the surface leakage is appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC649x inputs and the terminals of components connected to the op amp inputs, as in Figure 6-15. To have a significant effect, place guard rings on both the top and bottom of the PCB. This printed circuit foil must then be connected to a voltage that is at the same voltage as the amplifier inputs because no leakage current can flow between two points at the same potential.

For example, a PCB trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, can leak 5pA if the trace is a 5V bus adjacent to the pad of the input. This causes a 33 times degradation from the LMC649x actual performance. If a guard ring is used and held within 5mV of the inputs, then the same resistance of $10^{11}\Omega$ only causes 0.05pA of leakage current. Figure 6-15 to Figure 6-17 show typical connections of guard rings for standard op-amp configurations.

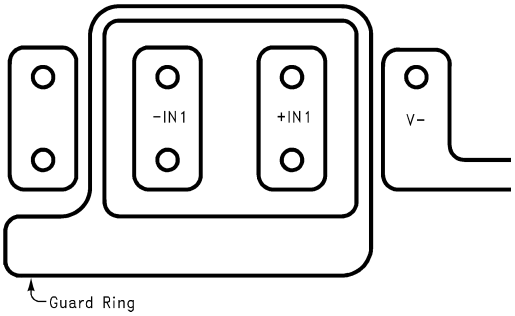


Figure 6-15. Examples of Guard Ring in PCB Layout

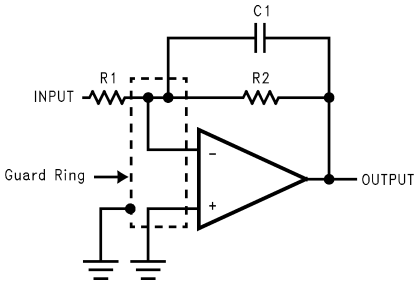


Figure 6-16. Inverting Amplifier

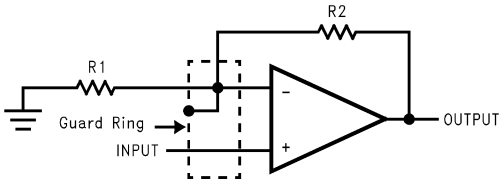


Figure 6-17. Noninverting Amplifier

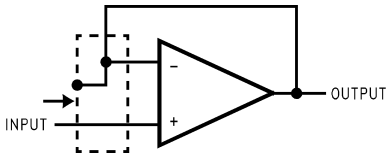
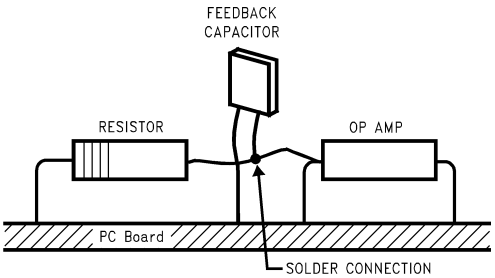


Figure 6-18. Follower

Be aware that when laying out a PCB for the sake of just a few circuits is inappropriate, the following technique is even better than a guard ring on a PCB. Do not insert the amplifier input pin into the board at all; instead, bend the input pin up in the air and use only air as an insulator because air is an excellent insulator. In this case, some of the advantages of PCB construction are lost, but the advantages of air are sometimes well worth the effort of using point-to-point up-in-the-air wiring. Figure 6-19 shows an example of air wiring.



Input pins are lifted out of PCB and soldered directly to components. All other pins connected to the PCB.

Figure 6-19. Air Wiring

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Device Support

7.1.1 Development Support

7.1.1.1 Spice Macromodel

A spice macromodel is available for the LMC649x. This model includes accurate simulation of:

- Input common-model voltage range
- Frequency and transient response
- GBW dependence on loading conditions
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions

and many other characteristics as listed on the macromodel disk.

Contact your local Texas Instruments sales office to obtain an operational amplifier spice model library disk.

7.1.1.2 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

7.1.1.3 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design tools and simulation web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

7.1.1.4 DIP-Adapter-EVM

Speed up your op amp prototyping and testing with the DIP-Adapter-EVM, which provides a fast, easy and inexpensive way to interface with small, surface-mount devices. Connect any supported op amp using the included Samtec terminal strips or wire them directly to existing circuits. The DIP-Adapter-EVM kit supports the following industry-standard packages: D or U (SOIC-8), PW (TSSOP-8), DGK (VSSOP-8), DBV (SOT-23-6, SOT-23-5 and SOT-23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6).

7.1.1.5 DIYAMP-EVM

The DIYAMP-EVM is a unique evaluation module (EVM) that provides real-world amplifier circuits, enabling the user to quickly evaluate design concepts and verify simulations. This EVM is available in three industry-standard packages (SC70, SOT23, and SOIC) and 12 popular amplifier configurations, including amplifiers, filters, stability compensation, and comparator configurations for both single and dual supplies.

7.1.1.6 TI Reference Designs

TI reference designs are analog solutions created by TI's precision analog applications experts. TI reference designs offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI reference designs are available online at https://www.ti.com/reference-designs.

7.1.1.7 Filter Design Tool

The filter design tool is a simple, powerful, and easy-to-use active filter design program. The filter design tool allows the user to create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the Design tools and simulation web page, the filter design tool allows the user to design, optimize, and simulate complete multistage active filter solutions within minutes.

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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PSpice® is a registered trademark of Cadence Design Systems, Inc.
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7.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (November 2023) to Revision F (February 2024)	Page
• Added data to *Thermal Information*	4
• Updated footnote (2) to detail how slew rate minimum value is specified in *Electrical Characteristics*	5

Changes from Revision D (March 2013) to Revision E (November 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added the *Pin Configuration and Functions*, *Specifications*, *ESD Ratings*, *Thermal Information*, *Application and Implementation*, *Application Information*, *Typical Applications*, *Layout*, *Layout Guidelines*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections	1
• Updated *Features*	1
• Deleted P (PDIP) packages from data sheet	1
• Updated application circuit in *Description*	1
• Moved ESD tolerance value from *Absolute Maximum Ratings* to *ESD Ratings*	4
• Updated note 1 of *Absolute Maximum Ratings*	4
• Changed *Operating Conditions* to *Recommended Operating Conditions* and deleted redundant table note	4
• Moved thermal information values from *Operating Conditions* to *Thermal Information*	4
• Updated format of *Electrical Characteristics*	5
• Deleted table notes 1, 2, and 3 from *Electrical Characteristics* to be consistent with standard TI data sheets	5
• Added ± to input offset voltage, input offset voltage drift, input bias current, and input offset current in *Electrical Characteristics*	5
• Updated parameter names to be consistent with modern data sheets	5
• Moved the *AC Electrical Characteristics* and *DC Electrical Characteristics* to *Electrical Characteristics*	5
• Changed supply current specification from total to per amplifier in *Electrical Characteristics*	5
• Deleted Figures 13 to 15, Figures 21 to 25, Figures 34 to 35, and Figures 51 to 54	8
• Added Input Offset Voltage vs Common-Mode Voltage plot in *Amplifier Topology* and related description	14
• Updated description of *Rail-to-Rail Output*	15

Changes from Revision C (March 2013) to Revision D (March 2013)	Page
• Changed layout of National Data Sheet to TI format	21

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMC6492AEM/NOPB	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	LMC64 92AEM
LMC6492AEMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMC64 92AEM
LMC6492AEMX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMC64 92AEM
LMC6492BEM/NOPB	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	LMC64 92BEM
LMC6492BEMX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMC64 92BEM
LMC6492BEMX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMC64 92BEM
LMC6494AEMX/NOPB	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LMC6494, LMC6494AEM) AEM
LMC6494AEMX/NOPB.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LMC6494, LMC6494AEM) AEM
LMC6494BEM/NOPB	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 125	LMC6494 BEM
LMC6494BEMX/NOPB	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(LMC6494, LMC6494BEM) BEM
LMC6494BEMX/NOPB.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LMC6494, LMC6494BEM) BEM
LMC6494BEMX/NOPB.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(LMC6494, LMC6494BEM) BEM

(1) **Status:** For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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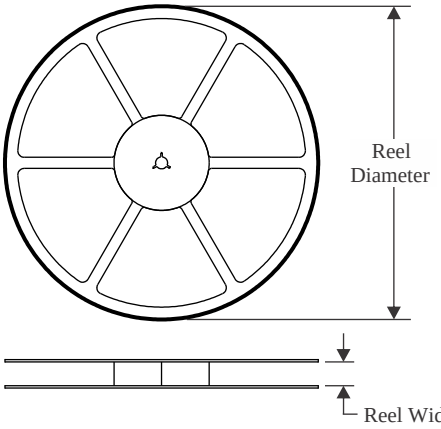
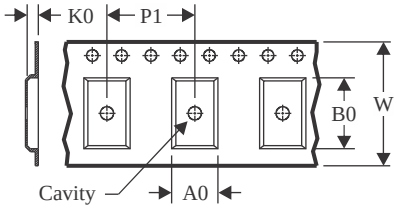
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

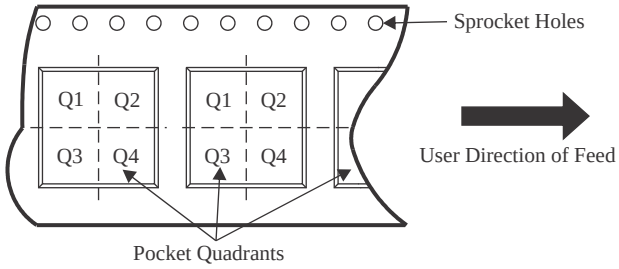


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

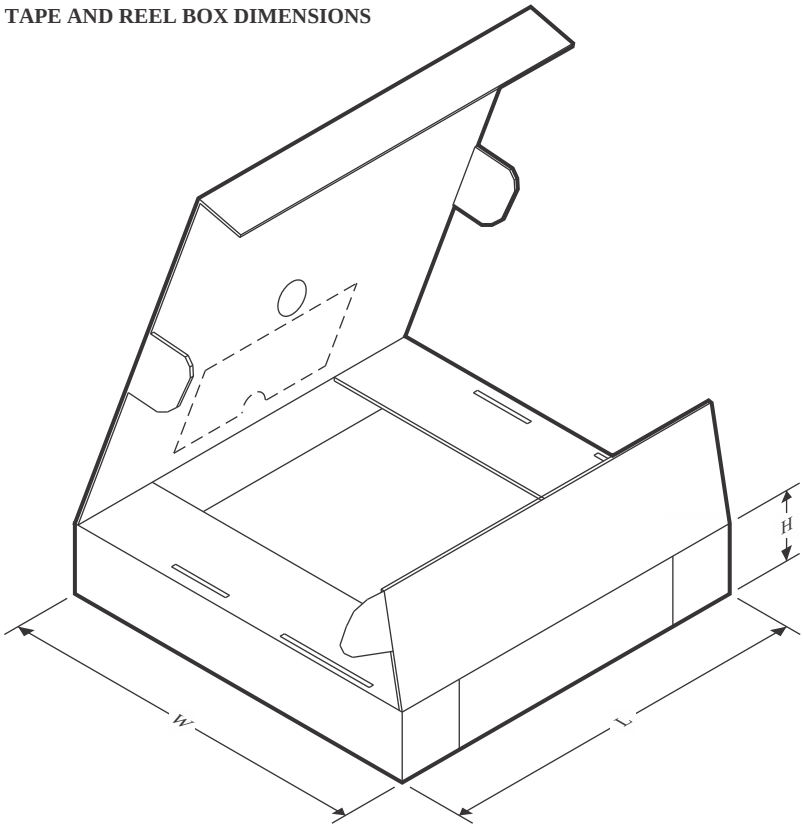
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

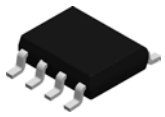
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC6492AEMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMC6492BEMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMC6494AEMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMC6494BEMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMC6494BEMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC6492AEMX/NOPB	SOIC	D	8	2500	353.0	353.0	32.0
LMC6492BEMX/NOPB	SOIC	D	8	2500	353.0	353.0	32.0
LMC6494AEMX/NOPB	SOIC	D	14	2500	353.0	353.0	32.0
LMC6494BEMX/NOPB	SOIC	D	14	2500	353.0	353.0	32.0
LMC6494BEMX/NOPB	SOIC	D	14	2500	356.0	356.0	35.0

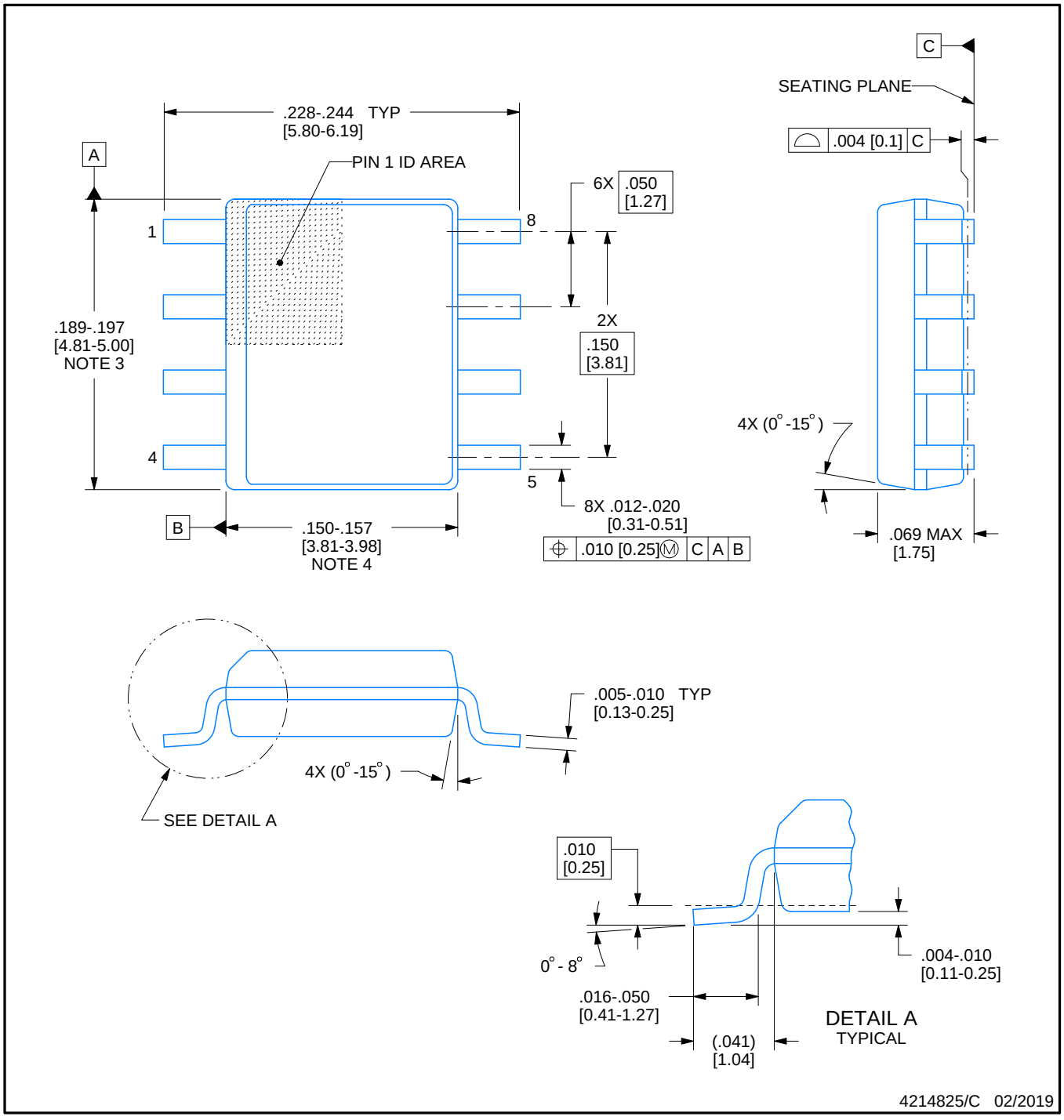


PACKAGE OUTLINE

D0008A

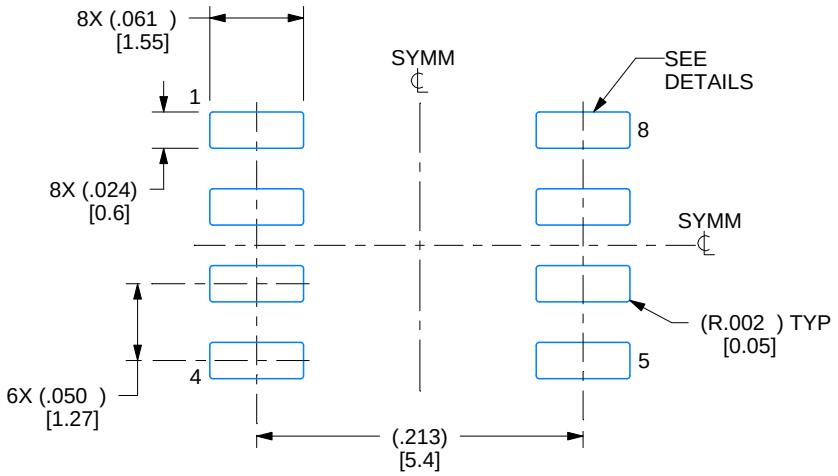
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

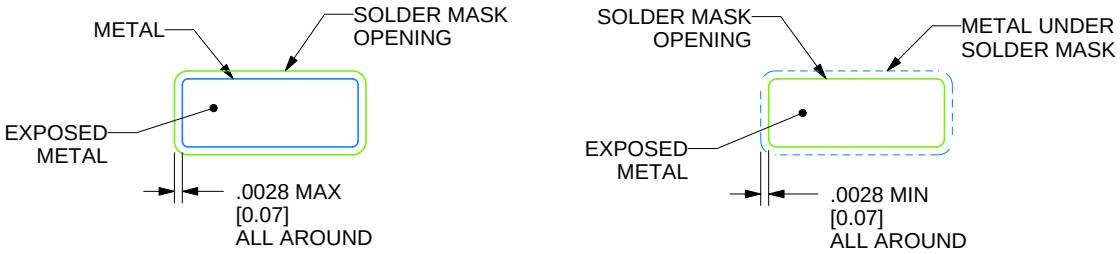


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

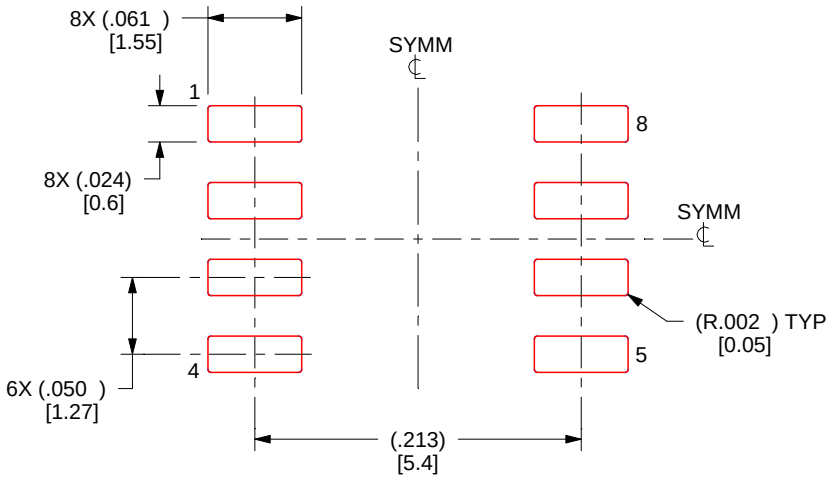
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

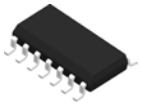


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

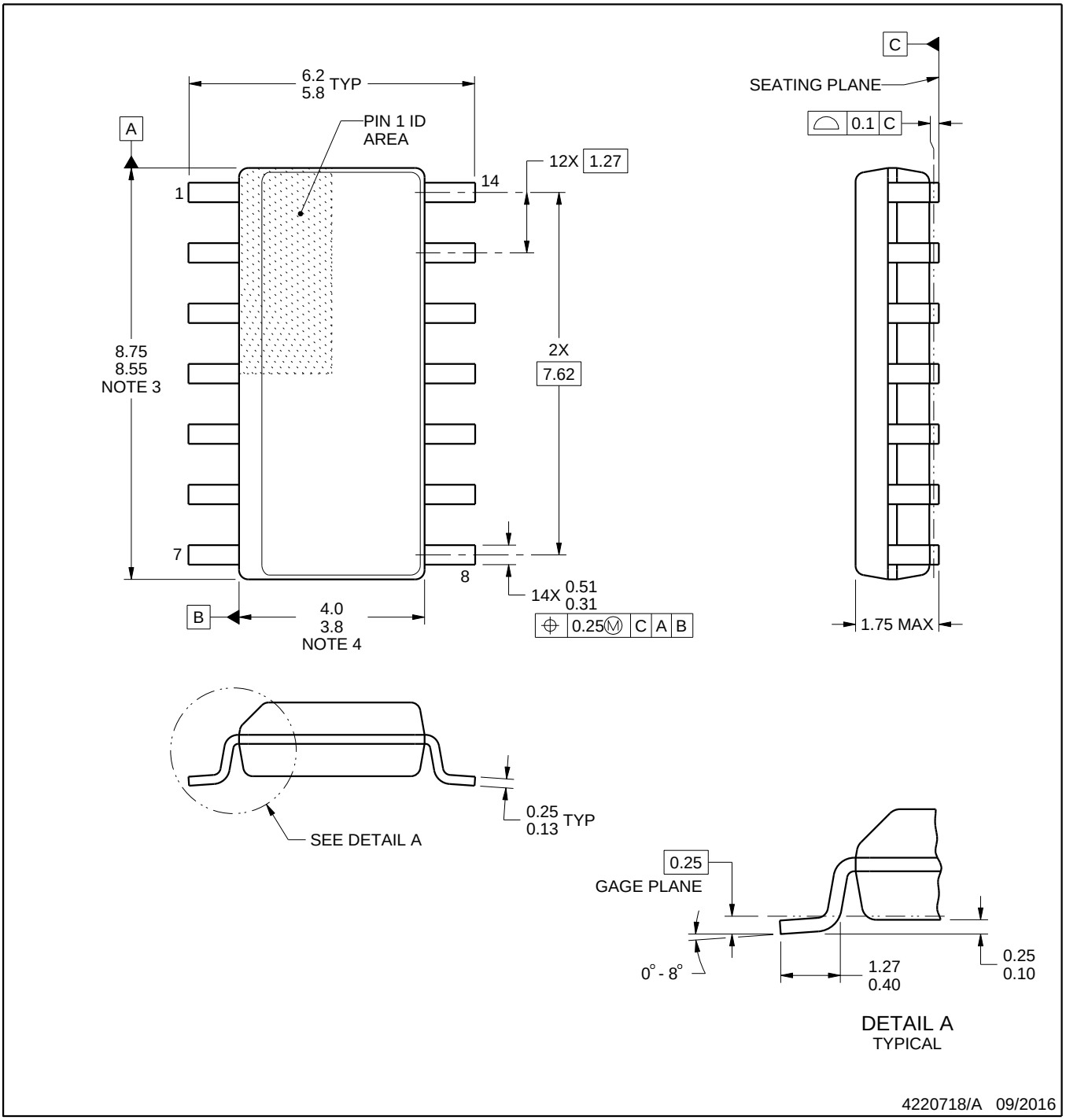


PACKAGE OUTLINE

D0014A

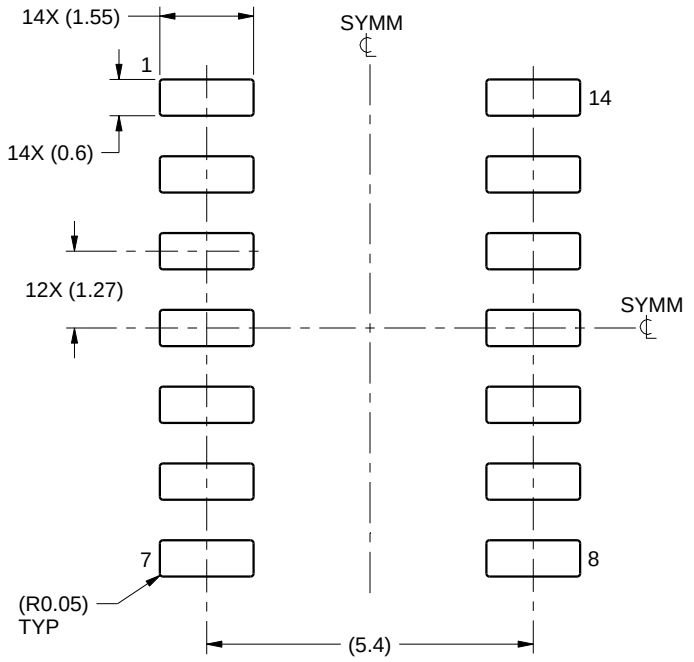
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

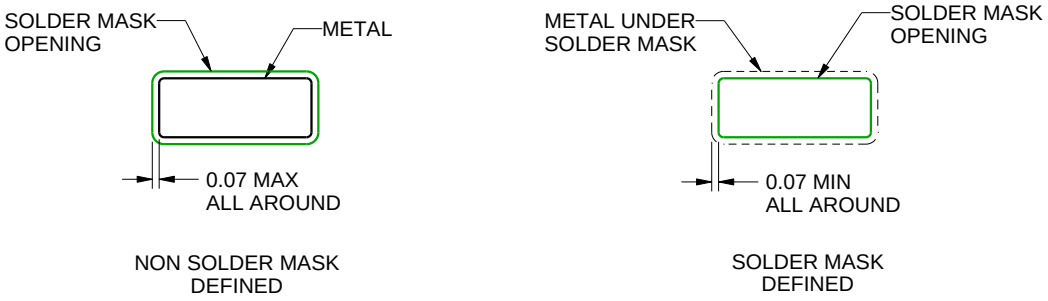


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

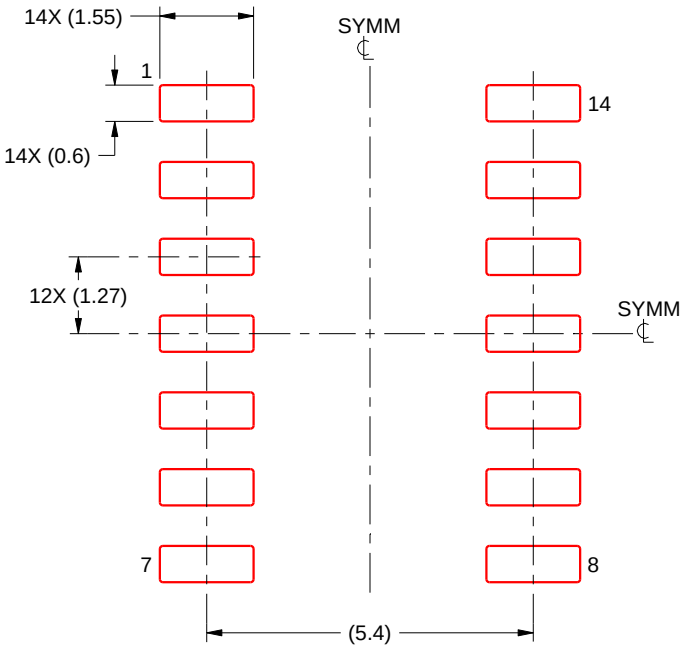
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025