LMG5126 Wide-Input, 2.5MHz, Boost Converter

1 Features

- Input voltage 6.5V to 42V
  - Minimum 2.5V for $V_{(BIAS)}$ ≥ 6.5V or V_{OUT} ≥ 6V
- Output Voltage 6V to 60V
  - 2% accuracy, internal feedback resistors
  - Bypass operation for V_I > V_{OUT}
    - Boot refresh out of audio >20kHz
  - Dynamic output voltage tracking
    - Digital PWM tracking (DTRK)
    - Analog tracking (ATRK)
  - Over voltage protection (65V, 50V, 35V, 25V)
- Low shutdown I_{SD} of 5µA typical (100uA maximum)
- Low operating I_Q of 1.5mA typical (2.5mA maximum)
- Stacking with interleaved multiphase operation
  - Up to 4-devices without external clock
- Switching frequency from 300kHz to 2.5MHz
  - Synchronization to external clock (SYNCIN)
  - Spread Spectrum (DRSS)
- Dynamically selectable switching modes (FPWM, Diode emulation)
- Current sense resistor or DCR sensing
- Average inductor current monitor
- Average input current limit
- Selectable current limit (29mV or 60mV)
- Selectable delay time (DLY)
- Power good indicator
- Programmable V_I undervoltage lockout (UVLO)
- Lead-less RLF-22 package with wettable flanks
- Create a custom design using the LMG5126 with the WEBENCH® Power Designer

2 Applications

- High-end audio power supply
- Voltage stabilizer module
- Start-stop application

3 Description

The LMG5126 is a stackable multiphase synchronous boost converter. The device provides a regulated output voltage for lower or equal input voltage also supporting V_I to V_{OUT} bypass mode to save power. Up to 4 devices can be stacked with or without external clock.

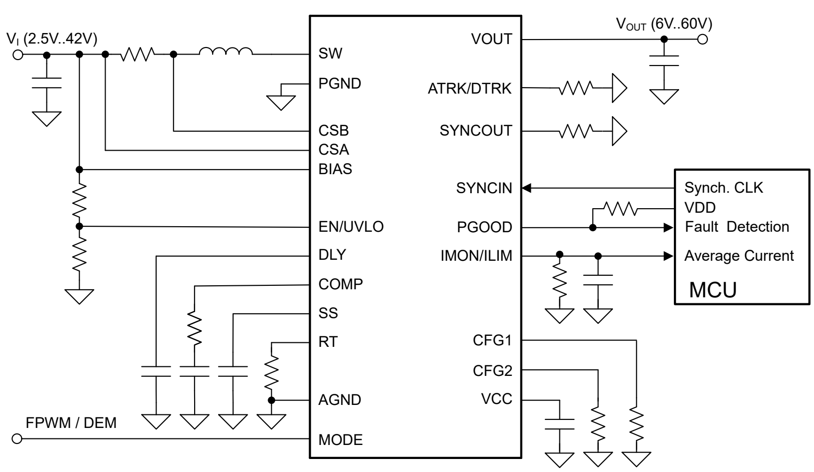
V_{OUT} can be dynamically programmed using the digital or analog ATRK/DTRK function. V_I can be as low as 2.5V after startup as the internal VCC supply is automatically switched from V_{BIAS} to V_{OUT} for V_{BIAS} < 6.5V. The fixed switching frequency is set between 300kHz and 2.5MHz via a resistor on the RT-pin or the SYNCIN clock. The switching modes FPWM or Diode emulation can be changed during operation.

The implemented protections peak current limit, average input current limit, 120% input current limit, average inductor current monitor, over- and undervoltage protection or the thermal shutdown protect the device and the application.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LMG5126	VBT (VQFN-FCRLF, 22)	6mm × 4.5mm

(1) For all available packages, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application

Table of Contents

4 Pin Configuration and Functions

Note

A top mounted heat sink must be insulative not to short the SW and PGND terminals on the exposed GaN dies.

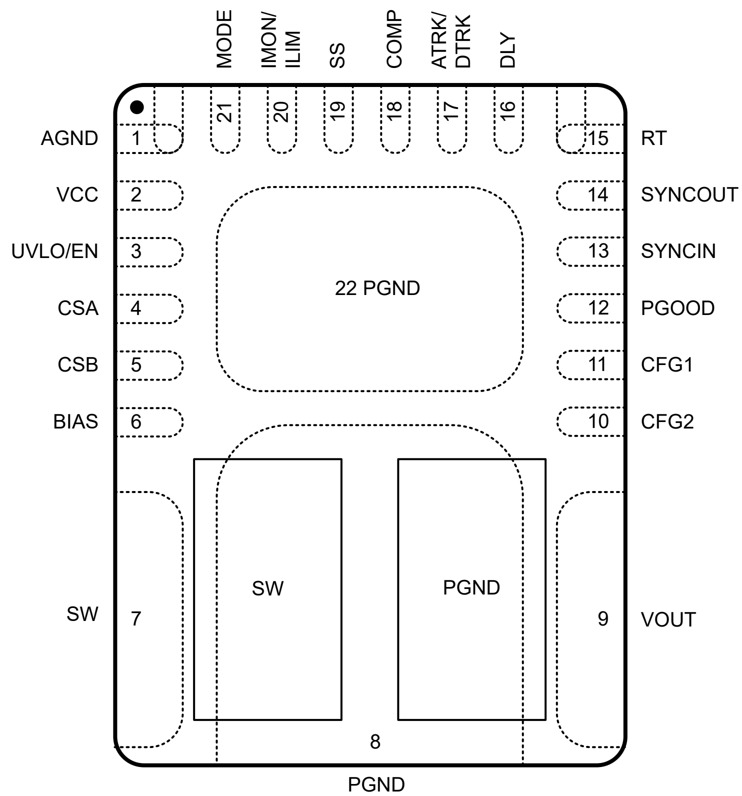


Figure 4-1. LMG5126 pin out (top view)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
AGND	1	G	Analog ground pin. Connect to the analog ground plane through a wide and short path.
ATRK/DTRK	17	I	Output regulation target programming pin. The output voltage regulation target can be programmed by connecting the pin through a resistor to AGND, or by controlling the pin voltage directly with a voltage in the recommended operating range of the pin from 0.2V to 2.0V. A digital PWM signal between 8% to 80% duty cycle sets the output voltage regulation in the recommended operating range.
BIAS	6	P	Supply voltage input to the VCC regulator. Connect a 1µF local BIAS capacitor from the pin to ground.
CFG1	11	I	Device configuration pin. Sets the Spread Spectrum mode, 120% peak current limit latch off, sense voltage and gate drive strength. Connect the pin through a resistor to AGND.
CFG2	10	I	Device configuration pin. Sets if the device is configured as single, primary or secondary device using the internal or external clock and the PGOOD configuration. Connect the pin through a resistor to AGND.
COMP	18	O	Output of the internal transconductance error amplifier. Connect the loop compensation components between the pin and AGND.
CSA	4	I	Current sense amplifier input. The pin operates as the positive input pin. Input to the internal undervoltage lockout for the input voltage. Connect the pin to the sense resistor.

Table 4-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
CSB	5	I	Current sense amplifier input. The pin operates as the negative input pin. Connect the pin to the sense resistor.
DLY	16	O	Average input current limit delay setting pin. A capacitor from DLY to AGND sets the delay from when V_{IMON} reaches 1.1V until the average input current limit is enabled.
EP	22	G	Exposed pad of the package. The Exposed pad must be connected to AGND and soldered to a large ground plane to reduce thermal resistance.
IMON/ILIM	20	O	Input current monitor and average input current limit setting pin. Sources a current proportional to the differential current sense voltage. A resistor is connected from this pin to AGND.
MODE	21	I	Operation mode selection pin selecting DEM or FPWM. Connect the pin through a resistor to AGND or VCC. The pin can also be connected to a controller.
PGND	8	G	Power ground connection pin for low-side FET.
PGOOD	12	O	Power-good indicator with open-drain output stage. The pin is pulled low when the output voltage is less than the undervoltage threshold or greater than the overvoltage threshold based on the CFG2-pin setting. It is also pulled low indicating faults. The pin can be left floating if not used.
RT	15	O	Switching frequency setting pin. The switching frequency is programmed by a single resistor between the pin and AGND. The switching frequency is dynamically programmable during operation.
SS	19	O	Soft-start time programming pin. An external capacitor and an internal current source set the ramp rate of the internal error amplifier reference during soft start. The device forces diode emulation during soft-start time.
SW	7	P	Switching node connection.
SYNCIN	13	I	External clock synchronization pin. Input for an external clock that overrides the free-running internal oscillator. Connect the SYNCIN pin to ground when SYNCIN is not used.
SYNCOUT	14	O	Clock output and OVP as well as ATRK current configuration pin. SYNCOUT provides a phase shifted clock output, set by the CFG2.pin. A resistor is connected to this pin to select the LMG5126 OVP level and enable the 20µA ATRK current.
UVLO/EN	3	I	Undervoltage lockout programming pin. The converter start-up and shutdown levels can be programmed by connecting this pin to the supply voltage through a resistor divider. If greater than $V_{UVLO\text{-}RISING}$, the device is enabled.
VCC	2	P	Output of the internal VCC regulator and supply voltage input of the internal FET drivers. Connect a 4.7µF capacitor between the pin and PGND.
VOUT	9	P	Output voltage pin. An internal feedback resistor voltage divider is connected from the pin to AGND.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

5 Specifications

5.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range (unless otherwise specified)[(1)]

		MIN	MAX	UNIT
Input[(2)]	BIAS to AGND	–0.3	50	V
	UVLO/EN to AGND	–0.3	BIAS + 0.3	
	CSA to AGND	–0.3	50	
	CSA to CSB	–0.3	0.3	
	VOUT to AGND	-0.3	75	
	SW to AGND	–5	75	
	SW to AGND (10ns)	–15	85	
	CFG1, CFG2, SYNCIN, ATRK/DTRK, DLY, MODE,	–0.3	5.5	
	RT to AGND	–0.3	2.5	
	GND to AGND	–0.3	0.3	
	GND to AGND (10ns)	–2	2	
Output[(2)]	VCC to AGND	–0.3	5.8[(3)]	V
	PGOOD, SYNCOUT, SS, COMP, IMON/ILIM to AGND	–0.3	5.5	
	SW, VOUT current (continuous), T_J = 25°C		35	A
	SW, VOUT current (pulsed, 300µs), T_J = 25°C		125	A
Operating junction temperature, T_J [(4)]		–40	150	°C
Storage temperature, T_{STG}		–55	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Do not apply an external voltage directly to COMP, SS, RT pins.
(3) Operating lifetime is derated when the pin voltage is greater than 5.5V.
(4) High junction temperatures degrade operating lifetimes. Operating lifetime is derated for junction temperatures greater than 125°C.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[(1)]		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins	±750	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

Over the recommended operating junction temperature range (unless otherwise specified)(1)

		MIN	NOM	MAX	UNIT
V_I	Boost Input Voltage (when BIAS ≥ 6.5V or VOUT ≥ 6V)	2.5		42	V
V_{OUT}	Boost Output Voltage	6		60	V
V_{BIAS}	BIAS Input Voltage	6.5		42	V
$V_{UVLO/EN}$	UVLO/EN Input Voltage	0		42	V
V_{MODE}	MODE Input Voltage	0		5.25	V
V_{CSA}, V_{CSB}	Current Sense Input Voltage	2.5		42	V
V_{ATRK}	ATRK Input Voltage	0.2		2	V
V_{DTRK}	DTRK Input Voltage	0		5.25	V
V_{DLY}	DLY Voltage	0		5.25	V
V_{PGOOD}	PGOOD Voltage	0		5.25	V
$V_{IMON/ILIM}$	IMON/ILIM Voltage	0		5.25	V
V_{SYNCIN}	Synchronization Pulse Input Voltage	0		5.25	V
f_{SW}	Switching Frequency Range	300		2500(2)	kHz
f_{SYNCIN}	Synchronization Pulse Frequency Range	300		2500(2)	kHz
f_{DTRK}	DTRK Frequency Range	100		2200	kHz
T_J	Operating Junction Temperature	–40		150(3)	°C

(1) *Operating Ratings* are conditions under the device is intended to be functional. For specifications and test conditions, see *Electrical Characteristics*
(2) Maximum switching frequency is programmed by $R_{RT.}$ The device supports up to 2500 kHz switching.
(3) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

5.4 Thermal Information

THERMAL METRIC(1)		LMG5126 VQFN-FCRLF 22 PINS	UNIT
R_{qJA}	Junction-to-ambient thermal resistance	29.1	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	1.0	°C/W
R_{qJB}	Junction-to-board thermal resistance	5.0	°C/W
y_{JT}	Junction-to-top characterization parameter	3.7	°C/W
y_{JB}	Junction-to-board characterization parameter	5.0	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	4.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

Typical values correspond to T_J = 25 °C. Minimum and maximum limits apply over T_J = -40 °C to 150 °C. Unless otherwise stated, V_I = V_{BIAS} = 12 V, V_{OUT} = 24 V, f_{SW} = 400 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT (BIAS, VCC)						
I_{SD}	V_I current in shutdown state (BIAS connected to V_I). Current into BIAS, CSA, CSB, SW.	$V_{UVLO/EN}$ = 0V, V_{OUT} = 12V, T_J = –40°C to 85°C		5	100	µA
I_{SD_BIAS}	BIAS-pin current in shutdown state.	$V_{UVLO/EN}$ = 0V, V_{OUT} = 12V, T_J = –40°C to 85°C		2	5	µA
I_{SD_VOUT}	VOUT-pin current in shutdown state.	$V_{UVLO/EN}$ = 0V, V_{OUT} = 12V, T_J = –40°C to 85°C		0.001	0.5	µA

Typical values correspond to T_J = 25 °C. Minimum and maximum limits apply over T_J = -40 °C to 150 °C. Unless otherwise stated, V_I = V_{BIAS} = 12 V, V_{OUT} = 24 V, f_{SW} = 400 kHz

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{Q\_BIAS\_FPWM}$	BIAS-pin quiescent current in active state, FPWM-Mode, internal clock (not-switching, RT and IMON current is excluded).		$V_{UVLO/EN}$ = 2.0V, CFG1 = level 10, CFG2 = level 1, V_{ATRK} = 0.8V, no load, T_J = –40°C to 125°C		1.5	2.5	mA
$I_{Q\_BIAS\_DEM}$	BIAS-pin quiescent current in active state, DEM-Mode, internal clock (not-switching, RT and IMON current is excluded).		$V_{UVLO/EN}$ = 2.0V, CFG1 = level 10, CFG2 = level 1, V_{ATRK} = 0.8V, no load, T_J = –40°C to 125°C		1.6	2	mA
$I_{Q\_VOUT\_FPWM}$	VOUT-pin quiescent current in active state, FPWM-Mode, internal clock (not-switching).		$V_{UVLO/EN}$ = 2.0V, CFG1 = level 10, CFG2 = level 1, V_{ATRK} = 0.8V, no load, T_J = –40°C to 125°C		20	750	µA
$I_{Q\_BIAS\_BYP}$	BIAS-pin current in bypass state (RT and IMON current is excluded).		$V_{UVLO/EN}$ = 2.0V, CFG1 = level 10, CFG2 = level 1, V_{OUT} = 12V, T_J = –40°C to 125°C		1.5	8.5	mA
I_{BIAS}	BIAS-pin bias current when VCC is supplied by BIAS, FPWM-Mode (not-switching, RT and IMON current is excluded).		V_{BIAS} = 12V, I_{VCC} = 100mA		100	110	mA
I_{VOUT}	VOUT-pin bias current when VCC is supplied by VOUT, FPWM-Mode (not-switching).		V_{BIAS} = 3.3V, I_{VCC} = 100mA		100	110	mA
VCC REGULLATOR (VCC)							
$V_{BIAS-RISING}$	Threshold to switch VCC supply from VOUT-pin to BIAS-pin		V_{BIAS} rising	6.0	6.25	6.5	V
$V_{BIAS-FALLING}$	Threshold to switch VCC supply from BIAS-pin to VOUT-pin		V_{BIAS} falling	5.6	5.9	6.2	V
$V_{BIAS-HYS}$	VCC supply threshold hysteresis			250	350		mV
$V_{VCC-REG1}$	VCC regulation		No load	5.1	5.3	5.5	V
$V_{VCC-REG2}$	VCC regulation during dropout		V_{BIAS} = 5.9V, I_{VCC} = 100mA	4.5	5.2		V
$V_{VCC-UVLO-RISING}$	VCC UVLO threshold		VCC rising	4.1	4.2	4.3	V
$V_{VCC-UVLO-FALLING}$	VCC UVLO threshold		VCC falling	3.8	3.9	4.0	V
$V_{VCC-UVLO-HYS}$	VCC UVLO threshold hysteresis		VCC falling		300		mV
I_{VCC-CL}	VCC sourcing current limit		V_{VCC} = 4V	100			mA
ENABLE (EN/UVLO)							
$V_{EN-RISING}$	Enable threshold		EN rising	0.50	0.55	0.6	V
$V_{EN-FALLING}$	Enable threshold		EN falling	0.40	0.45	0.50	V
V_{EN-HYS}	Enable hysteresis		EN falling		75		mV
R_{EN}	EN pulldown resistance		V_{EN} = 0.2V	30	37	50	kΩ
$V_{UVLO-RISING}$	UVLO threshold		UVLO rising	1.05	1.1	1.15	V
$V_{UVLO-FALLING}$	UVLO threshold		UVLO falling	1.025	1.075	1.125	V
$V_{UVLO-HYS}$	UVLO hysteresis		UVLO falling		25		mV
$I_{UVLO-HYS}$	UVLO pulldown hysteresis current		V_{UVLO} = 0.7V	9	10	11	µA
$I_{UVLO/EN}$	UVLO/EN-pin bias current		$V_{UVLO/EN}$ = 0.3V, pull-down resistor = active.		8	11	µA
			$V_{UVLO/EN}$ = 0.7V, 10µA current = active.	9	10	11	µA
			$V_{UVLO/EN}$ = 3.3V			1	µA
POWER SWITCH							
$R_{DS(on)}$	GaN FET on resistance	High-side	T_J = 25°C		4	8.5	mΩ
		Low-side			4	8.5	mΩ
CONFIGURATION (CFG1, CFG2, SYNCOUT)							
R_{CFGx_1}	CFGx level 1 resistance				0	0.1	kΩ

Typical values correspond to T_J = 25 °C. Minimum and maximum limits apply over T_J = -40 °C to 150 °C. Unless otherwise stated, V_I = V_{BIAS} = 12 V, V_{OUT} = 24 V, f_{SW} = 400 kHz

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{CFGx_2}	CFGx level 2 resistance			0.496	0.51	0.526	kΩ
R_{CFGx_3}	CFGx level 3 resistance			1.11	1.15	1.19	kΩ
R_{CFGx_4}	CFGx level 4 resistance			1.81	1.9	1.93	kΩ
R_{CFGx_5}	CFGx level 5 resistance			2.65	2.7	2.82	kΩ
R_{CFGx_6}	CFGx level 6 resistance			3.71	3.8	3.94	kΩ
R_{CFGx_7}	CFGx level 7 resistance			4.95	5.1	5.26	kΩ
R_{CFGx_8}	CFGx level 8 resistance			6.29	6.5	6.68	kΩ
R_{CFGx_9}	CFGx level 9 resistance			8.00	8.3	8.50	kΩ
R_{CFGx_10}	CFGx level 10 resistance			10.18	10.5	10.81	kΩ
R_{CFGx_11}	CFGx level 11 resistance			12.90	13.3	13.70	kΩ
R_{CFGx_12}	CFGx level 12 resistance			15.71	16.2	16.69	kΩ
R_{CFGx_13}	CFGx level 13 resistance			19.88	20.5	21.11	kΩ
R_{CFGx_14}	CFGx level 14 resistance			24.15	24.9	25.65	kΩ
R_{CFGx_15}	CFGx level 15 resistance			29.20	30.1	31.00	kΩ
R_{CFGx_16}	CFGx level 16 resistance			35.40	36.5	38.60	kΩ
$R_{SYNCOUT\_1}$	SYNCOUT level 1 resistance			0	24.9	26.15	kΩ
$R_{SYNCOUT\_2}$	SYNCOUT level 2 resistance			29.94	31.5	33.09	kΩ
$R_{SYNCOUT\_3}$	SYNCOUT level 3 resistance			37.92	39.9	41.91	kΩ
$R_{SYNCOUT\_4}$	SYNCOUT level 4 resistance			46.17	48.6	51.03	kΩ
$R_{SYNCOUT\_5}$	SYNCOUT level 5 resistance			58.44	61.5	64.59	kΩ
$R_{SYNCOUT\_6}$	SYNCOUT level 6 resistance			70.98	75	78.45	kΩ
$R_{SYNCOUT\_7}$	SYNCOUT level 7 resistance			85.8	90.9	94.83	kΩ
$R_{SYNCOUT\_8}$	SYNCOUT level 8 resistance			104.04	110	200	kΩ
SWITCHING FREQUENCY							
V_{RT}	RT regulation			0.7	0.75	0.8	V
f_{SW1}	Switching frequency		f_{SW} = 300kHz, RT = 104.4kΩ	255	300	345	kHz
f_{SW2}			f_{SW} = 2500kHz, RT = 12kΩ	2250	2500	2750	kHz
t_{ON-MIN}	Minimum controllable on-time		f_{SW} = 2500kHz	14	20	50	ns
$t_{OFF-MIN}$	Minimum forced off-time		f_{SW} = 2500kHz	45	65	85	ns
D_{MAX1}	Maximum duty cycle limit		f_{SW} = 300kHz	97%	98%	99%	
D_{MAX2}			f_{SW} = 2500kHz	78%	84%	90%	
SYNCHRONIZATION (SYNCIN, SYNCOUT)							
$f_{SYNC\_DET\_min}$	SYNCIN frequency activity detection	Spread Spectrum = off	f_{SW} = 300kHz	120			kHz
f_{SYNC_DET}	SYNCIN frequency activity detection vs RT set switching frequency	Spread Spectrum = off	RT = 12kΩ to 104.4kΩ	–60%			
	SYNCIN activity detection cycles				3		cycles
f_{SYNC}	Syncing frequency range from RT set frequency during synchronization.	single device	Frequency synchronized to ext. clock min. = 300kHz, max. = 2500kHz.	–45%		45%	
		multi device		–22%		22%	
V_{SYNCIN_H}	SYNCIN high level input voltage		SYNCIN rising	1.19		5.25	V
V_{SYNCIN_L}	SYNCIN low level input voltage		SYNCIN falling	–0.3		0.41	V
I_{SYNCIN}	SYNCIN bias current				0.01	1	µA
	Minimum SYNCIN pullup / pulldown pulse width			135			ns

Typical values correspond to T_J = 25 °C. Minimum and maximum limits apply over T_J = -40 °C to 150 °C. Unless otherwise stated, V_I = V_{BIAS} = 12 V, V_{OUT} = 24 V, f_{SW} = 400 kHz

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOUT PROGRAMMING (ATRK/DTRK)							
V_{OUT_REG}	V_{OUT} regulation with ATRK voltage		ATRK = 0.2V	5.85	6	6.15	V
			ATRK = 0.4V	11.82	12	12.18	V
			ATRK = 0.8V	23.64	24	24.36	V
			ATRK = 1.6V	47.28	48	48.72	V
			ATRK = 2V	59.10	60	60.90	V
G_{DTRK}	Conversion ratio of DTRK duty cycle to V_{ATRK}		f_{DTRK} = 100kHz, 2200kHz		25		mV / %
	DTRK duty cycle range			8%		80%	
V_{ATRK}	ATRK voltage for given DTRK duty cycle		f_{DTRK} = 100kHz, DC = 8%	0.192	0.2	0.208	V
			f_{DTRK} = 100kHz, DC = 40%	0.98	1	1.02	V
			f_{DTRK} = 100kHz, DC = 80%	1.98	2	2.02	V
			f_{DTRK} = 500kHz, DC = 8%	0.19	0.2	0.215	V
			f_{DTRK} = 500kHz, DC = 40%	0.98	1	1.02	V
			f_{DTRK} = 500kHz, DC = 80%	1.98	2	2.02	V
V_{DTRK_H}	DTRK high level input voltage		DTRK rising	1.19		5.25	V
V_{DTRK_L}	DTRK low level input voltage		DTRK falling	–0.3		0.41	V
I_{ATRK}	Source current when activated through resistor setting at SYNCOUT			19.8	20	20.2	µA
$I_{ATRK/DTRK}$	ATRK/DTRK-pin bias current		20µA current is disabled, $V_{ATRK/DTRK}$ = 2V		0.01	1	µA
	Minimum DTRK pull-up / pull-down pulse width			25			ns
SOFT START (SS)							
I_{SS}	Soft-start current			42.5	50	57.5	µA
$V_{SS-DONE}$	Soft-start done threshold			2.15	2.2	2.25	V
R_{SS}	SS pulldown switch R_{DSON}				37	70	Ω
V_{SS-DIS}	SS discharge detection threshold			20	45	70	mV
CURRENT SENSE (CSA, CSB)							
A_{CS}	Current sense amplifier gain				10		V/V
V_{CLTH}	Positive peak current limit threshold	60mV sensing	Referenced to CS input	54	60	66	mV
		29mV sensing		24	29	35	mV
V_{NCLTH}	Negative peak current limit threshold	60mV and 29mV sensing	Referenced to CS input, FPWM mode	–34	–28	–22	mV
V_{ICL}	Input current limit	60mV sensing	Referenced to CS input	64	72	84	mV
		29mV sensing		30	38	45	mV
ΔV_{ICL_CLTH}	Delta voltage between ICL and positive peak current threshold	60mV sensing	Delta voltage between ICL and positive peak current threshold	6	12		mV
		29mV sensing		3	6		mV
	Peak current limit trip delay				60		ns
V_{ZCD}	ZCD threshold (CSA – CSB)		CS input falling, DEM	0	3	6	mV
			CS input falling, DEM, T_J = 0°C to 85°C	0	3	5	mV
V_{ZCD_BYP}	ZCD threshold in bypass mode (CSA – CSB).			–6	–2.5	0	mV
V_{SLOPE}	Peak slope compensation amplitude		Referenced to CS input, f_{SW} = 300kHz	40	45	52	mV
I_{CSA}	CSA current		Device in Standby state, V_I = V_{BIAS} = V_{OUT} = 12V		150	170	µA
I_{CSB}	CSB current					1.2	µA

Typical values correspond to T_J = 25 °C. Minimum and maximum limits apply over T_J = -40 °C to 150 °C. Unless otherwise stated, V_I = V_{BIAS} = 12 V, V_{OUT} = 24 V, f_{SW} = 400 kHz

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT MONITOR / LIMITER WITH DELAY (IMON/ILIM)							
G_{IMON}	Transconductance Gain			0.320	0.333	0.346	µA/mV
I_{OFFSET}	Offset current			2.7	4	5	µA
V_{ILIM}	ILIM regulation target			0.93	1	1.07	V
V_{ILIM_th}	ILIM activation threshold			1.05	1.1	1.25	V
V_{ILIM_reset}	DLY reset threshold		ILIM falling, referenced to V_{ILIM}	85%	89%	93%	
I_{DLY}	DLY sourcing/sinking current			4	5	6	µA
$V_{DLY\_peak\_rise}$			V_{DLY} rising	2.45	2.6	2.75	V
$V_{DLY\_peak\_fall}$			V_{DLY} falling	2.25	2.4	2.55	V
V_{DLY_valley}					0.2		V
ERROR AMPLIFIER (COMP)							
Gm	Transconductance			0.7	1	1.3	mA/V
$A_{COMP-PWM}$	COMP-to-PWM gain				1		V/V
$V_{COMP-MAX}$	COMP maximum clamp voltage		COMP rising	2.3	2.55	2.9	V
$V_{COMP-MIN}$	COMP minimum clamp voltage, active in DEM		COMP falling	0.38	0.48	0.55	V
	COMP minimum clamp voltage, active in FPWM		COMP falling	0.13	0.16	0.19	V
$V_{COMP-offset}$	Offset in respect to min clamp		COMP falling	0.01	0.03	0.06	V
$I_{SOURCE-MAX}$	Maximum COMP sourcing current		V_{COMP} = 1V, V_{ATRK} = 2V	150			µA
$I_{SINK-MAX}$	Maximum COMP sinking current		V_{COMP} = 1V, V_{ATRK} = 0.5V	90			µA
OPERATION MODES							
V_{MODE_H}	MODE-pin high level	FPWM		1.19		5.25	V
V_{MODE_L}	MODE-pin low level	DEM		–0.3		0.41	V
I_{MODE}	MODE-pin bias current		MODE = 3.3V		0.01	1	µA
OVERVOLTAGE AND UNDERVOLTAGE MONITOR							
V_{OVP-H}	Overvoltage threshold rising		V_{OUT} rising (referenced to error amplifier reference)	108%	110%	112%	
V_{OVP-L}	Overvoltage threshold falling		V_{OUT} falling (referenced to error amplifier reference)	101%	103%	105%	
V_{OVP_max-H}	Max. overvoltage threshold rising	25V setting	V_{OUT} rising (referenced to error amplifier reference)	23	24	25	V
		35V setting		33	34	35	V
		50V setting		48	49	50	V
		65V setting		63	64	65	V
V_{OVP_max-L}	Max. overvoltage threshold falling	25V setting	V_{OUT} falling (referenced to error amplifier reference)	22	23	24	V
		35V setting		32	33	34	V
		50V setting		47	48	49	V
		65V setting		62	63	64	V
V_{UVP-H}	Undervoltage threshold		V_{OUT} rising (referenced to error amplifier reference)	91%	93%	95%	
V_{UVP-L}	Undervoltage threshold		V_{OUT} falling (referenced to error amplifier reference)	88%	90%	92%	
PGOOD							
R_{PGOOD}	PGOOD pull-down switch R_{DSON}		1mA sinking		90	180	Ω
	Minimum BIAS for valid PGOOD		R_{5V} = 7.81kΩ, V_{PGOOD} < 0.4V	2			V
THERMAL SHUTDOWN (TSD)							
$T_{TSD-RISING}$	Thermal shutdown threshold		Temperature rising		175		°C

Typical values correspond to T_J = 25 °C. Minimum and maximum limits apply over T_J = -40 °C to 150 °C. Unless otherwise stated, V_I = V_{BIAS} = 12 V, V_{OUT} = 24 V, f_{SW} = 400 kHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{TSD\text{-}HYS}$	Thermal shutdown hysteresis			15		°C
TIMINGS						
t_d	Dead time	Driver setting = strong		5		ns
$STANDBY_{timer}$	STANDBY timer		130	150	170	µs

5.6 Timing Requirements

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
OVERALL DEVICE FEATURES						
	Minimum time low EN toggle	time measured from EN toggle from H to L and from L to H	1			µs

5.7 Typical Characteristics

The following conditions apply (unless otherwise noted): T_J = 25°C; V_{BIAS} = 12V

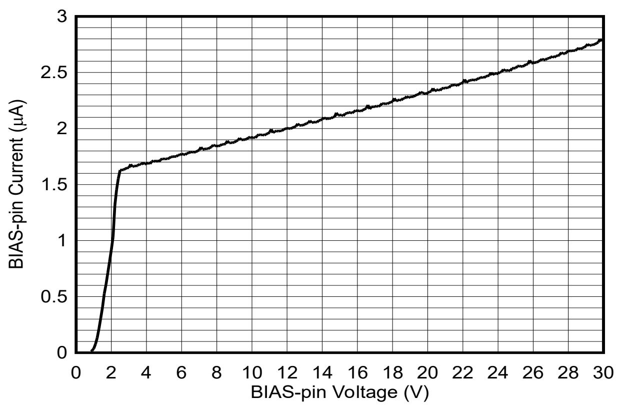


Figure 5-1. BIAS-Pin Current vs BIAS-Pin Voltage During shutdown

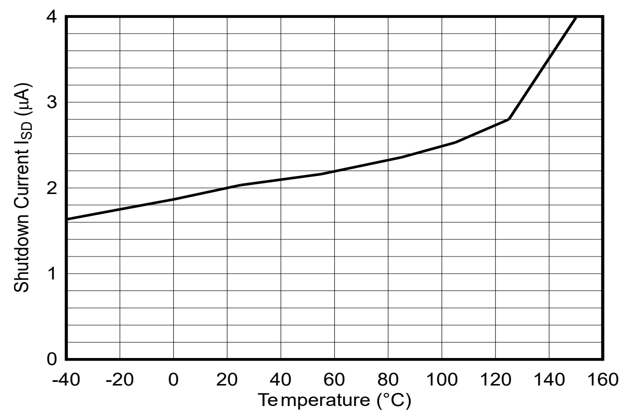


Figure 5-2. Shutdown Current vs Temperature

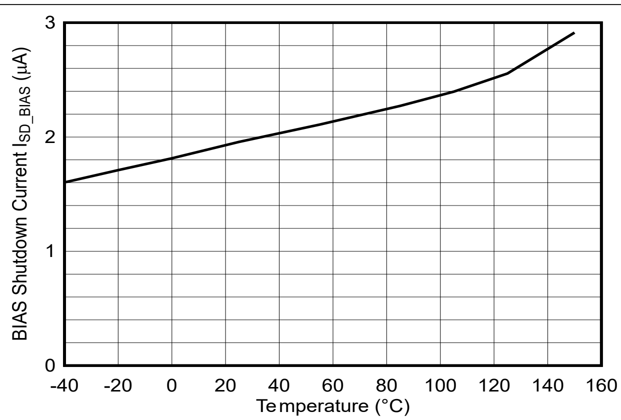
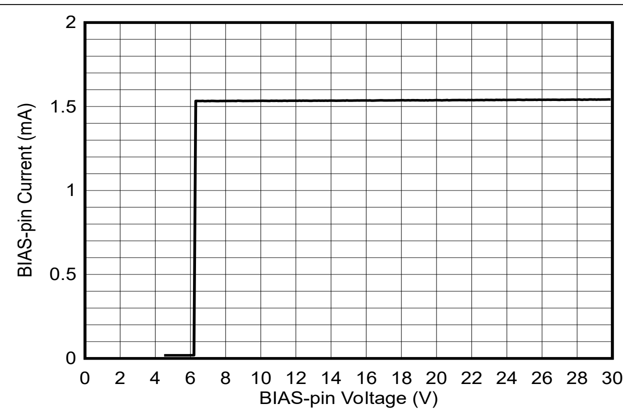


Figure 5-3. BIAS-Pin Current vs Temperature during Shutdown



MODE = FPWM

Figure 5-4. BIAS-Pin Quiescent Current vs BIAS-Pin Voltage

5.7 Typical Characteristics (continued)

The following conditions apply (unless otherwise noted): T_J = 25°C; V_{BIAS} = 12V

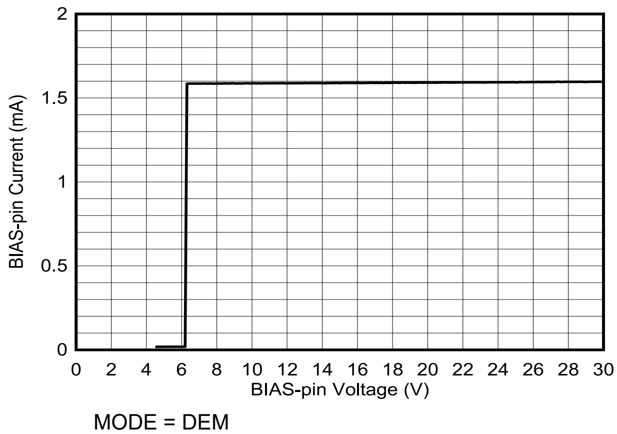


Figure 5-5. BIAS-Pin Quiescent Current vs BIAS-Pin Voltage

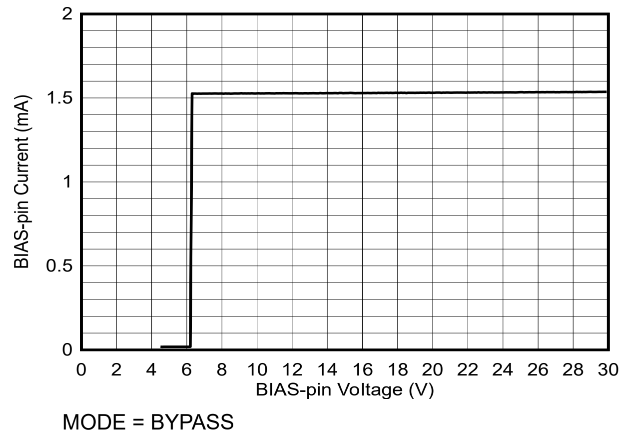


Figure 5-6. BIAS-Pin Quiescent Current vs BIAS-Pin Voltage

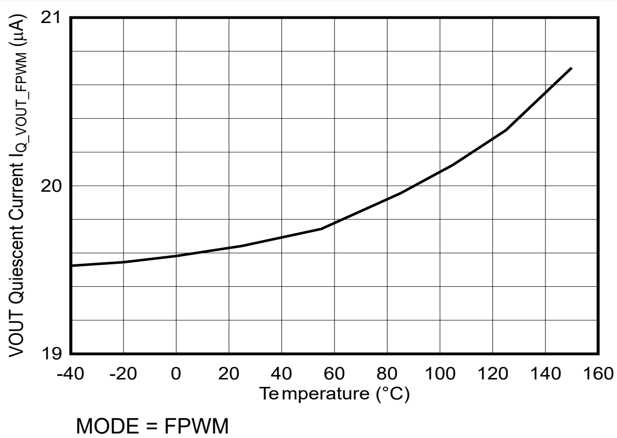


Figure 5-7. VOUT-pin Quiescent Current vs Temperature

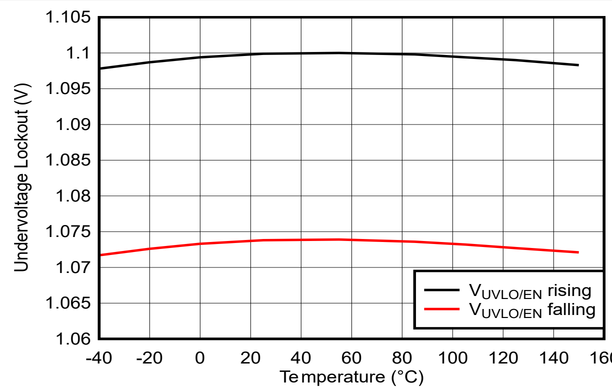


Figure 5-8. Undervoltage Lockout (UVLO) vs Temperature

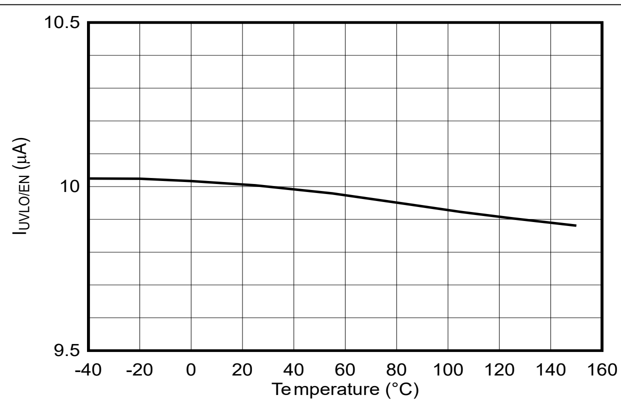


Figure 5-9. Undervoltage Lockout Hysteresis Current vs Temperature

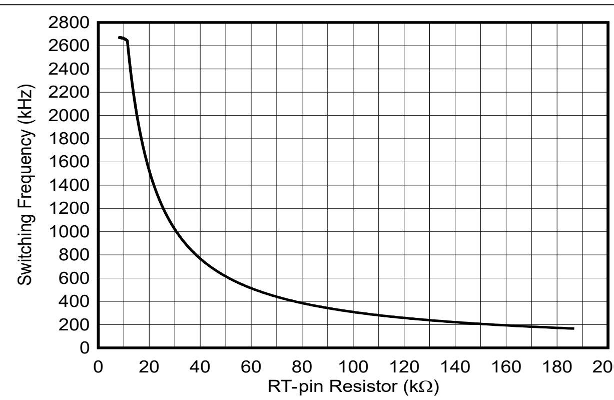


Figure 5-10. Switching Frequency vs RT Resistance

5.7 Typical Characteristics (continued)

The following conditions apply (unless otherwise noted): T_J = 25°C; V_{BIAS} = 12V

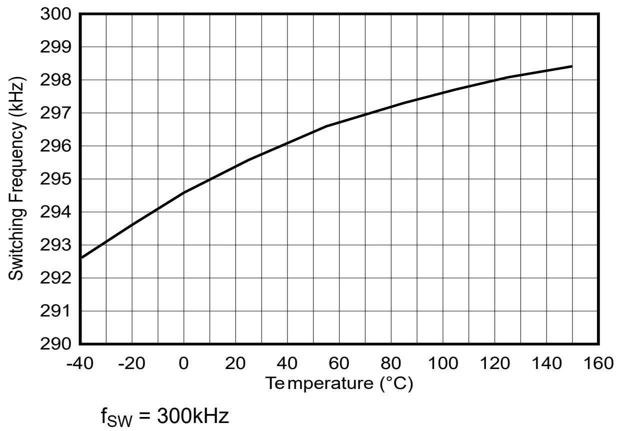


Figure 5-11. Switching Frequency vs Temperature

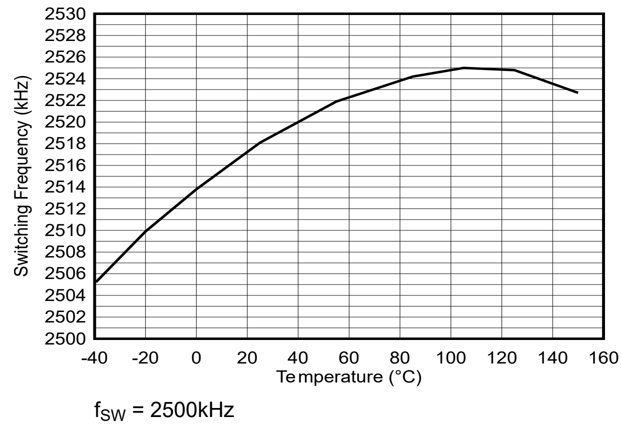


Figure 5-12. Switching Frequency vs Temperature

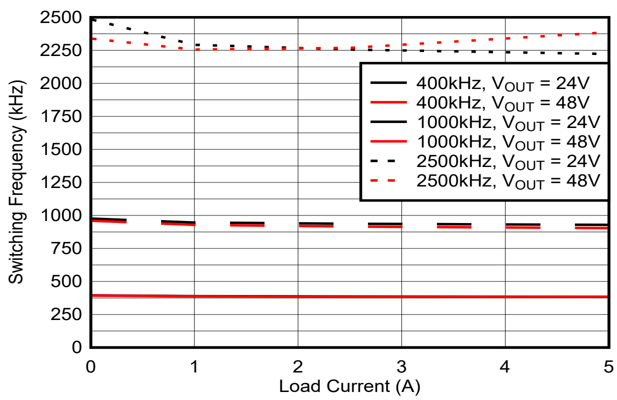


Figure 5-13. Switching Frequency vs Load Current

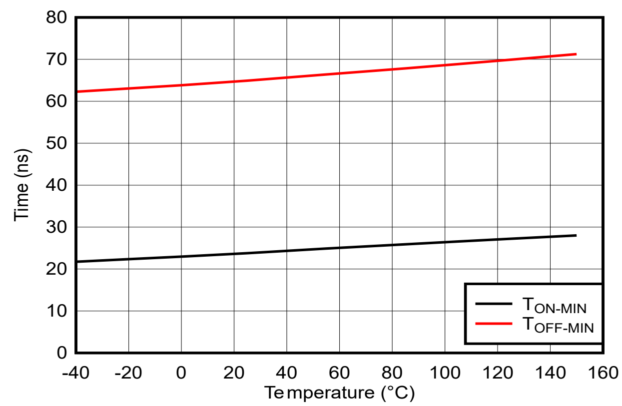


Figure 5-14. Minimum Controllable on Time vs Temperature

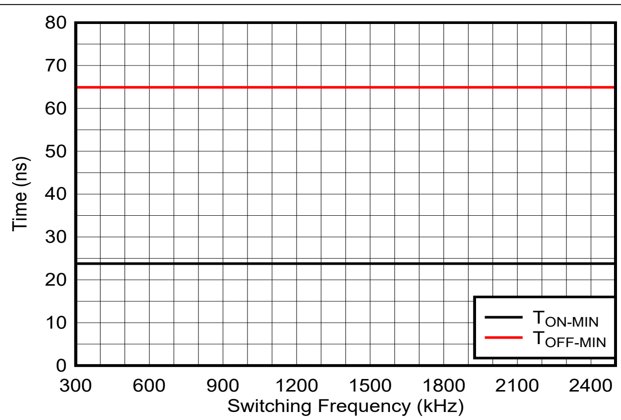


Figure 5-15. Minimum Controllable on Time vs Frequency

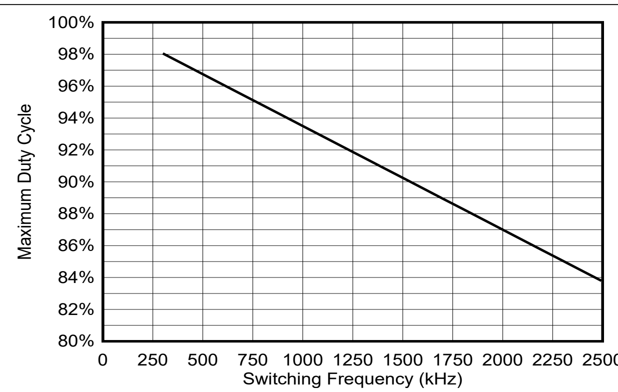
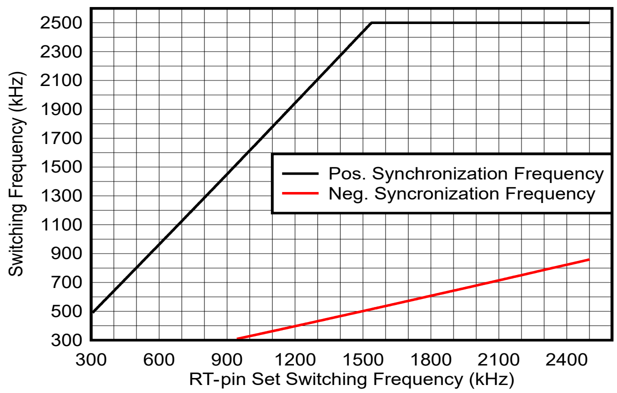


Figure 5-16. Maximum Duty Cycle vs Switching Frequency

5.7 Typical Characteristics (continued)

The following conditions apply (unless otherwise noted): T_J = 25°C; V_{BIAS} = 12V



Single Device

Figure 5-17. Synchronization Switching Frequency (SYNCIN) vs RT-Pin Set Switching Frequency

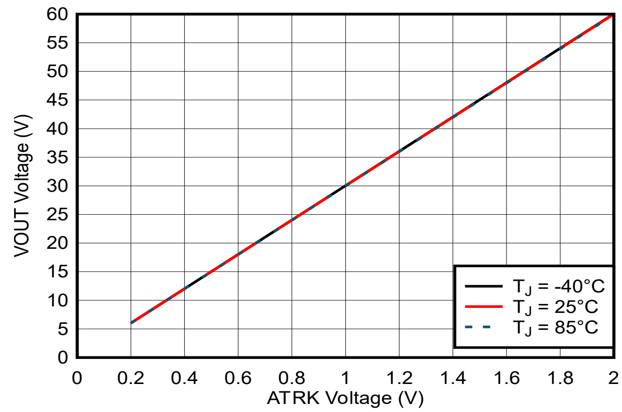
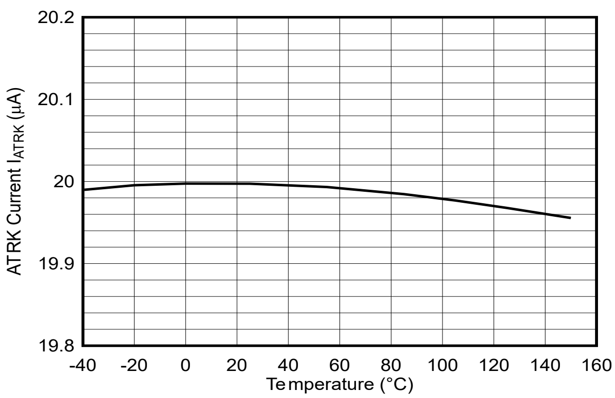


Figure 5-18. V_{OUT} Voltage vs V_{ATRK} Voltage



20µA ATRK Current

= active

Figure 5-19. ATRK Current I_{ATRK} vs Temperature

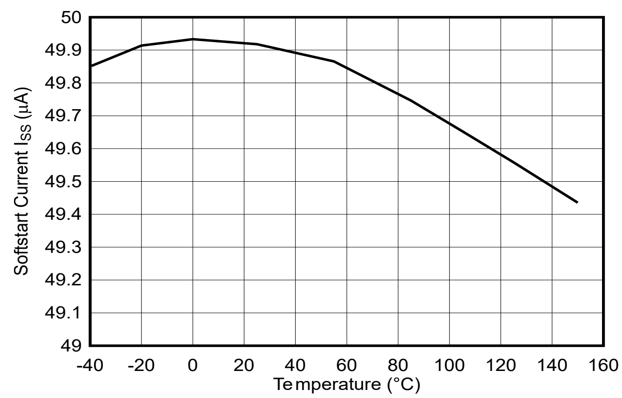


Figure 5-20. Softstart Current I_{SS} vs Temperature

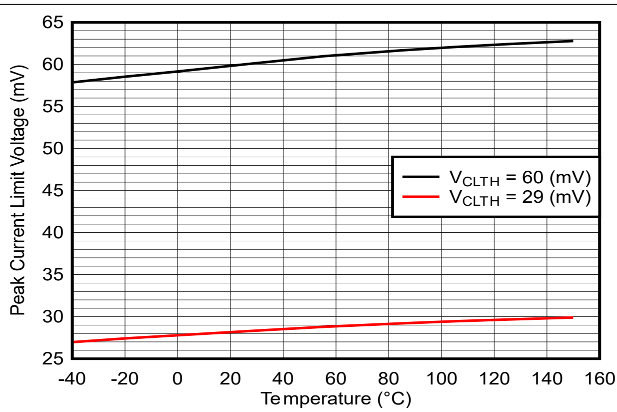


Figure 5-21. Peak Current Limit Voltage V_{CLTH} vs Temperature

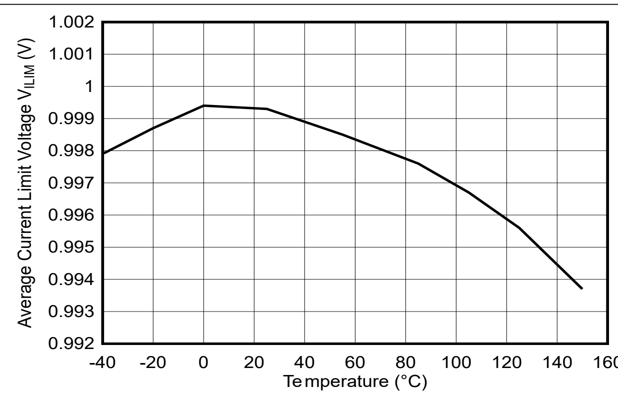


Figure 5-22. Average Current Limit Voltage V_{ILIM} vs Temperature

5.7 Typical Characteristics (continued)

The following conditions apply (unless otherwise noted): T_J = 25°C; V_{BIAS} = 12V

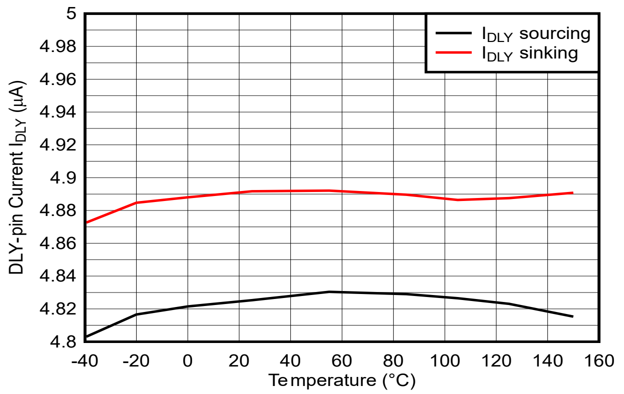


Figure 5-23. DLY Current I_{DLY} vs Temperature

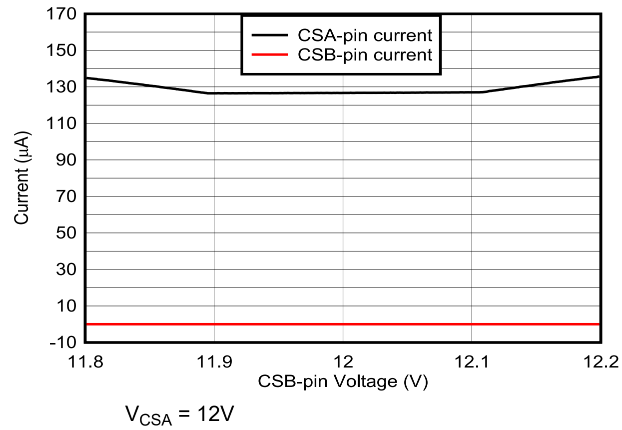


Figure 5-24. CSA and CSB Current vs CSB Voltage

6 Detailed Description

6.1 Overview

The LMG5126 is a wide input range boost converter using integrated GaN FETs. The device provides a regulated output voltage if the input voltage is equal or lower than the adjusted output voltage. The resistor-to-digital (R2D) interface offers the user a simple and robust selection of all the device functionality.

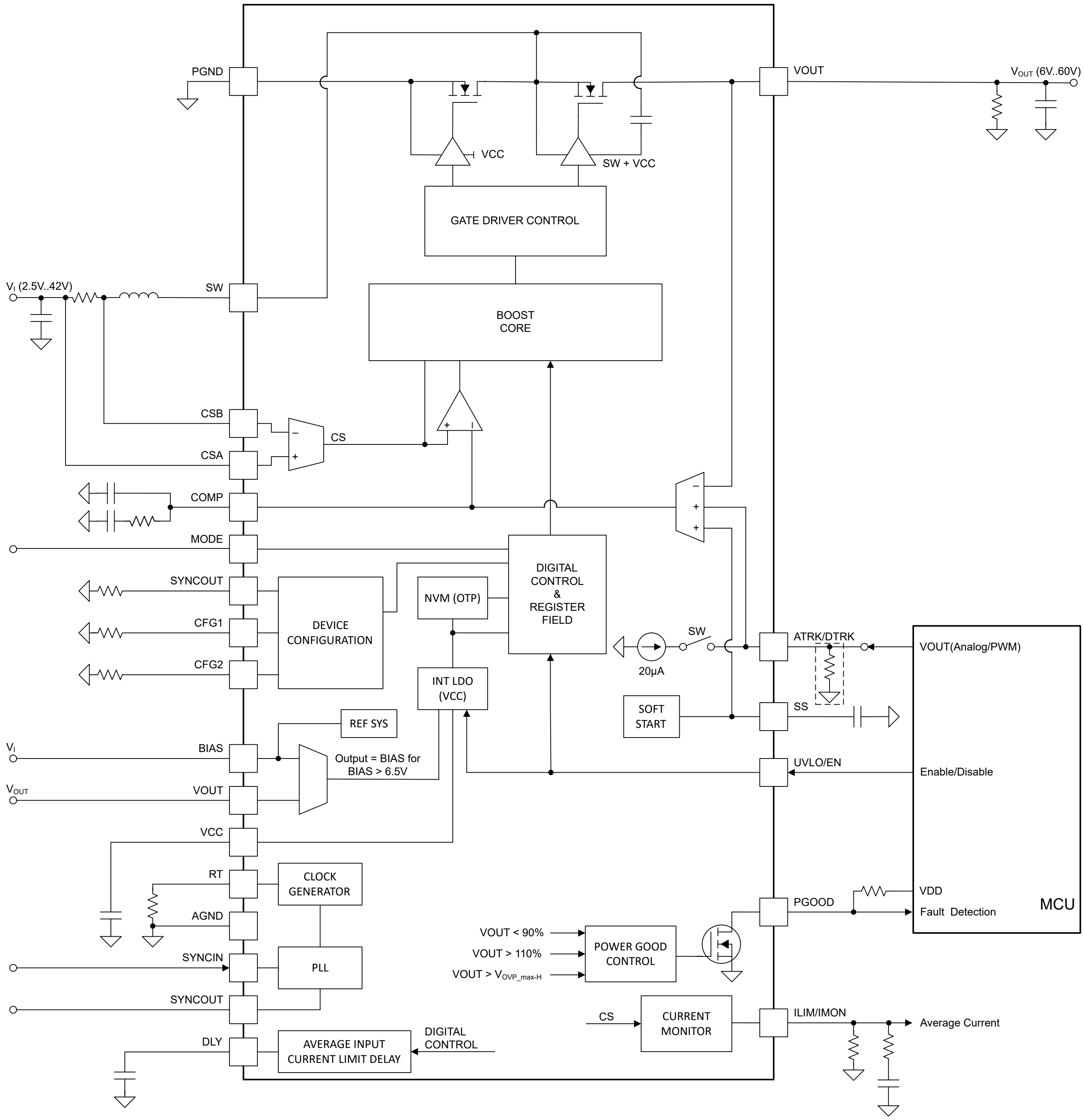
The operation modes DEM (Diode Emulation Mode) and FPWM (Forced Pulse Width Modulation) are on-the-fly pin-selectable during operation. The peak current mode control operates with fixed switching frequency set by the RT-pin. Through the activation of the dual random spread spectrum operation, EMI mitigation is achievable at any time of the design process.

The integrated average current monitor can help monitor or limit input current. The output voltage can be dynamically adjusted during operation (dynamic voltage scaling and envelope tracking). The adjustment is either possible by changing the analog reference voltage of the ATRK/DTRK-pin or the adjustment can be done directly with a PWM input signal on the ATRK/DTRK-pin.

The internal wide input LDOs provide a robust supply of the device functionality under different input and output voltage conditions. Due to the high drive capability and the automatic and headroom depended voltages selection, the power losses are kept at a minimum. The separate BIAS-pin can be connected to the input, output, or an external supply to further reduce power losses in the device. At all times, the internal supply voltage is monitored to avoid undefined failure handling.

The devices built-in protection features provide a safe operation under different fault conditions. There is a V_I undervoltage lockout protection to avoid brownout situations. Because the input UVLO threshold and hysteresis can be configured through an external feedback divider, the brownout is avoided under the different designs. The device has an output overvoltage protection. The selectable hiccup overcurrent protection avoids excessive short circuit currents by using the internal cycle-by-cycle peak current protection. Due to the integrated thermal shutdown, the device is protected against thermal damage caused by an overload condition. All output-related fault events are monitored and indicated at the open-drain PGOOD-pin of the device.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Device Configuration

The CFG1-pin defines the Clock Dithering, the 120% input current limit protection (I_{CL_latch}) and max. Overvoltage Protection behavior (OVP_{max_latch}), the sense voltage and the gate driver strength. The levels shown in Table 6-1 are selected by the specified resistors in Section 5.

Clock Dithering: Enables dual random spread spectrum (DRSS) clock dithering or disables clock dithering.

$latch_{ICL\&OVP\_max}$: When $latch_{ICL\&OVP\_max}$ is enabled and the peak current limit is exceeded by 20% or V_{OUT} reaches OVP_{max}, the device goes to the FAULT state (turns off and is latched). When $latch_{ICL\&OVP\_max}$ is disabled the device stays active and tries to limit the inductor current at peak current limit or V_{OUT} below the OVP_{max} level.

Sense Voltage: The device inductor peak current limit voltage $V_{(CSA\ -\ CSB)}$ at the sense resistor can be set to 29mV or 60mV.

Gate Drive Strength: The internal GaN FET gate driver strength can be set to weak (slower switch node rising/falling) or strong (faster switch node rising/falling). For highest performance (efficiency), the strong setting can be used, while for lowest EMI or not optimized PCB layout the weak setting is the better choice.

Table 6-1. CFG1-pin Settings

Level	Clock Dithering	$latch_{ICL\&OVP\_max}$	Gate Drive Strength	Sense Voltage
1	enabled (DRSS)	enabled	weak	29mV
2				60mV
3			strong	29mV
4				60mV
5		disabled	weak	29mV
6				60mV
7			strong	29mV
8				60mV
9	disabled	enabled	weak	29mV
10				60mV
11			strong	29mV
12				60mV
13		disabled	weak	29mV
14				60mV
15			strong	29mV
16				60mV

The CFG2-pin defines the power good pin OVP behavior and if the device uses the internal clock generator or an external clock applied at the SYNCIN-pin. Additionally, the CFG2-pin configures if the device is used as a single device or is part of a multi device configuration, the SYNCIN and SYNCOUT-pin is enabled/disabled accordingly. During clock synchronization the clock dither function is disabled. The levels shown in Table 6-2 are selected by the specified resistors in Section 5.

$PGOOD_{OVP\_enable}$: When $PGOOD_{OVP\_enable}$ is enabled the PGOOD-pin is pulled low for V_{OUT} above OVP (Overvoltage Protection) or below the UV (Undervoltage) threshold. If $PGOOD_{OVP\_enable}$ is disabled the PGOOD-pin is only pulled low when V_{OUT} is below UV (Undervoltage) threshold.

Single / Multichip:	Defines if the device is used stand-alone (single) using the internal oscillator or an external clock or in a multichip configuration. The device acts as controller in a multi device configuration when the device is configured as primary using the internal oscillator or an external clock applied at the SYNCIN-pin. At the SYNCOUT-pin a phase shifted clock (90°, 120° or 180°) is generated for the next device. The device is used as secondary syncing the clock to the SYNCIN-pin signal when the device is configured as secondary. At the SYNCOUT-pin a phase shifted clock (90° or 120°) can be generated for the next device.
SYNCIN:	Defines if the clock syncing function at the SYNCIN-pin is enabled or disabled. The device is only syncing to an external clock applied to the SYNCIN-pin when SYNCIN is active. The SYNCIN-pin circuit is disabled to save power when SYNCIN is disabled.
SYNCOUT:	Defines if the SYNCOUT-pin is enabled or disabled. A clock is only generated at the SYNCOUT-pin when SYNCOUT is active. The clock generation at the SYNCOUT-pin is disabled to save power when SYNCOUT is disabled.
SYNCOUT Phase Shift:	Phase shift of the SYNCOUT signal.
Clock Dithering:	In case the internal oscillator is used the clock dithering is set according to the CFG1-pin setting Clock Dithering Mode. When an external clock is used the clock dithering function is disabled ignoring the CFG1-pin setting.

Table 6-2. CFG2-pin Settings

<table>
<tr><th>Level</th><th>PGOOD$_{OVP_enable}$</th><th>Single / Multichip</th><th>SYNCIN</th><th>SYNCOUT</th><th>Clock Dithering</th></tr>
<tr><td>1</td><td rowspan="8">enabled</td><td>Single int. clock</td><td>disabled</td><td rowspan="2">disabled</td><td>CFG1-pin</td></tr>
<tr><td>2</td><td>Single ext. clock</td><td rowspan="7">enabled</td><td rowspan="7">disabled</td></tr>
<tr><td>3</td><td rowspan="3">Primary</td><td>90°</td></tr>
<tr><td>4</td><td>120°</td></tr>
<tr><td>5</td><td>180°</td></tr>
<tr><td>6</td><td rowspan="3">Secondary</td><td>disabled</td></tr>
<tr><td>7</td><td>90°</td></tr>
<tr><td>8</td><td>120°</td></tr>
<tr><td>9</td><td rowspan="8">disabled</td><td>Single int. clock</td><td>disabled</td><td rowspan="2">disabled</td><td>CFG1-pin</td></tr>
<tr><td>10</td><td>Single ext. clock</td><td rowspan="7">enabled</td><td rowspan="7">disabled</td></tr>
<tr><td>11</td><td rowspan="3">Primary</td><td>90°</td></tr>
<tr><td>12</td><td>120°</td></tr>
<tr><td>13</td><td>180°</td></tr>
<tr><td>14</td><td rowspan="3">Secondary</td><td>disabled</td></tr>
<tr><td>15</td><td>90°</td></tr>
<tr><td>16</td><td>120°</td></tr>
</table>

The SYNCOUT-pin is used at startup to define the maximum V_{OUT} Over Voltage Protection level (OVP_{max}) and the 20µA ATRK-pin current. Enable the 20µA ATRK-pin current to program V_{OUT} with a resistor, for voltage tracking TI recommends disabling the current. The levels shown in Table 6-3 are selected by the specified resistors in Section 5.

OVP_{max}:	Sets the maximum V_{OUT} overvoltage protection level to 25V, 35V, 50V or 65V.
20µA ATRK-pin current:	Enables and disables the 20µA ATRK-pin current.

Table 6-3. SYNCOUT-Pin Settings

Level	OVP_{max}	20µA ATRK-pin current
1	25V	enabled
2		disabled
3	35V	enabled
4		disabled
5	50V	enabled
6		disabled
7	65V	enabled
8		disabled

6.3.2 Device Enable/Disable (UVLO/EN)

During shutdown the UVLO/EN-pin is pulled low by the internal resistor R_{EN}. When $V_{UVLO/EN}$ rises above $V_{EN\text{-}RISING}$, R_{EN} is disabled and the $I_{UVLO/EN}$ (typically 10µA) current source is enabled to provide the UVLO functionality. The device boots up, reads the configuration and enters STANDBY state (see Functional State Diagram). When $V_{UVLO/EN}$ rises above $V_{UVLO\text{-}RISING}$ the $I_{UVLO/EN}$ current source is disabled and the device enters START state executing the soft-start ramping up V_{OUT} in DEM operation. A hysteresis $V_{EN\text{-}HYS}$ and $V_{UVLO\text{-}HYS}$ is implemented. Select the external UVLO resistor voltage divider (R_{UVT} and R_{UVB}) according to Equation 1 and Equation 2.

$$R_{UVT} = \frac{V_{I\_ON} - \frac{V_{UVLO-RISING}}{V_{UVLO-FALLING}} \times V_{I\_OFF}}{I_{UVLO-HYS}} \tag{1}$$

$$R_{UVB} = \frac{V_{UVLO-FALLING} \times R_{UVT}}{V_{I\_OFF} - V_{UVLO-FALLING}} \tag{2}$$

where

- V_{I_ON} is the input voltage where the device turns on.
- V_{I_OFF} is the input voltage where the device turns off.

A UVLO capacitor (C_{UVLO}) is required in case V_I drops below V_{OFF} momentarily during startup or a load transient at low V_I. If the required UVLO capacitor is large, an additional series UVLO resistor (R_{UVLOS}) can be used to quickly raise the voltage at the UVLO-pin when $I_{UVLO\text{-}HYS}$ is disabled.

The UVLO/EN-pin voltage is not allowed to exceed the BIAS-pin voltage +0.3V (see Absolute Maximum Ratings) as the ESD-diode between UVLO/EN-pin and BIAS-pin gets conducting. However, a higher voltage up to 42V (Recommended Operating Conditions) is applicable at the UVLO/EN-pin when the current is limited to maximum 100µA with a series resistor.

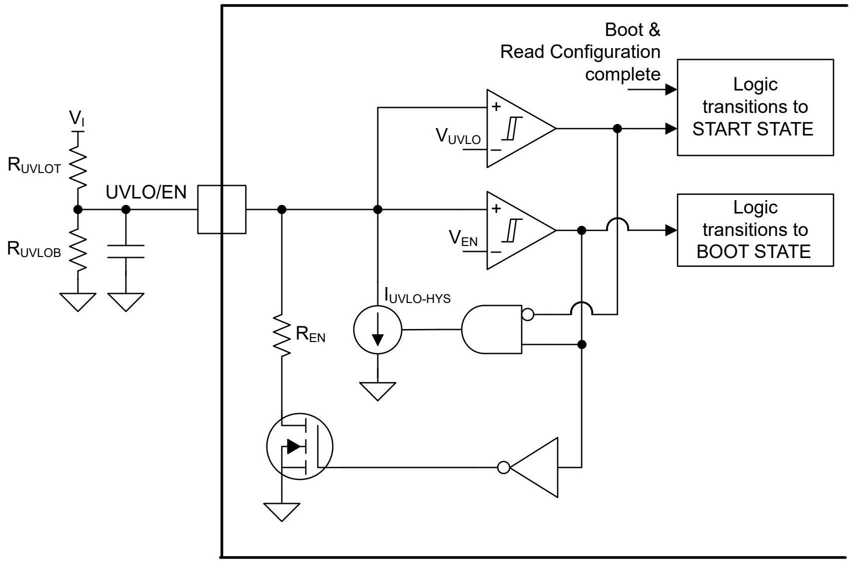


Figure 6-1. Functional Block Diagram UVLO and EN

6.3.3 Multi Device Operation

For multi device configuration the phase shift between the phases is set by the CFG2-pin (see CFG2-pin Settings). The CFG2-pin is read out during boot up and the setting is latched. The primary device switching frequency can be synchronized to an external clock applied at the SYNCIN-pin (see Switching Frequency and Synchronization (SYNCIN)). The primary device sets the switching frequency and communicates the operation mode via the SYNCOUT-pin to the secondary device.

Table 6-4. Primary to Secondary device communication

Pin	Primary SYNCIN = off	Primary SYNCIN = on	Secondary SYNCOUT = off	Secondary SYNCOUT = on
SYNCIN	Disabled	High: Use internal oscillator. Pulse: Sync to external clock. Low: Use internal oscillator.	High: Bypass mode. Pulse: Operation as defined by MODE-pin. Low: Stop switching.	High: Bypass mode. Pulse: Operation as defined by MODE-pin. Low: Stop switching.
SYNCOUT	High: Communicate bypass mode to secondary device. Pulse: Communicate normal operation. Low: Communicate stop switching to secondary device.	High: Communicate bypass mode to secondary device. Pulse: Communicate normal operation. Low: Communicate stop switching to secondary device.	Disabled	High: Communicate bypass mode to secondary device. Pulse: Communicate normal operation. Low: Communicate stop switching to secondary device.

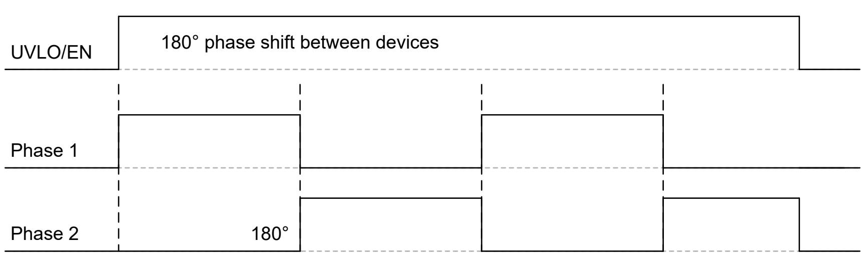


Figure 6-2. 2 Devices 2-phase Operation

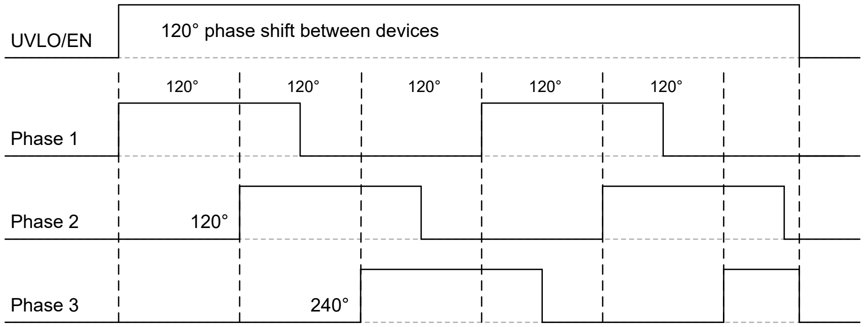


Figure 6-3. 3 Devices 3-phase Operation

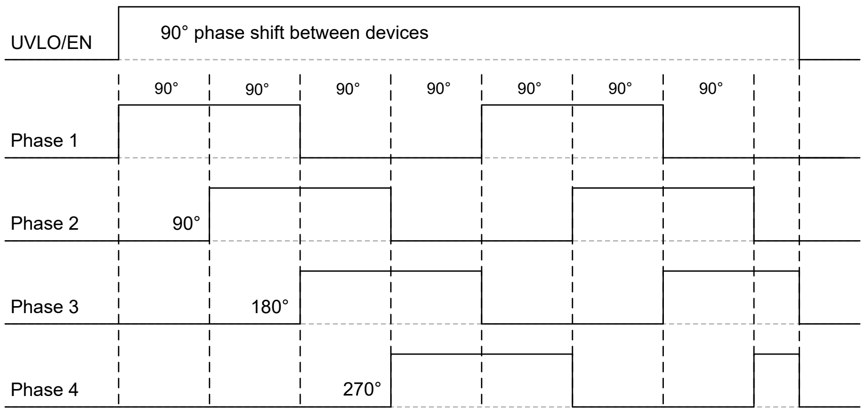


Figure 6-4. 4 Devices 4-phase Operation

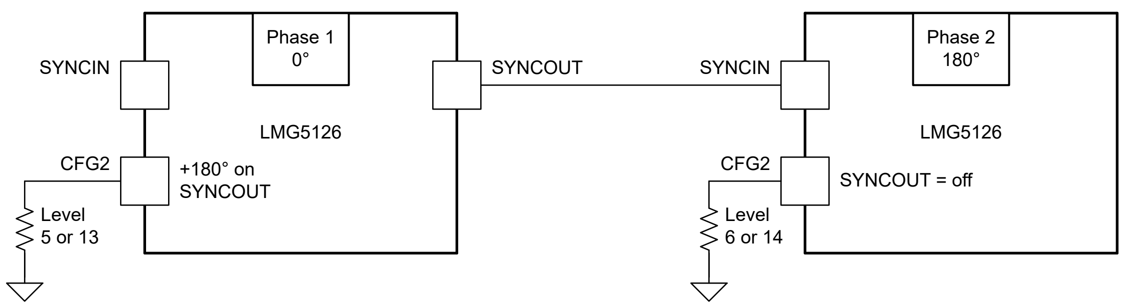


Figure 6-5. 2-Device Configuration

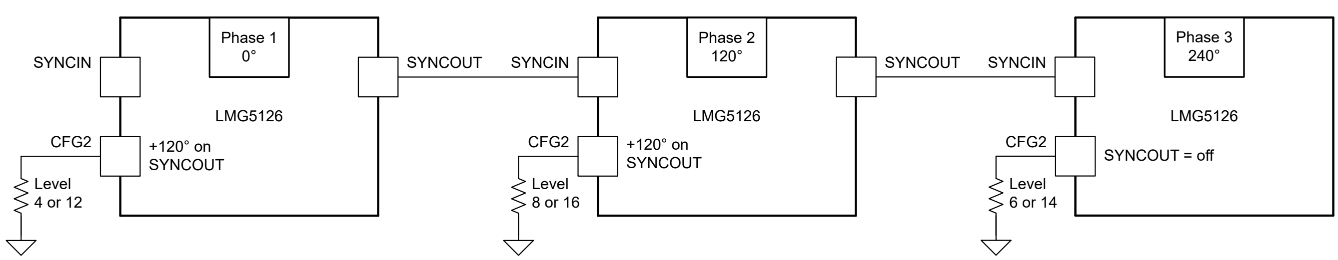


Figure 6-6. 3-Device Configuration

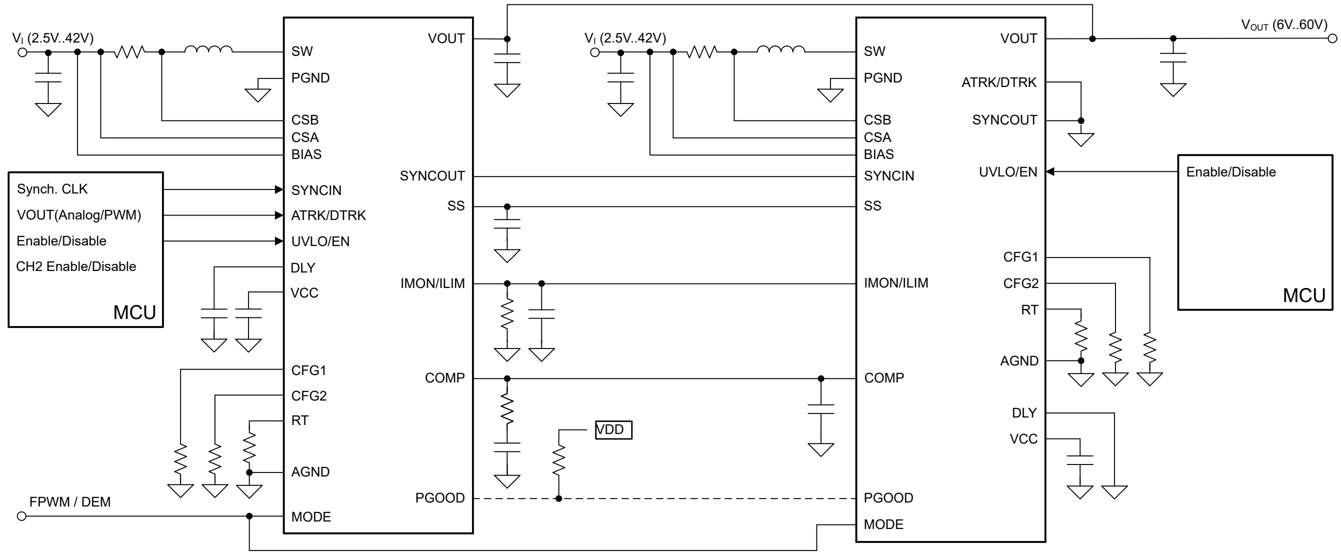


Figure 6-7. Typical Application 2-device, 2-phase Operation

6.3.4 Switching Frequency and Synchronization (SYNCIN)

The switching frequency of 300kHz to 2.5MHz is set by the RT resistor connected between the RT-pin and AGND. The RT resistor must be selected between 12kΩ and 100kΩ according to Equation 4. If configured to use an external clock the device can synchronize the switching frequency to an external clock applied at the SYNCIN-pin. For single device configuration within ±50% of the set frequency by the RT-pin, in multi device configuration within ±25%. The internal clock is synchronized at the rising edge of the external clock signal applied at the SYNCIN-pin. The CFG1-pin Spread Spectrum setting is ignored during frequency synchronization and clock dithering is disabled.

The device always starts with the internal clock and starts synchronizing to an applied external clock during the START PHASE and the ACTIVE state (see Functional State Diagram). The device synchronizes to the external clock as soon as the clock is applied and switches back to the internal clock in case the external clock stops.

$$F_{SW} = \frac{1}{\frac{R_{RT} \times s}{31.5G\Omega} + 18ns} \tag{3}$$

$$R_{RT} = \left(\frac{1}{F_{SW}} - 18\ ns\right) \times 31.5\frac{G\Omega}{s} \tag{4}$$

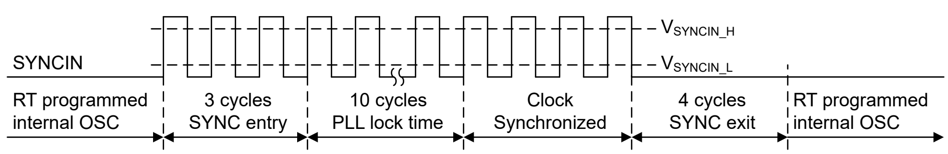


Figure 6-8. Clock Synchronization

6.3.5 Dual Random Spread Spectrum (DRSS)

The device provides a digital spread spectrum, which reduces the EMI of the power supply over a wide frequency range. Enable the spread spectrum by the CFG1-pin setting. When the spread spectrum is enabled, the internal modulator dithers the internal clock. When the device is configured to use an external clock applied at the SYNCIN-pin, the internal spread spectrum is disabled. DRSS combines a low frequency triangular modulation profile with a high frequency cycle-by-cycle random modulation profile. The low frequency triangular modulation improves performance in lower radio frequency bands (for example AM band), while the high frequency random modulation improves performance in higher radio frequency bands (for example FM band). In addition, the frequency of the triangular modulation is further modulated randomly to reduce the likelihood of any audible tones. To minimize output voltage ripple caused by spread spectrum, duty cycle is modified on a cycle-by-cycle basis to maintain a nearly constant duty cycle when dithering is enabled.

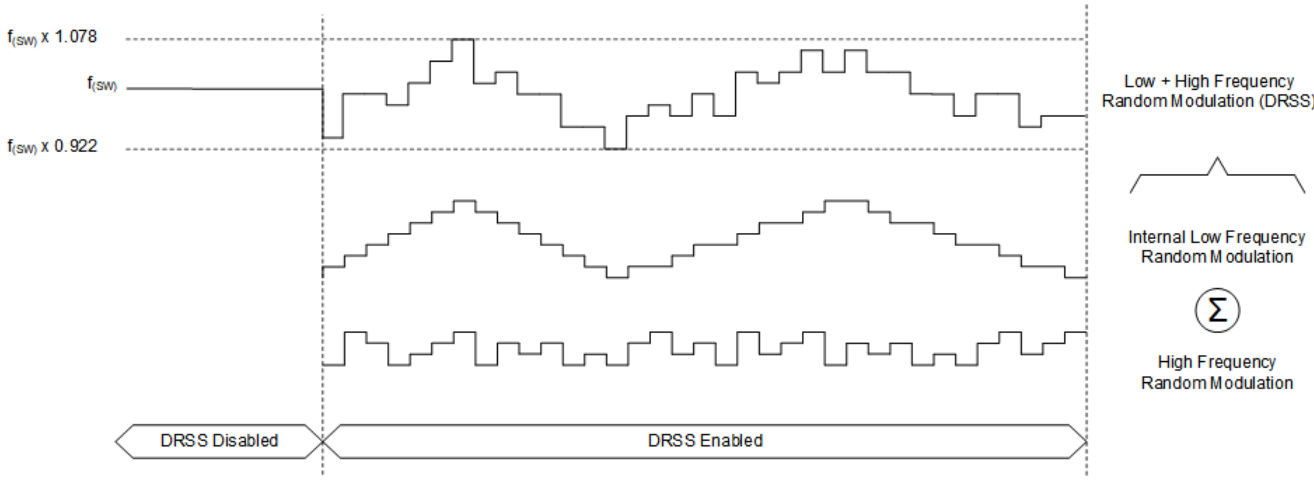


Figure 6-9. Dual Random Spread Spectrum

6.3.6 Operation Modes (BYPASS, DEM, FPWM)

The device supports bypass mode, forced PWM (FPWM) and diode emulation mode (DEM) operation. The mode can be changed on the fly and is set by the MODE-pin. Bypass mode is automatically activated for V_{OUT} < V_I. In multi-device stacked operation all devices must use the same mode.

The device operation mode is set to DEM for V_{MODE} < 0.4V and to FPWM for V_{MODE} > 1.2V.

Table 6-5. Mode-pin Settings

Operation Mode	MODE-pin
DEM	$V_{MODE} < 0.4V$
FPWM	$V_{MODE} > 1.2V$

In Diode Emulation Mode (DEM) current flow from V_{OUT} to V_I is prevented. The SW-pin voltage is monitored during the high-side on time and the high-side switch is turned off when the voltage falls below the zero current detection threshold V_{ZCD}. The device works in Discontinuous Conduction Mode (DCM) for light load and finally skips pulses, which improves light load efficiency. In DEM operation when COMP falls below typically 460mV the controller starts skipping pulses. Calculate the skip entry point for the input current with formula Equation 5 and for the output current with formula Equation 6. The internal boot capacitor needs to stay charged also during pulse skipping to drive the high side FET which causes boot refresh pulses. As current flow from V_{OUT} to V_I is prevented, a minimum load according to Equation 7 and Equation 8 is required to prevent V_{OUT} voltage runaway during pulse skipping. In case there is not enough load to compensate for the boot refresh pulses, V_{OUT} increases to the programmed V_{OVP_max} level.

$$I_{I\_skip} = \frac{1.5\mu \times \frac{V_I}{L}}{0.48 \times \frac{f_{SW}}{40K} + 250\mu \times R_{SNS} \times \frac{V_I}{L}} \quad (5)$$

$$I_{OUT\_skip} = \frac{\frac{V_I}{V_{OUT}} \times \frac{V_I}{L} \times 1.5\mu}{0.48 \times \frac{f_{SW}}{40K} + 250\mu \times R_{SNS} \times \frac{V_I}{L}} \quad (6)$$

$$I_{OUT\_LOAD} = \frac{V_I^2 \times F_{SW} \times 0.0484\mu s^2}{2 \times (V_{OUT} - V_I) \times L} \quad (7)$$

$$R_{LOAD} = \frac{2 \times V_{OUT} \times (V_{OUT} - V_I) \times L}{V_I^2 \times F_{SW} \times 0.0484 \mu s^2} \quad (8)$$

In Forced Pulse With Modulation Mode (FPWM) the converter keeps switching also for light load with fixed frequency in continuous conduction mode (CCM). This mode improves light load transient response.

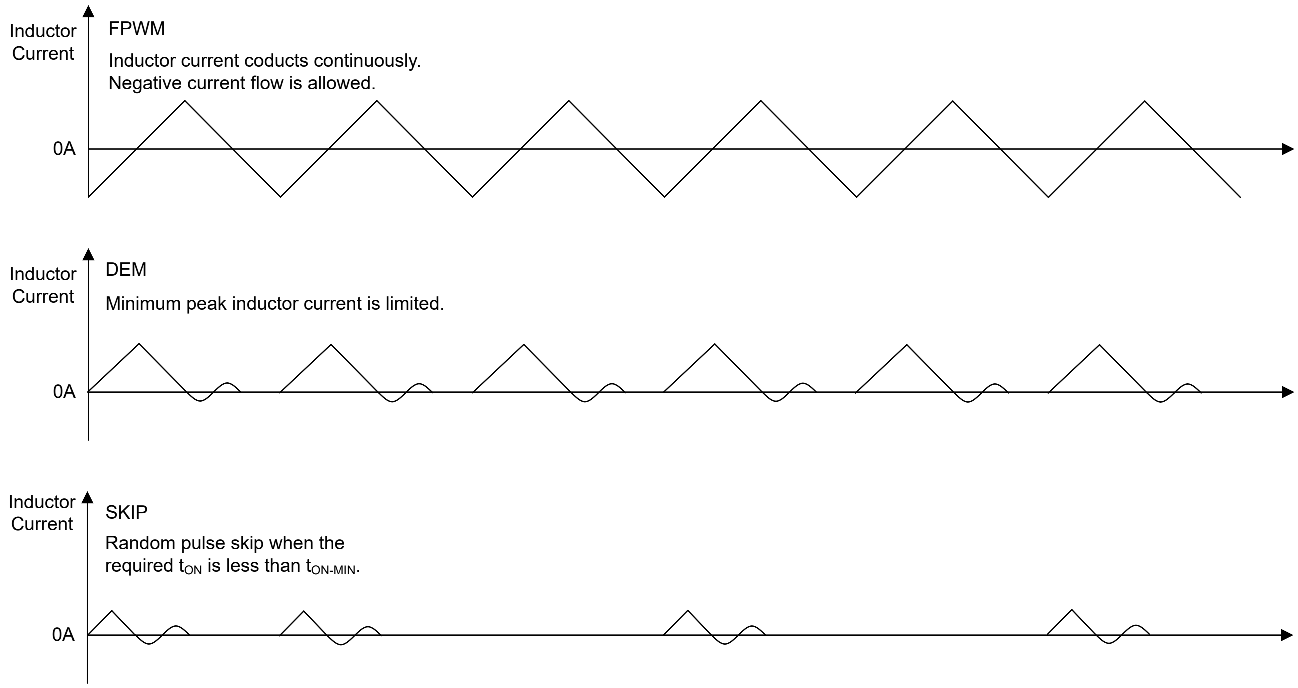


Figure 6-10. Inductor current waveform for the different operation modes.

In Bypass Mode (BYPASS) V_I is connected to V_{OUT} (no regulation) by turning on the high side FET. Positive current flowing from V_I to V_{OUT} cannot be controlled while current flow from V_{OUT} to V_I is prevented for DEM setting and limited to V_{NCLTH} for FPWM setting. During Bypass Mode the device initiates boot refresh pulses with a frequency >20kHz to keep the boot capacitor charged.

The device enters and exits Bypass mode when the conditions in table Bypass Mode Entry, Exit are met.

Table 6-6. Bypass Mode Entry, Exit

Operation Mode	Bypass	Conditions
DEM / FPWM	Entry	$V_{OUT} < V_I - 100mV$ and $V_{COMP} < V_{COMP-MIN} + 100mV$
DEM	Exit	$V_{COMP} > V_{COMP-MIN} + 100mV$ || $(V_{CSA} - V_{CSB}) < V_{ZCD\_BYP}$
FPWM	Exit	$V_{COMP} > V_{COMP-MIN} + 100mV$ || $(V_{CSA} - V_{CSB}) < V_{NCLTH}$

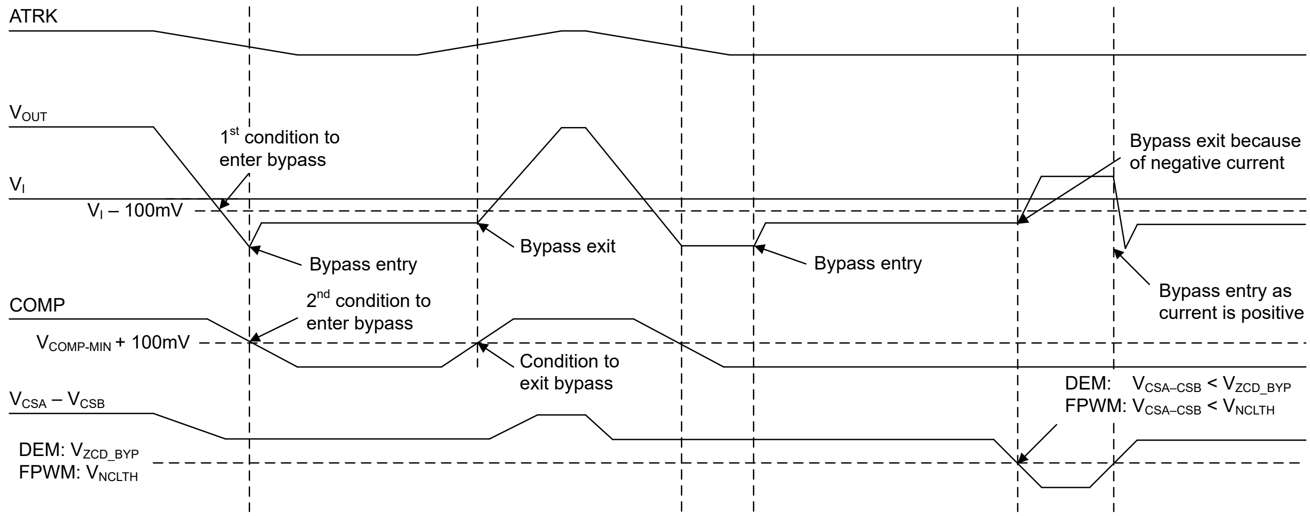


Figure 6-11. Bypass Mode Entry, Exit

6.3.7 VCC Regulator, BIAS (BIAS-pin, VCC-pin)

The gate driver is powered by an internal 5V VCC regulator. The VCC regulator is sourced from the BIAS-pin supporting up to 42V for V_{BIAS} > $V_{BIAS\text{-}RISING}$ or the VOUT-pin for V_{BIAS} < $V_{BIAS\text{-}FALLING}$. Connect the BIAS-pin to a voltage ≥2.5V (for example V_I or 5V) as the reference system is permanently supplied by the BIAS-pin and shuts down for voltages <2V. The recommended VCC capacitor value is 4.7µF.

The integrated current limit prevents device damage when VCC is overloaded or the VCC-pin is shorted to ground. VCC can source up to 100mA ($I_{VCC\text{-}CL}$).

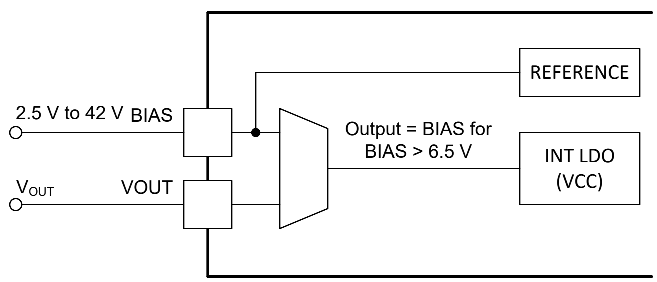


Figure 6-12. On the Fly BIAS Supply Selection

6.3.8 Soft Start (SS-pin)

At start-up during the START state (see Functional State Diagram) the device regulates the error amplifiers reference to the SS-pin voltage or the ATRK/DTRK-pin voltage, whichever is lower. The regulated reference results in a gradual rise of the output voltage V_{OUT}. During soft start the device forces diode emulation mode (DEM) until the soft start done signal is generated.

The external soft start capacitor is first discharged to the $V_{SS\text{-}DIS}$ voltage, then charged by the I_{SS} current and the soft start done signal is generated when $V_{SS\text{-}DONE}$ is reached. The soft start time (t_{SS}) varies with the input supply voltage as V_{OUT} is equal to V_I at startup. In figure Soft Start at the time t_1 the soft start current is activated. At t_2 the soft start voltage reached the V_I voltage level and V_{OUT} starts to rise until V_{OUT} reaches the programmed V_{OUT} value at t_3. The soft start done signal is generated at t_4 when the SS-pin voltage reaches $V_{SS\text{-}DONE}$. The SS-pin voltage continues to rise until V_{VCC} is reached where the soft start current is deactivated.

$$t_{SS\_t1\_t4} = 2.2 \times \frac{C_{SS}}{I_{SS}} \tag{9}$$

$$t_{SS\_t2\_t3} = \frac{C_{SS}}{I_{SS}} \times \frac{V_{OUT} - V_I}{30} \tag{10}$$

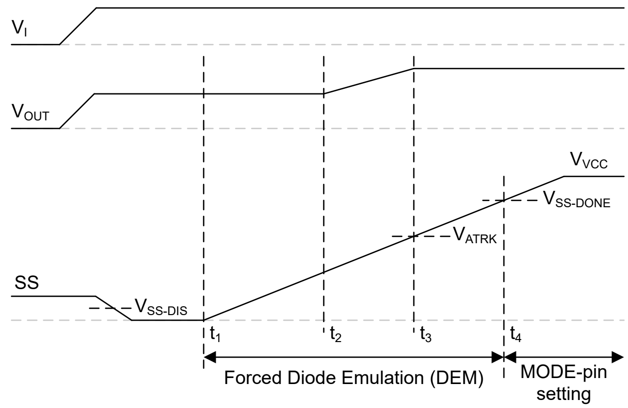


Figure 6-13. Soft Start

6.3.9 V_{OUT} Programming (VOUT, ATRK, DTRK)

The output voltage V_{OUT} is sensed at the VOUT-pin. Program V_{OUT} between 6V and 60V by connecting a 10kΩ to 100kΩ resistor at the ATRK/DTRK-pin, applying a voltage between 0.2V and 2V or a digital signal between 8% and 80% duty cycle. At startup during the STANDBY state (see Functional State Diagram) the ATRK/DTRK-pin programming method analog signal or digital signal is detected. At the transition to the START state the ATRK/DTRK-pin programming method is latched and cannot be changed during operation. Allow a DTRK signal to be present for at least three cycles so that the DTRK signal is detected before the programming method latches. ATRK supports up to 10kHz signals, however, change the ATRK-pin voltage or the DTRK duty cycle slow enough that V_{OUT} is able to follow. In case the ATRK/DTRK-pin set reference voltage is changed faster than the converters bandwidth, the inductor current exceeds peak current limit until the slope compensation settles. The device tries to regulate V_{OUT} as well for ATRK < 0.2V or > 2V, but performance is not endured. Enable the 20µA current by SYNCOUT setting for V_{OUT} programming by resistor. The 20µA current is sourced through the ATRK-pin and generates the required ATRK voltage for the target VOUT voltage via the external resistor. For analog tracking (ATRK) or digital tracking (DTRK), TI recommends to disable the 20uA current.

Equation for programming V_{OUT} by resistor:

$$R_{ATRK} = \frac{V_{OUT}}{6V} \times 10k\Omega \tag{11}$$

Equation for programming V_{OUT} by voltage (ATRK):

$$V_{OUT} = V_{ATRK} \times 30 \tag{12}$$

Equation for programming V_{OUT} by digital signal (DTRK):

$$V_{OUT} = 0.75 \frac{V}{\%} \times \text{Duty Cycle} \tag{13}$$

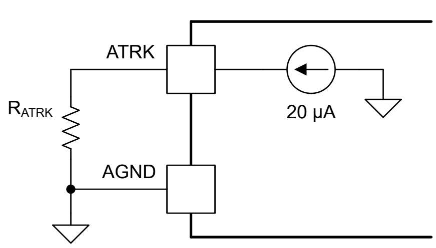


Figure 6-14. V_{OUT} Programming by Resistor

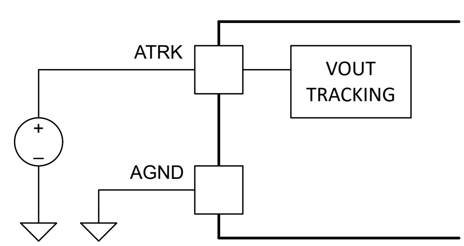


Figure 6-15. V_{OUT} Tracking by Analog Voltage

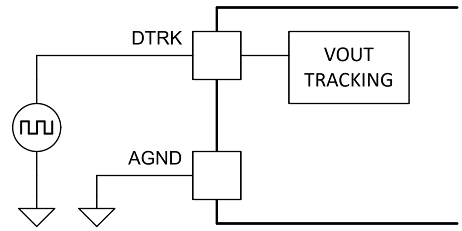


Figure 6-16. V_{OUT} Tracking by Digital Signal

6.3.10 Protections

The device has the following protections implemented. Figure 6-17 shows in which state of the Functional State Diagram which protection is active. The protection is active for the grey shaded states having the same grey shading, for example TSD is active in STANDBY state including THERMAL SHUTDOWN state but not in FAULT state.

- Thermal shutdown (TSD) turning off the device at high temperature.
- Undervoltage Lockout (UVLO) turning off the device at low supply voltage.
- VCC Undervoltage Lockout (VCC UVLO) avoiding too low low-side gate driver voltage. The device stops switching until VCC is recovered.
- BOOT CAP Undervoltage Lockout (BOOT CAP UVLO) avoiding too low high-side gate driver voltage. The device initiates refresh pulses (512 cycles hiccup mode off time). See GAN Drivers, Integrated Boot Capacitor and Diode, and Hiccup Mode Fault Protection for details.
- Overvoltage Protection (OVP), when triggered the device stops switching until V_{OUT} is back on target. There are two OVPs implemented:
  - OVP_{max}, which is a programmable absolute value (typically 64V, 49V, 34V, or 24V). When triggered the device either stops switching and enters FAULT state ($latch_{ICL\&OVP\_max}$ = 1) or stops switching until V_{OUT} is back on target ($latch_{ICL\&OVP\_max}$ = 0).
  - OVP, which triggers when V_{OUT} is 110% of the programmed value. When triggered the device stops switching until V_{OUT} is back on target.
- Undervoltage Protection (UVP), when triggered the device continues operation but pulls the PGOOD-pin low.
- Peak Current Limit (PCL), limiting the switch current. See Current Sense Setting and Switch Peak Current Limit (CSA, CSB) for details.
- Input Current Limit (ICL), limiting the peak switch current to 120% of the peak current limit. This protection is enabled and disabled by $latch_{ICL\&OVP\_max}$ programming.
- Average Input Current Limit (ILIM), limiting the average input current to the programmed value by R_{ILIM}. See Input Current Limit and Monitoring (ILIM, IMON, DLY) for details.

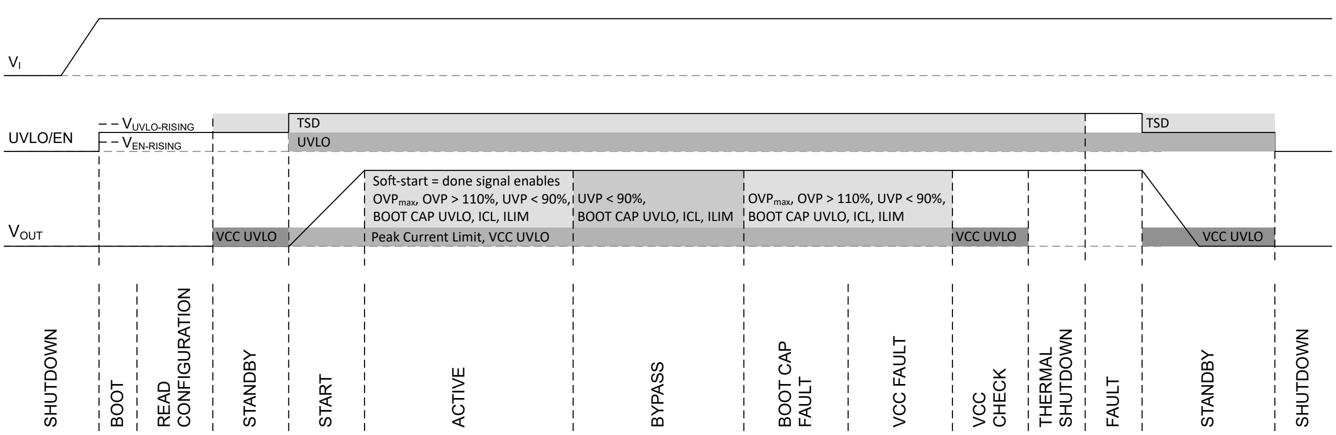


Figure 6-17. Protections

6.3.10.1 V_{OUT} Overvoltage Protection (OVP)

The Overvoltage Protection (OVP) monitors the VOUT-pin using two thresholds. The programmable threshold V_{OVP_max-H} limiting V_{OUT} to 64V, 49V, 34V or 24V, and the V_{OVP-H} threshold limiting the programmed V_{OUT} to 110% of the programmed voltage. In BYPASS state the 110% $_{OVP-H}$ detection is disabled, but the V_{OVP_max-H} is active.

When V_{OUT} rises above the V_{OVP-H} threshold (not active during Bypass), the low-side driver is turned off and the high-side driver is turned on. Current flow from V_I to V_{OUT} is monitored through CSA - CSB allowing current flow from V_I to V_{OUT}. The high-side driver is turned off when the current from V_I to V_{OUT} is zero or negative preventing current flow from V_{OUT} to V_I. When V_{OUT} falls below the V_{OVP_max-L} or V_{OVP-L} threshold the device continues normal operation.

The programmable $latch_{ICL\&OVP\_max}$ bit sets the device behavior when V_{OUT} rises above the V_{OVP_max-H} threshold. When $latch_{ICL\&OVP\_max}$ = 0 the device behaves like triggering V_{OVP-H}, for $latch_{ICL\&OVP\_max}$ = 1 the drivers are turned off and the device enters FAULT state. For $latch_{ICL\&OVP\_max}$ = 1a power cycle or toggling the UVLO/EN-pin is needed to re-start the device once OVP_{max} is triggered.

6.3.10.2 Thermal Shutdown (TSD)

An internal thermal shutdown (TSD) protects the device by disabling the low side driver and enabling the high side driver with 100% duty cycle if the junction temperature (T_J) exceeds the $T_{TSD-RISING}$ threshold. During thermal shutdown the device initiates boot refresh pulses with a frequency >20kHz to keep the boot capacitor charged. After the junction temperature (T_J) is reduced by the $T_{TSD-HYS}$ hysteresis, the device continues operation according to the Functional State Diagram.

6.3.11 Power-Good Indicator (PGOOD-pin)

The device provides a power-good indicator (PGOOD) to simplify sequencing and supervision. PGOOD is an open-drain output and a pullup resistor can be externally connected. The PGOOD switch opens when the VOUT pin voltage is higher than the V_{UVP-H} undervoltage threshold. PGOOD is pulled low under the following conditions:

- The VOUT-pin voltage is below the V_{OUT} falling undervoltage threshold V_{UVP-L}.
- The VOUT-pin voltage is above the 110% V_{OVP_H} or the programmed V_{OVP_max-H} rising threshold and the $PGOOD_{OVP\_enable}$ function is enabled (see CFG2-pin Settings). PGOOD is not pulled low when the $PGOOD_{OVP\_enable}$ function is disabled.
- The device is in SHUTDOWN state and V_{BIAS} is greater than approximately 1.7V (see Functional State Diagram).
- The EN/UVLO-pin voltage is falling below the undervoltage lockout threshold voltage $V_{UVLO-FALLING}$.
- The VCC regulator voltage VCC falls below the undervoltage lockout threshold $V_{VCC-UVLO-FALLING}$.
- Thermal Shutdown is triggered (see Functional State Diagram).
- The integrated BOOT CAP voltage is below the V_{HB} falling $V_{HB-UVLO}$ threshold and boot refresh enters the 512 cycles hiccup mode off time (see GAN Drivers, Integrated Boot Capacitor and Diode, and Hiccup Mode Fault Protection). PGOOD is only pulled low during the Hiccup off-time.
- The switch peak current limit is exceeded by 20% and the $latch_{ICL\&OVP\_max}$ function is enabled (see CFG1-pin Settings).
- An OTP memory fault occurred (CRC fault).

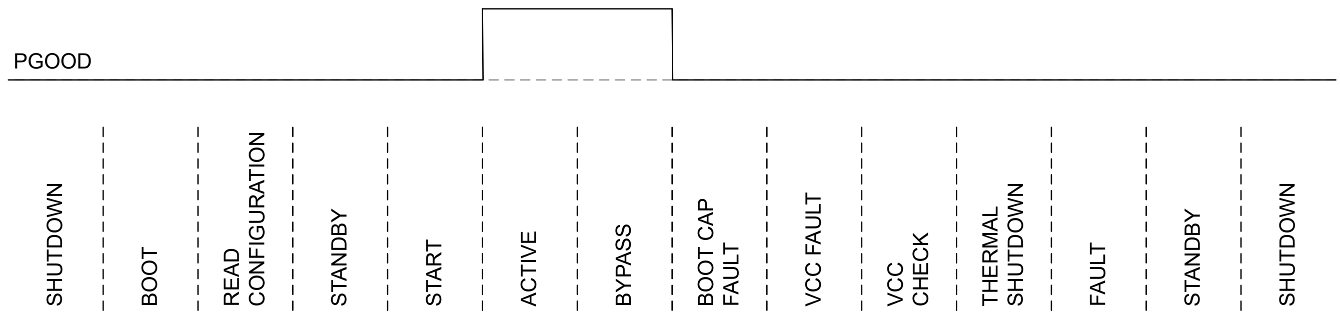


Figure 6-18. PGOOD Status for All Device States

6.3.12 Slope Compensation (CSA, CSB)

The current sense amplifier has a gain of 10 (ACS) and an internal slope compensation ramp is added to prevent subharmonic oscillation at high duty cycles. The slope of the compensation ramp must be greater than at least half of the sensed inductor current falling slope, which is fulfilled when Margin in Equation 14 is >1.

$$\frac{V_{OUT} - V_{I}}{2 \times L} \times R_{SNS} \times \mathrm{Margin} < V_{SLOPE} \times f_{SW} \tag{14}$$

6.3.13 Current Sense Setting and Switch Peak Current Limit (CSA, CSB)

The peak current limit is set by the sense resistor R_{SNS}. The positive peak current limit is active when CSA − CSB reaches the threshold V_{CLTH} (typical 60mV or 29mV). The negative peak current limit is active when V_{NCLTH} (typical −28mV) is reached. R_1 and R_2 in Figure 6-19 are 0Ω, R_3 is open.

$$R_{SNS} = \frac{I_{peak\_lim}}{V_{CLTH}} \tag{15}$$

Adjust the peak current limit by adding the resistors R_1, R_2 and R_3. Resistors R_1 and R_2 need to have the same value. Select the resistors <1Ω because the CS amplifier is supplied by the CSA pin. Select R_3 between 1Ω and 20Ω.

$$I_{peak\_lim} = \left(\frac{R_1 + R_2}{R_3} + 1\right) \times \frac{V_{CLTH}}{R_{SNS}} \tag{16}$$

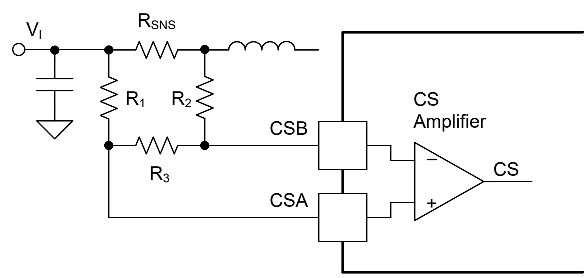


Figure 6-19. Peak Limit adjustment through additional resistors

The negative peak current limit of typically −28mV is an additional safety protection and usually not reached as the negative current is already limited by the COMP-pin voltage. V_{COMP} is clamped at typically 160mV, which limits the switch current at around −20mV sense voltage.

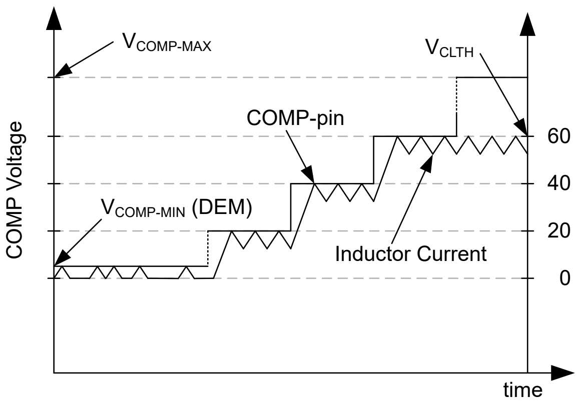


Figure 6-20. COMP-pin and Sense Resistor Voltage limiting the switch current (DEM)

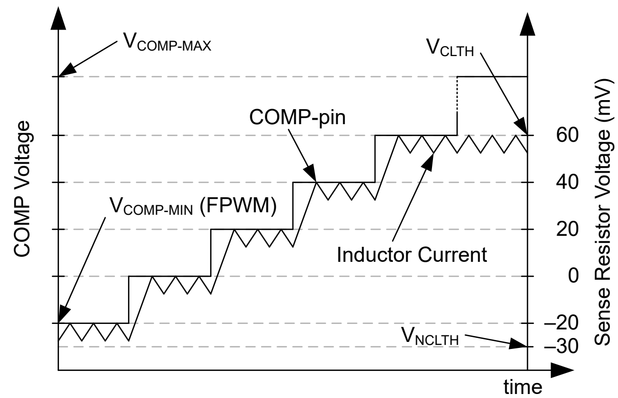


Figure 6-21. COMP-pin and Sense Resistor Voltage limiting the switch current (FPWM)

6.3.14 Input Current Limit and Monitoring (ILIM, IMON, DLY)

Monitor the average V_I input current at the IMON-pin. The average sensed current at the CSA and CSB pins generates a source current at the IMON-pin, which is converted to a voltage by the resistor R_{IMON}. The resulting voltage V_{IMON} is calculated according to Equation 18, the required resistor R_{IMON} according to Equation 17. V_{IMON} regulates up to 3V and is self-protecting not reaching the absolute maximum value.

$$R_{IMON} = \frac{V_{IMON}}{R_{CS} \times I_{IN} \times G_{IMON} + I_{OFFSET}} \tag{17}$$

$$V_{IMON} = \left(R_{CS} \times I_{IN} \times G_{IMON} + I_{OFFSET}\right) \times R_{IMON} \tag{18}$$

R_{CS} is the sense resistor, I_{IN} is the input current, G_{IMON} the transconductance gain and I_{OFFSET} the offset current given in the electrical characteristics table.

Limit the average input current by choosing an appropriate resistor connected to the ILIM-pin. When the input current limit is active, V_{OUT} is regulated down until the set average input current limit is reached. In case V_{OUT} is regulated below the V_I voltage the current cannot be limited anymore. The DLY-pin capacitor C_{DLY} adds an additional delay time t_{DLY} to activate and deactivate the average input current limit (see Average Current Limit). When the ILIM-pin voltage reaches the threshold V_{ILIM_th} (typical 1.1V) the source current I_{DLY} is activated charging up the DLY-pin capacitor C_{DLY}. The DLY-pin voltage V_{DLY} rises until $V_{DLY\_peak\_rise}$ is reached, which activates the average input current limit. The ILIM-pin voltage is regulated to V_{ILIM} (typically 1V) and the input current is regulated down to the average input current limit set by R_{ILIM} resulting in a V_{OUT} drop. To exit the average current limit regulation the output load has to decrease, which causes V_{OUT} to rise and V_{ILIM} to fall below V_{ILIM_reset} (typical 0.89V). V_{ILIM_reset} activates the sink current I_{DLY}, which discharges the DLY-pin capacitor C_{DLY}. When V_{DLY} reaches $V_{DLY\_peak\_fall}$ the average input current limit is deactivated and the DLY-pin is discharged to V_{DLY_valley}. The required resistor R_{ILIM} is calculated according to Equation 19, the capacitor C_{DLY} according to Equation 21.

$$R_{ILIM} = \frac{1V}{R_{CS} \times I_{IN\_LIM} \times G_{IMON} + I_{OFFSET}} \tag{19}$$

$$t_{DLY} = \frac{2.6 \times C_{DLY}}{5 \times 10^{-6}} \tag{20}$$

$$C_{DLY} = t_{DLY} \times \frac{5 \times 10^{-6}}{2.6} \tag{21}$$

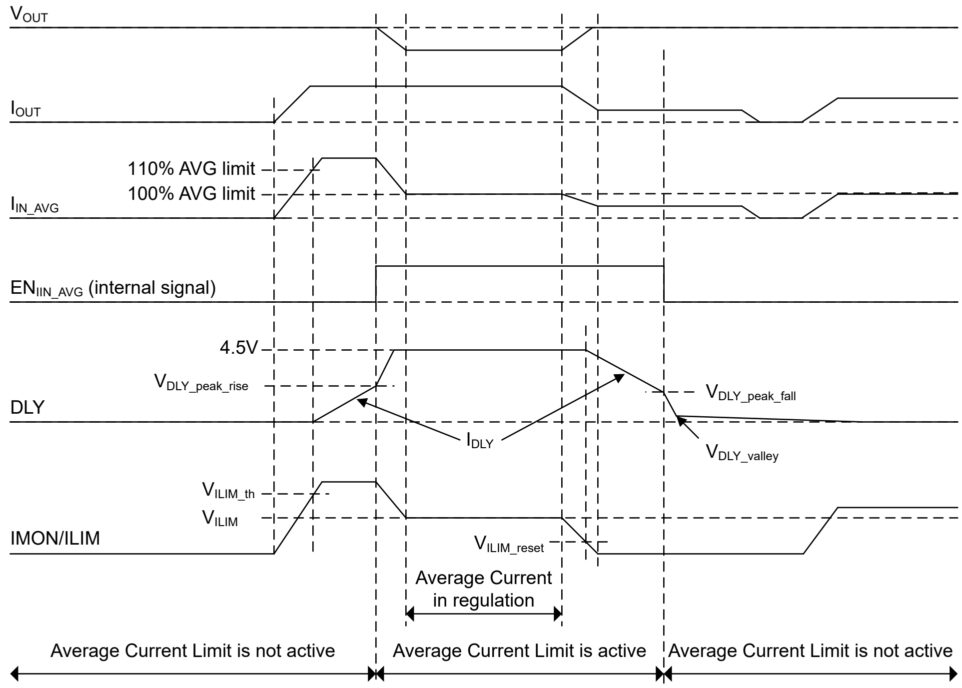


Figure 6-22. Average Current Limit

While a constant delay is added by the DLY-pin capacitor a V_{OUT} load dependent delay can be added by adding a RC tank to the ILIM/IMON-pin in parallel to the R_{ILIM} resistor. The RC tank resistor R_{C_IMON} is calculated according to Equation 22 and the capacitor C_{IMON} according to Equation 23.

$$R_{C\_IMON} = \frac{1}{20\pi \times C_{IMON}} \tag{22}$$

$$C_{IMON} = \frac{t_{delay}}{R_{IMON} \times \ln\left(\frac{R_{IMON} \times I_{MON} - V_{IMON\_0A}}{R_{IMON} \times I_{MON} - V_{ILIM}}\right)} \tag{23}$$

6.3.15 Maximum Duty Cycle and Minimum Controllable On-time Limits

To cover the non-ideal factors caused by resistive elements, a maximum duty cycle limit D_{MAX} and a minimum forced off-time is implemented. In CCM operation the minimum supported input voltage V_{I_MIN} for a programmed output voltage V_{OUT} is defined by the maximum duty cycle D_{MAX} (see Equation 24). In DEM operation the minimum input voltage V_{I_MIN} is not limited by D_{MAX}.

$$V_{I\_MIN} \cong V_{OUT} \times (1 - D_{MAX}) + I_{I\_MAX} \times \left(R_{DCR} + R_{SNS} + R_{DS(ON)}\right) \tag{24}$$

where

- I_{I_MAX} is the maximum input current at minimum input voltage V_{I_MIN}
- R_{DCR} is the DC resistance of the inductor
- R_{SNS} is the resistance of the sense resistor
- $R_{DS(ON)}$ is the on resistance of the device

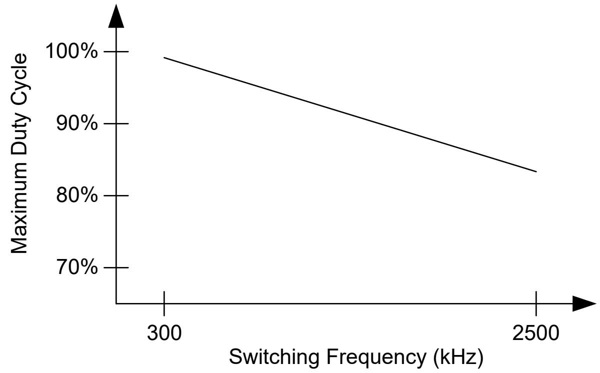


Figure 6-23. Switching Frequency vs Maximum Duty Cycle

At very light load condition or when V_I is close to V_{OUT} the device skips the low-side driver pulses if the required on-time is less than $t_{ON\text{-}MIN}$ to avoid V_{OUT} runaway. This pulse skipping appears as a random behavior. If V_I is further increased to the voltage higher than V_{OUT}, the required on-time becomes zero and eventually the device enters bypass operation which turns on the high-side driver 100%.

6.3.16 GAN Drivers, Integrated Boot Capacitor and Diode, and Hiccup Mode Fault Protection

The device integrates GAN drivers driving the integrated GAN FETs. The low side driver is powered by VCC and the high side driver is powered by the integrated boot capacitor. When the SW-pin voltage is approximately 0V by turning on the low-side FET, the integrated boot capacitor C_{boot} is charged from VCC through the internal boot diode. During shutdown, the gate drivers outputs are high impedance.

In case the integrated boot capacitor voltage is too low to drive the GAN FET, the hiccup mode fault protection is triggered by $V_{BOOT\text{-}UVLO}$. If the integrated boot capacitors voltage is less than the UVLO threshold ($V_{BOOT\text{-}UVLO}$), the low side driver turns on by force for 160ns to replenish the boot capacitor. The device allows up to two consecutive replenish switching cycles. After the maximum two consecutive boot replenish switching cycles, the device skips switching for 13 cycles. If the device fails to replenish the boot capacitor after four sets of the two consecutive replenish switching cycles, the device stops switching and enters 512 cycles of hiccup mode off-time. During the hiccup mode off-time PGOOD = low and the SS-pin is grounded.

6.3.17 Signal Deglitch Overview

The following image shows the signal deglitching. For all signals, the rising and falling edge is deglitched with the same deglitch time.

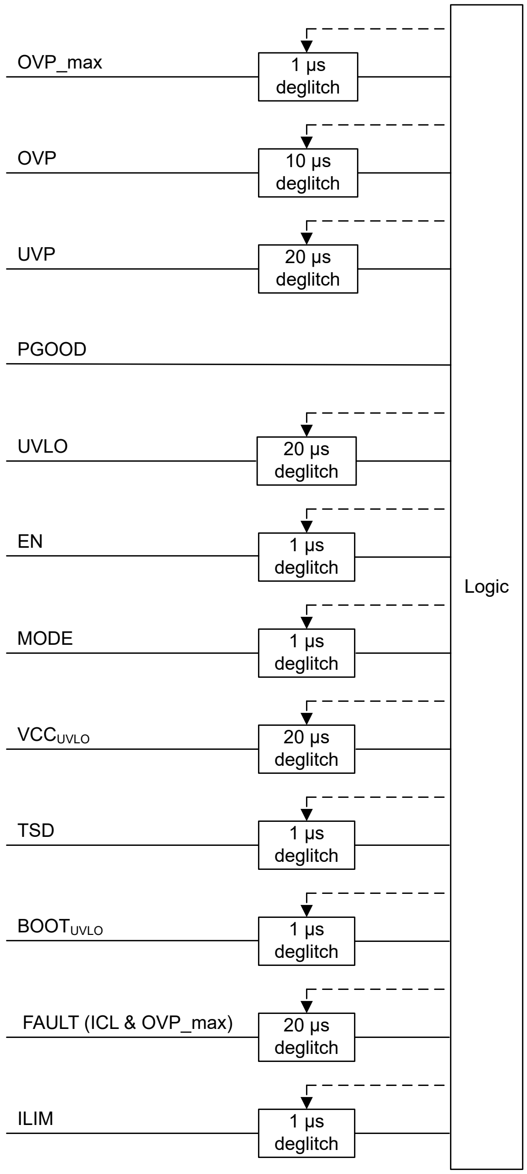


Figure 6-24. Signal Deglitching

6.4 Device Functional Modes

The different operation modes are shown in the Functional State Diagram.

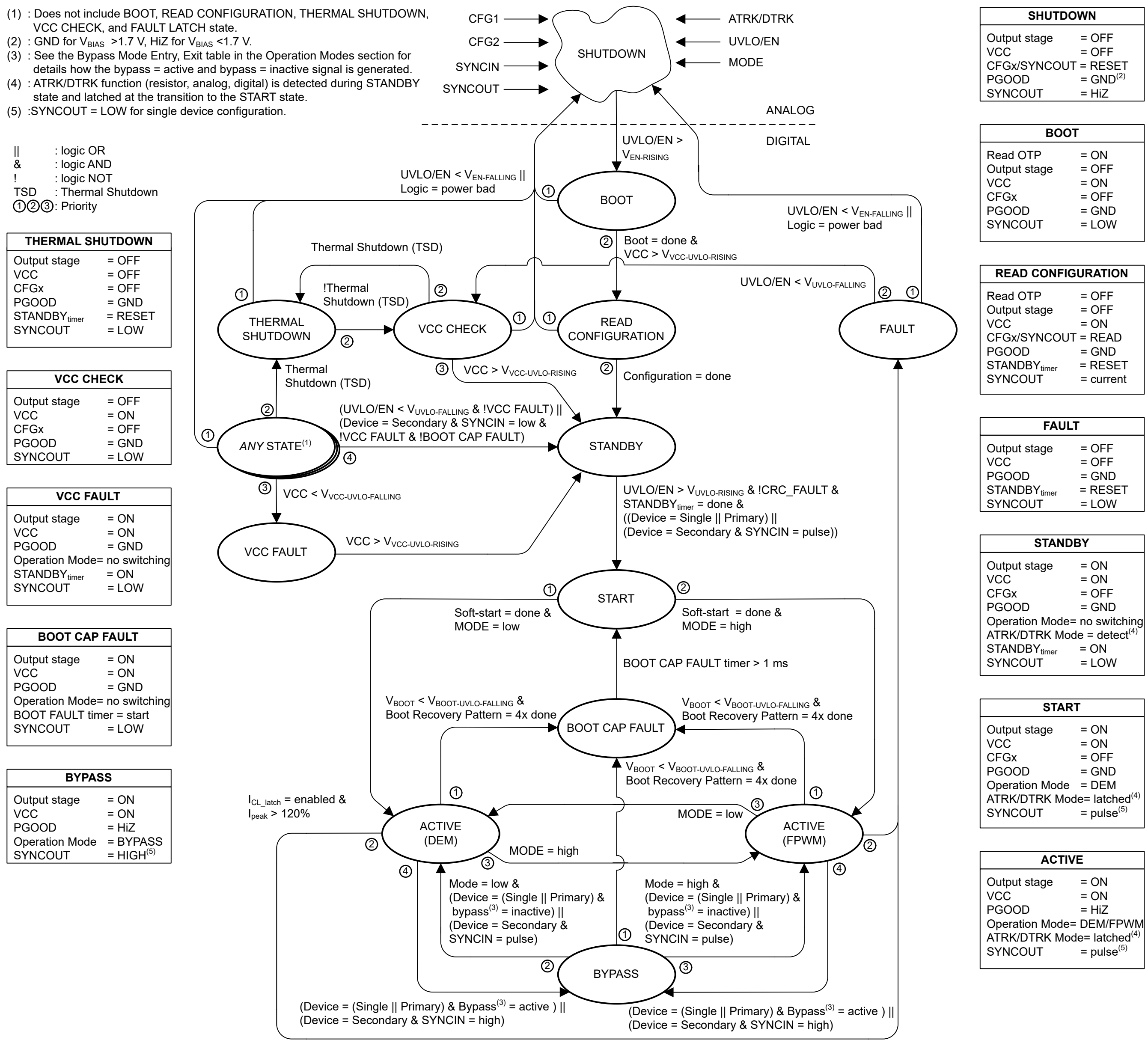


Figure 6-25. Functional State Diagram

6.4.1 Shutdown State

The device shuts down for UVLO/EN pin = low consuming 2μA from the BIAS pin and 5μA from the pins connected to V_I. In shutdown, COMP, SS, and PGOOD are grounded. The VCC regulator is disabled.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The device integrates several optional features to meet system design requirements, including input UVLO, programmable soft-start time, clock synchronization, spread spectrum, Average input current regulation, inductor current monitoring, 5V compatible BIAS pin for enhanced thermal capability, cold crank support, synchronization and dynamic output voltage tracking.

Refer to LMG5126 evaluation module for typical application and curves.

Use the LMG5126 Quick start calculator to expedite the process of designing a regulator for a given application.

Alternately, use the WEBENCH® circuit design and selection simulation services to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design.

This section presents a simplified discussion of the design process.

7.1.1 Feedback Compensation

The open-loop response of a boost regulator is defined as the product of modulator transfer function and feedback transfer function. When plotted on a dB scale, the open loop gain is shown as the sum of modulator gain and feedback gain. The modulator transfer function of a current mode boost regulator including a power stage transfer function with an embedded current loop can be simplified as one pole, one zero, and one right-half-plane zero (RHPZ) system.

The modulator transfer function is defined as follows:

$$\frac{\hat{v}_{out}}{\hat{v}_{comp}} = A_M \times \frac{\left(1 + \frac{s}{\omega_{Z\_ESR}}\right)\left(1 - \frac{s}{\omega_{RHPZ}}\right)}{1 + \frac{s}{\omega_{P\_LF}}} \times G_{ACB}(s) \quad (25)$$

where

- Modulator DC gain:

$$A_M = \frac{R_{out} \times D'}{2 \times A_{cs} \times R_{cs\_eq}} \quad (26)$$

- Load pole:

$$\omega_{P\_LF} = \frac{2}{R_{out} \times C_{out}} \quad (27)$$

- ESR zero:

$$\omega_{Z\_ESR} = \frac{1}{R_{ESR} \times C_{out}} \quad (28)$$

- RHPZ:

$$\omega_{RHPZ} = \frac{R_{out} \times D'^2}{L_{m\_eq}} \quad (29)$$

- The equivalent load resistance:

$$R_{out} = \frac{V_{out}^2}{P_{out\_total}} \tag{30}$$

- The equivalent inductance:

$$L_{m\_eq} = \frac{L_m}{N_p} \tag{31}$$

- The equivalent current sense resistor:

$$R_{cs\_eq} = \frac{R_{cs}}{N_p} \tag{32}$$

- N_p is the number of the phases.

If the equivalent series resistance (ESR) of C_{out} (R_{ESR}) is small enough and the RHPZ frequency is far away from the target crossover frequency, the modulator transfer function can be further simplified to a one pole system and the voltage loop can be closed with only two loop compensation components, R_{COMP} and C_{COMP}, leaving a single pole response at the crossover frequency. A single pole response at the crossover frequency yields a very stable loop with 90 degrees of phase margin.

As shown in Figure 7-1, a g_m amplifier is utilized as the output voltage error amplifier. The feedback transfer function includes the feedback resistor divider gain and loop compensation of the error amplifier. R_{COMP}, C_{COMP}, and C_{HF} configure the error amplifier gain and phase characteristics, create a pole at origin, a low frequency zero and a high frequency pole.

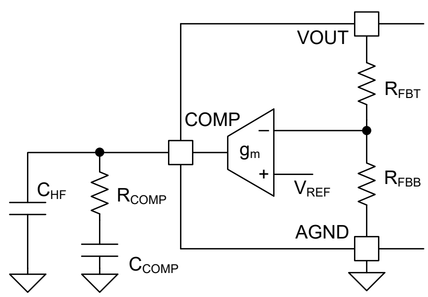


Figure 7-1. Type II g_m Amplifier Compensation

Feedback transfer function is defined as follows:

$$-\frac{\hat{v}_{comp}}{\hat{v}_{out}} = \frac{A_{VM} \times \omega_{Z\_EA}}{s} \times \frac{1 + \frac{s}{\omega_{Z\_EA}}}{1 + \frac{s}{\omega_{P\_EA}}} \tag{33}$$

where

- The middle-band voltage gain:

$$A_{VM} = K_{FB} \times g_m \times R_{COMP} \tag{34}$$

- The feedback resistor divider gain:

$$K_{FB} = \frac{R_{FBB}}{R_{FBT} + R_{FBB}} \tag{35}$$

For the internal feedback resistor divider:

$$K_{FB} = \frac{1}{30} \tag{36}$$

- Low frequency zero:

$$\omega_{Z\_EA} = \frac{1}{R_{COMP} \times C_{COMP}} \tag{37}$$

- High frequency pole:

$$\omega_{P\_EA} \cong \frac{1}{R_{COMP} \times C_{HF}} \tag{38}$$

The pole at the origin minimizes the output steady state error. Place the low frequency zero to cancel the load pole of the modulator. The high frequency pole can be used to cancel the zero created by the output capacitor ESR or to decrease noise susceptibility of the error amplifier. By placing the low frequency zero an order of magnitude less than the crossover frequency, the maximum amount of phase boost can be achieved at the crossover frequency. Place the high frequency pole beyond the crossover frequency since the addition of C_{HF} adds a pole in the feedback transfer function.

The crossover frequency (open loop bandwidth) is typically limited to one fifth of the RHPZ frequency.

For higher crossover frequency, R_{COMP} can be increased, while proportionally decreasing C_{COMP}. Conversely, decreasing R_{COMP} while proportionally increasing C_{COMP}, results in lower bandwidth while keeping the same zero frequency in the feedback transfer function.

7.2 Typical Application

7.2.1 Application

A typical application example is a single-phase boost converter as shown in Figure 7-2. This converter is designed for Class-H audio amplifier. The output voltage is adjustable up to 60V.

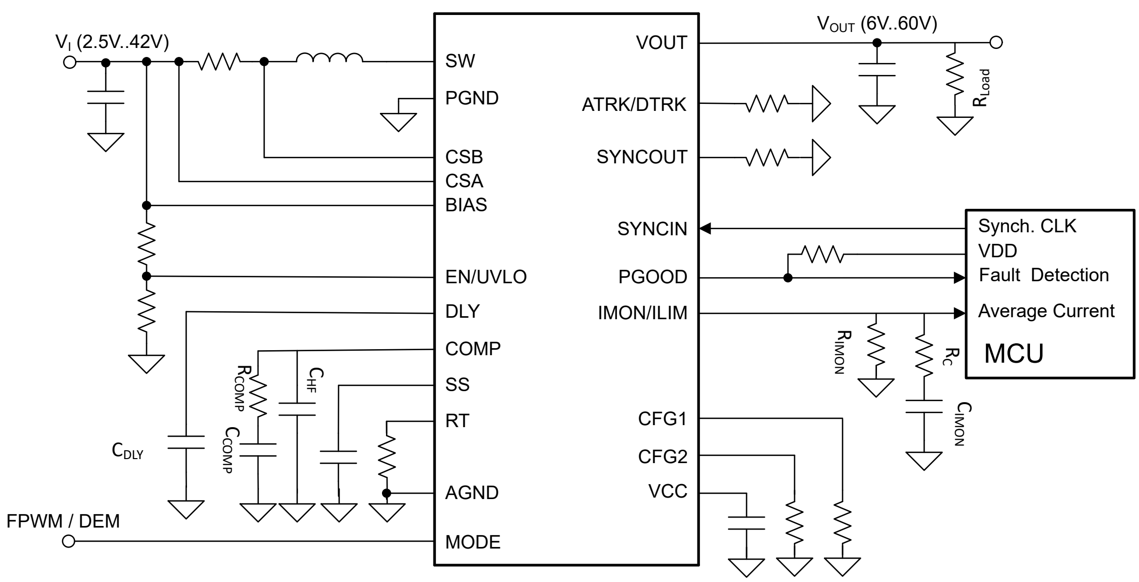


Figure 7-2. Schematic of single-phase Boost Converter

7.2.2 Design Requirements

Table 7-1. Design Parameters

PARAMETER	VALUE
Minimum input voltage V_{in_min}	9V
Typical input voltage V_{in_typ}	14.4
Maximum input voltage V_{in_max}	18V
Nominal Output voltage V_{out_nom}	24V

Table 7-1. Design Parameters (continued)

PARAMETER	VALUE
Maximum output Voltage V_{out_max}	45V
Maximum output power P_{out_total}	400W
Estimated efficiency, η	95%

7.2.3 Detailed Design Procedure

7.2.3.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMG5126 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer gives a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

7.2.3.2 Determine the Total Phase Number

Interleaved operation offers many advantages in high current applications such as higher efficiency, lower component stresses and reduced input and output ripple. For dual phase interleaved operation, the output power path is split reducing the input current in each phase by one-half. Ripple currents in the input and output capacitors are reduced significantly since each channel operates 180 degrees out of phase from the other. As shown in Input Current Ripple Reduced With Dual Phase Interleaving, the input current ripple is reduced significantly.

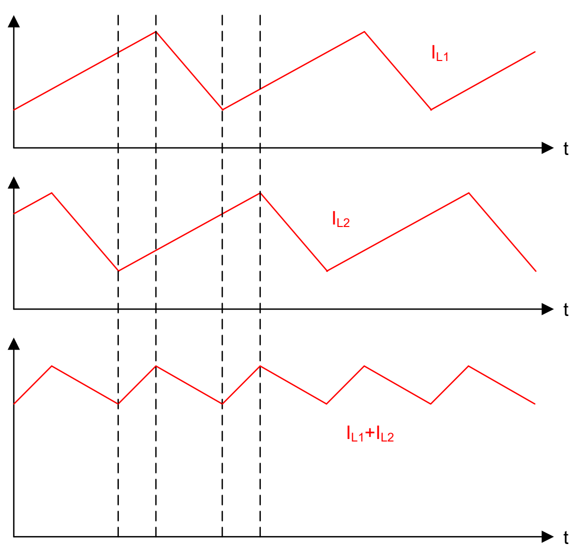


Figure 7-3. Input Current Ripple Reduced With Dual Phase Interleaving

Here, 1phase is selected for the design:

$$N_p = 1 \tag{39}$$

The total power P_{out_total} is shared among phases, the power of each phase is found as:

$$P_{out} = \frac{P_{out\_total}}{N_p} = 400W \tag{40}$$

7.2.3.3 Determining the Duty Cycle

In CCM, the duty cycle is defined as:

$$D = \frac{V_{out} - V_{in}}{V_{out}} \tag{41}$$

$$D' = 1 - D \tag{42}$$

In this application the maximum duty cycle is found using:

$$D_{max} = \frac{V_{out\_max} - V_{in\_min}}{V_{out\_max}} = 0.8 \tag{43}$$

7.2.3.4 Timing Resistor R_T

Generally, higher switching frequency (f_{sw}) leads to smaller size and higher losses. Operation around 400kHz is a reasonable compromise considering size, efficiency and EMI. The value of R_T for 400kHz switching frequency is calculated as follows:

$$R_T = \left(\frac{1}{f_{sw}} - 18ns\right) \times 31.5\frac{\Omega}{ns} = 78.2k\Omega \tag{44}$$

A standard value of 78.7kΩ is chosen for R_T.

7.2.3.5 Inductor Selection L_m

Three main parameters are considered when selecting the inductance value: inductor current ripple ratio (RR), falling slope of the inductor current and the RHPZ frequency of the control loop.

- The inductor current ripple ratio is selected to balance the winding loss and core loss of the inductor. As the ripple current increases the core loss increases and the copper loss decreases.
- Verify that the falling slope of the inductor current is small enough to prevent sub-harmonic oscillation. A larger inductance value results in a smaller falling slope of the inductor current.
- Place the RHPZ at a high frequency, allowing a higher crossover frequency of the control loop. As the inductance value decrease the RHPZ frequency increases.

According to peak current mode control theory, the slope of the slope compensation ramp must be greater than half of the sensed inductor current falling slope to prevent subharmonic oscillation at high duty cycle, that is:

$$V_{slope} \times f_{sw} > \frac{V_{out\_max} - V_{in\_min}}{2 \times L_m} \times R_{cs} \tag{45}$$

where

- V_{slope} is a 48mV peak (at 100% duty cycle) slope compensation ramp at the input of the current sense amplifier.

The lower limit of the inductance can be found as:

$$L_m > \frac{V_{out\_max} - V_{in\_min}}{2 \times V_{slope} \times f_{sw}} \times R_{cs} \tag{46}$$

Estimating R_{cs} = 2mΩ,:

$$L_m > 1.9\mu H \tag{47}$$

The RHPZ frequency can be found as:

$$\omega_{RHPZ} = \frac{R_{out} \times D'^2}{L_{m\_eq}} \tag{48}$$

Verify that the crossover frequency is lower than 1/5 of RHPZ frequency

$$f_c < \frac{1}{5} \times \frac{\omega_{RHPZ}}{2\pi} \tag{49}$$

Assume a crossover frequency of 1kHz is desired, the upper limit of the inductance can be found as:

$$L_m < 6.2\mu H \tag{50}$$

The inductor ripple current is typically set between 30% and 70% of the full load current, known as a good compromise between core loss and winding loss of the inductor.

Per phase input current can be calculated as:

$$I_{in\_vinmax} = \frac{P_{out}}{V_{in\_max}} = 23.4A \tag{51}$$

In continuous conduction mode (CCM) operation, the maximum ripple ratio occurs at a duty cycle of 33%. The input voltage that result in a maximum ripple ratio can be found as:

$$V_{in\_RRmax} = V_{out\_max} \times (1 - 0.33) = 30V \tag{52}$$

Thus, use the maximum input voltage V_{in_max} to calculate the maximum ripple ratio.

For this example, a ripple ratio of 0.3, 30% of the input current is chosen. Knowing the switching frequency and the typical output voltage, the inductor value can be calculated as follows:

$$L_m = \frac{V_{in\_max}}{I_{in} \times RR} \times \frac{1}{f_{sw}} \times \left(1 - \frac{V_{in\_max}}{V_{out\_max}}\right) = \frac{18V}{23.4A \times 0.3} \times \frac{1}{400kHz} \times 0.6 = 3.8\mu H \tag{53}$$

The closest standard value of 3.3μH is chosen for L_m.

The inductor ripple current at typical input voltage can be calculated as:

$$I_{pp} = \frac{V_{in\_typ}}{L_m} \times \frac{1}{f_{sw}} \times \left(1 - \frac{V_{in\_typ}}{V_{out}}\right) = 4.36A \tag{54}$$

If a ferrite core inductor is selected, make sure the inductor does not saturate at peak current limit. The inductance of a ferrite core inductor is almost constant until saturation. Ferrite core has low core loss with a big size.

For powder core inductor, the inductance decreases slowly with increased DC current. This leads to higher ripple current at high inductor current. For this example, the inductance drops to 70% at peak current limit compared to 0A. The current ripple at peak current limit can be found as:

$$I_{pp\_bias} = \frac{V_{in\_typ}}{0.7 \times L_m} \times \frac{1}{f_{sw}} \times \left(1 - \frac{V_{in\_typ}}{V_{out}}\right) = 6.8A \tag{55}$$

7.2.3.6 Current Sense Resisitor R_{cs}

The maximum per phase average input current at typical input voltage and maximum output voltage is calculated as:

$$I_{in\_vintyp} = \frac{P_{out}}{\eta \times V_{in\_typ}} = 29.2A \tag{56}$$

The peak current is calculated as:

$$I_{pk\_vintyp} = I_{in\_vintyp} + \frac{I_{pp\_bias}}{2} = 29.2A + \frac{6.8A}{2} = 32.6A \tag{57}$$

The current sense resistor is found as:

$$R_{cs} = \frac{V_{CLTH}}{I_{pk\_vintyp}} = \frac{60mV}{32.6A} = 1.84m\Omega \tag{58}$$

A standard value of 2mΩ is chosen for R_{cs}.

7.2.3.7 Current Sense Filter R_{CSFA}, R_{CSFB}, C_{CS}

RC filters are suggested for current sensing. 100pF of C_{CS} and 1Ω of R_{CSFA}, R_{CSFB} are normal recommendations. Place C_{CS} close to the device.

Route CSA and CSB traces together with Kelvin connections to the current sense resistors.

Increase C_{CS} and R_{CSFB} to increase the RC time constant. Increasing R_{CSFA} brings significant current sensing error.

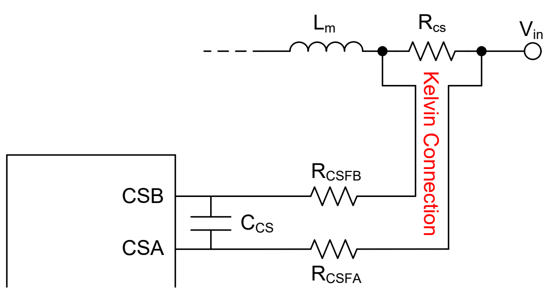


Figure 7-4. Current Sense Filter

7.2.3.8 Snubber Components

A resistor-capacitor snubber network from the switch node to ground reduces ringing and spikes at the switching node. Excessive ringing and spikes cause erratic operation and couple noise to the output voltage. Selecting the values for the snubber is best accomplished through empirical methods. First, make sure the lead lengths for the snubber connections are very short. Start with a resistor value between 5 and 50Ω. Increasing the value of the snubber capacitor results in more damping, but this action also results higher snubber losses. Select a minimum value for the snubber capacitor that provides adequate damping of the spikes on the switch waveform at heavy load. A snubber cannot be necessary with an optimized layout.

7.2.3.9 V_{out} Programming

For fixed output voltage, V_{OUT} can be programmed by connecting a resistor to ATRK/DTRK and turn on precise internal 20µA current source.

$$R_{ATRK} = \frac{V_{out\_max}}{6V} \times 10k\Omega = 75k\Omega \tag{59}$$

For class-H audio application, V_{out} can be adjusted to optimize the efficiency. Analog tracking or digital tracking can be applied with ATRK/DTRK.

For analog tracking, apply a voltage to ATRK/DTRK to program V_{out}. The voltage can be found as:

$$V_{ATRK\_max} = \frac{V_{out\_max}}{30} = 1.5V \tag{60}$$

$$V_{ATRK\_nom} = \frac{V_{out\_nom}}{30} = 0.8V \tag{61}$$

The output voltage can also be programmed by digital PWM signal (DTRK). The duty cycle D_{TRK} can be found as:

$$D_{TRK} = \frac{V_{out\_max}}{0.75V} \times 100\% = 60\% \tag{62}$$

$$D_{TRK\_min} = \frac{V_{out\_min}}{0.75V} \times 100\% = 10.7\% \tag{63}$$

Make sure the DTRK frequency is between 100kHz and 2200kHz. The DTRK PWM signal must be applied when the IC is enabled.

A two stage RC filter with offset can be utilized to convert a digital PWM signal to analog voltage as shown in Figure 7-5.

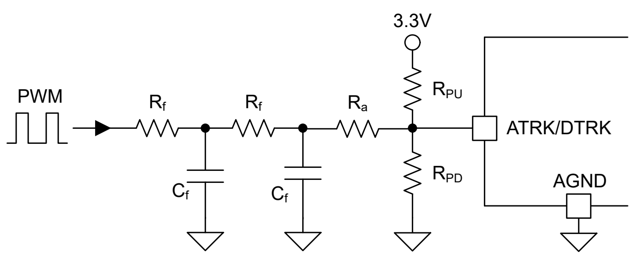


Figure 7-5. Two Stage RC Filter to ATRK/DTRK

The two stage RC filter is used to filter the PWM signal into a smooth analog voltage. The two stage RC filter is selected considering voltage ripple and settling time on ATRK/DTRK.

100% PWM duty cycle sets the output voltage to V_{out_max} and 0% PWM duty cycle sets the output voltage to V_{out_min}. R_t and R_b are used to adjust ATRK/DTRK offset voltage.

The V_{trk_max} and V_{trk_min} can be found as,

$$V_{ATRK\_max} = V_{dd}\frac{R_b}{(2R_f + R_a)\|R_t + R_b} \tag{64}$$

$$V_{ATRK\_min} = V_{dd}\frac{(2R_f + R_a)\|R_b}{(2R_f + R_a)\|R_b + R_t} \tag{65}$$

Where V_{dd} is the amplitude of the PWM signal; d is the PWM duty cycle.

The AC transfer function from input to V_{ATRK} can be found as,

$$G_{trk}(s) = \frac{\frac{R_L}{2R_f + R_L}}{1 + 2\zeta\frac{s}{\omega_n} + \left(\frac{s}{\omega_n}\right)^2} \quad (66)$$

Where

$$R_L = R_a + R_b \| R_t \quad (67)$$

$$\omega_n = \frac{1}{R_f \times C_f\sqrt{\frac{R_L}{2R_f + R_L}}} \quad (68)$$

$$\zeta = \frac{1}{2}\left(\frac{R_f}{R_L} + 3\right)\sqrt{\frac{R_L}{2R_f + R_L}} \quad (69)$$

The roots of the denominator can be found as,

$$s_1 = -\zeta\omega_n + \omega_n\sqrt{\zeta^2 - 1} \quad (70)$$

$$s_2 = -\zeta\omega_n - \omega_n\sqrt{\zeta^2 - 1} \quad (71)$$

As ζ>1, this is an over-damped second order system. s_1 is the dominate pole. 2% settling time t_s can be estimated as,

$$t_s = \frac{1}{s_1} \times \ln\left(-\frac{0.02 \times 2s_1\sqrt{\zeta^2 - 1}}{\omega_n}\right) \quad (72)$$

In this application, 400kHz PWM frequency is used. R_f=4.99kΩ, C_f=47nF, R_a=1.5kΩ, R_t=51kΩ, R_b=7.87kΩ are selected. The 2% settling time is around 1.3ms.

7.2.3.10 Input Current Limit (ILIM/IMON)

The transient power is high in audio applications. For this application 400W is selected as peak output power. But the average power is typically much lower than the peak power. 240W is selected as average power. With proper ILIM/IMON setting, the average input current is limited to less than 240W while allowing 400W peak for 300ms. When the average current loop is triggered, V_{OUT} drops till the input and output power is balanced.

The per phase input current at average output power and typical input voltage is found as,

$$I_{avg} = \frac{P_{avg\_total}}{1 \times \eta \times V_{in\_typ}} = 17.5A \quad (73)$$

22A is selected as the average input current limit.

$$I_{lim} = 22A \quad (74)$$

The current out of ILIM/IMON is found as,

$$I_{MON\_lim} = (R_{cs} \times I_{lim} \times G_{IMON} + I_{OFFSET}) = (2m\Omega \times 22A \times 0.333mA/V + 4\mu A) = 18.6\mu A \quad (75)$$

R_{ILIM} is calculated as:

$$R_{IMON} = \frac{V_{ILIM}}{I_{MON}} = \frac{1V}{11\mu A} = 53.7k\Omega \quad (76)$$

A standard value of 53.6kΩ is chosen for R_{IMON}.

As shown in Figure 7-6, use C_{IMON} and R_c to create a proper delay before the average current loop is triggered.

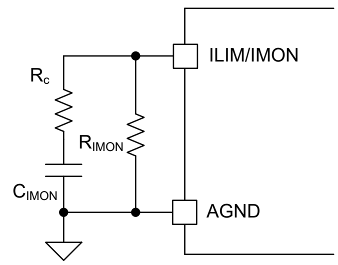


Figure 7-6. ILIM/IMON Pin Configuration

In this application 300ms delay for 400W is required.

At zero load current out of ILIM/IMON is found as,

$$I_{MON\_0A} = I_{OFFSET} = 4\mu A \tag{77}$$

The ILIM/IMON voltage at zero load is calculated as,

$$V_{IMON\_0A} = R_{IMON} \times I_{MON\_0A} = 0.21V \tag{78}$$

At 400W, 1.6 times the rated power, the current out of ILIM/IMON is found as,

$$I_{MON\_tr} = (R_{cs} \times 1.6 \times I_{lim} \times G_{IMON} + I_{OFFSET}) = (2m\Omega \times 35.2A \times 0.333mA/V + 4\mu A) = 27.4\mu A \tag{79}$$

C_{IMON} is determined by,

$$C_{IMON} = \frac{t_{delay}}{R_{IMON} \times \ln\left(\frac{R_{IMON} \times I_{MON\_tr} - V_{IMON\_0A}}{R_{IMON} \times I_{MON\_tr} - V_{ILIM\_th}}\right)} = 4.5\mu F \tag{80}$$

A standard value of 4.7µF is chosen for C_{IMON}.

R_c is determined by,

$$R_c = \frac{1}{20\pi \times C_{IMON}} = 3.38k \tag{81}$$

A standard value of 3.4kΩ is chosen for R_c.

7.2.3.11 Minimum Load Resistor

To avoid the output voltage from running away during pulse skipping in DEM, a minimum load resistor has to be placed at the output.

Refer to the Operation Modes section.

Calculate the minimum load resistor as:

$$R_{LOAD} = \frac{2 \times V_{OUT\_nom} \times \left(V_{OUT\_nom} - V_{I\_max}\right) \times L}{V_{I\_max}^2 \times F_{SW} \times 0.0484\mu s^2} = 67.3k\Omega \tag{82}$$

A standard value of 66.5kΩ is chosen for R_{Load}.

7.2.3.12 UVLO Divider

The desired start-up voltage and the hysteresis are set by the voltage divider R_{UVT}, R_{UVB}. For this design, the start-up voltage (V_{in_on}) is set to 8.5V which is 0.5V below V_{in_min}. UVLO hysteresis voltage is set to 1V. This action results UVLO shutdown voltage (V_{in_off}) of 7.5V. The values of R_{UVT}, R_{UVB} are calculated as follows:

$$R_{UVT} = \frac{V_{in\_on} - \frac{V_{UVLO\_RISING}}{V_{UVLO\_FALLING}} \times V_{in\_off}}{I_{UVLO\_HYS}} = \frac{8.5V - \frac{1.1V}{1.075V} \times 7.5V}{10\mu A} = 82.6k\Omega \quad (83)$$

A standard value of 82.5kΩ is chosen for R_{UVT}.

$$R_{UVB} = \frac{V_{UVLO\_FALLING} \times R_{UVT}}{V_{in\_off} - V_{UVLO\_FALLING}} = \frac{1.075V \times 82.5k\Omega}{7.5V - 1.075V} = 13.8k\Omega \quad (84)$$

A standard value of 13.8kΩ is chosen for R_{UVB}.

A 100nF UVLO capacitor (C_{UVLO}) is selected in case V_{in} drops below V_{in_off} momentarily during the start-up or during a severe load transient at the low input voltage.

7.2.3.13 Soft Start

The soft-start time at maximum output voltage is the longest. To obtain a 6ms soft-start time, the soft-start capacitor is found as,

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{ATRK\_max}}\left(\frac{V_{out\_max}}{V_{out\_max} - V_{in\_typ}}\right) = \frac{50\mu A \times 6ms}{1.5V}\left(\frac{45V}{45V - 14.4V}\right) = 0.29\mu F \quad (85)$$

A standard value of 0.33µF is chosen for C_{SS}.

7.2.3.14 Output Capacitor C_{out}

The output capacitors smooth the output voltage ripple and provide a source of charge during load transient conditions.

Ripple current rating of output capacitor must be carefully selected. In boost regulator, the output is supplied by discontinuous current and the ripple current requirement is usually high. In practice, the ripple current requirement can be dramatically reduced by placing high-quality ceramic capacitors earlier than the bulk aluminum capacitors close to the power switches.

The output voltage ripple is dominated by ESR of the output capacitors. Paralleling output capacitor is a good choice to minimize effective ESR and split the output ripple current into capacitors.

The single phase boost output RMS ripple current can be expressed as:

$$I_{1p\_rms} \cong I_{out} \times \sqrt{\frac{D}{D'}} \quad (86)$$

The output RMS current is reduced with interleaving as shown in Figure 7-7. Dual phase interleaved boost output RMS ripple current can be expressed as:

$$I_{out\_2p\_rms} \cong \begin{cases} \frac{I_{out}}{\sqrt{2}} \times \frac{\sqrt{D \times (1 - 2D)}}{D'}, & D < 0.5 \\ \frac{I_{out}}{\sqrt{2}} \times \sqrt{\frac{2D - 1}{D'}}, & D \geq 0.5 \end{cases} \quad (87)$$

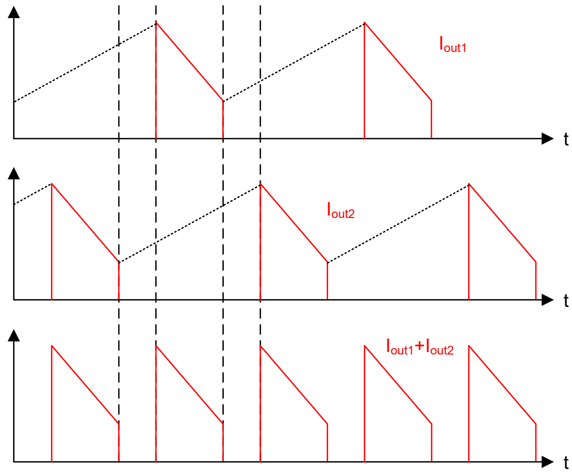


Figure 7-7. Normalized Output Capacitor RMS Ripple Current

Decoupling capacitors are critical for minimized voltage spike of the MOSFETs. This is also important from EMI view. Quite a few 0603/100nF ceramic capacitors are placed close to the MOSFETs following "vertical loop" concept. Refer to *Improve High-Current DC/DC Regulator EMI Performance for Free With Optimized Power Stage Layout* application brief for more details.

A few 10µF ceramic capacitors are also necessary to reduce the output voltage ripple and split the output ripple current.

Typically, aluminum capacitors are required for high capacitance. In this example, four 150µF aluminum capacitors are selected.

The output transient response is closely related to the bandwidth of the loop gain and the output capacitance. According to *How to Determine Bandwidth from the Transient-response Measurement* technical article, the overshoot or undershoot V_p can be estimated as:

$$V_p = \frac{\Delta I_{tran}}{2\pi \times f_c \times C_{out}} \tag{88}$$

where ΔI_{tran} is the transient load current step.

Please be aware that Equation 88 is valid only if the converter is always operating in CCM or FPWM during load step. If the converter enters DCM or pulsing skip mode at light load, the overshoot is worse.

Due to the inherent path from input to output, unlimited inrush current can flow when the input voltage rises quickly and charges the output capacitor. The slew rate of input voltage rising must be controlled by a hot-swap or by starting the input power supply softly for the inrush current not to damage the inductor, sense resistor or high-side FET.

7.2.3.15 Input Capacitor C_{in}

Input capacitors are always required to provide a stable input voltage. It is necessary that the input capacitors is able to handle the inductor ripple current.

The single phase boost input RMS ripple current is expressed as,

$$I_{in\_1p\_rms} = \frac{I_{pp}}{\sqrt{12}} \tag{89}$$

The input capacitor is also an important part of the input filter. Higher capacitance and ESR help damping the input filter better. Aluminum electrolytic capacitor is a good choice for input capacitor with high capacitance and ESR. Refer to *Input Filter Design for Switching Power Supplies* application note for more details.

7.2.3.16 VCC Capacitor C_{VCC}

The primary purpose of the VCC capacitor is to supply the peak transient currents of the gate driver as well as provide stability for the VCC regulator. Use good-quality, low-ESR, ceramic capacitor for C_{VCC}. Place C_{VCC} close to the pins of the device.

A value of 4.7µF was selected for this design example.

7.2.3.17 BIAS Capacitor

Use a high-quality, ceramic capacitor for C_{BIAS}. Place C_{BIAS} physically close to the device.

A value of 1µF is selected for this design example.

7.2.3.18 VOUT Capacitor

Use a high-quality, ceramic capacitor for C_{OUT}. Place C_{OUT} physically close to the device.

A value of 0.1µF is selected for this design example.

7.2.3.19 Loop Compensation

R_{COMP}, C_{COMP} and C_{HF} configure the error amplifier gain and phase characteristics to produce a stable voltage loop. For a quick start, follow the following four steps:

1. Select crossover frequency, f_C. Select the cross over frequency (f_C) at one fifth of the RHPZ frequency or one tenth of the switching frequency whichever is lower. Choose RHPZ with minimum input voltage and maximum output voltage.

$$\frac{f_{sw}}{10} = 40\text{kHz} \tag{90}$$

$$\frac{f_{RHPZ}}{5} = \frac{R_{out} \times D'^2}{5 \times 2\pi \times L_{m\_eq}} = 1.9\text{kHz} \tag{91}$$

   Crossover frequency f_c=1.9kHz is selected.
2. Determine required R_{COMP}

   Knowing f_c, R_{COMP} is calculated as follows:

$$R_{COMP} = \frac{2\pi \times f_c \times C_{out} \times A_{cs} \times R_{cs\_eq}}{D' \times K_{FB} \times g_m \times G_{ACB}(2\pi \times f_c)} = \frac{2\pi \times 1.9\text{kHz} \times 700\mu\text{F} \times 10 \times 2\text{m}\Omega}{0.2 \times \frac{1}{30} \times 1\frac{\text{mA}}{\text{V}} \times \frac{1}{2}} = 50.1\text{k}\Omega \tag{92}$$

   A standard value of 50kΩ is selected for R_{COMP}
3. Determine C_{COMP}

   Place ω_{Z_EA} at the load pole frequency ω_{P_LF} to cancel load pole. Knowing R_{COMP}, C_{COMP} is calculated as follows:

$$C_{COMP} = \frac{1}{R_{COMP} \times \omega_{P\_LF}} = \frac{1}{50\text{k}\Omega \times \frac{2}{5\Omega 700\mu\text{F}}} = 35\text{nF} \tag{93}$$

   A standard value of 35nF is selected for C_{COMP}
4. Determine C_{HF}.

   Place ω_{HF} at ω_{RHPZ} or ω_{Z_ESR} zero whichever is lower. Knowing R_{COMP}, RHPZ and ESR zero, C_{HF} is calculated as follows:

$$C_{HF} = \frac{1}{R_{COMP} \times \omega_{HF}} = \frac{1}{50\text{k}\Omega \times 9.5\text{kHz}} = 2\text{nF} \tag{94}$$

   A standard value of 2.2nF is selected for C_{HF}.

7.2.4 Application Curves

7.2.4.1 Efficiency

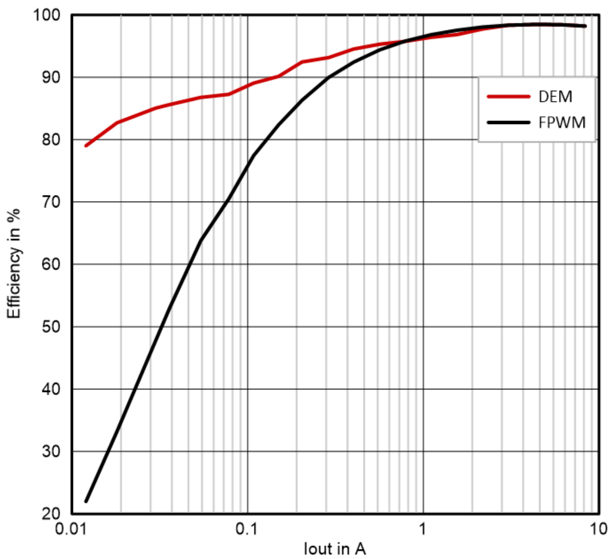


Figure 7-8. Efficiency vs Output Current, V_{in} = 14.4V, V_{out} = 24V

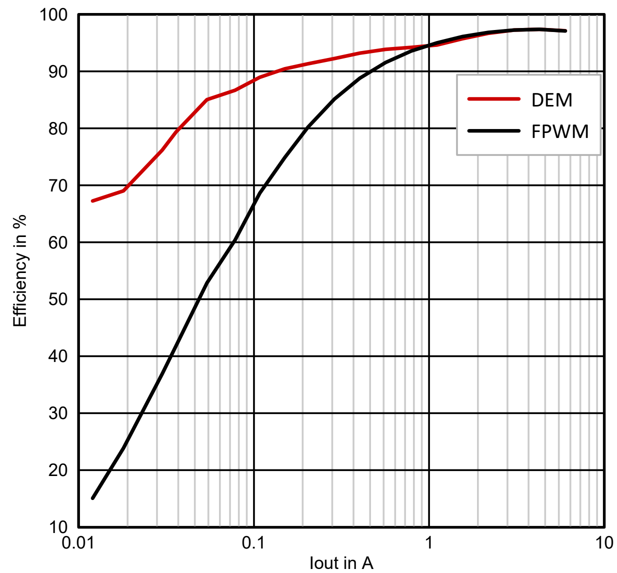


Figure 7-9. Efficiency vs Output Current, V_{in} = 14.4V, V_{out} = 45V

7.2.4.2 Steady State Waveforms

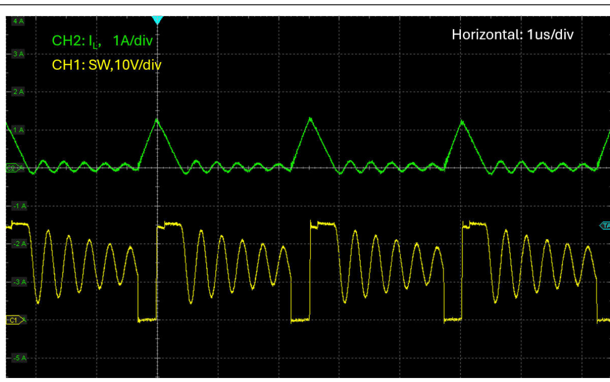


Figure 7-10. V_{in} = 14.4V, V_{out} = 24V, DEM, I_{load}= 0.1A

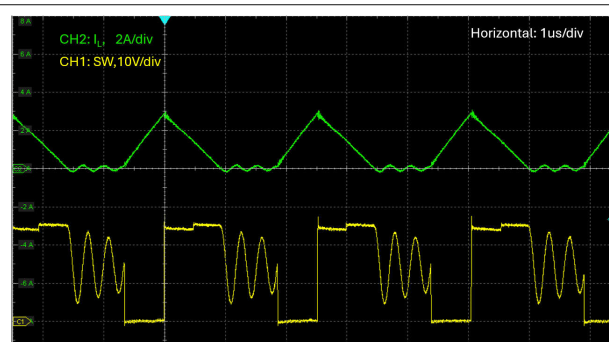


Figure 7-11. V_{in} = 14.4V, V_{out} = 24V, DEM, I_{load}= 0.5A

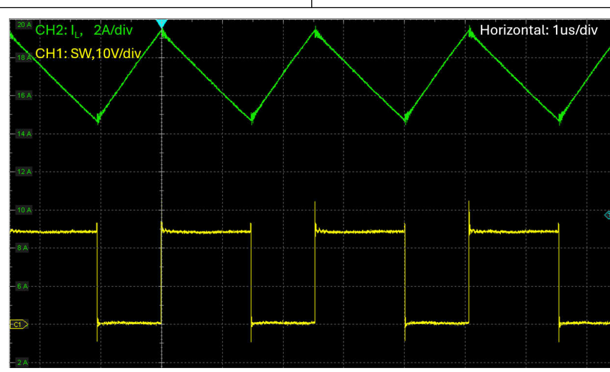


Figure 7-12. V_{in} = 14.4V, V_{out} = 24V, DEM, I_{load}= 10A

7.2.4.3 Step Load Response

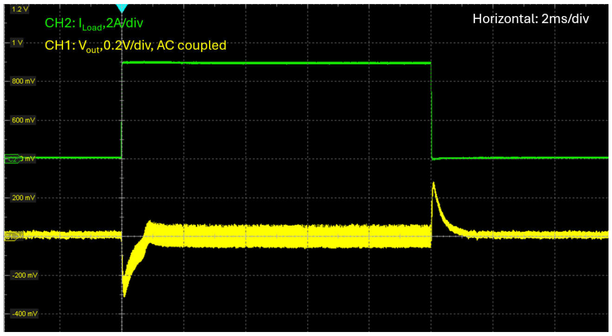


Figure 7-13. Load Transient, V_{in} = 14V, V_{out} = 24V, FPWM, I_{load} = 0A to 5A at 1A/µs

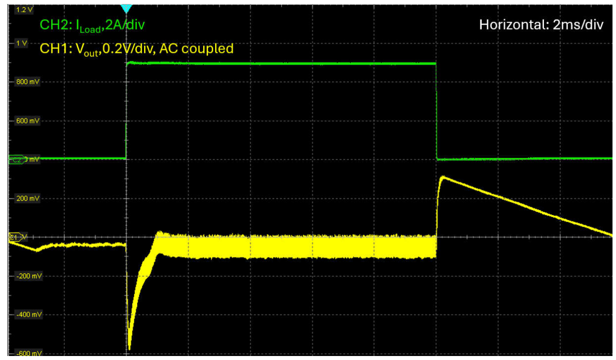


Figure 7-14. Load Transient, V_{in} = 14V, V_{out} = 24V, DEM, I_{load} = 0A to 5A at 1A/µs

7.2.4.4 Thermal Performance

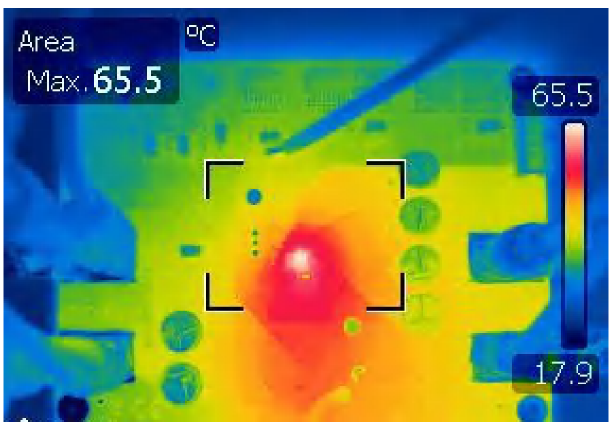


Figure 7-15. V_{IN} = 14.4V, V_{OUT} = 24V, P_{OUT} = 240W, Natural Convection

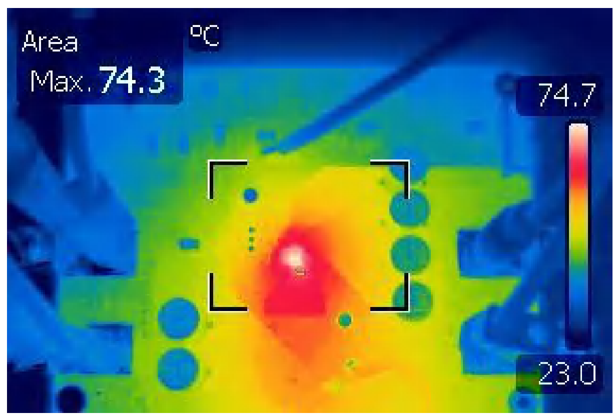


Figure 7-16. V_{IN} = 14.4V, V_{OUT} = 45V, P_{OUT} = 240W, Natural Convection

7.3 Power Supply Recommendations

The LMG5126 is designed to operate over a wide input voltage range. The characteristics of the input supply must be compatible with the Absolute Maximum Ratings and Recommended Operating Conditions. In addition, the input supply must be capable of delivering the required input current to the fully loaded regulator. Use Equation 95 to estimate the average input current.

$$I_I = \frac{P_O}{V_I \eta} \tag{95}$$

where

- η the efficiency.

One way to get a value for the efficiency is the data from the efficiency graphs in Section 7.2.4.1 in the worst case operation mode. For most applications, the boost operation is the region of highest input current.

If the device is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse effect on converter operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an under-damped resonant circuit. This circuit can cause overvoltage transients at V_I each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. One way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps to damp the input resonant circuit and reduce any voltage overshoots. An EMI input filter is often used in front of the converter power stage. Unless carefully designed, the EMI input filter can lead to instability as well as some of the previously mentioned affects.

7.4 Layout

7.4.1 Layout Guidelines

The performance of switching converters heavily depends on the quality of the PCB layout. Poor PCB design can cause among others converter instability, load regulation problems, noise or EMI issues. Do not use thermal relieved connections in the power path for VCC because the thermal relieved connections add significant inductance.

- Place the VCC and BIAS capacitors close to the corresponding device pins. Connect the capacitors with short and wide traces to minimize inductance as the capacitors carry high peak currents. Connect the VCC capacitors ground to power ground (PGND) and the BIAS capacitors ground to analog ground (AGND).
- Place CSA and CSB filter resistors and capacitors close to the corresponding device pins to minimize noise coupling between the filter and the device. Route the traces to the sense resistor R_{CS}, which is placed close to the inductor, as differential pair and surrounded by ground to avoid noise coupling. Use Kelvin connections to the sense resistor.
- Place the compensation network R_{COMP} and C_{COMP} as well as the frequency setting resistor R_{RT} close to the corresponding device pins and connect them with short traces to avoid noise coupling. Connect the analog ground pin AGND to these components.
- Place the ATRK resistor R_{ATRK} (when used) close to the ATRK pin and connect R_{ATRK} to AGND.
- The layout of following components is not as critical:
  - Soft-Start capacitor C_{SS}
  - DLY capacitor C_{DLY}
  - ILIM/IMON resistor and capacitor R_{ILIM} and C_{ILIM}
  - CFG1, CFG2 and SYNCOUT resistors
  - UVLO/EN resistors
- Place the filter V_{OUT} capacitors (small size ceramic) close to the VOUT-pin. Use short and wide traces to minimize the power stage loop C_{OUT} to VOUT connection to avoid high voltage spikes.
- Connect the PGND-pin connection with short and wide traces to the V_{OUT} and V_I capacitors ground to minimize inductance causing high voltage spikes.
- TI recommends connecting the AGND and PGND pin directly to the exposed pad (EP) to form a star connection at the device.
- Connect the device exposed pad (EP) with several vias to a ground plane to conduct heat away.
- Separate power and signal traces and use a ground plane to provide noise shielding.

To spread the heat generated by the converter and the inductor, place the inductor away from the converter. However the longer the trace between the inductor and the converter the higher the EMI and noise emissions. For highest efficiency, connect the inductor by wide and short traces to minimize resistive losses.

7.4.2 Layout Example

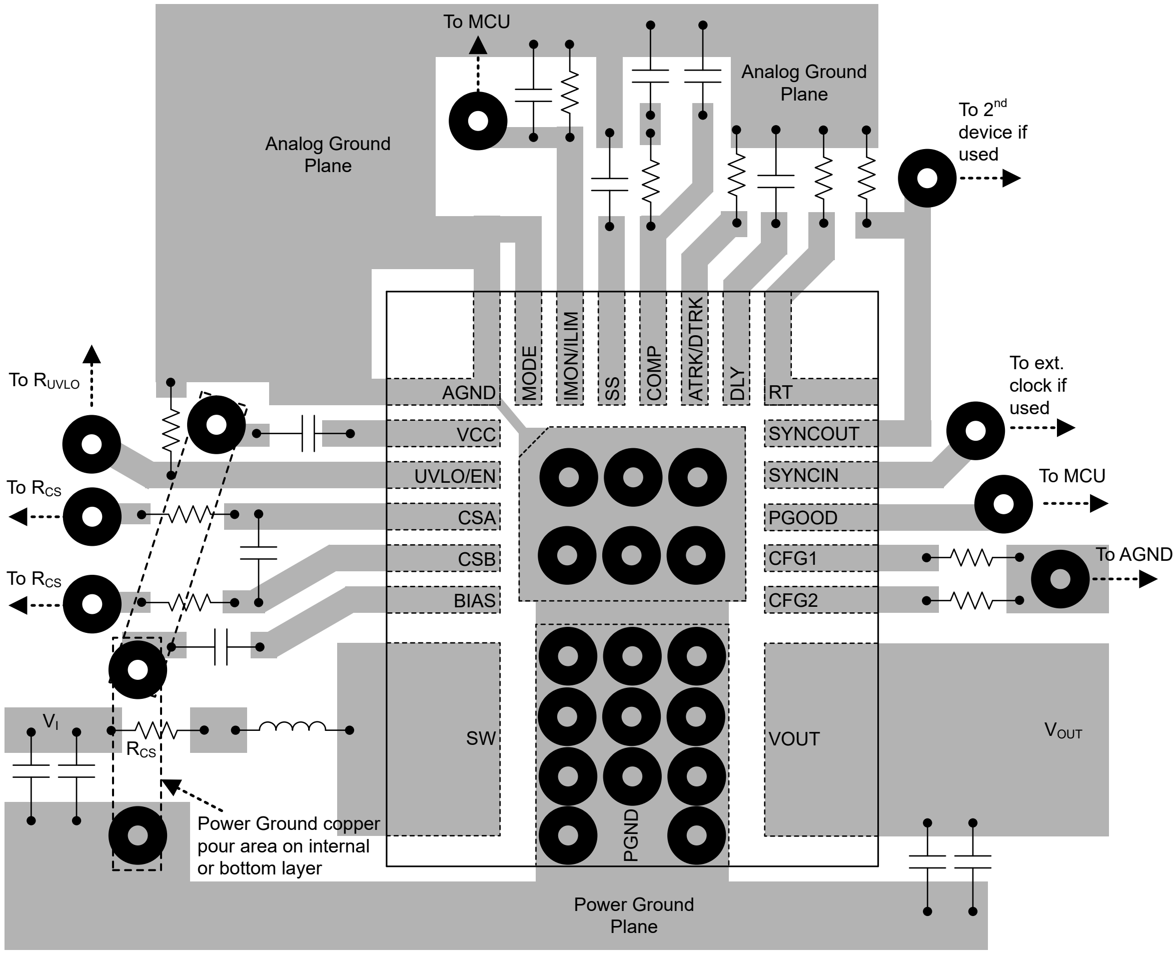


Figure 7-17. Layout Example

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Device Support

8.1.1 Third-Party Products Disclaimer

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8.1.2 Development Support

8.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMG5126 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer gives a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2 Documentation Support

8.2.1 Related Documentation

- Texas Instruments, *Improve High-Current DC/DC Regulator EMI Performance for Free With Optimized Power Stage Layout* application brief
- Texas Instruments, *Input Filter Design for Switching Power Supplies* application note

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.5 Trademarks

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2024) to Revision A (December 2025)	Page
• Changed data sheet status from Advance Information to Production Data	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
XLMG5126VBTT	Active	Preproduction	VQFN-FCRLF (VBT) | 22	250 | SMALL T&R	-	Call TI	Call TI	-40 to 125	
XLMG5126VBTT.A	Active	Preproduction	VQFN-FCRLF (VBT) | 22	250 | SMALL T&R	-	Call TI	Call TI	-40 to 125	
XLMG5126VBTT.B	Active	Preproduction	VQFN-FCRLF (VBT) | 22	250 | SMALL T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

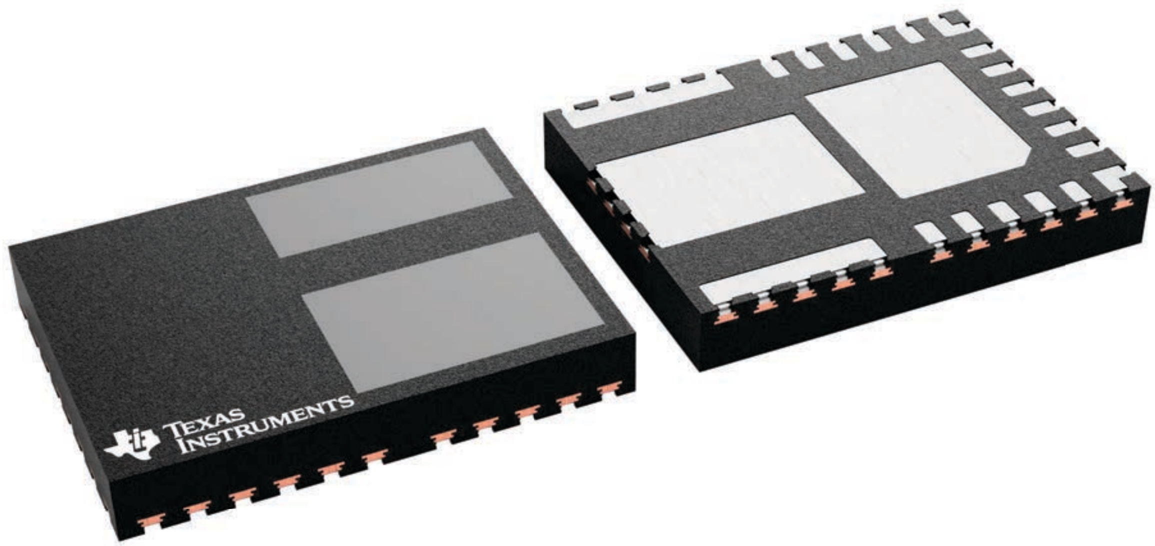
VBT 22

VQFN-FCRLF - 0.85 mm max height

4.5 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4231389/A