LMH6554 2.8-GHz Ultra Linear Fully Differential Amplifier

1 Features

- Small-Signal Bandwidth 2.8 GHz
- 2 V_{PP} Large-Signal Bandwidth 1.8 GHz
- 0.1 dB Gain Flatness 830 MHz
- OIP3 at 150 MHz 46.5 dBm
- HD2/HD3 at 75 MHz –96 / –97 dBc
- Input Noise Voltage 0.9 nV/√Hz
- Input Noise Current 11 pA/√Hz
- Slew Rate 6200 V/µs
- Power 260 mW
- Typical Supply Current 52 mA
- 14-Lead UQFN Package

2 Applications

- Differential ADC Driver
- Single-Ended to Differential Converter
- High-Speed Differential Signaling
- IF/RF and Base-band Gain Blocks
- SAW Filter Buffer/Driver
- Oscilloscope Probes
- Automotive Safety Applications
- Video Over Twisted Pair
- Differential Line Driver

3 Description

The LMH6554 device is a high-performance fully differential amplifier designed to provide the exceptional signal fidelity and wide large-signal bandwidth necessary for driving 8- to 16-bit high-speed data acquisition systems. Using TI's proprietary differential current mode input stage architecture, the LMH6554 has unity gain, small-signal bandwidth of 2.8GHz and allows operation at gains greater than unity without sacrificing response flatness, bandwidth, harmonic distortion, or output noise performance.

The low-impedance differential output of the device is designed to drive ADC inputs and any intermediate filter stage. The LMH6554 delivers 16-bit linearity up to 75 MHz when driving 2V peak-to-peak into loads as low as 200 Ω.

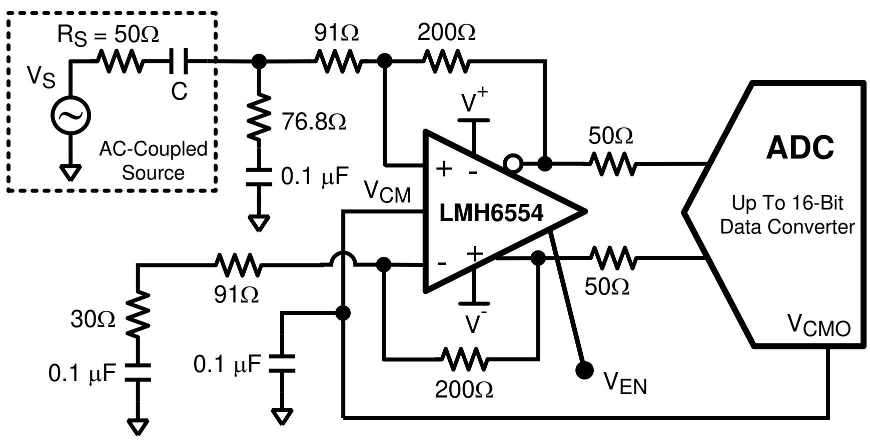
The LMH6554 is fabricated in TI's advanced complementary BiCMOS process and is available in a space-saving 14-lead UQFN package for higher performance.

Device Information (1)

PART NUMBER	PACKAGE	PACKAGE SIZE (2)
LMH6554	UQFN (14)	2.50 mm × 2.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Schematic

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4 Pin Configuration and Functions

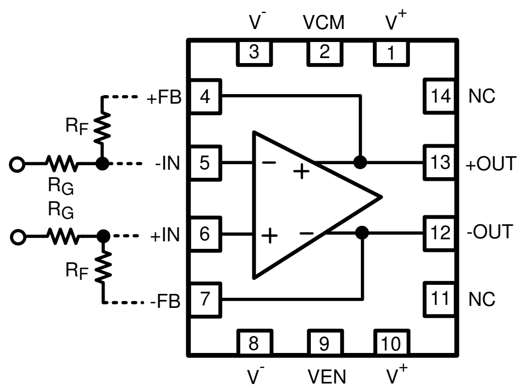


Figure 4-1. NHJ Package 14 Pins Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
-FB	7	O	Feedback from -OUT
+FB	4	O	Feedback from +OUT
+IN	6	I	Positive Input
-IN	5	I	Negative Input
NC	11	—	No Connection
NC	14	—	No Connection
-OUT	12	O	Negative Output
+OUT	13	O	Positive Output
VCM	2	I	Output Common Mode Voltage
VEN	9	I	Enable
V-	3	P	Negative Supply
V-	8	P	Negative Supply
V+	1	P	Positive Supply
V+	10	P	Positive Supply

5 Specifications

5.1 Absolute Maximum Ratings

(1) (2) (3)	MIN	MAX	UNIT
Supply Voltage ($V_S = V^+ - V^-$)		5.5	V
Common Mode Input Voltage	V^-	V^+	V
Maximum Operating Junction Temperature		150	°C
Maximum Input Current		30	mA
Maximum Output Current (pins 12, 13)			mA
Soldering Information [4] Infrared or Convection (30 sec)		260	°C
Storage Temperature, T_{stg}	−65	150	°C

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur.*Section 5.3* indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the *Section 5.5* tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The maximum output current (I_{OUT}) is determined by device power dissipation limitations. See *Section 7.4.3* for more details.
(4) For soldering specifications, see *Absolute Maximum Ratings for Soldering*.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±750	
		Machine model (MM)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions [1]

	MIN	NOM	MAX	UNIT
Operating Temperature Range	−40		+125	°C
Total Supply Voltage Temperature Range	4.7		5.25	V

5.4 Thermal Information

THERMAL METRIC [1]		LMH6554	UNIT
		NHJ	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics: +5 V

Unless otherwise specified, all limits are ensured for T_A = +25°C, A_V = +2, V^+ = +2.5 V, V− = −2.5 V, R_L = 200 Ω, V_{CM} = $(V^+ + V^-)$ / 2, R_F = 200 Ω, for single-ended in, differential out.[(1)]

PARAMETER		TEST CONDITIONS	MIN [(4)]	TYP [(3)]	MAX [(4)]	UNIT
AC PERFORMANCE (DIFFERENTIAL)						
SSBW	Small Signal −3 dB Bandwidth [(4)]	A_V = 1, V_{OUT} = 0.2 V_{PP}		2800		MHz
		A_V = 2, V_{OUT} = 0.2 V_{PP}		2500		
		A_V = 4, V_{OUT} = 0.2 V_{PP}		1600		
LSBW	Large Signal Bandwidth	A_V = 1, V_{OUT} = 2 V_{PP}		1800		MHz
		A_V = 2, V_{OUT} = 2 V_{PP}		1500		
		A_V = 2, V_{OUT} = 1.5 V_{PP}		1900		
0.1 dBBW	0.1 dB Bandwidth	A_V = 2, V_{OUT} = 0.2 V_{PP}, R_F = 250Ω		830		MHz
SR	Slew Rate	4V Step		6200		V/µs
t_r/t_f	Rise/Fall Time	2V Step, 10–90%		290		ps
		0.4V Step, 10–90%		150		
$T_{s\_0.1}$	0.1% Settling Time	2V Step, R_L = 200Ω		4		ns
	Overdrive Recovery Time	V_{IN} = 2V, A_V = 5 V/V		6		ns
DISTORTION AND NOISE RESPONSE						
HD2	2nd Harmonic Distortion	V_{OUT} = 2 V_{PP}, f = 20 MHz		-102		dBc
		V_{OUT} = 2 V_{PP}, f = 75 MHz		-96		
		V_{OUT} = 2 V_{PP}, f = 125 MHz		-87		
		V_{OUT} = 2 V_{PP}, f = 250 MHz		−79		
		V_{OUT} = 1.5 V_{PP}, f = 250 MHz		−81		
HD3	3rd Harmonic Distortion	V_{OUT} = 2 V_{PP}, f = 20 MHz		−110		dBc
		V_{OUT} = 2 V_{PP}, f = 75 MHz		−97		
		V_{OUT} = 2 V_{PP}, f = 125 MHz		−87		
		V_{OUT} = 2 V_{PP}, f = 250 MHz		−70		
		V_{OUT} = 1.5 V_{PP}, f = 250 MHz		−75		
OIP3	Output 3rd-Order Intercept	f = 150 MHz, V_{OUT} = 2V_{PP} Composite		46.5		dBm
IMD3	Two-Tone Inter-Modulation	f = 150 MHz, V_{OUT} = 2V_{PP} Composite		−97		dBc
e_n	Input Voltage Noise Density	f = 10 MHz		0.9		nV/√Hz
i_{n+}	Input Noise Current	f = 10 MHz		11		pA/√Hz
i_{n-}	Input Noise Current	f = 10 MHz		11		pA/√Hz
NF	Noise Figure [(8)]	50Ω System, A_V = 7.3, 100 MHz		7.7		dB
INPUT CHARACTERISTICS						
I_{BI+} / I_{BI-}			−75	−29	20	µA
TCIbi	Input Bias Current Temperature Drift			8		µA/°C
I_{BID}	Input Bias Current [(6)]	V_{CM} = 0V, V_{ID} = 0V, $I_{BOFFSET}$ = $(I_{B-} - I_{B+})/2$	−10	1	10	µA
TCIbo	Input Bias Current Diff Offset Temperature Drift [(3)]			0.006		µA/°C
CMRR	Common Mode Rejection Ratio	DC, V_{CM} = 0V, V_{ID} = 0V		83		dB
R_{IN}	Differential Input Resistance	Differential		19		Ω
C_{IN}	Differential Input Capacitance	Differential		1		pF
CMVR	Input Common Mode Voltage Range	CMRR > 32 dB	±1.25	±1.3		V
OUTPUT PERFORMANCE						
	Output Voltage Swing [(3)]	Single-Ended Output	±1.35	±1.42		V

Unless otherwise specified, all limits are ensured for T_A = +25°C, A_V = +2, V^+ = +2.5 V, V− = −2.5 V, R_L = 200 Ω, V_{CM} = $(V^+ + V^-) / 2$, R_F = 200 Ω, for single-ended in, differential out.[1]

PARAMETER		TEST CONDITIONS	MIN [4]	TYP [3]	MAX [4]	UNIT
I_{OUT}	Output Current [3]	V_{OUT} = 0V	±120	±150		mA
I_{SC}	Short Circuit Current	One Output Shorted to Ground V_{IN} = 2V Single-Ended [2]		150		mA
	Output Balance Error	ΔVOUT Common Mode /ΔV_{OUT} Differential, ΔV_{OD} = 1V, f < 1 MHz		−64		dB
OUTPUT COMMON MODE CONTROL CIRCUIT						
	Common Mode Small Signal Bandwidth	$V_{IN+} = V_{IN-}$ = 0V		500		MHz
	Slew Rate	$V_{IN+} = V_{IN-}$ = 0V		200		V/µs
V_{OSCM}	Input Offset Voltage	Common Mode, V_{ID} = 0, V_{CM} = 0V	−16	−6.5	4	mV
I_{OSCM}	Input Offset Current	[5]		6	18	µA
	Voltage Range		±1.18	±1.25		V
	CMRR	Measure V_{OD}, V_{ID} = 0V		82		dB
	Input Resistance			180		kΩ
	Gain	$\Delta V_{OCM}/\Delta V_{CM}$	0.99	0.995	1.0	V/V
MISCELLANEOUS PERFORMANCE						
Z_T	Open Loop Transimpedance Gain	Differential		180		kΩ
PSRR	Power Supply Rejection Ratio	DC, $\Delta V^+ = \Delta V^-$ = 1V	74	95		dB
I_S	Supply Current [3]	R_L = ∞	46	52	57	mA
		R_L = ∞, At extreme temperatures			60	mA
	Enable Voltage Threshold	Single 5V Supply [7]		2.5		V
	Disable Voltage Threshold	Single 5V Supply [7]		2.5		V
	Enable/Disable Time			15		ns
I_{SD}	Supply Current, Disabled	Enable=0, Single 5-V supply	450	510	770	µA
		Enable=0, Single 5-V supply, At extreme temperatures			850	µA

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. See Section 5.4 for information on temperature de-rating of this device." Min/Max ratings are based on product characterization and simulation. Individual parameters are tested as noted.
(2) Short circuit current should be limited in duration to no more than 10 seconds. See *Section 7.4.3* for more details.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods.
(5) Negative input current implies current flowing out of the device.
(6) I_{BI} is referred to a differential output offset voltage by the following relationship: $V_{OD(OFFSET)} = I_{BI} * 2R_F$.
(7) V_{EN} threshold is typically +/-0.3V centered around $(V^+ + V^-) / 2$ relative to ground.
(8) For test schematic, refer to Figure 7-10.

5.6 Typical Performance Characteristics V_S = ±2.5 V

(T_A = 25°C, R_F = 200 Ω, R_G = 90 Ω, R_T = 76.8 Ω, R_L = 200 Ω, A_V = +2, for single ended in, differential out, unless specified).

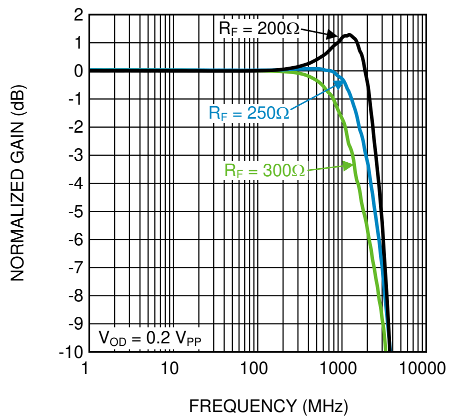


Figure 5-1. Frequency Response vs R_F

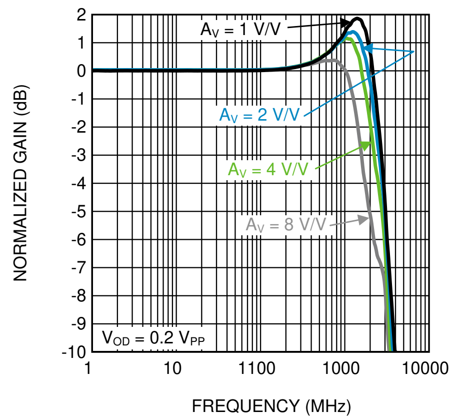


Figure 5-2. Frequency Response vs Gain

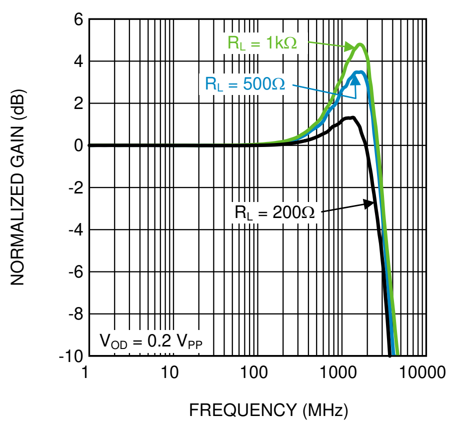


Figure 5-3. Frequency Response vs R_L

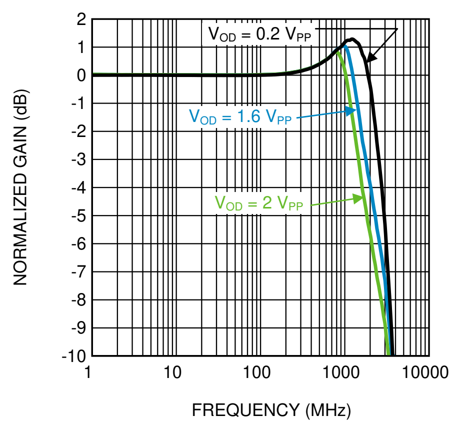


Figure 5-4. Frequency Response vs Output Voltage (V_{OD})

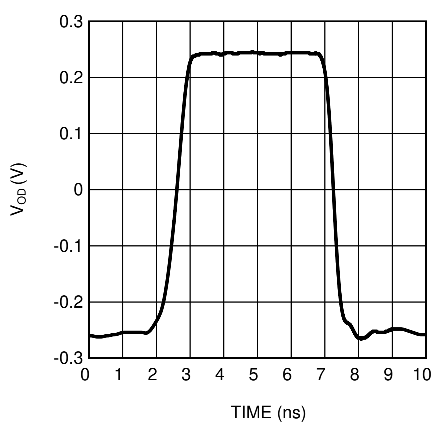


Figure 5-5. 0.5 V_{PP} Pulse Response Single-Ended Input

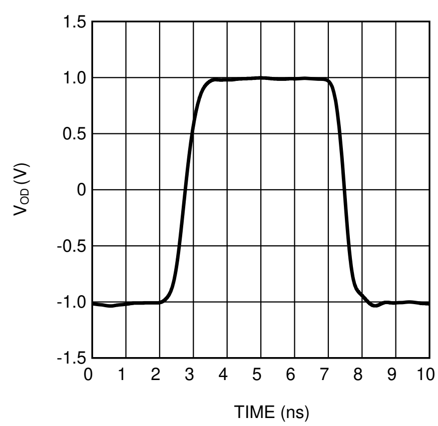


Figure 5-6. 2 V_{PP} Pulse Response Single-Ended Input

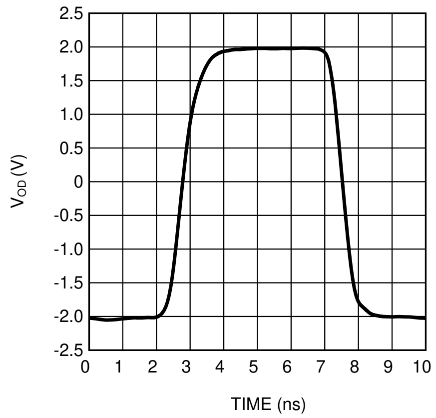


Figure 5-7. 4 V_{PP} Pulse Response Single-Ended Input

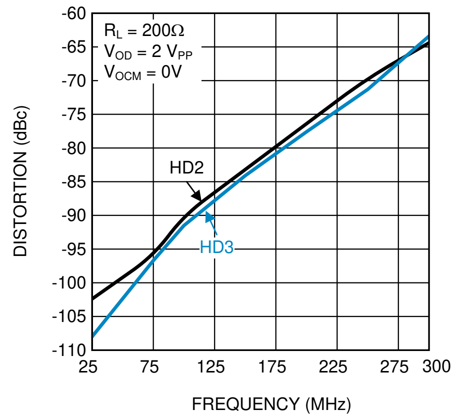


Figure 5-8. Distortion vs Frequency Single-Ended Input

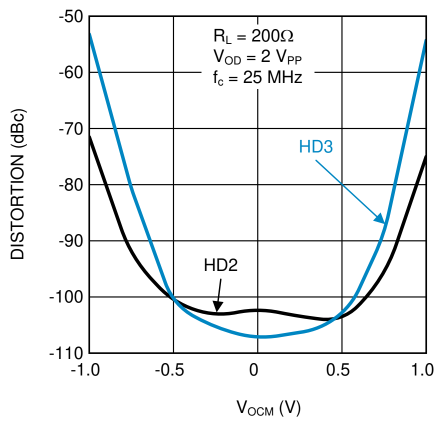


Figure 5-9. Distortion vs Output Common Mode Voltage

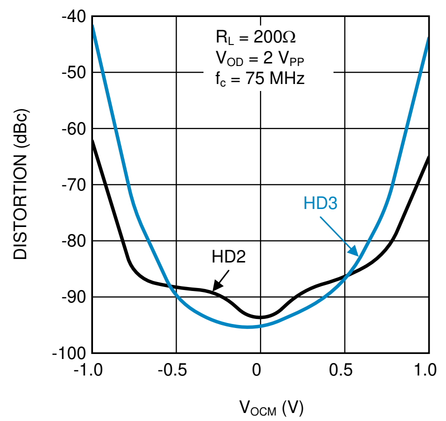


Figure 5-10. Distortion vs Output Common Mode Voltage

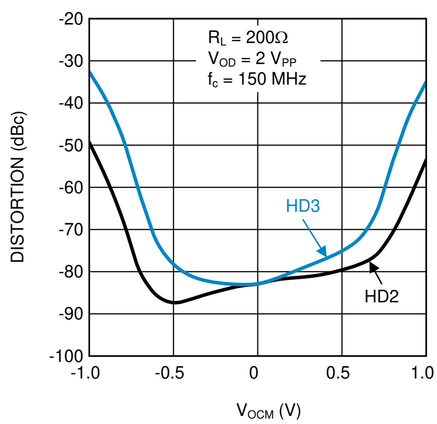


Figure 5-11. Distortion vs Output Common Mode Voltage

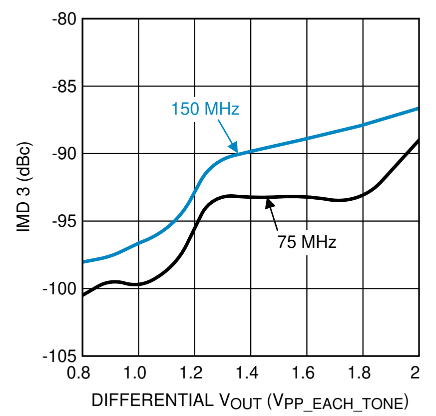


Figure 5-12. 3rd Order Inter-Modulation Products vs V_{OUT}

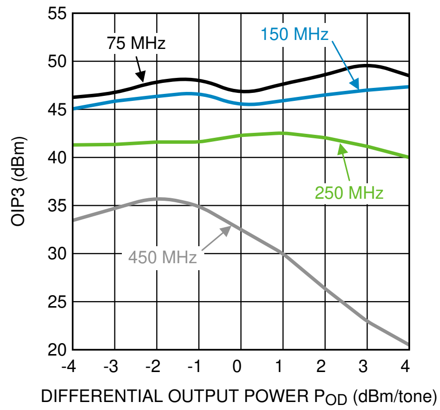


Figure 5-13. OIP3 vs Output Power P_{OUT}

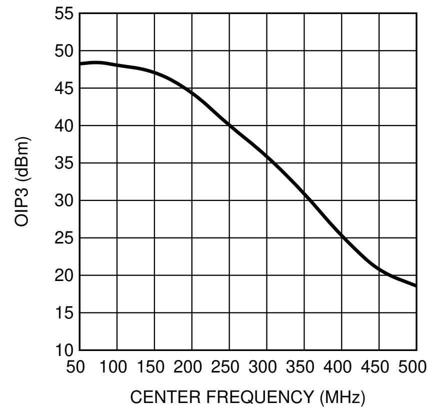


Figure 5-14. OIP3 vs Center Frequency

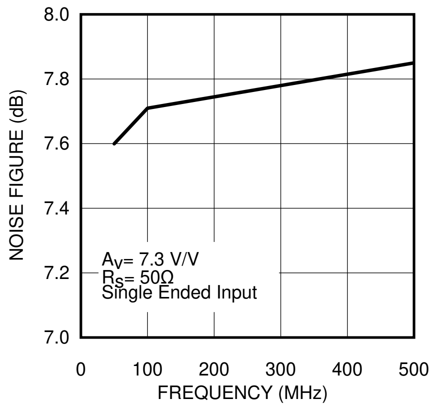


Figure 5-15. Noise Figure vs Frequency

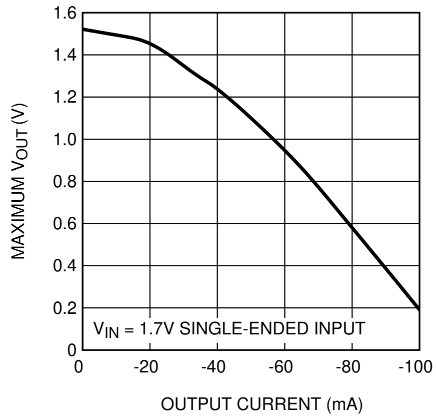


Figure 5-16. Maximum V_{OUT} vs I_{OUT}

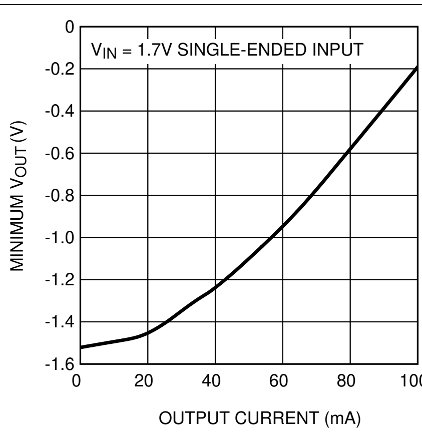


Figure 5-17. Minimum V_{OUT} vs I_{OUT}

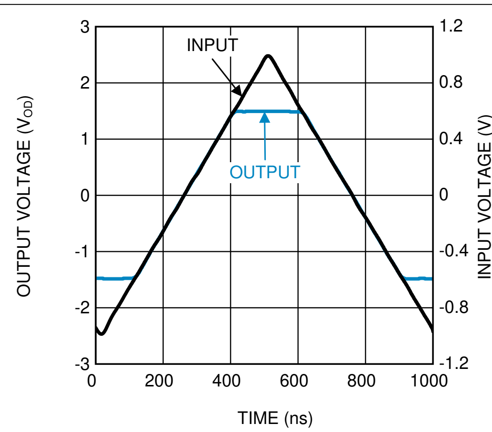


Figure 5-18. Overdrive Recovery

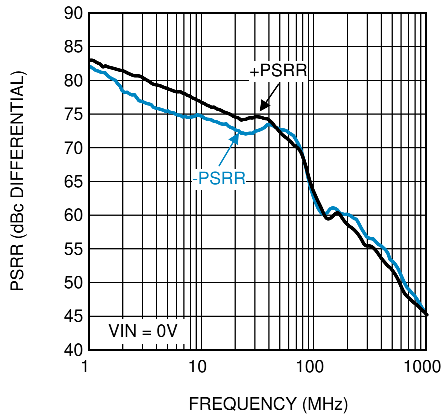


Figure 5-19. PSRR

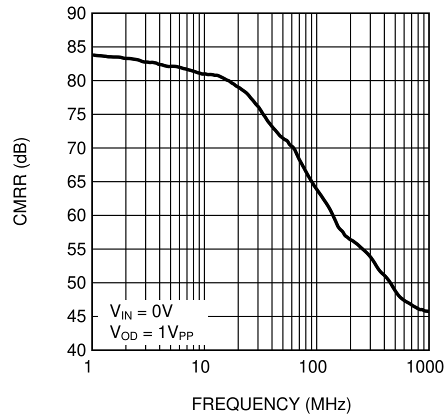


Figure 5-20. CMRR

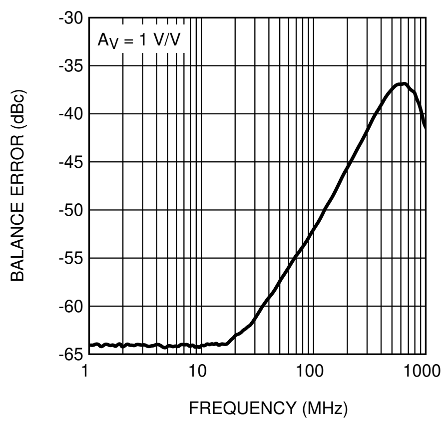


Figure 5-21. Balance Error

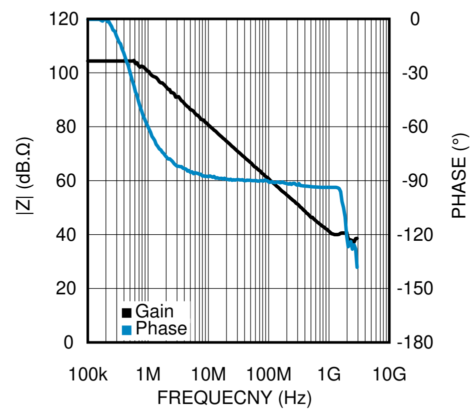


Figure 5-22. Open Loop Transimpedance

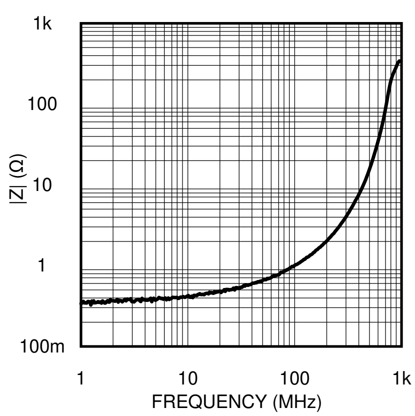


Figure 5-23. Closed-Loop Output Impedance

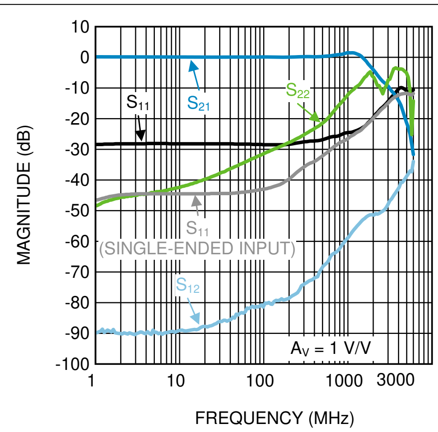


Figure 5-24. Differential S-Parameter Magnitude vs Frequency

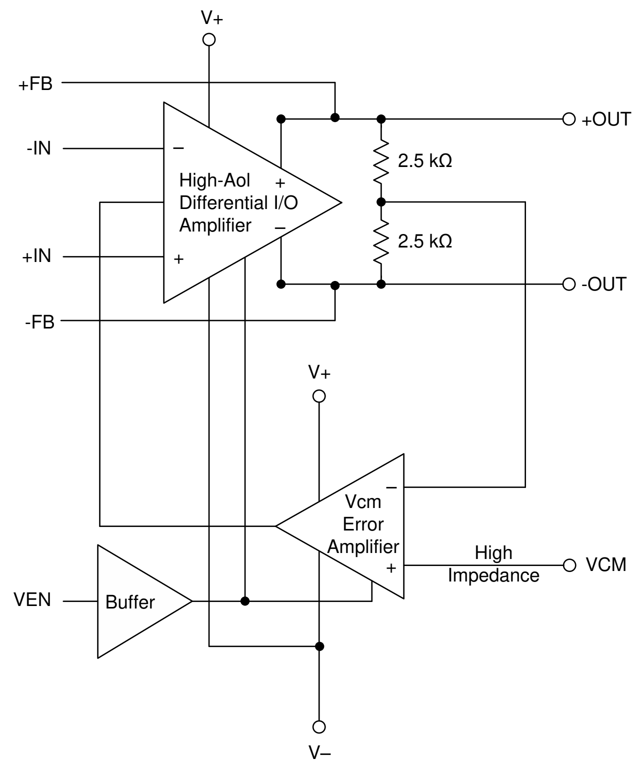
6 Detailed Description

6.1 Overview

The LMH6554 is a fully differential, current feedback amplifier with integrated output common mode control, designed to provide low distortion amplification to wide bandwidth differential signals. The common mode feedback circuit sets the output common mode voltage independent of the input common mode, as well as forcing the V+ and V− outputs to be equal in magnitude and opposite in phase, even when only one of the inputs is driven as in single to differential conversion.

The proprietary current feedback architecture of the LMH6554 offers gain and bandwidth independence with exceptional gain flatness and noise performance, even at high values of gain, simply with the appropriate choice of RF1 and RF2. Generally RF1 is set equal to RF2, and RG1 equal to RG2, so that the gain is set by the ratio RF/RG. Matching of these resistors greatly affects CMRR, DC offset error, and output balance.

6.2 Functional Block Diagram



6.3 Feature Description

The proprietary current feedback architecture of the LMH6554 offers gain and bandwidth independence with exceptional gain flatness and noise performance, even at high values of gain, simply with the appropriate choice of RF1 and RF2. Generally RF1 is set equal to RF2, and RG1 equal to RG2, so that the gain is set by the ratio RF/RG. Matching of these resistors greatly affects CMRR, DC offset error, and output balance. A maximum of 0.1% tolerance resistors are recommended for desired performance, and the amplifier is internally compensated to operate with optimum gain flatness with RF value of 200 Ω depending on PCB layout, and load resistance. The output common mode voltage is set by the VCM pin with a fixed gain of 1V/V. This pin must be driven by a low impedance reference and must be bypassed to ground with a 0.1µF ceramic capacitor. Any unwanted signal coupling into the VCM pin is passed along to the outputs, reducing the performance of the amplifier. The LMH6554 can be configured to operate on a single 5V supply connected to V+ with V- grounded or configured for a split supply operation with V+ = +2.5V and V− = −2.5V. Operation on a single 5V supply, depending on gain, is limited by the input common mode range; therefore, AC coupling can be required.

6.4 Device Functional Modes

This wideband FDA requires external resistors for correct signal-path operation. When configured for the desired input impedance and gain setting with these external resistors, the amplifier can be either on with the PD pin asserted to a voltage greater than Vs– + 1.7V, or turned off by asserting PD low. Disabling the amplifier shuts off the quiescent current and stops correct amplifier operation. The signal path is still present for the source signal through the external resistors. The Vocm control pin sets the output average voltage. Left open, Vocm defaults to an internal mid-supply value. Driving this high-impedance input with a voltage reference within the valid range sets a target for the internal Vcm error amplifier.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The LMH6554 is a fully differential, current feedback amplifier with integrated output common mode control, designed to provide low distortion amplification to wide bandwidth differential signals. The common mode feedback circuit sets the output common mode voltage independent of the input common mode, as well as forcing the V^+ and V^- outputs to be equal in magnitude and opposite in phase, even when only one of the inputs is driven as in single to differential conversion.

The proprietary current feedback architecture of the LMH6554 offers gain and bandwidth independence with exceptional gain flatness and noise performance, even at high values of gain, simply with the appropriate choice of R_{F1} and R_{F2}. Generally R_{F1} is set equal to R_{F2}, and R_{G1} equal to R_{G2}, so that the gain is set by the ratio R_F/R_G. Matching of these resistors greatly affects CMRR, DC offset error, and output balance. A maximum of 0.1% tolerance resistors are recommended for desired performance, and the amplifier is internally compensated to operate with optimum gain flatness with R_F value of 200 Ω depending on PCB layout, and load resistance.

The output common mode voltage is set by the V_{CM} pin with a fixed gain of 1V/V. This pin must be driven by a low impedance reference and must be bypassed to ground with a 0.1-μF ceramic capacitor. Any unwanted signal coupling into the V_{CM} pin is passed along to the outputs, reducing the performance of the amplifier.

The LMH6554 can be configured to operate on a single 5V supply connected to V+ with V- grounded or configured for a split supply operation with V^+ = +2.5V and V^- = −2.5V. Operation on a single 5V supply, depending on gain, is limited by the input common mode range; therefore, AC coupling can be required. Split supplies allows much less restricted AC and DC coupled operation with optimum distortion performance.

7.2 Typical Applications

7.2.1 Single-Ended Input to Differential Output Operation

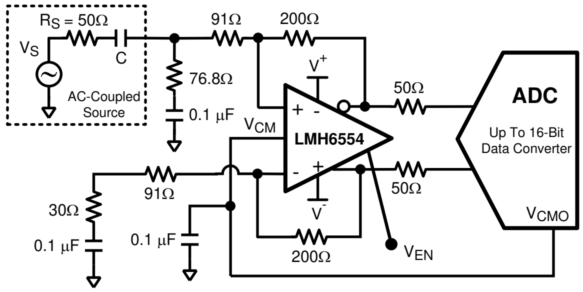


Figure 7-1. Single-Ended Input to Differential Output Schematic

7.2.1.1 Design Requirements

One typical application for the LMH6554 is to drive an ADC as shown in Figure 7-1. The following design is a single-ended to differential circuit with an input impedance of 50 Ω and an output impedance of 100 Ω. The VCM voltage of the amplifier needs to be set to the same voltage as the ADC reference voltage, which is typically 1.2 V. Figure 7-3 shows the design equations required to set the external resistor values. This design also requires a gain of 2 and -96 dBc THD at 75 MHz.

7.2.1.2 Detailed Design Procedure

To match the input impedance of the circuit in Figure 7-3 to a specified source resistance, RS, requires that RT || RIN = RS. The equations governing RIN and AV for single-to-differential operation are also provided in Figure 7-3. These equations, along with the source matching condition, must be solved iteratively to achieve the desired gain with the proper input termination. Component values for several common gain configuration in a 50 Ω environment are given in Table 7-1.

7.2.1.2.1 Enable / Disable Operation

The LMH6554 is equipped with an enable pin (V_{EN}) to reduce power consumption when not in use. The V_{EN} pin, when not driven, floats high (on). When the V_{EN} pin is pulled low, the amplifier is disabled and the amplifier output stage goes into a high impedance state so the feedback and gain set resistors determine the output impedance of the circuit. For this reason input to output isolation is poor in the disabled state and the part is not recommended in multiplexed applications where outputs are all tied together.

With a 5V difference between V^+ and V^-, the V_{EN} threshold is ½ way between the supplies (for example 2.5V with 5V single supply) as shown in Figure 7-2. R2 maintains active (enable) mode with V_{EN} floating, and R1 provides input current limiting. V_{EN} also has ESD diodes to either supply.

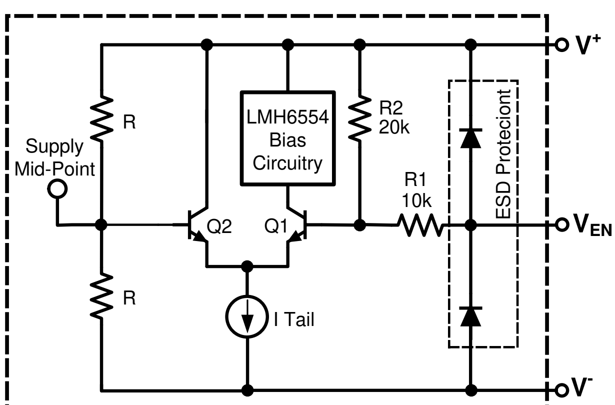
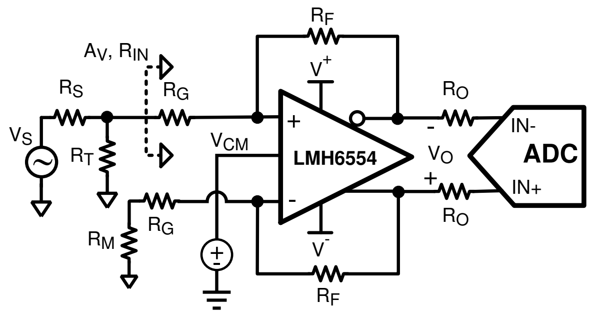


Figure 7-2. Enable Block Diagram

7.2.1.2.2 Single-Ended Input to Differential Output Operation

In many applications, it is required to drive a differential input ADC from a single ended source. Traditionally, transformers have been used to provide single to differential conversion, but these are inherently bandpass by nature and cannot be used for DC coupled applications. The LMH6554 provides excellent performance as a single-ended input to differential output converter down to DC. Figure 7-3 shows a typical application circuit where an LMH6554 is used to produce a balanced differential output signal from a single ended source.



$$A_V = \left(\frac{2(1-\beta_1)}{\beta_1 + \beta_2}\right) \qquad \beta_1 = \left(\frac{R_G}{R_G + R_F}\right)$$

$$R_{IN} = \left(\frac{2R_G + R_M(1-\beta_2)}{1+\beta_2}\right) \qquad \beta_2 = \left(\frac{R_G + R_M}{R_G + R_F + R_M}\right)$$

$$R_S = R_T \,||\, R_{IN} \qquad R_M = R_T \,||\, R_S$$

Figure 7-3. Single-Ended Input with Differential Output

When using the LMH6554 in single-to-differential mode, the complimentary output is forced to a phase inverted replica of the driven output by the common mode feedback circuit as opposed to being driven by its own complimentary input. Consequently, as the driven input changes, the common mode feedback action results in a varying common mode voltage at the amplifier's inputs, proportional to the driving signal. Due to the non-ideal common mode rejection of the amplifier's input stage, a small common mode signal appears at the outputs which is superimposed on the differential output signal. The ratio of the change in output common mode voltage to output differential voltage is commonly referred to as output balance error. The output balance error response of the LMH6554 over frequency is shown in the *Section 5.6*.

To match the input impedance of the circuit in Figure 7-3 to a specified source resistance, R_S, requires that $R_T \,||\, R_{IN} = R_S$. The equations governing R_{IN} and A_V for single-to-differential operation are also provide in Figure 7-3. These equations, along with the source matching condition, must be solved iteratively to achieve the desired gain with the proper input termination. Component values for several common gain configuration in a 50Ω environment are given in Table 7-1.

Table 7-1. Gain Component Values for 50 Ω System

GAIN	R_F	R_G	R_T	R_M
0dB	200Ω	191Ω	62Ω	27.7Ω
6dB	200Ω	91Ω	76.8Ω	30.3Ω
12dB	200Ω	35.7Ω	147Ω	37.3Ω

7.2.1.2.3 Driving Capacitive Loads

As noted previously, capacitive loads must be isolated from the amplifier output with small valued resistors. This is particularly the case when the load has a resistive component that is 500Ω or higher. A typical ADC has capacitive components of around 1pF and the resistive component can be 1000Ω or higher. If driving a transmission line, such as 50Ω coaxial or 100Ω twisted pair, using matching resistors is sufficient to isolate any subsequent capacitance. For other applications, see Figure 7-5 in *Section 5.6*.

7.2.1.3 Application Curves

Many application circuits have capacitive loading. As shown in Figure 7-4, amplifier bandwidth is reduced with increasing capacitive load, so parasitic capacitance must be strictly limited.

To maintain stability resistance must be added between the capacitive load and the amplifier output pins. The value of the resistor is dependent on the amount of capacitive load as shown in Figure 7-5. This resistive value is a suggestion. System testing is required to determine the desired value. Using a smaller resistor retains more system bandwidth at the expense of overshoot and ringing, while larger values of resistance reduces overshoot but also reduces system bandwidth.

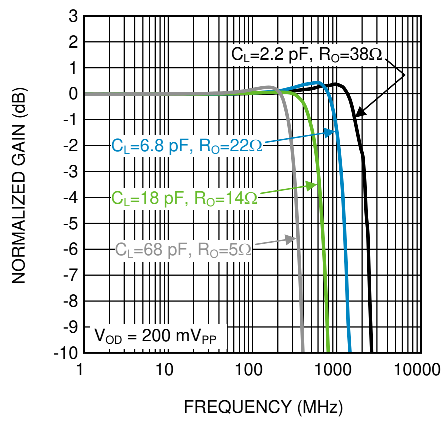


Figure 7-4. Frequency Response vs Capacitive Load

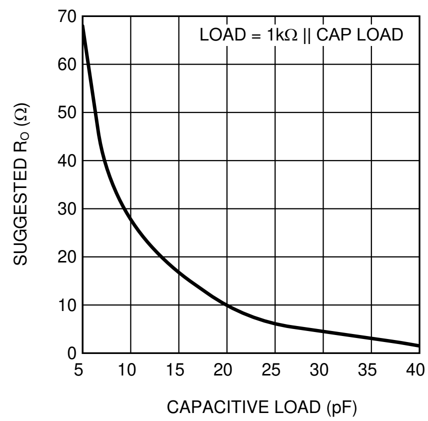


Figure 7-5. Suggested R_{OUT} vs Capacitive Load

7.2.2 Fully Differential Operation

The LMH6554 performs best in a fully differential configuration. The circuit shown in Figure 7-6 is a typical fully differential application circuit and can be used to drive an analog to digital converter (ADC). In this circuit the closed loop gain is $A_V = V_{OUT} / V_{IN} = R_F / R_G$, where the feedback is symmetric. The series output resistors, R_O, are optional and help keep the amplifier stable when presented with a capacitive load. Refer to the *Section 7.2.1.2.3* section for details.

Here is the expression for the input impedance, R_{IN}, as defined in Figure 7-6:

$R_{IN} = 2R_G$

When driven from a differential source, the LMH6554 provides low distortion, excellent balance, and common mode rejection. This is true provided the resistors R_F, R_G and R_O are well matched and strict symmetry is observed in board layout. With an intrinsic device CMRR of greater than 70 dB, using 0.1% resistors gives a worst case CMRR of around 50 dB for most circuits.

The circuit configuration shown in Figure 7-6 is used to measure differential S-parameters in a 100Ω environment at a gain of 1V/V. Refer to Figure 5-24 in *Section 5.6* for measurement results.

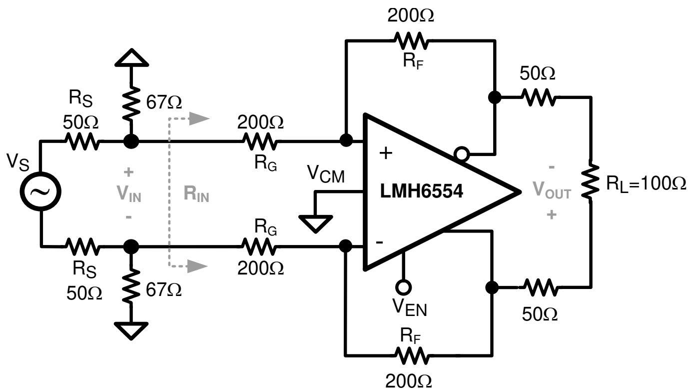


Figure 7-6. Differential S-Parameter Test Circuit

7.2.3 Single Supply Operation

Single 5V supply operation is possible: however, as discussed earlier, AC input coupling is recommended due to input common mode limitations. An example of an AC coupled, single supply, single-to-differential circuit is shown in Figure 7-7. Note that when AC coupling, both inputs need to be AC coupled irrespective of single-to-differential or differential-differential configuration. For higher supply voltages DC coupling of the inputs may be possible provided that the output common mode DC level is set high enough so that the amplifier's inputs and outputs are within their specified operation ranges.

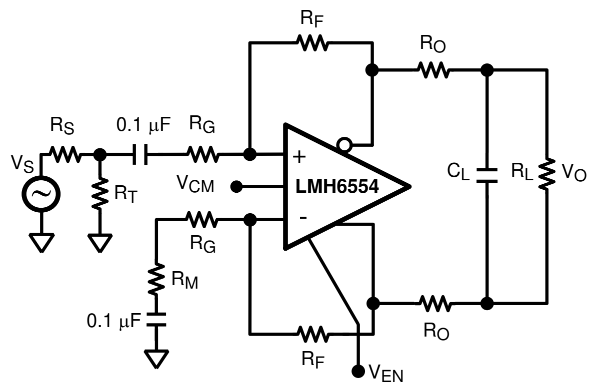


Figure 7-7. AC Coupled for Single Supply Operation

For optimum performance, split supply operation is recommended using +2.5-V and −2.5-V supplies; however, operation is possible on split supplies as low as +2.35 V and −2.35 V and as high as +2.65 V and −2.65 V. Provided the total supply voltage does not exceed the 4.7-V to 5.3-V operating specification, non-symmetric supply operation is also possible and in some cases advantageous. For example, if a 5-V DC coupled operation is required for low power dissipation but the amplifier input common mode range prevents this operation, it is still possible with split supplies of (V+) and (V-). Where (V+)-(V-) = 5 V and V+ and V- are selected to center the amplifier input common mode range to suit the application.

7.2.4 Driving Analog-to-Digital Converters

Analog-to-digital converters present challenging load conditions. Analog-to-digital converters typically have high impedance inputs with large and often variable capacitive components. Figure 7-8 shows the LMH6554 driving an ultra-high-speed Gigasample ADC the ADC10D1500. The LMH6554 common mode voltage is set by the ADC10D1500. The circuit in Figure 7-8 has a 2nd order bandpass LC filter across the differential inputs of the ADC10D1500. The ADC10D1500 is a dual channel 10–bit ADC with maximum sampling rate of 3 GSPS when operating in a single channel mode and 1.5 GSPS in dual channel mode.

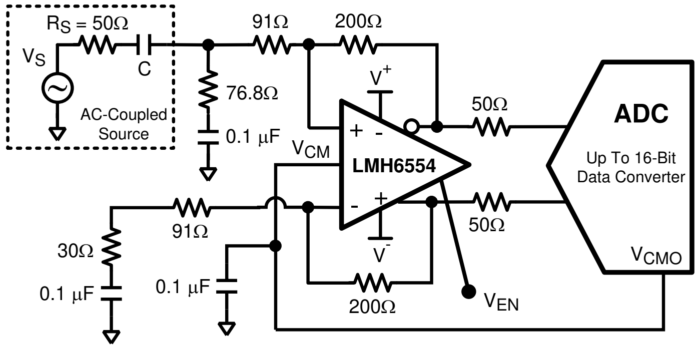


Figure 7-8. Driving a 10-bit Gigasample ADC

Figure 7-9 shows the SFDR and SNR performance vs. frequency for the LMH6554 and ADC10D1500 combination circuit with the ADC input signal level at −1dBFS. To properly match the input impedance seen at the LMH6554 amplifier inputs, R_M is chosen to match Z_S || R_T for proper input balance. The amplifier is configured to provide a gain of 2V/V in single to differential mode. An external bandpass filter is inserted in series between the input signal source and the amplifier to reduce harmonics and noise from the signal generator.

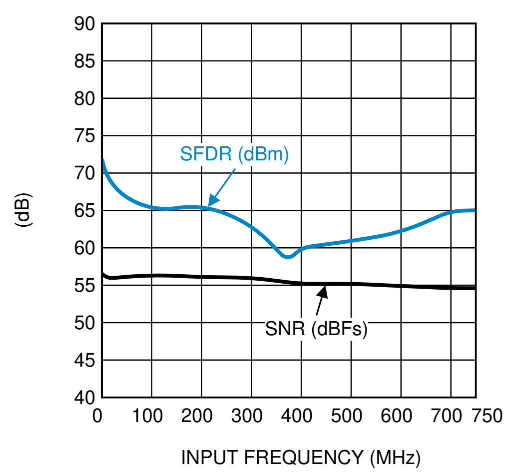


Figure 7-9. LMH6554 / ADC10D1500 SFDR and SNR Performance vs. Frequency

The amplifier and ADC is located as close together as possible. Both devices require that the filter components be in close proximity to them. The amplifier needs to have minimal parasitic loading on the outputs and the ADC is sensitive to high frequency noise that can couple in on the inputs. Some high performance ADCs have an input stage that has a bandwidth of several times the sample rate. The sampling process results in all input signals presented to the input stage mixing down into the first Nyquist zone (DC to Fs/2).

7.2.5 Output Noise Performance and Measurement

Unlike differential amplifiers based on voltage feedback architectures, noise sources internal to the LMH6554 refer to the inputs largely as current sources, hence the low input referred voltage noise and relatively higher input referred current noise. The output noise is therefore more strongly coupled to the value of the feedback resistor and not to the closed loop gain, as is the case with a voltage feedback differential amplifier. This allows operation of the LMH6554 at much higher gain without incurring a substantial noise performance penalty, simply by choosing a desired feedback resistor.

Figure 7-10 shows a circuit configuration used to measure noise figure for the LMH6554 in a 50Ω system. A feedback resistor value of 200Ω is chosen for the UQFN package to minimize output noise while simultaneously allowing both high gain (7V/V) and proper 50Ω input termination. Refer to *Section 7.2.1.2.2* for the calculation of resistor and gain values.

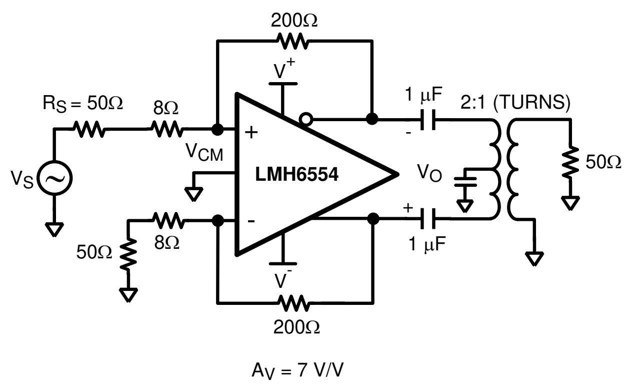


Figure 7-10. Noise Figure Circuit Configuration

7.2.6 Balanced Cable Driver

With up to 5.68 V_{PP} differential output voltage swing the LMH6554 can be configured as a cable driver. The LMH6554 is also designed for driving differential cables from a single ended source as shown in Figure 7-11.

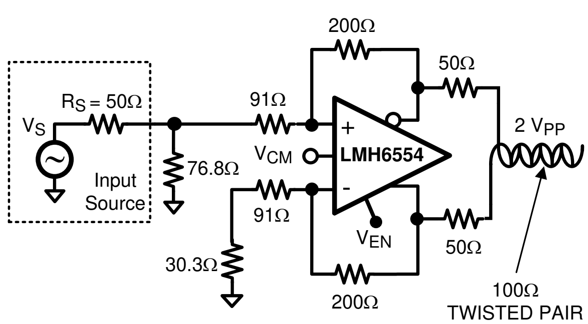


Figure 7-11. Fully Differential Cable Driver

7.3 Power Supply Recommendations

The LMH6554 can be used with any combination of positive and negative power supplies as long as the combined supply voltage is between 4.7V and 5.25 V. The LMH6554 provides the best performance when the output voltage is set at the mid supply voltage, and when the total supply voltage is set to 5V.

Power supply bypassing as shown in *Section 7.3.1* is important and power supply regulation must be within 5% or better.

7.3.1 Power Supply Bypassing

The LMH6554 requires supply bypassing capacitors as shown in Figure 7-12 and Figure 7-13. The 0.01-μF and 0.1-μF capacitors should be lead-less SMT ceramic capacitors and should be no more than 3 mm from the supply pins. These capacitors should be star routed with a dedicated ground return plane or trace for best harmonic distortion performance. Thin traces or small vias will reduce the effectiveness of bypass capacitors. Also shown in both figures is a capacitor from the VCM and V_{EN} pins to ground. These inputs are high impedance and can provide a coupling path into the amplifier for external noise sources, possibly resulting in loss of dynamic range, degraded CMRR, degraded balance and higher distortion.

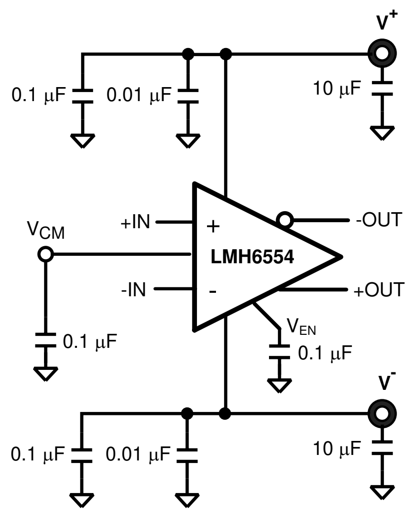


Figure 7-12. Split Supply Bypassing Capacitors

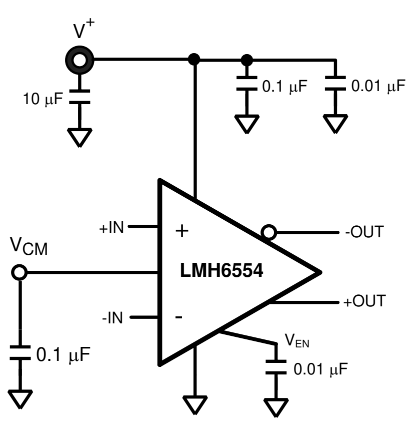


Figure 7-13. Single Supply Bypassing Capacitors

7.4 Layout

7.4.1 Layout Guidelines

The LMH6554 is a high speed, high performance amplifier. To get maximum benefit from the differential circuit architecture board layout and component selection is very critical. The circuit board has a low inductance ground plane and well bypassed broad supply lines. External components must be lead-less surface mount types. The feedback network and output matching resistors must be composed of short traces and precision resistors (0.1%). The output matching resistors must be placed within 3 or 4mm of the amplifier as well as the supply bypass capacitors. Refer to *Section 7.3.1* for recommendations on bypass circuit layout. Evaluation boards are available through the product folder on ti.com.

By design, the LMH6554 is relatively insensitive to parasitic capacitance at the inputs. Nonetheless, ground and power plane metal must be removed from beneath the amplifier and from beneath R_F and R_G for best performance at high frequency.

With any differential signal path, symmetry is very important. Even small amounts of asymmetry can contribute to distortion and balance errors.

7.4.2 Layout Example

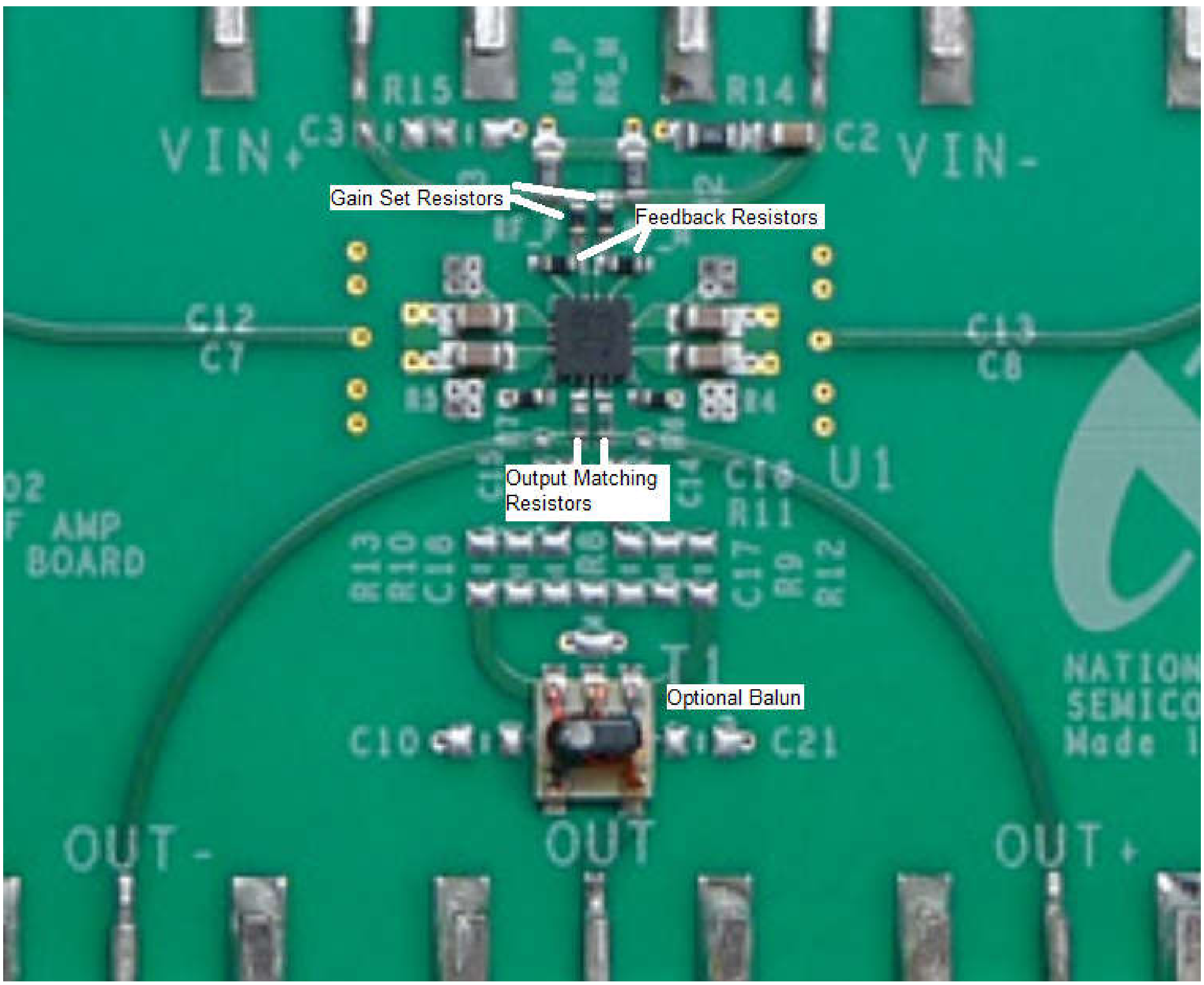


Figure 7-14. Layout Schematic

7.4.3 Power Dissipation

The LMH6554 is optimized for maximum speed and performance in a small form factor 14 lead UQFN package. To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the T_{JMAX} is never exceeded due to the overall power dissipation.

Follow these steps to determine the maximum power dissipation for the LMH6554:

1. Calculate the quiescent (no-load) power:

$$P_{AMP} = I_{CC} * (V_S) \quad (1)$$

where

- $V_S = V^+ - V^-$. (Be sure to include any current through the feedback network if V_{CM} is not mid-rail)

2. Calculate the RMS power dissipated in each of the output stages:

$$P_D\,(rms) = rms\,((V_S - V+_{OUT}) * I+_{OUT}) + rms\,((V_S - V-_{OUT}) * I-_{OUT}) \quad (2)$$

where

- V_{OUT} and I_{OUT} are the voltage
- the current measured at the output pins of the differential amplifier as if they were single ended amplifiers
- V_S is the total supply voltage

3. Calculate the total RMS power:

$$P_T = P_{AMP} + P_D \quad (3)$$

The maximum power that the LMH6554 package can dissipate at a given temperature can be derived with the following equation:

$$P_{MAX} = (150° - T_{AMB})/\ \theta_{JA} \quad (4)$$

where

- T_{AMB} = Ambient temperature (°C)
- θ_{JA} = Thermal resistance, from junction to ambient, for a given package (°C/W)
- For the 14 lead UQFN package, θ_{JA} is 60°C/W

Note

If V_{CM} is not 0V then there will be quiescent current flowing in the feedback network. This current should be included in the thermal calculations and added into the quiescent power dissipation of the amplifier.

7.4.4 ESD Protection

The LMH6554 is protected against electrostatic discharge (ESD) on all pins. The LMH6554 can survive 2000 V Human Body model and 250 V Machine model events. Under normal operation the ESD diodes have no affect on circuit performance. There are occasions when the ESD diodes are evident. If the LMH6554 is driven by a large signal while the device is powered down the ESD diodes conducts. The current that flows through the ESD diodes either exits the chip through the supply pins or flows through the device, hence powering up a chip with a large signal applied to the input pins is possible to. Using the shutdown mode is one way to conserve power and still prevent unexpected operation.

8 Device and Documentation Support

8.1 Device Support

8.2 Documentation Support

8.2.1 Related Documentation

See LMH6554 Product Folder for evaluation board availability and ordering information.

8.3 Trademarks

All trademarks are the property of their respective owners.

9 Revision History

Changes from Revision P (January 2015) to Revision Q (March 2026) — **Page**

- Updated supply current, disabled max value from 570µA to 770µA in *Electrical Characteristics: +5 V* 4
- Updated supply current, disabled max value at extreme temperature from 600µA to 850µA in *Electrical Characteristics: +5 V* 4

Changes from Revision O (March 2013) to Revision P (January 2015) — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section............ 1

Changes from Revision N (March 2013) to Revision O (March 2013) — **Page**

- Changed layout of National Data Sheet to TI format............22

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMH6554LE/NOPB	Active	Production	UQFN (NHJ) | 14	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	AJA
LMH6554LE/NOPB.A	Active	Production	UQFN (NHJ) | 14	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	AJA
LMH6554LEE/NOPB	Active	Production	UQFN (NHJ) | 14	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	AJA
LMH6554LEE/NOPB.A	Active	Production	UQFN (NHJ) | 14	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	AJA
LMH6554LEX/NOPB	Active	Production	UQFN (NHJ) | 14	4500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	AJA
LMH6554LEX/NOPB.A	Active	Production	UQFN (NHJ) | 14	4500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	AJA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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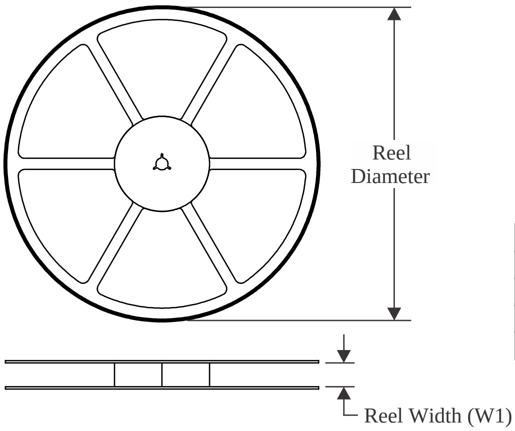
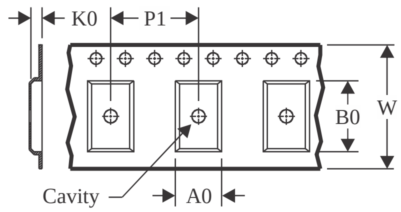
TAPE AND REEL INFORMATION

REEL DIMENSIONS

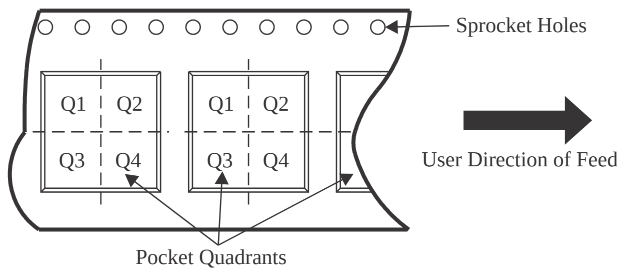


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

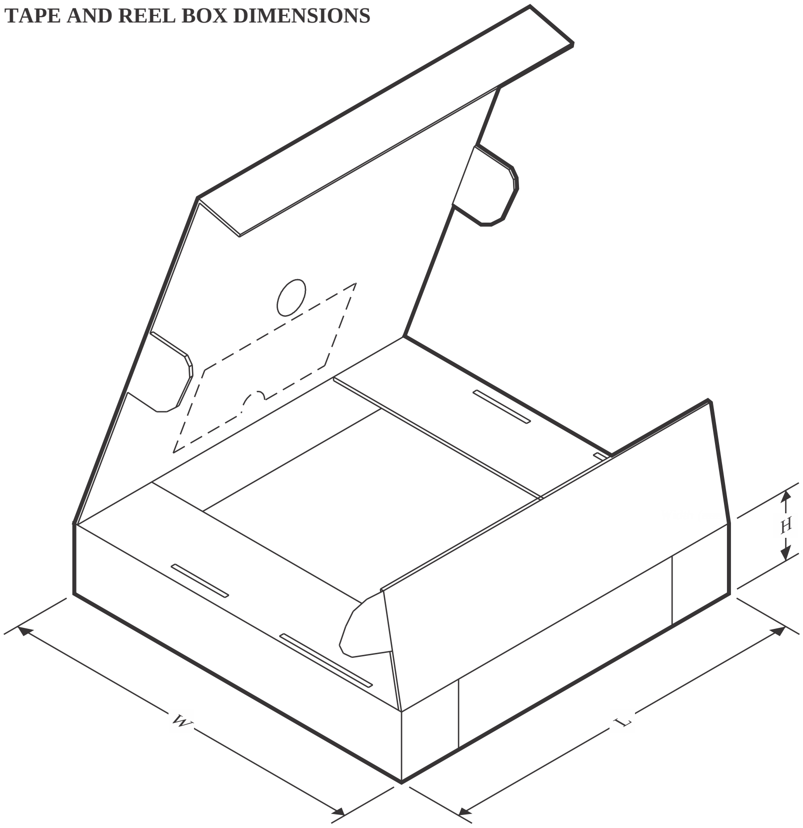
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6554LE/NOPB	UQFN	NHJ	14	1000	177.8	12.4	2.8	2.8	1.0	8.0	12.0	Q1
LMH6554LEE/NOPB	UQFN	NHJ	14	250	177.8	12.4	2.8	2.8	1.0	8.0	12.0	Q1
LMH6554LEX/NOPB	UQFN	NHJ	14	4500	330.0	12.4	2.8	2.8	1.0	8.0	12.0	Q1

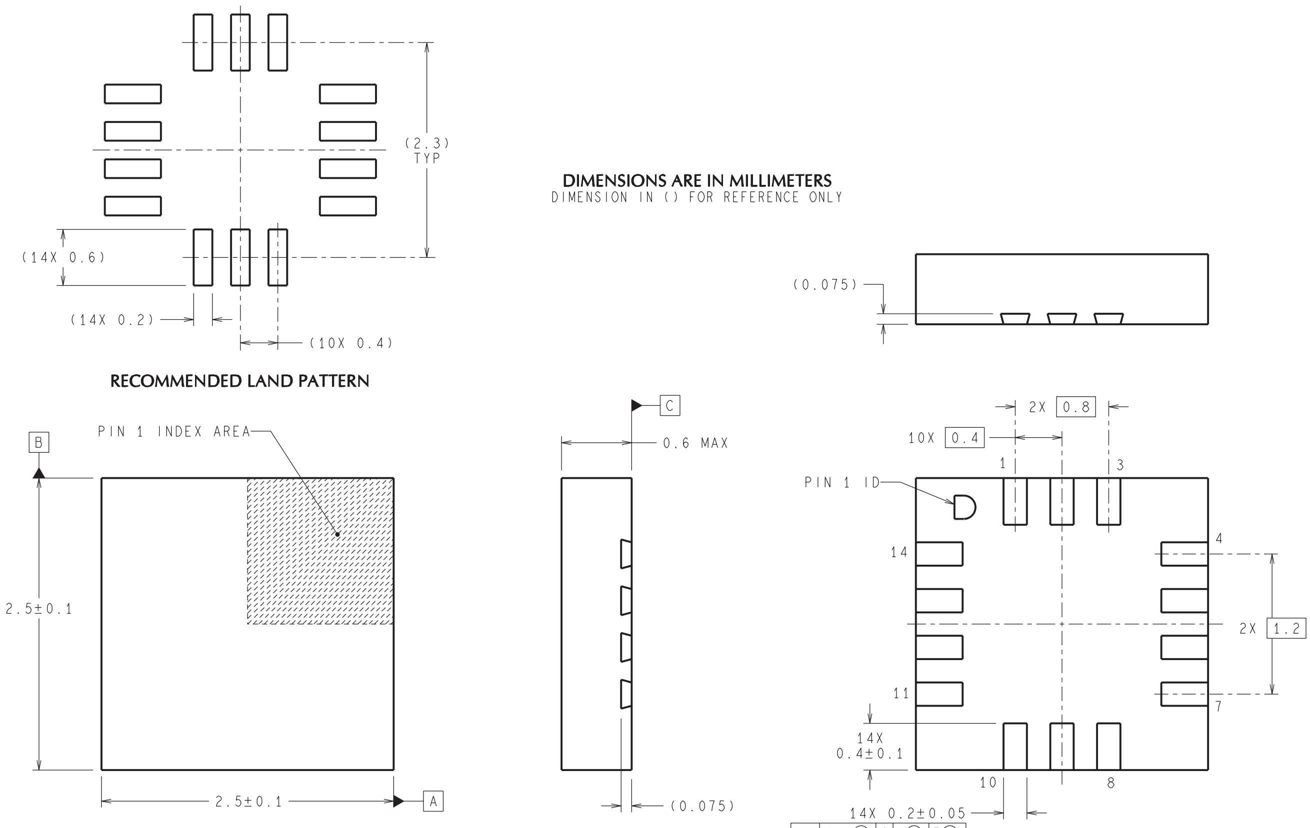
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6554LE/NOPB	UQFN	NHJ	14	1000	208.0	191.0	35.0
LMH6554LEE/NOPB	UQFN	NHJ	14	250	208.0	191.0	35.0
LMH6554LEX/NOPB	UQFN	NHJ	14	4500	356.0	356.0	36.0

NHJ0014A



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