# LMK5C33216 Ultra-Low Jitter Clock Synchronizer with JESD204B for Wireless Communications with BAW

## 1 Features

- BAW APLL with 40 fs RMS jitter at 491.52 MHz
- Three high-performance digital phase locked loops (DPLLs) with paired analog phase locked loops (APLLs)
  - Programmable DPLL loop bandwidth from 0.01 Hz to 4 kHz
  - -116 dBc/Hz at 100 Hz offset at 122.88 MHz DPLL TDC noise with ≥ 20 MHz TDC rate
- Two differential or single-ended DPLL inputs
  - 1 Hz to 800 MHz differential
  - Hitless switching with phase cancellation and/or phase slew control
  - Priority based reference selection
- 16 outputs with programmable format
  - 1000 MHz LVPECL/LVDS/HSDS
  - 3000 MHz CML on OUT4 and OUT6
  - 200 MHz LVCMOS on OUT0 and OUT1
- Single 3.3-V supply with internal LDOs
- $I^2C$ or 3-wire/4-wire SPI interface
- Requires single XO/TCXO/OCXO
- 40-bit DPLL or APLL DCO, < 1 ppt
- Holdover with phase build out upon exit
- Zero delay mode with programmable delay
- User programmable EEPROM
- Supports 105 °C PCB temperature

## 2 Applications

- 4G and 5G Wireless Networks
- Base Band Unit (BBU)
- Active Antenna Unit (AAU)
- Remote Radio Unit (RRU)
- Network Switch (5G HUB)
- Small Cell

## 3 Description

The LMK5C33216 is a high-performance network clock generator, synchronizer, and jitter attenuator with advanced reference clock selection and hitless switching capabilities designed to meet the stringent requirements of communications infrastructure applications.

The LMK5C33216 integrates 3 DPLLs with programmable loop bandwidth and no external loop filters, maximizing flexibility and ease of use. Each DPLL phase locks a paired APLL to a DPLL reference input. The APLL reference determines the long term frequency accuracy.

The 3 APLLs may operate independent of their paired DPLL and be cascaded from another APLL to provide programmable frequency translation. APLL3 features ultra high performance PLL with TI's proprietary Bulk Acoustic Wave (BAW) VCBO technology and can generate output clocks with 40-fs RMS jitter independent of the jitter and frequency of the XO and reference inputs. APLL1 and APLL2 provide options for additional frequency domains.

The device is fully programmable through $I^2C$ or SPI interface. The onboard EEPROM can be used to customize system start-up clocks.

**Device Information** (1)

| PART NUMBER | IN | OUT | PACKAGE | BODY SIZE (NOM) |
|---|---|---|---|---|
| LMK5C33216 | 2 | 16 | VQFN (64) | 9.00 mm × 9.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

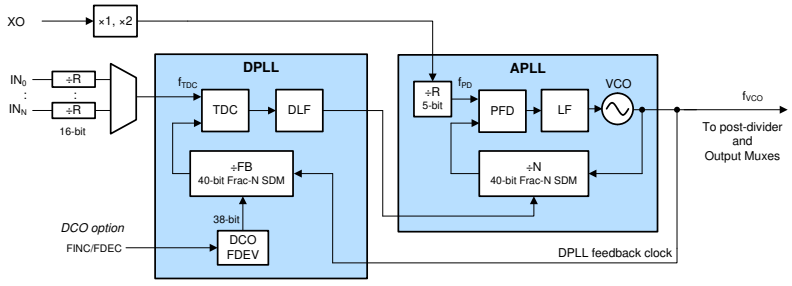



**Figure 3-1. Block Diagram of Paired DPLL and APLL**

# Table of Contents



## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (December 2020) to Revision B (March 2021) | Page |
|---|---|
| • Changed *Functional Block Diagram* APLL1 and APLL2 VCO frequency ranges | 24 |
| • Changed *DPLL Mode* section and changed section title to *DPLL* | 26 |
| • Changed *DPLL Independent Mode* section and changed section title to *Independent DPLL Operation* | 27 |
| • Changed phrase "determined by the DPLL bandwidth" to "determined by the filtering of the DPLL bandwidth" in *Hitless Switching* | 41 |
| • Removed the LOR amplitude detector (LOR_AMP) from Figure 9-22 | 48 |
| • Changed $DEN_{APLL}$ equation definition from: programmable $2^{24}$ to: programmable 1 to $2^{24}$ | 50 |
| • Changed open collector CML output modes from: up to 3 GHz to: up to 2975 MHz | 55 |
| • Added SYNC_EN = 1 to the SYNC group requirements in *Output Synchronization (SYNC)* | 57 |
| • Changed SYNC_GPIO_EN = 1 to: GPIOx_MODE = 31 for the SYNC event | 57 |
| • Changed Table 9-5 for reduced APLL2 frequency | 58 |
| • Changed Figure 9-31 with proper ToD counter register address location | 58 |
| • Changed *GPIO Pin as a Trigger Source* section title to *GPIO Pin as a ToD Trigger Source* | 61 |
| • Added statement on changing input validation registers while in operation | 63 |
| • Added DPLLx_EN and APLLx_NUM_STAT information to *APLL Frequency Control* | 70 |
| • Changed txt format to text format in *Register Map Generation* | 74 |

| Changes from Revision * (November 2020) to Revision A (December 2020) | Page |
|---|---|
| • Changed device status from Advanced Information to Production Data | 1 |

# 5 Device Comparison

**Table 5-1. Device Comparison Table**

| ORIGINAL PART NUMBER | NEW PART NUMBER | IN | OUT |
|---|---|---|---|
| LMK5C33216 | LMK5C33216 | 2 | 16 |

# 6 Pin Configuration and Functions

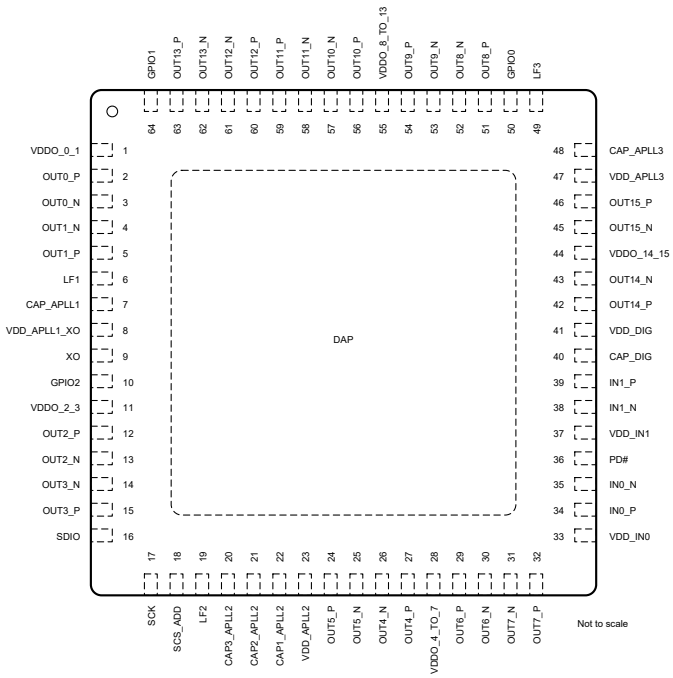



**Figure 6-1. LMK5C33216 RGC Package 64-Pin VQFN Top View**

**Table 6-1. LMK5C33216 Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| **POWER** | | | |
| VDDO_0_1 | 1 | P | Power supply for OUT0 and OUT1 |
| VDD_APLL1_XO | 8 | P | Power supply for XO and APLL1 |
| VDDO_2_3 | 11 | P | Power supply for OUT2 and OUT3 |
| VDD_APLL2 | 23 | P | Power supply for APLL2 |
| VDDO_4_TO_7 | 28 | P | Power supply for OUT4 to OUT7 |
| VDD_IN0 | 33 | P | Power supply for IN0 DPLL reference |
| VDD_IN1 | 37 | P | Power supply for IN1 input port |
| VDD_DIG | 41 | P | Power supply for digital |
| VDDO_14_15 | 44 | P | Power supply for OUT14 and OUT15 |
| VDD_APLL3 | 47 | P | Power supply for APLL3 |
| VDDO_8_TO_13 | 55 | P | Power supply for OUT8 to OUT13 |
| DAP | N/A | G | Ground |
| **CORE BLOCKS** [2] | | | |

**Table 6-1. LMK5C33216 Pin Functions (continued)**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| LF1 | 6 | A | External loop filter cap for APLL1 (100 nF) |
| CAP_APLL1 | 7 | A | LDO bypass capacitor for APLL1 VCO (10 µF) |
| LF2 | 19 | A | External loop filter cap for APLL2 (100 nF) |
| CAP3_APLL2 | 20 | A | Internal bias bypass capacitor for APLL2 VCO (10 µF) |
| CAP2_APLL2 | 21 | A | Internal bias bypass capacitor for APLL2 VCO (10 µF) |
| CAP1_APLL2 | 22 | A | LDO bypass capacitor for APLL2 VCO (10 µF) |
| CAP_DIG | 40 | A | LDO bypass capacitor for Digital Core Logic (100 nF) |
| CAP_APLL3 | 48 | A | Internal bias bypass capacitor for APLL3 (10 µF) |
| LF3 | 49 | A | External loop filter cap for APLL3 (470 nF) |
| **INPUT BLOCKS** | | | |
| XO | 9 | I | XO/TCXO/OCXO input pin |
| IN0_P | 34 | I | Reference to DPLLx or buffered to OUT0 or OUT1 |
| IN0_N | 35 | I | |
| IN1_N | 38 | I | Reference to DPLLx or buffered to OUT0 or OUT1 |
| IN1_P | 39 | I | |
| **OUTPUT BLOCKS** | | | |
| OUT0_P | 2 | O | Clock Output 0. Sources from all DPLL references, XO, all VCO post-dividers. Support SYSREF output. Programmable formats: LVPECL, LVDS, HSDS, 1.8-V LVCMOS, or 2.65-V LVCMOS. |
| OUT0_N | 3 | O | |
| OUT1_N | 4 | O | Clock Output 1. Sources from all DPLL references, XO, all VCO post-dividers. Support SYSREF output. Programmable formats: LVPECL, LVDS, HSDS, 1.8-V LVCMOS, or 2.65-V LVCMOS. |
| OUT1_P | 5 | O | |
| OUT2_P | 12 | O | Clock Output 2. Sources from VCO1 and VCO2. No SYSREF output. Programmable formats: LVPECL, LVDS, or HSDS. |
| OUT2_N | 13 | O | |
| OUT3_N | 14 | O | Clock Output 3. Sources from VCO1 and VCO2. No SYSREF output. Programmable formats: LVPECL, LVDS, or HSDS. |
| OUT3_P | 15 | O | |
| OUT5_P | 24 | O | Clock Output 5. Sources from VCO2 and VCO3. Support SYSREF output. Programmable formats: LVPECL, LVDS, or HSDS. |
| OUT5_N | 25 | O | |
| OUT4_N | 26 | O | Clock Output 4. Sources from VCO2 and VCO3. Support SYSREF output. Programmable formats: LVPECL, LVDS, HSDS, or CML. High-frequency output with channel divider bypass in open-collector CML format. |
| OUT4_P | 27 | O | |
| OUT6_P | 29 | O | Clock Output 6. Sources from VCO2 and VCO3. Support SYSREF output. Programmable formats: LVPECL, LVDS, HSDS, or CML. High-frequency output with channel divider bypass in open-collector CML format. |
| OUT6_N | 30 | O | |
| OUT7_N | 31 | O | Clock Output 7. Sources from VCO2 and VCO3. Support SYSREF output. Programmable formats: LVPECL, LVDS, or HSDS. |
| OUT7_P | 32 | O | |
| OUT14_P | 42 | O | Clock Output 14. Sources from VCO1, VCO2, and VCO3. No SYSREF output. Programmable formats: LVPECL, LVDS, or HSDS. |
| OUT14_N | 43 | O | |
| OUT15_N | 45 | O | Clock Output 15. Sources from VCO1, VCO2, and VCO3. No SYSREF output. Programmable formats: LVPECL, LVDS, or HSDS. |
| OUT15_P | 46 | O | |
| OUT8_P | 51 | O | Clock Output 8. Sources from VCO2 and VCO3. Support SYSREF output. Programmable formats: LVPECL, LVDS, or HSDS. |
| OUT8_N | 52 | O | |
| OUT9_N | 53 | O | Clock Output 9. Sources from VCO2 and VCO3. Support SYSREF output. Programmable formats: LVPECL, LVDS, or HSDS. |
| OUT9_P | 54 | O | |
| OUT10_P | 56 | O | Clock Output 10. Sources from VCO2 and VCO3. Support SYSREF output. Programmable formats: LVPECL, LVDS, or HSDS. |
| OUT10_N | 57 | O | |

**Table 6-1. LMK5C33216 Pin Functions (continued)**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| OUT11_N | 58 | O | Clock Output 11. Sources from VCO2 and VCO3. Support SYSREF output. Programmable formats: LVPECL, LVDS, or HSDS. |
| OUT11_P | 59 | O | |
| OUT12_P | 60 | O | Clock Output 12. Sources from VCO2 and VCO3. Support SYSREF output. Programmable formats: LVPECL, LVDS, or HSDS. |
| OUT12_N | 61 | O | |
| OUT13_N | 62 | O | Clock Output 13. Sources from VCO2 and VCO3. Support SYSREF output. Programmable formats: LVPECL, LVDS, or HSDS. |
| OUT13_P | 63 | O | |
| **LOGIC CONTROL/STATUS** | | | |
| GPIO2(3) | 10 | I/O, S | POR: ROM page select<br>Normal Operation: GPIO input or output (see description) |
| SDIO(4) | 16 | I/O | SPI or $I^2C$ Data (SDA) |
| SCK(4) | 17 | I | SPI or $I^2C$ Clock (SCL) |
| SCS_ADD(3) | 18 | I, S | SPI Chip Select (2-state) or POR: $I^2C$ address select, LSB (3-state) |
| PD# | 36 | I | Device power down (Active low), internal 200-kΩ pullup to $V_{CC}$ |
| GPIO0(3) | 50 | I/O, S | POR: ROM page select<br>Normal Operation: GPIO input or output (see description) |
| GPIO1(3) | 64 | I/O, S | POR: $I^2C$ or SPI select<br>Normal Operation: GPIO input or output (see description) |

(1) P = Power, G = Ground, I = Input, O = Output, I/O = Input or Output, A = Analog, S = Configuration.

(2) Do not apply external stimulus to core pins. These performance critical pins are not designed to meet normal latch up testing compliance levels. For best filtering performance, capacitors should be placed close to the IC.

(3) When 3 level mode is enabled during power supply ramp or when PD# is LOW: internal voltage divider of 555 kΩ to $V_{CC}$ and 201 kΩ to GND. When 2 level input mode is enabled: internal 408-kΩ pulldown to GND.

(4) 670-kΩ pullup to internal 2.6-V LDO.

# 7 Specifications

## 7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| VDD(2) | Core supply voltages | -0.3 | 3.6 | V |
| VDDO(3) | Output supply voltages | -0.3 | 3.6 | V |
| $V_{IN}$ | Input voltage range for clock and logic inputs | -0.3 | VDD+0.3 | V |
| $V_{OUT\_LOGIC}$ | Output voltage range for logic outputs | -0.3 | VDD+0.3 | V |
| $V_{OUT}$ | Output voltage range for clock outputs | -0.3 | VDDO+0.3 | V |
| $T_j$ | Junction temperature | | 150 | °C |
| $T_{stg}$ | Storage temperature range | -65 | 150 | °C |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) VDD refers to all core supply pins or voltages. All VDD core supplies should be powered-on before the PD# is pulled high to trigger the internal power-on reset (POR).

(3) VDDO refers to all output supply pins or voltages. VDDO_x refers to the output supply for a specific output channel, where x denotes the channel index.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±750 | |
| | | Machine model (MM), per JEDEC specification JESD22-A115-A, all pins | ±200 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VDD(1) | Core supply voltages | 3.135 | 3.3 | 3.465 | V |
| VDDO_x(2) | Output supply voltages(3) | 3.135 | 3.3 | 3.465 | V |
| $V_{IN}$ | Input voltage range for clock and logic inputs | 0 | | 3.465 | V |
| $T_J$ | Junction temperature | | | 135 | °C |
| $T_{CONT-LOCK}$ | Continuous lock over temperature - no VCO recalibration needed | | | 125 | °C |
| $t_{VDD}$ | Power supply ramp time(4) | 0.01 | | 100 | ms |

(1) VDD refers to all core supply pins or voltages. All VDD core supplies should be powered-on before internal power-on reset (POR).

(2) VDDO refers to all output supply pins or voltages. VDDO_x refers to the output supply for a specific output channel, where x denotes the channel index.

(3) CMOS output voltage levels are determined by internal programming of the CMOS output LDO to support either 1.8 V or 2.65 V.

(4) Time for VDD to ramp monotonically above 2.7 V for proper internal power-on reset. For slower or non-monotonic VDD ramp, hold PD# low until after VDD voltages are valid.

## 7.4 Thermal Information

| THERMAL METRIC(1) (2) (3) | | LMK5C33216 RGC (VQFN) 64 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 21.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 11.1 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 6.5 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 0.8 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.3 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 6.3 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

(2) The thermal information is based on a 10-layer 200 mm x 250 mm board with 49 thermal vias (7 x 7 pattern, 0.3 mm holes).

(3) $\Psi_{JB}$ can allow the system designer to measure the board temperature ($T_{PCB}$) with a fine-gauge thermocouple and back-calculate the device junction temperature, $T_J = T_{PCB} + (\Psi_{JB} \times \text{Power})$. Measurement of $\Psi_{JB}$ is defined by JESD51-6.

## 7.5 Electrical Characteristics

Over Recommended Operating Conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $IDD_{PD\#}$ | Total Supply Current (all supply pins, 3.3 V) | Device powered-down (PD# pin held low) | | 132 | | mA |
| $IDD_{CFG1}$ | Total Supply Current (all supply pins, 3.3 V) | DPLL3 with 10 MHz input. APLL2 = 5625 MHz, APLL3 = 2457.6 MHz. Outputs: 4x 491.52 MHz HSDS. 4x 7.68 MHz HSDS SYSREF. 2x 312.5 MHz LVDS. | | 875 | 1050 | mA |

## 7.5 Electrical Characteristics (continued)

Over Recommended Operating Conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Reference Input Characteristics (INx)** | | | | | | |
| $f_{IN}$ | Input frequency range | INx; Single Ended - LVCMOS input | 1E-6 | | 200 | MHz |
| | | INx; Differential input | 5 | | 800 | |
| $V_{IH}$ | LVCMOS Input high voltage | DC-coupled input mode | 1.2 | | VDD + 0.3 | V |
| $V_{IL}$ | LVCMOS Input low voltage | | | | 0.5 | V |
| $V_{IN-SE}$ | Single-ended input voltage swing | AC-coupled input mode | 0.4 | | 2 | $V_{pp}$ |
| $V_{IN-DIFF}$ | Differential input voltage swing, peak-peak ($\|V_P - V_N\|$ x 2) | Differential input | 0.4 | | 2 | $V_{pp}$ |
| $V_{ICM}$ | Input Common Mode | Differential input | 0.1 | | 2 | V |
| dV/dt | Input slew rate | Single-ended input, non-driven input tied to GND | 0.2 | 0.5 | | V/ns |
| | | Differential input | 0.2 | 0.5 | | V/ns |
| IDC | Input Clock Duty Cycle | Non 1 PPS signal | 40 | | 60 | % |
| $t_{PULSE-1PPS}$ | 1PPS pulse width for input | 1 PPS signal | 100 | | | ns |
| $I_{IN-DC}$ | DC input leakage current | Single pin INx_P or INx_N, 50-Ω and 100-Ω internal terminations disabled, AC coupled mode enabled or disabled | -350 | | 350 | µA |
| **XO/TCXO Input Characteristics (XO)** | | | | | | |
| $f_{CLK}$ | Input frequency range | | 10 | | 100 | MHz |
| $V_{IH}$ | LVCMOS Input high voltage | DC-coupled input mode | 1.4 | | VDD + 0.3 | V |
| $V_{IL}$ | LVCMOS Input low voltage | | | | 0.8 | V |
| $V_{IN-SE}$ | Single-ended input voltage swing | AC-coupled input mode | 0.4 | | VDD + 0.3 | $V_{pp}$ |
| dV/dt | Input slew rate | | 0.2 | 0.5 | | V/ns |
| IDC | Input duty cycle | | 40 | | 60 | % |
| $I_{IN-DC}$ | DC Input leakage current | Single pin XO_P, 50-Ω and 100-Ω internal terminations disabled | -350 | | 350 | µA |
| **APLL/VCO Characteristics** | | | | | | |
| $f_{VCO1}$ | VCO1 Frequency range | | 4.8 | | 5.35 | GHz |
| $f_{VCO2}$ | VCO2 Frequency range | | 5.6 | | 5.95 | GHz |
| $f_{VCO3}$ | VCO3 Frequency range | | 2.457477120 | 2.4576 | 2.457722880 | GHz |
| **LVDS Output Characteristics (OUTx)** | | | | | | |
| $f_{OUT}$ | Maximum output frequency(2) | | 1000 | | | MHz |
| $V_{OD}$ | Output voltage swing ($\|V_{OH} - V_{OL}\|$) | OUT_x_AMP = 0, $V_{OS}$ = 1.2 V | | 300 | | mV |
| | | OUT_x_AMP = 1, $V_{OS}$ = 1.2 V | | 400 | | mV |
| | | OUT_x_AMP = 2, $V_{OS}$ = 1.2 V | | 500 | | mV |
| | | OUT_x_AMP = 3, $V_{OS}$ 1.2 V | | 600 | | mV |
| $V_{OUT-DIFF}$ | Differential output voltage swing, peak-to-peak | | | 2×$V_{OD}$ | | V |

## 7.5 Electrical Characteristics (continued)

Over Recommended Operating Conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OS}$ | Output common mode | OUT_x_AMP = 1, DC shift setting 2 | | 0.7 | | V |
| | | OUT_x_AMP = 1, DC shift setting 4 | | 0.8 | | V |
| | | OUT_x_AMP = 1, DC shift setting 6 | | 1.0 | | V |
| | | OUT_x_AMP = 1, DC shift setting 8 | | 1.2 | | V |
| | | OUT_x_AMP = 1, DC shift setting 10 | | 1.4 | | V |
| | | OUT_x_AMP = 1, DC shift setting 12 | | 1.6 | | V |
| $t_{SK}$ | Output-to-output skew, same group(4) | Same post divider, output divide values, and output format | | | 50 | ps |
| $t_{SK\_GRP}$ | Output-to-output skew, between groups(4) | Same post divider, output divide values, and output format. Not including OUT14 and OUT15. | | | 80 | ps |
| | | Same post divider, output divide values, and output format | | | 150 | ps |
| $t_R/t_F$ | Output rise/fall time | 20% to 80%, < 500 MHz | | 150 | 300 | ps |
| | | ± 100 mV around center point | | 50 | 150 | ps |
| $PN_{FLOOR}$ | Output phase noise floor(3) ($f_{OFFSET}$ > 10 MHz) | 122.88 MHz | | -160 | | dBc/Hz |
| ODC | Output duty cycle(10) | | 45 | | 55 | % |
| **HSDS Output Characteristics (OUTx)** | | | | | | |
| $f_{OUT}$ | Maximum output frequency(2) | | 1000 | | | MHz |
| $V_{OD}$ | Output voltage swing ($\|V_{OH} - V_{OL}\|$) | OUT_x_AMP = 1, boost off, $V_{OS}$ = 1.2 V | | 400 | | mV |
| | | OUT_x_AMP = 2, boost on, $V_{OS}$ = 1.2 V | | 800 | | mV |
| | | OUT_x_AMP = 3, boost off, $V_{OS}$ = 1.2 V | | 600 | | mV |
| | | OUT_x_AMP = 2, boost on, $V_{OS}$ = 1.6 V | | 800 | | mV |
| | | OUT_x_AMP = 3, boost on, $V_{OS}$ = 1.2 V | | 850 | | mV |
| | | OUT_x_AMP = 3, boost on, $V_{OS}$ = 1.6 V | | 910 | | mV |
| $V_{OUT-DIFF}$ | Differential output voltage swing, peak-to-peak | | | $2\times V_{OD}$ | | V |
| $V_{OS}$ | Output common mode | OUT_x_AMP = 1, boost on, DC shift setting 2 | | 0.8 | | V |
| | | OUT_x_AMP = 1, boost on, DC shift setting 4 | | 1.0 | | V |
| | | OUT_x_AMP = 1, boost on, DC shift setting 6 | | 1.2 | | V |
| | | OUT_x_AMP = 1, boost on, DC shift setting 8 | | 1.4 | | V |
| | | OUT_x_AMP = 1, boost on, DC shift setting 10 | | 1.6 | | V |
| $t_{SK}$ | Output-to-output skew, same group(4) | Same post divider, output divide values, and output format | | | 50 | ps |

## 7.5 Electrical Characteristics (continued)

Over Recommended Operating Conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{SK\_GRP}$ | Output-to-output skew, between groups[4] | Same post divider, output divide values, and output format. Not including OUT14 and OUT15. | | | 80 | ps |
| | | Same post divider, output divide values, and output format. | | | 150 | ps |
| $t_R/t_F$ | Output rise/fall time | 20% to 80%, < 500 MHz | | 130 | 300 | ps |
| | | ± 100 mV around center point | | 50 | 120 | ps |
| $PN_{FLOOR}$ | Output phase noise floor[3] ($f_{OFFSET}$ > 10 MHz) | 122.88 MHz | | -162 | | dBc/Hz |
| ODC | Output duty cycle[10] | | 45 | | 55 | % |
| **LVPECL Output Characteristics (OUTx)** | | | | | | |
| $f_{OUT}$ | Maximum output frequency[2] | | 1000 | | | MHz |
| $V_{OD}$ | Output voltage swing ($\|V_{OH} - V_{OL}\|$) | OUT_x_AMP = 0, $V_{OS}$ = 1.2 V | | 450 | | mV |
| | | OUT_x_AMP = 1, $V_{OS}$ = 1.2 V | | 600 | | mV |
| | | OUT_x_AMP = 2, $V_{OS}$ = 1.2 V | | 800 | | mV |
| | | OUT_x_AMP = 2, $V_{OS}$ = 1.6 V | | 700 | | mV |
| | | OUT_x_AMP = 3, $V_{OS}$ = 1.2 V | | 930 | | mV |
| | | OUT_x_AMP = 3, $V_{OS}$ = 1.6 V | | 840 | | mV |
| $V_{OUT-DIFF}$ | Differential output voltage swing, peak-to-peak | | | $2\times V_{OD}$ | | V |
| $V_{OS}$ | Output common mode | OUT_x_AMP = 1, DC shift setting 2 | | 0.7 | | V |
| | | OUT_x_AMP = 1, DC shift setting 4 | | 0.8 | | V |
| | | OUT_x_AMP = 1, DC shift setting 6 | | 1.0 | | V |
| | | OUT_x_AMP = 1, DC shift setting 8 | | 1.2 | | V |
| | | OUT_x_AMP = 1, DC shift setting 10 | | 1.4 | | V |
| | | OUT_x_AMP = 1, DC shift setting 12 | | 1.5 | | V |
| $t_{SK}$ | Output-to-output skew, same group[4] | Same post divider, output divide values, and output format | | | 50 | ps |
| $t_{SK\_GRP}$ | Output-to-output skew, between groups[4] | Same post divider, output divide values, and output format | | | 80 | ps |
| | | Same post divider, output divide values, and output format. Not including OUT14 and OUT15. | | | 150 | ps |
| $t_R/t_F$ | Output rise/fall time | 20% to 80% | | 150 | 300 | ps |
| | | ± 100 mV around center point | | | 200 | ps |
| $PN_{FLOOR}$ | Output phase noise floor[3] ($f_{OFFSET}$ > 10 MHz) | 122.88 MHz | | -162 | | dBc/Hz |
| ODC | Output duty cycle[10] | | 45 | | 55 | % |

## 7.5 Electrical Characteristics (continued)

Over Recommended Operating Conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **CML Open Collector Output Characteristics (OUTx)** | | | | | | |
| $f_{OUT}$ | Output frequency(2) | OUT4 or OUT6 CML open collector outputs | | | 3000 | MHz |
| $V_{OD}$ | Output voltage swing ($\|V_{OH} - V_{OL}\|$) | Normal swing, OUT_x_AMP = 1, 2949.12 MHz | 400 | 600 | | mV |
| $V_{OD}$ | Output voltage swing ($\|V_{OH} - V_{OL}\|$) | High swing, OUT_x_AMP = 2, 2949.12 MHz | 600 | 800 | | mV |
| $V_{OUT-DIFF}$ | Differential output voltage swing, peak-to-peak | | | $2\times V_{OD}$ | | $V_{pp}$ |
| $t_{SK}$ | Output-to-output skew | Same post divider, output divide values, and output type | | | 50 | ps |
| $t_R/t_F$ | Output rise/fall time | 20% to 80%, 2949.12 MHz | | 150 | 300 | ps |
| | | ± 100 mV around center point, 2949.12 MHz | | 25 | 100 | ps |
| $PN_{FLOOR}$ | Output duty cycle(10) | 2949.12 MHz | | -156 | | dBc/Hz |
| ODC | Output duty cycle | | 45 | | 55 | % |

## 7.5 Electrical Characteristics (continued)

Over Recommended Operating Conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **1.8-V LVCMOS Output Characteristics (OUT0/1)** | | | | | | |
| $f_{OUT}$ | Maximum output frequency | | 200 | | | MHz |
| $V_{OH}$ | Output high voltage | $I_{OH}$ = 1 mA | 1.5 | | | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 1 mA | | | 0.2 | V |
| $I_{OH}$ | Output high current | $V_O$ = 0.9 V | | -18 | | mA |
| $I_{OL}$ | Output low current | | | 18 | | mA |
| $t_R/t_F$ | Output rise/fall time | 20% to 80% | | 150 | | ps |
| $t_{SK}$ | Output-to-output skew | Same post divider, output divide values, and output type | | | 100 | ps |
| | | Same post divider, output divide values, LVCMOS-to-DIFF | | | 1.5 | ns |
| $PN_{FLOOR}$ | Output phase noise floor ($f_{OFFSET}$ > 10 MHz) | 66.66 MHz | | -155 | | dBc/Hz |
| ODC | Output duty cycle(10) | | 45 | | 55 | % |
| $R_{OUT}$ | Output impedance | | | 50 | | Ω |

## 7.5 Electrical Characteristics (continued)

Over Recommended Operating Conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **2.65-V LVCMOS Output Characteristics (OUT0/1)** | | | | | | |
| $f_{OUT}$ | Maximum output frequency | | 200 | | | MHz |
| $V_{OH}$ | Output high voltage | $I_{OH}$ = 1 mA | 2.3 | | | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 1 mA | | | 0.2 | V |
| $I_{OH}$ | Output high current | $V_O$ = 1.25 V | | -25 | | mA |
| $I_{OL}$ | Output low current | | | 25 | | mA |
| $t_R/t_F$ | Output rise/fall time | 20% to 80% | | 150 | | ps |
| $t_{SK}$ | Output-to-output skew | Same post divider, output divide values, and output type | | | 100 | ps |
| | | Same post divider, output divide values, LVCMOS-to-DIFF | | | 1.5 | ns |
| $PN_{FLOOR}$ | Output phase noise floor ($f_{OFFSET}$ > 10 MHz) | 66.66 MHz | | -155 | | dBc/Hz |
| ODC | Output duty cycle(10) | | 45 | | 55 | % |
| $R_{OUT}$ | Output impedance | | | 50 | | Ω |
| **3-Level Logic Input Characteristics (GPIO0, GPIO1, GPIO2, SCS_ADD)** | | | | | | |
| $V_{IH}$ | Input high voltage | | 1.4 | | | V |
| $V_{IM}$ | Input mid voltage | | 0.6 | | 1 | V |
| $V_{IM}$ | Input mid voltage self-bias | Input floating with internal bias and PD# pulled low | 0.7 | | 0.9 | V |
| $V_{IL}$ | Input low voltage | | | | 0.4 | V |
| $I_{IH}$ | Input high current | $V_{IH}$ = VDD | -40 | | 40 | µA |
| $I_{IL}$ | Input low current | $V_{IL}$ = GND | -40 | | 40 | µA |
| $C_{IN}$ | Input capacitance | | | 2 | | pF |

## 7.5 Electrical Characteristics (continued)

Over Recommended Operating Conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **2-Level Logic Input Characteristics (PD#, SCK, SDIO, SCS_ADD; GPIO0, GPIO1 and GPIO2 after power up)** | | | | | | |
| $V_{IH}$ | Input high voltage | | 1.2 | | | V |
| $V_{IL}$ | Input low voltage | | | | 0.4 | V |
| $I_{IH}$ | Input high current | $V_{IH}$ = VDD, except PD# | -40 | | 40 | µA |
| $I_{IL}$ | Input low current | $V_{IL}$ = GND, except PD# | -40 | | 40 | µA |
| $C_{IN}$ | Input capacitance | | | 2 | | pF |
| **Logic Output Characteristics (GPIO0, GPIO1, GPIO2, SDIO)** | | | | | | |
| $V_{OH}$ | Output high voltage | $I_{OH}$ = 1 mA | 2.4 | | | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 1 mA | | | 0.4 | V |
| $t_R/t_F$ | Output rise/fall time | 20% to 80%, LVCMOS mode, 1 kΩ to GND | | 500 | | ps |
| **SPI Timing Requirements (SDIO, SCK, SCS_ADD)** | | | | | | |
| $f_{SCK}$ | SPI clock rate | | | | 20 | MHz |
| | SPI clock rate; during SRAM read and write operations | | | | 5 | MHz |
| $t_1$ | SCS to SCK setup time (start communication cycle) | | 10 | | | ns |
| $t_2$ | SDI to SCK setup time | | 10 | | | ns |
| $t_3$ | SDI to SCK hold time | | 10 | | | ns |
| $t_4$ | SCK high time | | 25 | | | ns |
| $t_5$ | SCK low time | | 25 | | | ns |
| $t_6$ | SCK to SDO valid read-back data | | | | 20 | ns |
| $t_7$ | SCS pulse width | | 20 | | | ns |
| $t_8$ | SCK to SCS setup time (end communication cycle) | | 10 | | | ns |
| **$I^2C$ Timing Requirements (SDIO, SCK)** | | | | | | |
| $V_{IH}$ | Input high voltage | | 1.2 | | | V |
| $V_{IL}$ | Input low voltage | | | | 0.5 | V |
| $I_{IH}$ | Input leakage | | -15 | | 15 | µA |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 3 mA | | | 0.3 | V |
| $f_{SCL}$ | $I^2C$ clock rate | Standard | | | 100 | kHz |
| | | Fast mode | | | 400 | |
| $t_{SU(START)}$ | START condition setup time | SCL high before SDA low | 0.6 | | | µs |
| $t_{H(START)}$ | START condition hold time | SCL low after SDA low | 0.6 | | | µs |
| $t_{W(SCLH)}$ | SCL pulse width high | | 0.6 | | | µs |
| $t_{W(SCLL)}$ | SCL pulse width low | | 1.3 | | | µs |
| $t_{SU(SDA)}$ | SDA setup time | | 100 | | | ns |
| $t_{H(SDA)}$ | SDA hold time | SDA valid after SCL low | 0 | | 0.9 | µs |
| $t_{R(IN)}$ | SDA/SCL input rise time | | | | 300 | ns |
| $t_{F(IN)}$ | SDA/SCL input fall time | | | | 300 | ns |
| $t_{F(OUT)}$ | SDA output fall time | $C_{BUS}$ ≤ 400 pF | | | 300 | ns |
| $t_{SU(STOP)}$ | STOP condition setup time | | 0.6 | | | µs |
| $t_{BUS}$ | Bus free time between STOP and START | | 1.3 | | | µs |

## 7.5 Electrical Characteristics (continued)

Over Recommended Operating Conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Other Characteristics** | | | | | | |
| $t_{PHO-VAR}$ | Input-to-output phase offset variation over PVT | Zero delay mode, RF clocks only, INx = 122.88 MHz, OUTx = 2949.12 MHz or 2457.6 MHz or 1474.56 MHz or 1228.8 MHz or 737.28 MHz or 614.4 MHz or 153.6 MHz or 122.88 MHz | -200 | | 200 | ps |
| $t_{ANA-DEL-ERR}$ | Analog delay error for any step setting(9) | VCBO = 2457.6 MHz, PLL3_PRI_DIV = ÷5, OUTx = 491.52 MHz, Analog Delay step = 32.8 ps | -16 | | 16 | ps |
| $t_{DIG-DEL}$ | Digital delay step size on device clock and SYSREF outputs | SYSREF analog delay off for half cycle steps and OUT_x_y_SR_CH_DIV_BYPASS = 1 | | ½ VCO post divider cycle | | |
| PSNR | Spur induced by power supply noise ($V_N$ = 50 mVpp)(5) (6) | Vcc = 3.3V, HSDS, LVDS, and LVPECL output | | -75 | | dBc |
| SPUR | Highest Spur level at 100 Hz to 40 MHz offset(6) (7) | $f_{OUTx}$ = 122.88 MHz from VCO3, VCO2 = 5625 MHz, and VCO1 = 5000 MHz | | -90 | | dBc |
| | Highest spur level within12 kHz to 40 MHz band(6) (7) | $f_{OUTx}$ = 122.88 MHz, AC-DIFF or LVDS (all outputs operating with differential level and no SYSREF) | | -75 | | dBc |
| **PLL Clock Output Performance Characteristics** | | | | | | |
| RJ1 | RMS phase jitter of DPLL1/ APLL1 (12 kHz to 20 MHz)(3) (7) | XO = 38.88 MHz, APLL1 = 5000 MHz or 5156.25 MHz, OUTx = 312.5 or 322.265625 MHz, all differential output types | | 200 | 250 | fs RMS |
| RJ2 | RMS phase jitter of DPLL2/ APLL2 (12 kHz to 20 MHz)(3) (7) | XO = 38.88 MHz, APLL2 = 5898.24 MHz or 5650 MHz, OUTx = 245.76 MHz or 312.5 MHz, all differential output types | | 120 | 180 | fs RMS |
| RJ3 | RMS phase jitter of DPLL3/ APLL3 (12 kHz to 20 MHz)(3) (7) | XO = 38.88 MHz, APLL3 = 2457.6 MHz, OUTx = 245.76 MHz, all differential output types | | 50 | 80 | fs RMS |
| RJ4 | RMS phase jitter of DPLL3/ APLL3 (12 kHz to 20 MHz)(3) (7) | XO = 38.88 MHz, APLL3 = 2457.6 MHz, OUTx = 491.52 MHz, all differential output types | | 40 | 70 | fs RMS |
| PN-APLL3 | Phase Noise of DPLL3/APLL3 at 800 kHz offset | 38.88 MHz XO, VCO3 = 2457.6 MHz, 2457.6 MHz CML output | | -147 | | dBc/Hz |
| $PN_{TDC}$ | Output close-in phase noise for DPLL1 and DPLL2 ($f_{OFFSET}$ = 100 Hz) | 122.88 MHz AC-DIFF or LVDS, TCXO = 38.88 MHz, $f_{TDC}$ > 20 MHz, DPLL-BW = 1 kHz | | -116 | | dBc/Hz |
| | Output close-in phase noise for DPLL3 ($f_{OFFSET}$ = 100 Hz) | 122.88 MHz AC-DIFF or LVDS, TCXO = 38.88 MHz, $f_{TDC}$ > 20 MHz, DPLL-BW = 1 kHz | | -110 | | dBc/Hz |
| BW | DPLL bandwidth range(8) | Programmed bandwidth setting | 0.01 | | 4000 | Hz |
| $J_{PK}$ | DPLL closed-loop jitter peaking(11) | $f_{IN}$ = 25 MHz, $f_{OUT}$ = 10 MHz, DPLL BW = 0.1 Hz or 10 Hz | | 0.1 | | dB |
| $J_{TOL}$ | Jitter tolerance | Compliant with G.8262 Options 1 and 2, Jitter modulation = 10 Hz, 25.78125 Gbps | | 6455 | | UI p-p |
| $t_{HITLESS}$ | Phase transient during hitless switch | Valid for a single switchover event between two clock inputs at the same frequency 122.88 MHz | -100 | | 100 | ps |

## 7.5 Electrical Characteristics (continued)

Over Recommended Operating Conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{HITLESS}$ | Frequency transient during hitless switch | Valid for a single switchover event between two clock inputs at the same frequency 122.88 MHz | -10 | | 10 | ppb |

(1) Total device current can be estimated by summing the individual IDD_x and IDDO_x per pin for all blocks enabled in a given configuration.
(2) An output frequency over the $f_{OUT}$ max spec is possible, but the output swing may be less than the $V_{OD}$ min spec.
(3) Any output clock except OUT2, OUT3, OUT14, or OUT15.
(4) Output groups are (OUT0 and 1), (OUT2 and 3), (OUT4 to 7), (OUT8 to 13) and (OUT14 and 15).
(5) PSNR is the single-sideband spur level (in dBc) measured when sinusoidal noise with amplitude $V_N$ and frequency between 100 kHz and 1 MHz is injected onto VDD and VDDO_x pins.
(6) $DJ_{SPUR}$ (ps pk-pk) = [2 × $10^{(dBc/20)}$ / (π × $f_{OUT}$) × 1E6], where dBc is the PSNR or SPUR level (in dBc) and $f_{OUT}$ is the output frequency (in MHz).
(7) Excludes output crosstalk and integer-boundary spurs.
(8) DPLL loop bandwidth must be less than 1/100 of TDC frequency and less than 1/10 of APLL loop bandwidth.
(9) Analog delay step size and worst case time error is a function of the input frequency to the SYSREF block and analog delay block configuration. Maximum analog delay error is half the analog delay step size.
(10) Parameter is specified for PLL outputs divided from either VCO domain.
(11) The TICS Pro software configures the closed-loop jitter peaking for 0.1 dB or less based on the programmed DPLL bandwidth setting.

## 7.6 Timing Diagrams

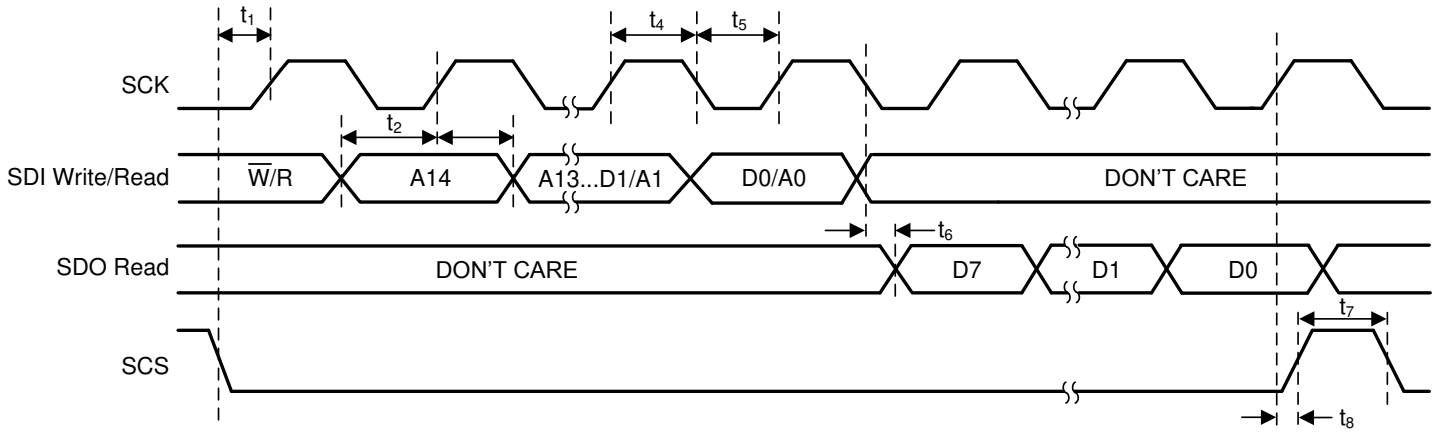



**Figure 7-1. SPI Write Timing Diagram**

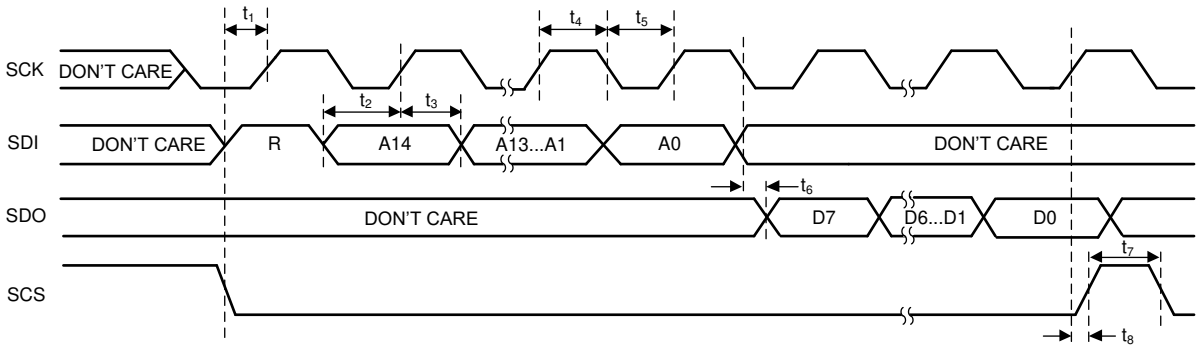



**Figure 7-2. SPI 4-Wire Read Timing Diagram**

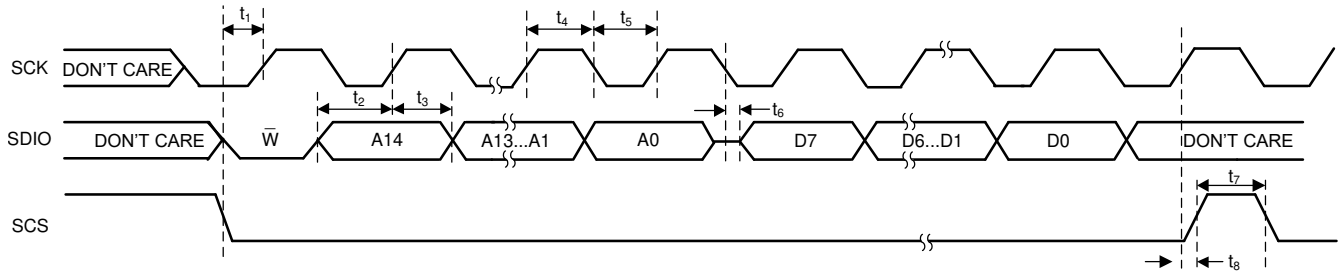



**Figure 7-3. SPI 3-Wire Read Timing Diagram**

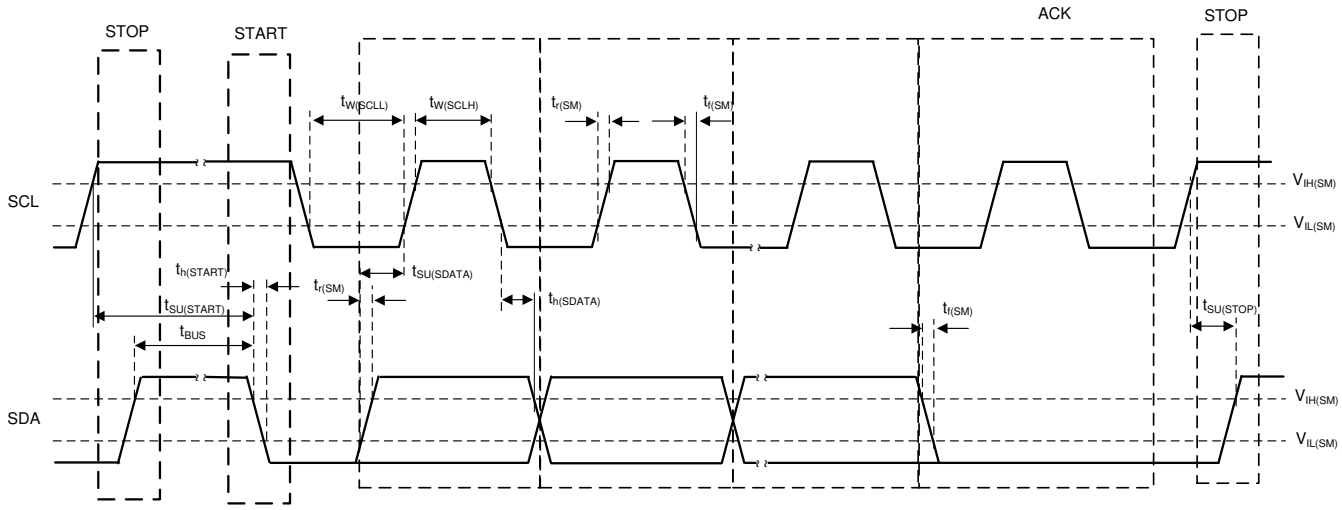



**Figure 7-4. I²C Timing Diagram**

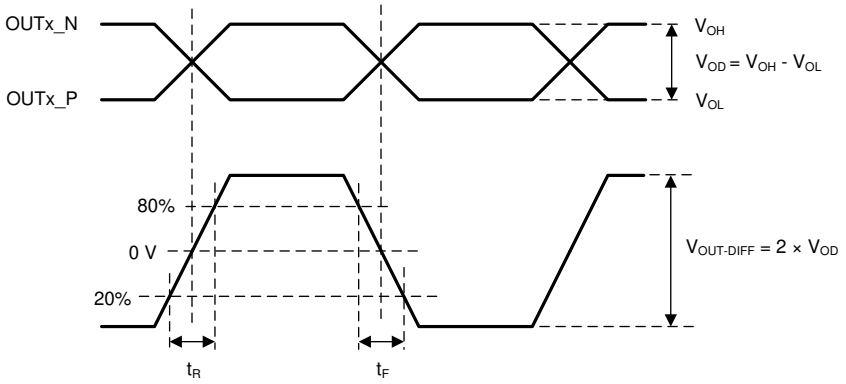



**Figure 7-5. Differential Output Voltage and Rise/Fall Time**

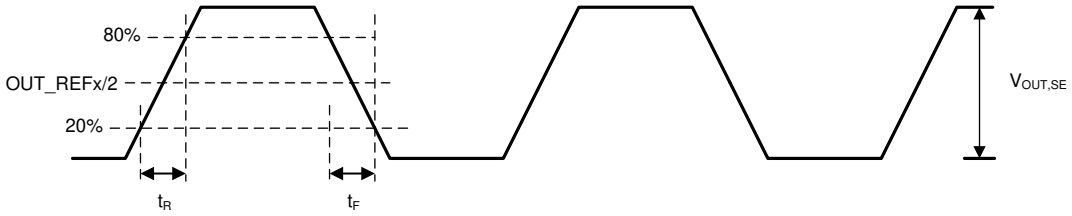



**Figure 7-6. Single-Ended Output Voltage and Rise/Fall Time**

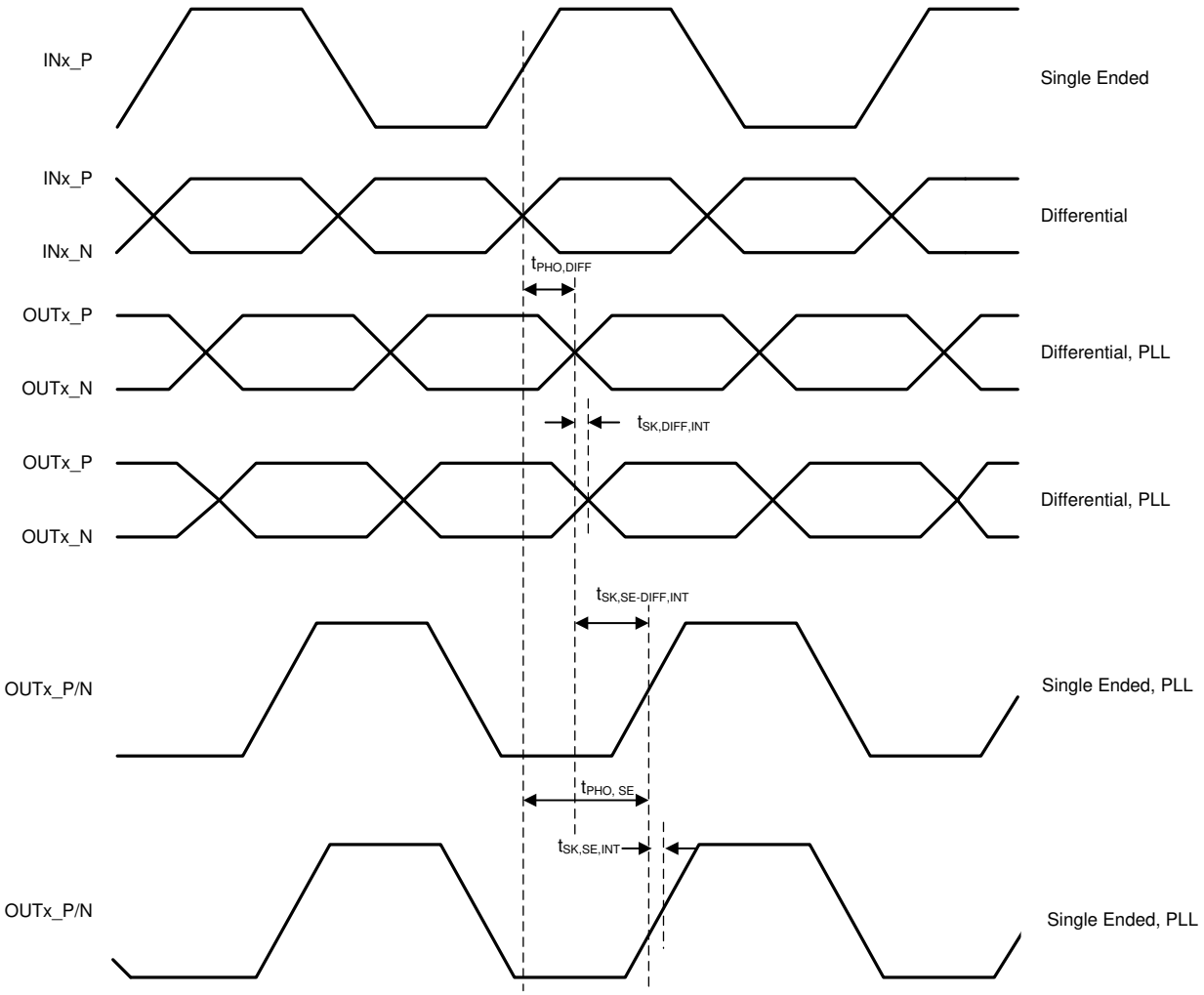



**Figure 7-7. Differential and Single-Ended Output Skew and Phase Offset**

# 8 Parameter Measurement Information

## 8.1 Differential Voltage Measurement Terminology

The differential voltage of a differential signal can be described by two different definitions, causing confusion when reading data sheets or communicating with other engineers. This section will address the measurement and description of a differential signal so that the reader is able to understand and distinguish between the two different definitions when used.

The first definition used to describe a differential signal is the absolute value of the voltage potential between the inverting and noninverting signal. The symbol for this first measurement is typically $V_{ID}$ or $V_{OD}$ depending on if an input or output voltage is being described.

The second definition used to describe a differential signal is to measure the potential of the noninverting signal with respect to the inverting signal. The symbol for this second measurement is $V_{SS}$ and is a calculated parameter. Nowhere in the IC does this signal exist with respect to ground, it only exists in reference to its differential pair. $V_{SS}$ can be measured directly by oscilloscopes with floating references, otherwise this value can be calculated as twice the value of $V_{OD}$ as described in the first description.

Figure 8-1 illustrates the two different definitions side-by-side for inputs and Figure 8-2 illustrates the two different definitions side-by-side for outputs. The $V_{ID}$ and $V_{OD}$ definitions show $V_A$ and $V_B$ DC levels that the noninverting and inverting signals toggle between with respect to ground. $V_{SS}$ input and output definitions show that if the inverting signal is considered the voltage potential reference, the noninverting signal voltage potential is now increasing and decreasing above and below the noninverting reference. Thus the peak-to-peak voltage of the differential signal can be measured.

$V_{ID}$ and $V_{OD}$ are often defined as volts (V) and $V_{SS}$ is often defined as volts peak-to-peak ($V_{PP}$).

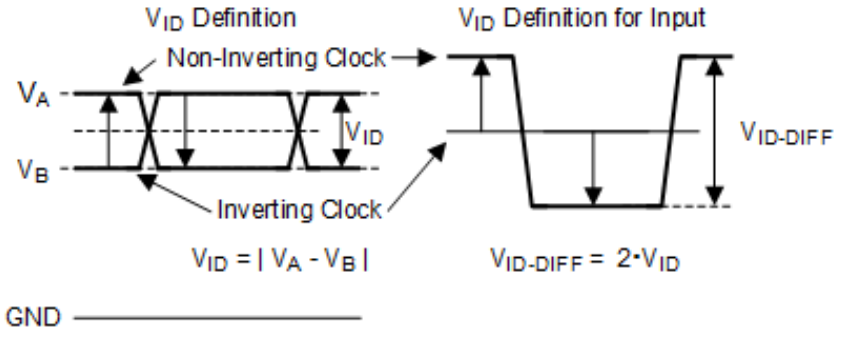



**Figure 8-1. Two Different Definitions for Differential Input Signals**

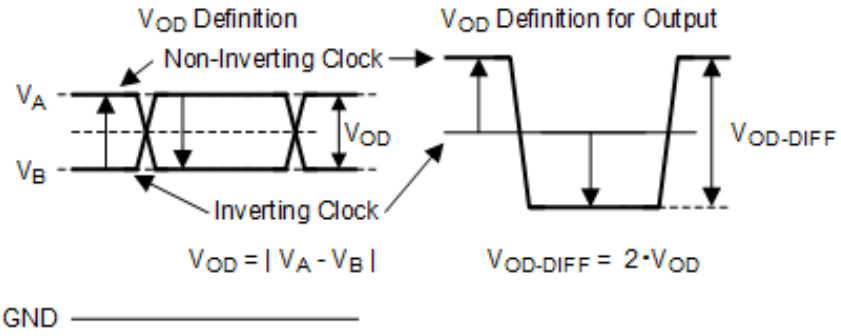



**Figure 8-2. Two Different Definitions for Differential Output Signals**

## 8.2 Output Clock Test Configurations

This section describes the characterization test setup of each block in the LMK5C33216.

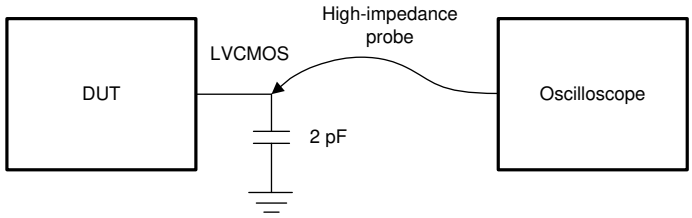



**Figure 8-3. LVCMOS Output DC Test Configuration**

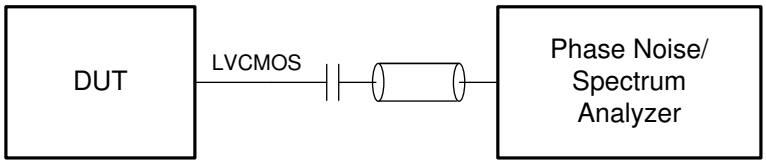



**Figure 8-4. LVCMOS Output Phase Noise Test Configuration**

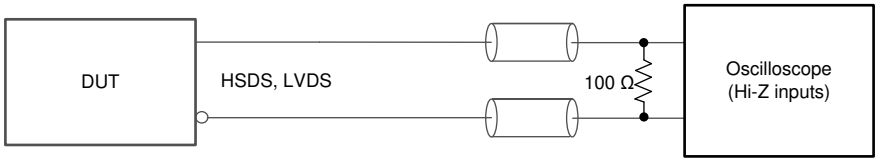



**Figure 8-5. HSDS, LVDS Output DC Test Configuration**

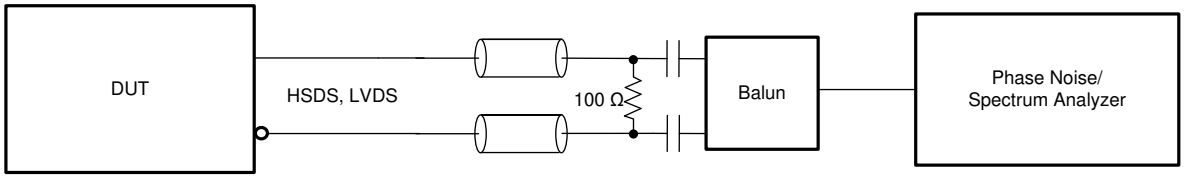



**Figure 8-6. HSDS, LVDS Output Phase Noise Test Configuration**

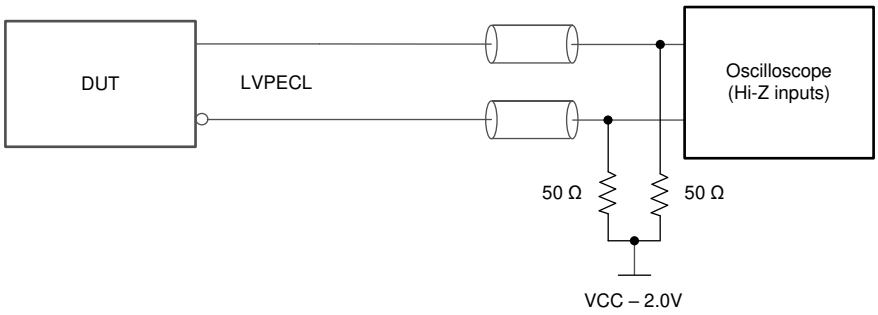



**Figure 8-7. LVPECL Output DC Test Configuration**

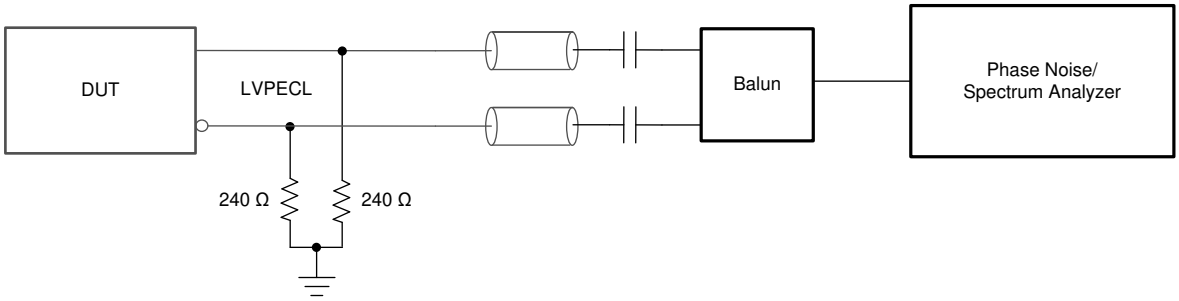



**Figure 8-8. LVPECL Output Phase Noise Test Configuration**

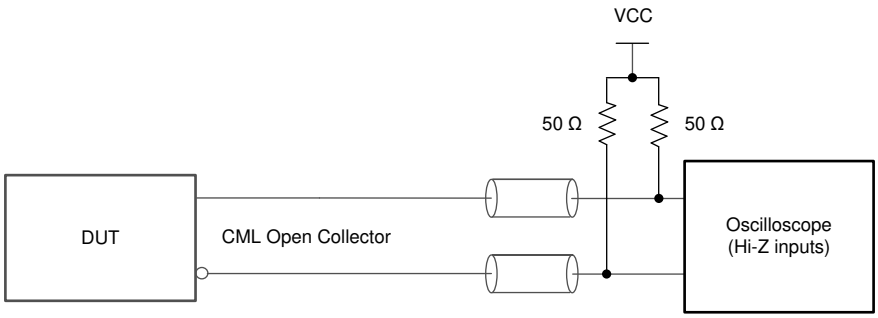



**Figure 8-9. CML Open Collector Output DC Test Configuration**

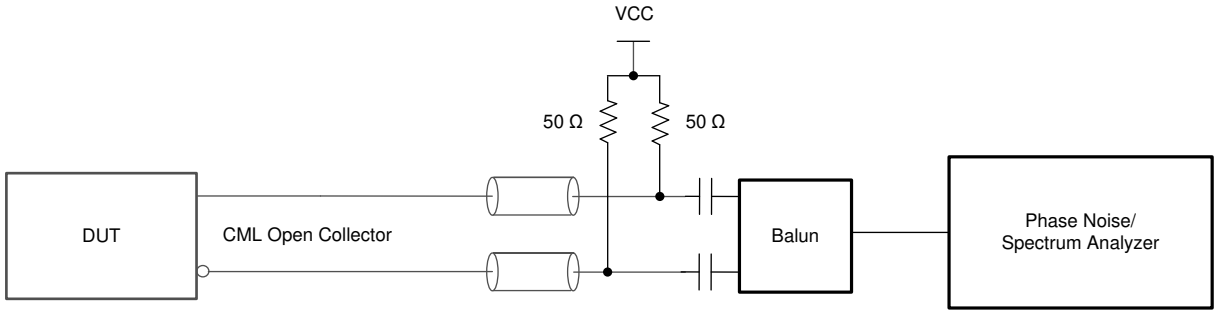
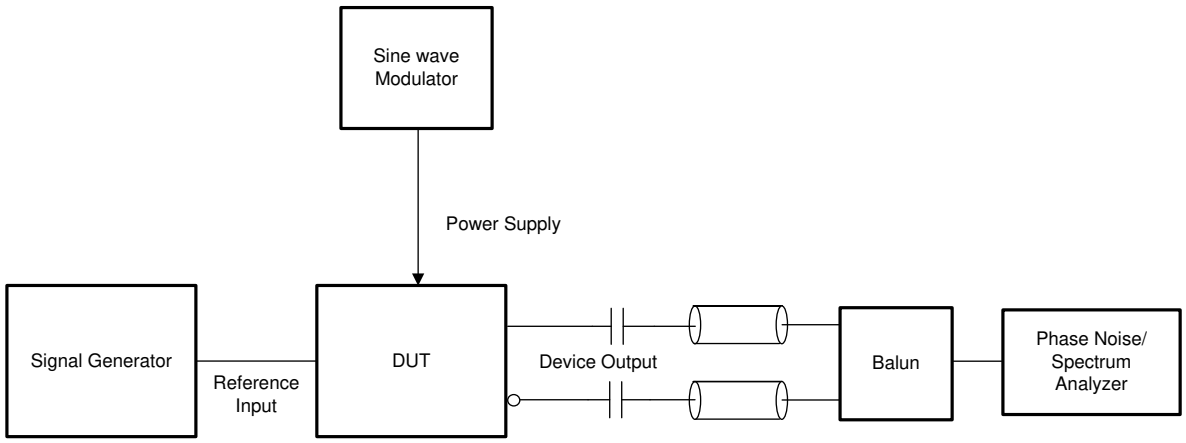



**Figure 8-10. CML Open Collector Output Phase Noise Test Configuration**




Single-sideband spur level measured in dBc with a known noise amplitude and frequency injected onto the device power supply.

**Figure 8-11. Power Supply Noise Rejection (PSNR) Test Configuration**

# 9 Detailed Description

## 9.1 Overview

The LMK5C33216 has two reference inputs, three digital PLL (DPLL), three analog PLLs (APLLs) with integrated VCOs, and sixteen output clocks. APLL3 uses an ultra-high performance BAW VCO (VCBO) with a very high quality factor, and thus minimizes dependency on the phase noise or frequency of the external oscillator (XO) input clock. TI's VCBO technology reduces the overall solution cost to meet the free-run and holdover frequency stability requirements. An XO, TCXO, or OCXO should be selected based on system holdover stability requirements. Each APLL can be controlled by the corresponding DPLL, allowing the APLL domain to be locked to the DPLL reference input for synchronous clock generation. Each APLL can select a reference from XO port or another APLL divided clock. Each DPLL can select a reference from reference inputs or another APLL divided clock.

The DPLL reference input mux supports automatic input selection based on priority and reference signal monitoring criteria. Manual input selection is also possible through software or pin control. The device provides hitless switching between reference sources with proprietary phase cancellation and phase slew control for superior phase transient performance. The reference clock input monitoring block monitors the clock inputs and will perform a hitless switchover or holdover when a loss of reference (LOR) is detected. A LOR condition will be detected upon any violation of the threshold limits set for the input monitors, which include frequency, missing and early pulse, runt pulse, and 1-PPS (pulse-per-second) detectors. The threshold limits for each input detector can be set and enabled per reference clock input. The tuning word history monitor feature determines the initial output frequency accuracy upon entry into holdover based on the historical average frequency when locked, thereby minimizing the frequency and phase disturbance during a LOR condition.

The LMK5C33216 has sixteen outputs with programmable output driver types, allowing up to sixteen differential clocks, or a combination of differential and single-ended clocks. Up to four single-ended 1.8-V or 2.65-V LVCMOS clocks (each from _P and _N outputs from OUT0 and OUT1). Each output clock derives from one of three APLL/VCO domains through the output muxes. Output 0 (OUT0) and Output 1 (OUT1) are the most flexible and may select their source from the XO, reference input, or any APLL domain. A 1-PPS output can be supported on Output 0 (OUT0) and Output 1 (OUT1). The output dividers have a SYNC feature to allow multiple outputs to be phase-aligned. If needed, the user can enable the zero-delay mode (ZDM) synchronization to achieve deterministic phase alignment between an APLL clock on OUT0 and the selected reference input. ZDM feedback paths are also available on OUT4 for DPLL2, and OUT10 for DPLL3.

To support IEEE 1588 PTP secondary clock or other clock steering applications, the DPLL supports DCO mode with less than 1-ppt (part per trillion) frequency resolution for precise frequency and phase adjustment through software or pin control.

The device is fully programmable through $I^2C$ or SPI and supports start-up frequency configuration with factory pre-programmed internal ROM pages. A programmable EEPROM overlay, which allows POR configuration of registers related to APLL and output configuration, provides flexible power up output clocks. Internal LDO regulators provide excellent PSNR to reduce the cost and complexity of the power delivery network. The clock input and PLL monitoring status are visible through the GPIO status pins and interrupt registers readback for full diagnostic capability.

## 9.2 Functional Block Diagram

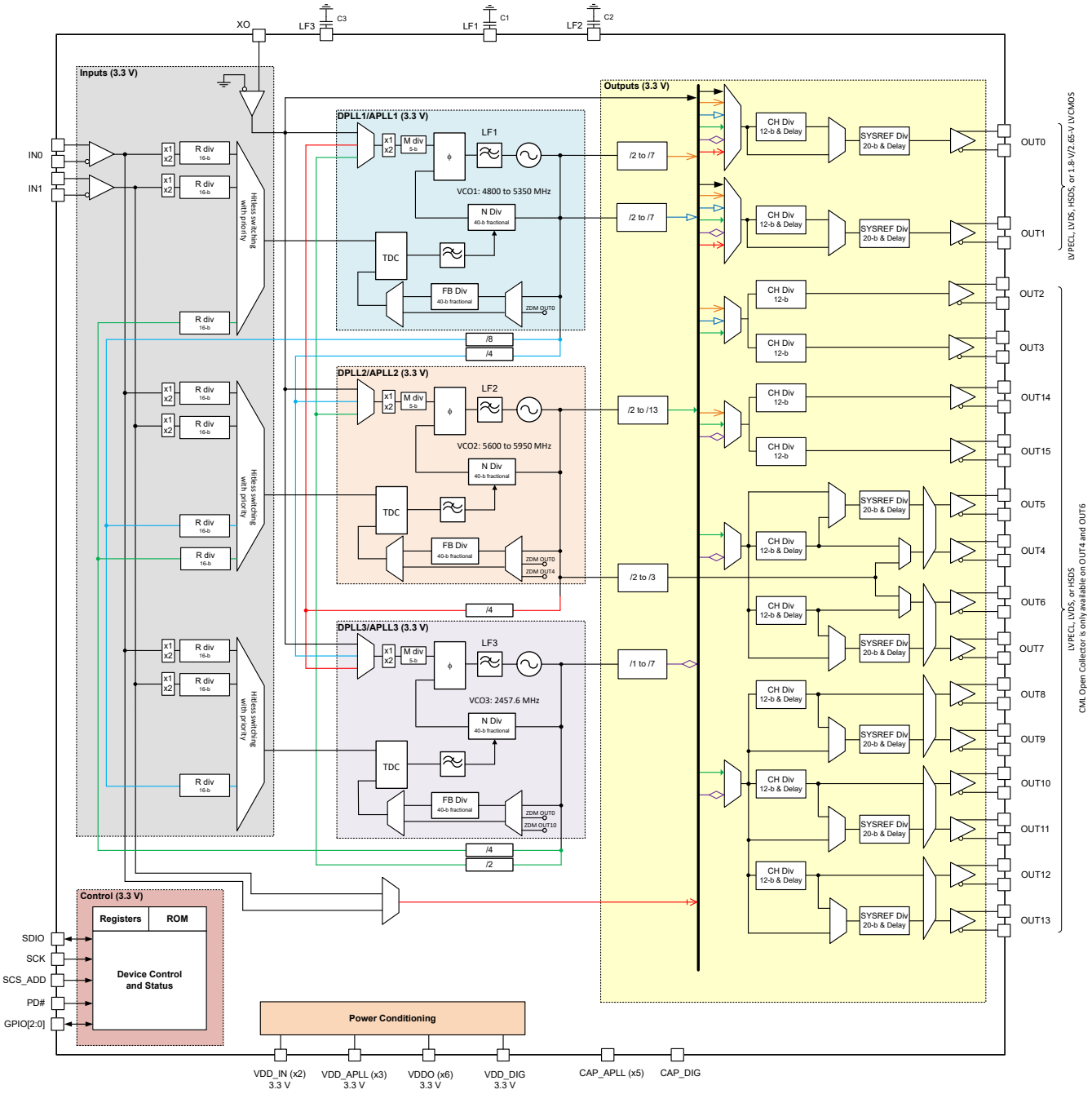



**Figure 9-1. LMK5C33216 Top-Level Block Diagram**

### 9.2.1 PLL Architecture Overview

Figure 9-2 shows the PLL architecture implemented in the LMK5C33216. APLL1 with integrated LC VCO (VCO1) can be used as a clock generation domain. APLL1's numerator in feedback N divider can be controlled by DPLL1. APLL2 with integrated LC VCO (VCO2) can generate another additional clock domain. APLL2's numerator in feedback N divider can be controlled by DPLL2. The third channel consists of a digital PLL (DPLL3) and analog PLL (APLL3) with integrated BAW VBCO (VCO3).

The DPLL is comprised of a time-to-digital converter (TDC), digital loop filter (DLF), and programmable 40-bit fractional feedback (FB) divider with sigma-delta-modulator (SDM). The APLLs are comprised of a reference (R) divider, phase-frequency detector (PFD), loop filter (LF), fractional feedback (N) divider with SDM, and VCO.

Each DPLL has a reference selection mux that allows the DPLL to be either locked to another APLL's VCO domian (DPLL Cascaded, except APLL2) or locked to the reference input (Non-Cascaded) providing unique flexibility in frequency and phase control across multiple clock domains..

Each APLL has a reference selection mux that allows the APLL to be either locked to another APLL's VCO domain (APLL Cascaded) or locked to the XO input (Non-Cascaded).

Do not cascade one VCO output to both the DPLL reference and APLL reference of the same DPLL/APLL pair.

Each APLL has a fixed 40 bit denominator controllable by the DPLL. When operating an APLL without the DPLL, a programmable 24 bit denominator is also available allowing an APLL to cascade between frequency domains with 0 ppm frequency error.

Any unused DPLL or APLL should be disabled (powered-down) to save power. Each APLL's VCO drives the clock distribution blocks via their respective VCO post-dividers. If the post-divider setting is 1 for VCO3, the post-divider is bypassed and VCO3 feeds the output clock distribution blocks directly.

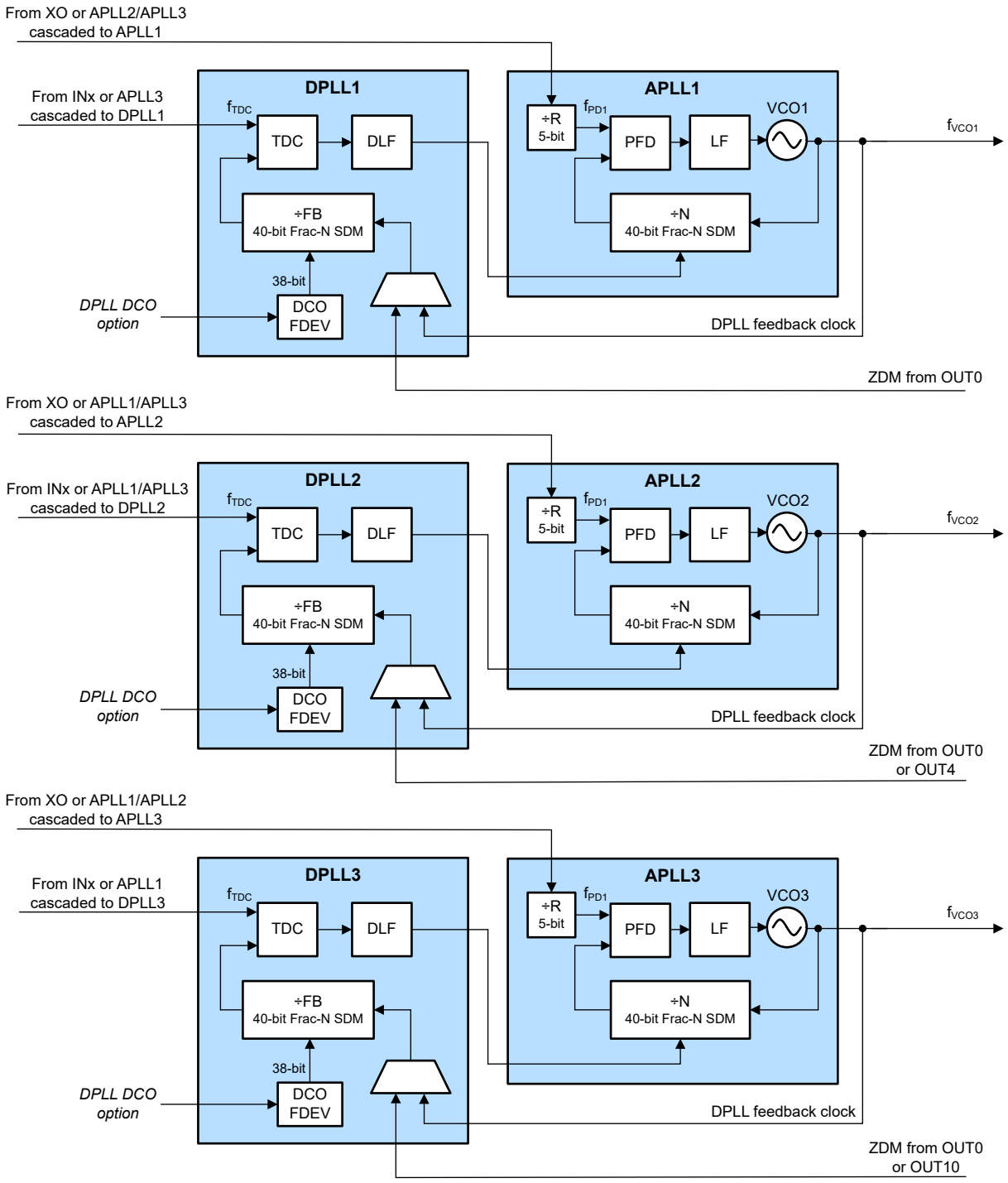



**Figure 9-2. PLL Architecture**

The following sections describe the basic principles of DPLL and APLL operation.. See Section 9.4.2 for more details on the PLL modes of operation including holdover.

### 9.2.2 DPLL

When DPLL operation is enabled, the clock source on XO pin determines the free-run and holdover frequency stability and accuracy of the output clocks. The VCBO determines the APLL3 output clock phase noise and jitter performance over the 12-kHz to 20-MHz integration band, regardless of the frequency and jitter of the XO pin input. This increased immunity from reference noise degradation allows the APLL3 to use a cost-effective,

low-frequency TCXO or OCXO as the external XO input while still maintaining standards-compliant frequency stability and low loop bandwidth (≤10 Hz) required for SynchE and PTP synchronization applications. APLL1 and APLL2 with standard LC type VCOs can be optimized for best jitter performance over the DC to 100 kHz integration band by using a wide loop bandwidth with a clean reference and a high phase detector frequency. When encountering system performance limitations arising from XO frequency or phase noise, there are unique cascading options to provide a clean high frequency reference for APLL1 and APLL2. The LMK5C33216 allows selecting the divided output from the VCBO (APLL3 Cascaded) which can significantly reduce APLL1 and APLL2 output RMS jitter.

If DCO mode is enabled on a DPLL, a frequency deviation step value (FDEV) can be programmed and used to adjust (increment or decrement) the DPLL's FB divider SDM. The DCO frequency adjustment effectively propagates through the APLL domain to the output clocks and any cascaded DPLL/APLL domains.

The programmed DPLL loop bandwidth ($BW_{DPLL}$) should be lower than all of the following:

1. 1/100th of the DPLL TDC rate.
2. 1/10th the APLL loop bandwidth.
3. The maximum DPLL bandwidth setting of 4 kHz.

#### *9.2.2.1 Independent DPLL Operation*

In the independent mode, each DPLL can select a reference as preferred. DPLL's can share the same reference, or each select a different reference. At start-up, each APLL will lock to the XO input after initialization and operate in free-run mode. Once a valid DPLL reference input is detected, each DPLL begins lock acquisition on independent reference priority. Each DPLL's TDC compares the phase of the selected reference input clock and the FB divider clock from the respective VCO and generates a digital correction word corresponding to the phase error. The correction word is filtered by the digital loop filter (DLF), and the DLF output adjusts the APLL N divider SDM to pull the VCO frequency into lock with the reference input.

As each DPLL can work independently in this mode, the DPLLs can lock or unlock without impacting other channels.

When selecting an XO frequency, TI recommends to avoid ratios falling near integer or half integer boundaries to minimize spurious noise. Ideally, the selected frequency that would ensure each APLL fractional-N divide ratio (NUM/DEN) is between 0.125 to 0.875 with the exception of the range between 0.45 to 0.55. Higher frequency XO is better for jitter performance, especially for APLL1 and APLL2 outputs. If the XO frequency or phase noise performance has gap for APLL1 or APLL2, there is an option to adopt cascaded mode using APLL3 as the reference to APLL1 or APLL2.

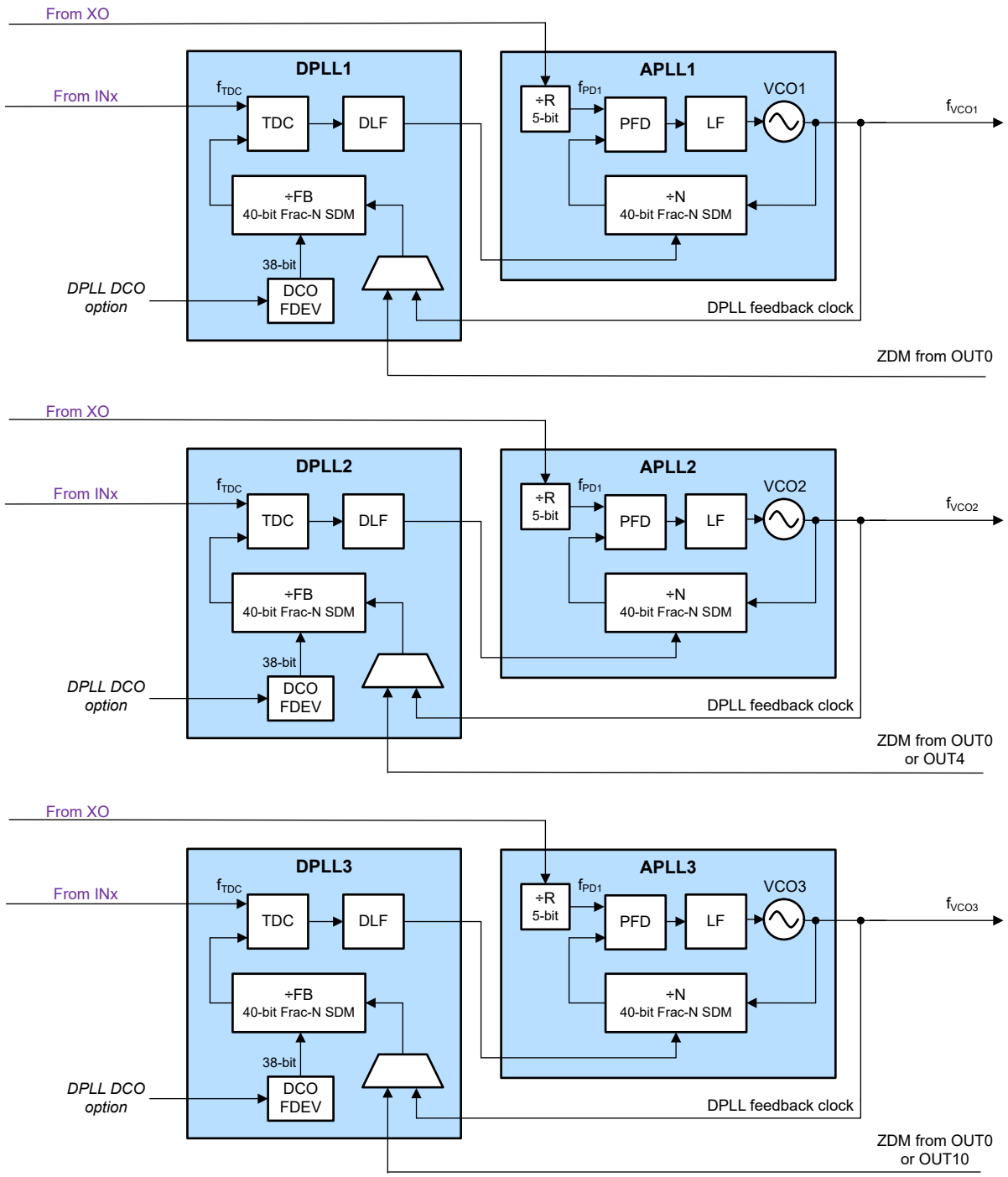



**Figure 9-3. DPLL Independent Mode**

#### 9.2.2.2 Cascaded DPLL Operation

Figure 9-4 shows an example where DPLL1 and DPLL2 is in cascaded mode from APLL3. APLL1, APLL2 and APLL3 lock their VCO frequency to the external XO input and operates in free-run mode without valid reference input. In this example, DPLL3 is the main DPLL, DPLL1 and DPLL2 are cascaded DPLLs.

Once a valid DPLL reference input is detected, the main DPLL begins lock acquisition. The DPLL3 TDC compares the phase of the selected reference input clock with the FB divider clock from the respective VCO and generates a digital correction word corresponding to the phase error. The correction word is filtered by the DLF, and the DLF output adjusts the APLL N divider SDM to pull the VCO frequency into lock with the reference input.

Cascading of DPLLs provides clean, low jitter output clocks synchronized with DPLL3. Note in cascaded DPLL mode, the best jitter performance and frequency stability will be achieved after DPLL3 locked.

DPLL3 lock status may not necessarily impact DPLL1 and DPLL2 lock status. If APLL3 is in free-run mode or holdover mode, and the VCBO frequency offset ppm value is still a valid reference for DPLL1 and DPLL2, then cascaded DPLL1, APLL1, DPLL2 and APLL2 are able to maintain lock status, while APLL1 and APLL2 outputs track the same frequency offset as APLL3. When all enabled DPLLs and APLLs are locked, all enabled outputs will be synchronized to the reference selected by the main DPLL.

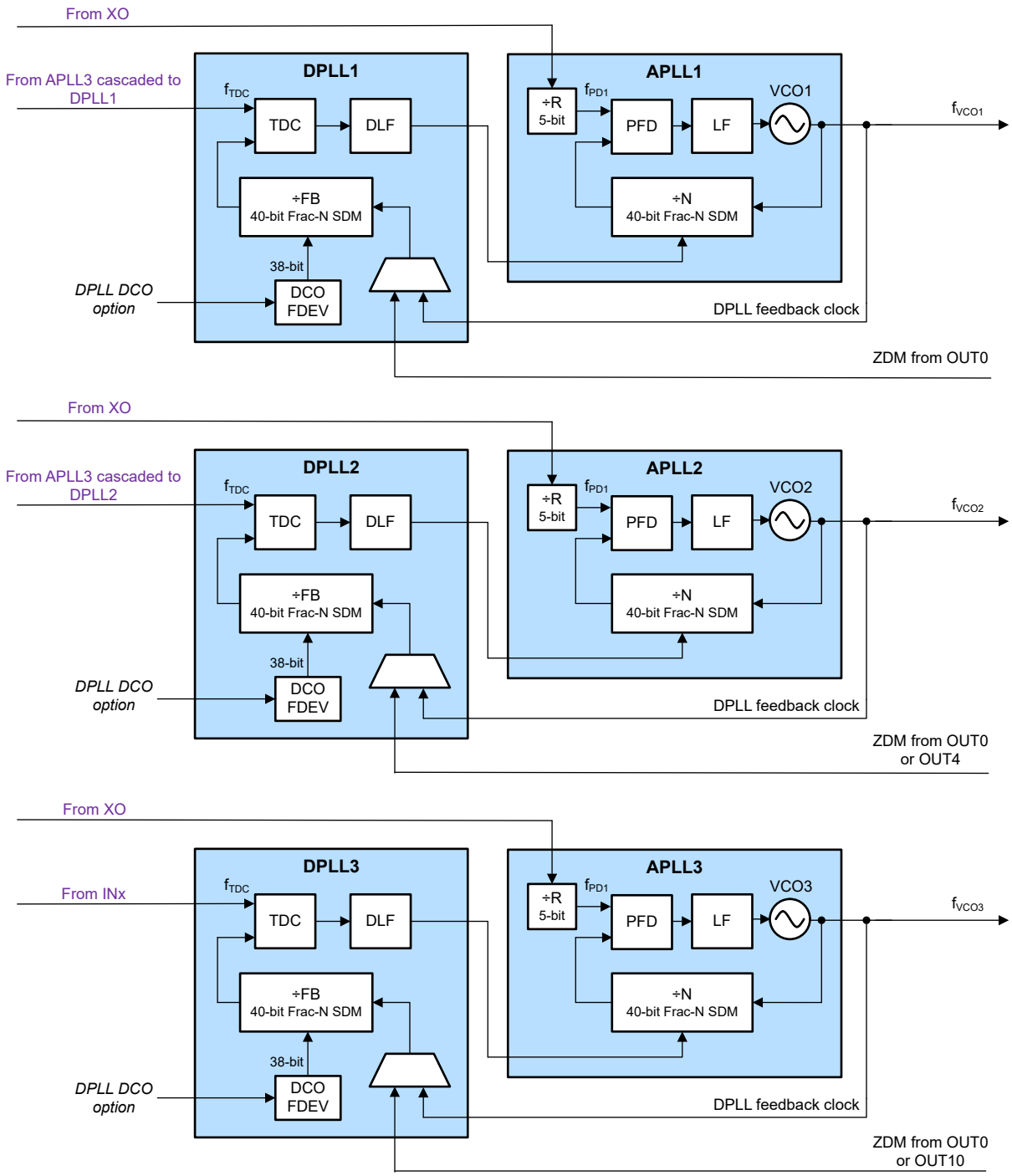



**Figure 9-4. DPLL Cascaded Mode**

#### 9.2.2.3 APLL Cascaded with DPLL

Figure 9-5 shows APLL1 and APLL2 are in cascaded mode from APLL3, VCO3 is held around its nominal center frequency of 2457.6 MHz while APLL1 and APLL2 lock. Subsequently, APLL3 locks the VCO3 frequency to the external XO input and operates in free-run mode. Cascaded PLLs lock to a divided frequency from the source VCO. Once a valid DPLL reference input is detected beyond a minimum valid time, the DPLLs begin lock acquisition. Each DPLL TDC compares the phase of the selected reference input clock and the FB divider clock from the respective VCO and generates a digital correction word corresponding to the phase error. At beginning, the TDC simply cancels out the phase error with no filtering correction word. Then subsequent correction words are filtered by the DLF, and the DLF output adjusts the APLL N divider SDM to pull the VCO frequency into lock with the reference input.

Using the VCBO as a cascade source to APLL1 or APLL2 provides the APLL a high-frequency, ultra-low-jitter reference clock. This unique cascading feature can provide improved close in phase noise performance if the XO/TCXO/OCXO is a low frequency or has poor phase noise performance. Note that in cascaded DPLL operation the best jitter performance and frequency stability will be achieved after DPLL3 locked.

DPLL3 lock status will impact DPLL1 and DPLL2 lock status. If APLL3 is in free-run mode or holdover mode, the VCBO frequency offset ppm value could introduce a similar frequency offset at APLL1 and APLL2 outputs even though DPLL1 and DPLL2 can stay in locked status. In this configuration example, ensure DPLL3 and APLL3 are locked first, toggle PLL1 or PLL2 enable cycle (APLLx_EN bit = 0 → 1) to calibrate VCO1 or VCO2, and then double check PLL1 or PLL2 lock status.

In above example, APLL3 is upstream PLL, while APLL1 and APLL2 are downstream PLLs. If there are system start-up requirements on the clock sequencing, APLL1 or APLL2 also can be configured as the upstream PLL.

When cascading PLLs, the downstream APLL may use the DPLL or bypass and power down the DPLL depending on performance requirements. If DPLL1 and DPLL2 are disabled from above APLL cascaded mode, then DPLL3-only cascade mode may be used (Figure 9-6). In this case, VCO1 or VCO2 can track the VCO3 domain during DPLL3 lock acquisition and locked modes, allowing APLL1 or APLL2's clock domain to be synchronized to the DPLL3 reference input.

When a DPLL is disabled, it is recommended to use the 24-bit numerator and programmable 24-bit denominator instead of the fixed 40-bit denominator to eliminate frequency error from APLL reference to output.

Do not cascade one VCO output to both the DPLL reference and APLL reference of the same DPLL/APLL pair.

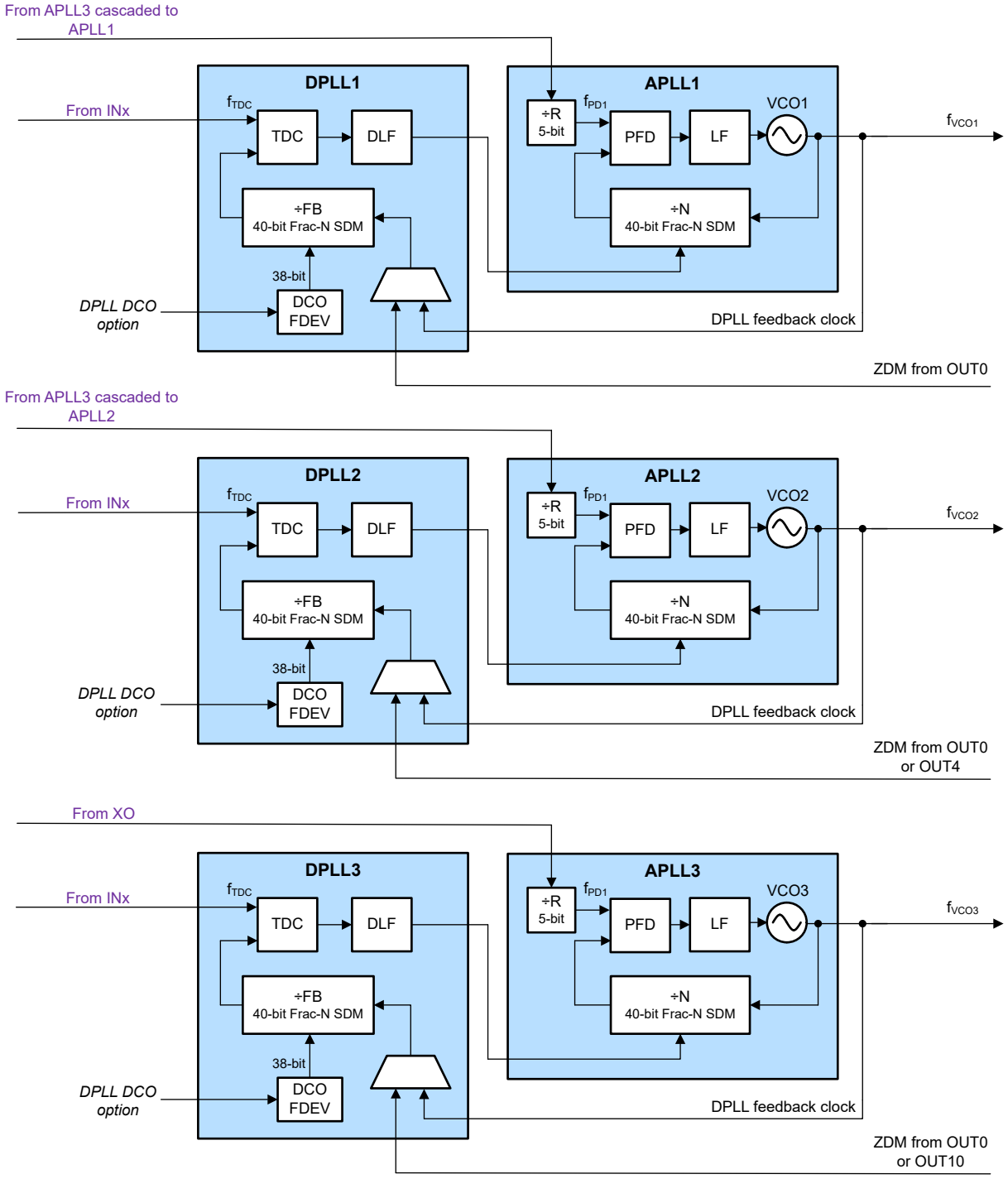



**Figure 9-5. APLL Cascaded with DPLLs Enabled Example**

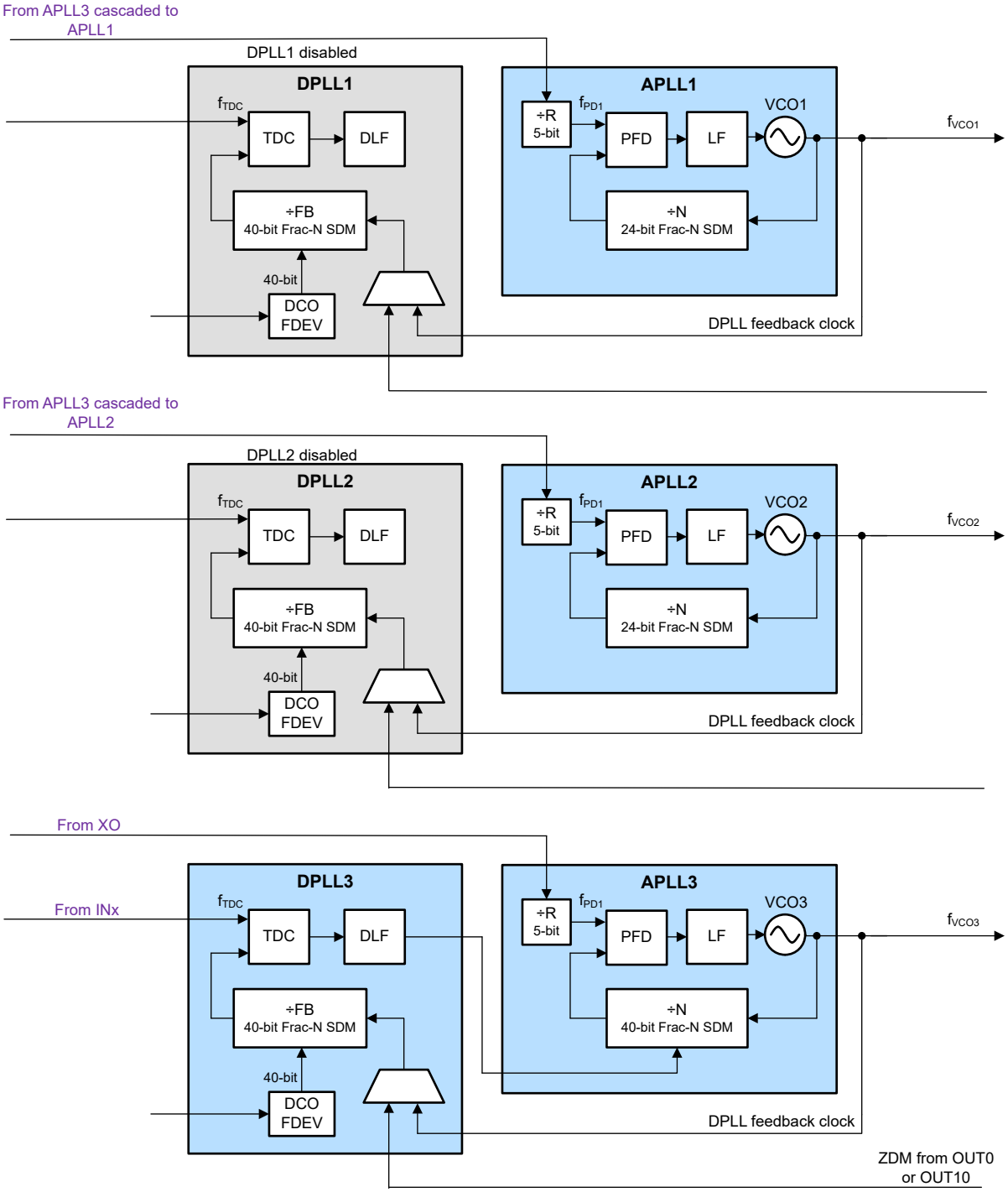



**Figure 9-6. APLL Cascaded with DPLLs Disabled Example**

### 9.2.3 APLL-Only Mode

In APLL-only mode, the external XO input source determines the free-run frequency stability and accuracy of the output clocks. The DPLL blocks are not used and do not affect the APLLs. APLLs still can operate in cascaded mode or non-cascaded mode and also have DCO option through control register writes.

The principle of operation for APLL-only mode after power-on reset and initialization is as follows. If APLL1 or APLL2 is in cascaded mode as shown in Figure 9-6 (DPLL3 also is not used), VCO1 or VCO2 will track the VCO3 domain. APLLs lock in APLL priority order using bits: APLLx_STRT_PRTY. Cascading APLL1 or APLL2 from VCO3 provides a high-frequency, ultra-low-jitter reference clock to minimize the APLL2 or APLL3 in-band phase noise/jitter degradation could otherwise occur from a lower performance XO/TCXO/OCXO.

If APLL1 or APLL2 is not cascaded as shown in Figure 9-7, VCO1 or VCO2 will lock to the XO input in APLLx_STRT_PRTY order after initialization and operate independent of the APLL3 domain.

When operating in APLL-Only mode, it is recommended for frequency accuracy to use a 24-bit numerator and a programmable 24-bit denominator (PLLx_MODE = 0) instead of a fixed 40-bit denominator (PLLx_MODE = 1).

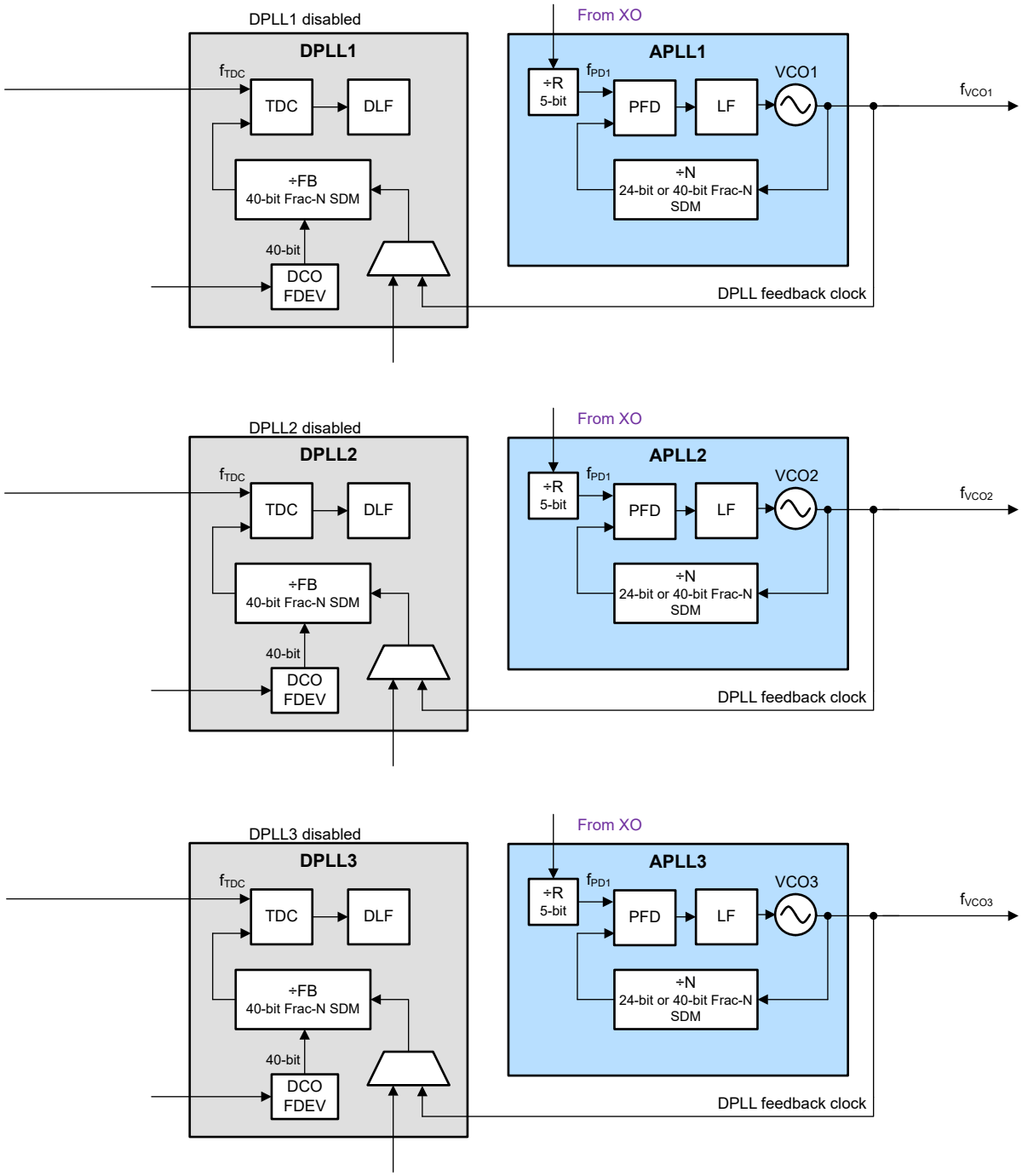



**Figure 9-7. APLL-Only Independent Mode**

## 9.3 Feature Description

The following sections describe the features and functional blocks of the LMK5C33216.

### 9.3.1 Oscillator Input (XO)

The XO input is the reference clock for the fractional-N APLLs when APLLs are not used in cascade mode. The XO input determines the output frequency accuracy and stability in free-run or holdover modes.

For proper DPLL operation, the XO frequency must have a **non-integer relationship** with the VCO frequency so the respective APLL N divider has a fractional divider ratio. For APLL-only mode, the XO frequency can have an integer or fractional relationship with the VCOs frequencies.

For applications requiring DPLL functionality, such as SyncE and IEEE 1588 for eCPRI, the XO input can be driven by a TCXO, OCXO, or external traceable clock that conforms to the frequency accuracy and holdover stability required by the applicable synchronization standard. TCXO and OCXO frequencies of 10, 13, 14.4, 19.44, 24, 25, 27, 38.88, and 48 MHz are commonly available and cost-effective options that allow the APLL3 to operate in fractional mode for a VCO3 frequency of 2457.6 MHz.

An XO/TCXO/OCXO source with low frequency or high phase jitter/noise floor will have no impact on the APLL3 output jitter performance because the VCBO determines the jitter and phase noise over the 12-kHz to 20-MHz integration bandwidth.

The XO input buffer has programmable input on-chip termination and AC-coupled input biasing configurations as shown in Figure 9-8. The buffered XO path also drives the input monitoring blocks.

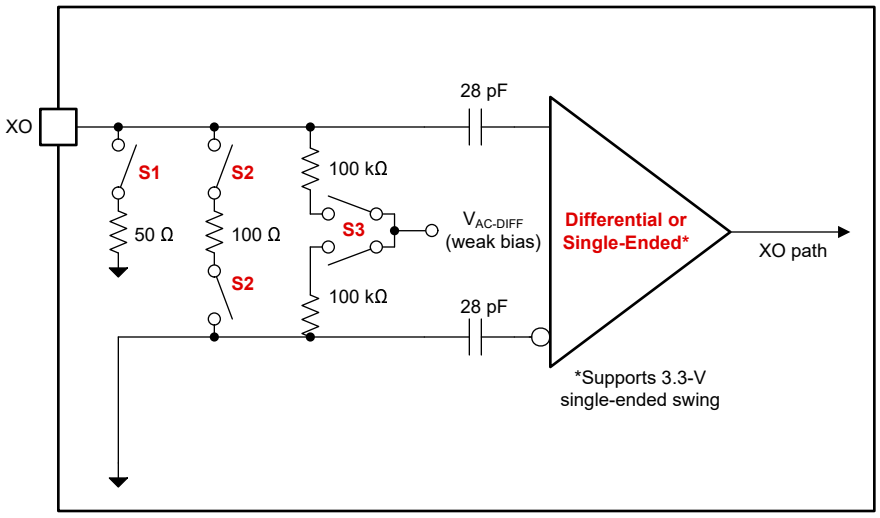



**Figure 9-8. XO Input Buffer**

Table 9-1 lists the typical XO input buffer configurations for common clock interface types.

**Table 9-1. XO Input Buffer Modes**

| XO_TYPE | INPUT TYPES | INTERNAL SWITCH SETTINGS | |
|---|---|---|---|
| | | INTERNAL TERM. (S1, S2)(1) | INTERNAL BIAS (S3)(2) |
| 0x00 | DC (external termination) | OFF | OFF |
| 0x01 | AC (external termination) | OFF | ON (1.3 V) |
| 0x03 | AC (internal 100-Ω to GND) | 100 Ω | ON (1.3 V) |
| 0x04 | DC (internal 50-Ω to GND) | 50 Ω | OFF |
| 0x05 | AC (internal 50-Ω to GND) | 50 Ω | ON (1.3 V) |
| 0x08 | LVCMOS | OFF | OFF |
| 0x0C | LVCMOS (internal 50-Ω to GND) | 50 Ω | OFF |

(1) S1, S2: OFF = External termination is assumed.
(2) S3: OFF = External input bias or DC coupling is assumed.

### 9.3.2 Reference Inputs

The reference inputs (IN0 and IN1) can accept differential or single-ended clocks. Each input has programmable input type, termination, and DC-coupled or AC-coupled input biasing configurations as shown in Figure 9-9. Each input buffer drives the reference input mux of the DPLL block. The DPLL input mux can select from any of the reference inputs. The DPLL can switch between inputs with different frequencies provided they can be divided-down to a common frequency by DPLL R dividers. The reference input paths also drive the various detector blocks for reference input monitoring and validation. DC-path switch can bypass internal AC-coupling capacitors to make low frequency input work robustly.

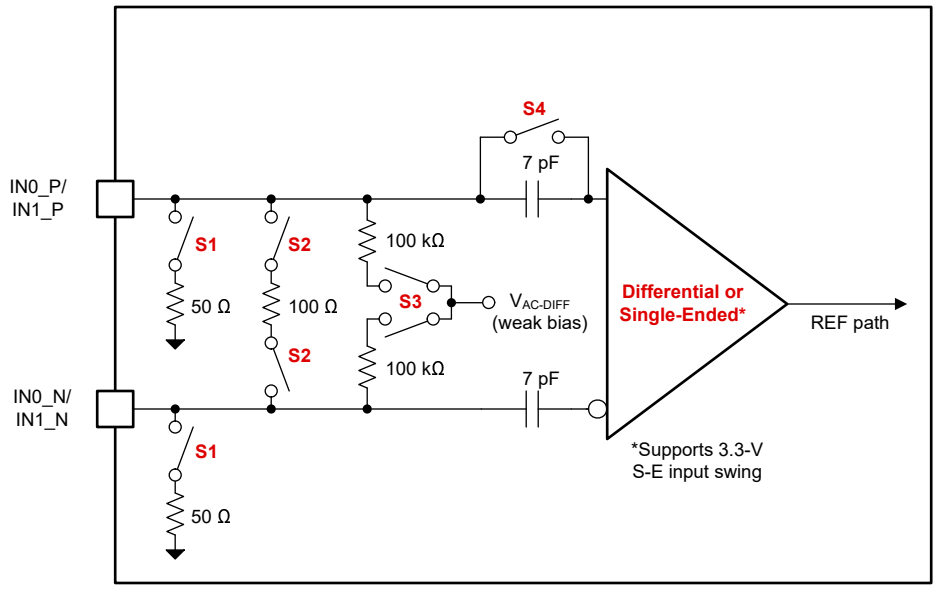



**Figure 9-9. Reference Input Buffer**

Table 9-2 lists the reference input buffer configurations for common clock interface types.

**Table 9-2. Reference Input Buffer Modes**

| REFx_DC_COUPLED_EN, REFx_TYPE | INPUT TYPES | INTERNAL SWITCH SETTINGS | | | |
|---|---|---|---|---|---|
| | | INTERNAL SINGLE-END TERM. (S1)(2) | INTERNAL DIFFERENTIAL TERM. (S2) (2) | INTERNAL BIAS (S3)(3) | LVCMOS/DIFF INTERNAL AC CAPACITOR BYPASS MODE (S4) (1) |
| 0x00, 0x00 | DC-Differential (external termination) | OFF | OFF | OFF | OFF |
| 0x00, 0x01 | AC-Differential (external termination) | OFF | OFF | ON (1.3 V) | OFF |
| 0x00, 0x02 | DC-Differential (internal termination) | OFF | 100 Ω | OFF | OFF |
| 0x00, 0x03 | LVDS / HSDS, AC-Differential (internal termination) | OFF | 100 Ω | ON (1.3 V) | OFF |
| 0x00, 0x04 | HCSL,DC-Differential (internal termination 50-Ω) | 50 Ω | OFF | OFF | OFF |
| 0x00, 0x05 | LVPECL,AC-Differential (internal termination 50-Ω) | 50 Ω | OFF | ON (1.3 V) | OFF |
| 0x00, 0x08 | LVCMOS(External DC-coupling, internal AC coupling) | OFF | OFF | OFF | OFF |

**Table 9-2. Reference Input Buffer Modes (continued)**

| REFx_DC_COUPLED_EN, REFx_TYPE | INPUT TYPES | INTERNAL SWITCH SETTINGS | | | |
|---|---|---|---|---|---|
| | | INTERNAL SINGLE-END TERM. (S1)(2) | INTERNAL DIFFERENTIAL TERM. (S2) (2) | INTERNAL BIAS (S3)(3) | LVCMOS/DIFF INTERNAL AC CAPACITOR BYPASS MODE (S4) (1) |
| 0x01, 0x08 | LVCMOS (External DC-coupling, internal DC coupling) | OFF | OFF | OFF | ON |
| 0x01, 0x0C | LVCMOS(External DC-coupling, internal DC coupling, internal termination 50-Ω) | 50 Ω | OFF | OFF | ON |

(1) S4: OFF = Differential input amplitude detector is used for all input types except LVCMOS or Single-ended.
(2) S1, S2: OFF = External termination is assumed.
(3) S3: OFF = External input bias or DC coupling is assumed.

### 9.3.3 Clock Input Interfacing and Termination

Figure 9-10 through Figure 9-15 show the recommended input interfacing and termination circuits. Unused clock inputs can be left floating or pulled down.

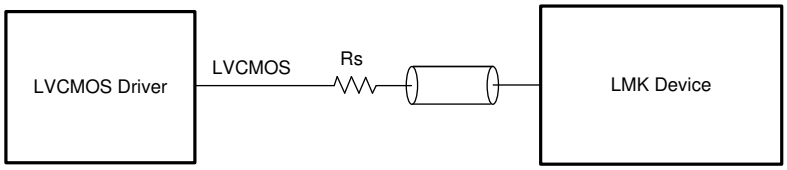



**Figure 9-10. Single-Ended LVCMOS (1.8 V, 2.5 V, 3.3 V) to Reference (INx_P) or XO Input (XO)**

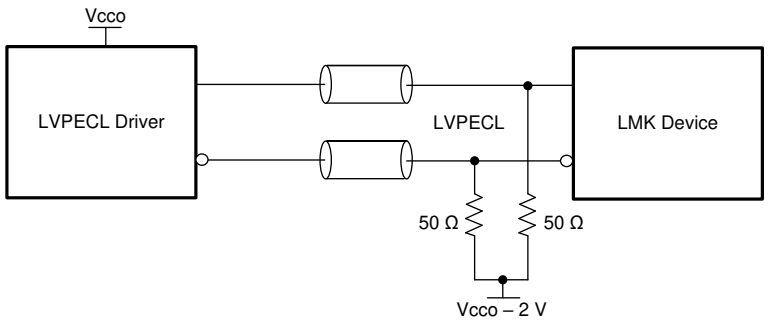



**Figure 9-11. DC-Coupled LVPECL to Reference (INx)**

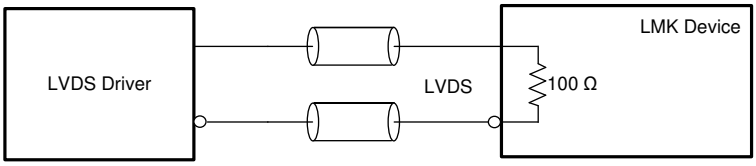



**Figure 9-12. DC-Coupled HSDS/LVDS to Reference (INx)**

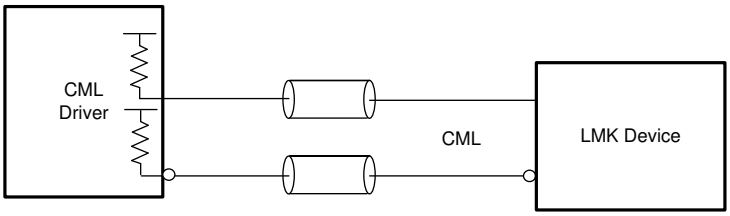



**Figure 9-13. DC-Coupled CML (Source Terminated) to Reference (INx)**

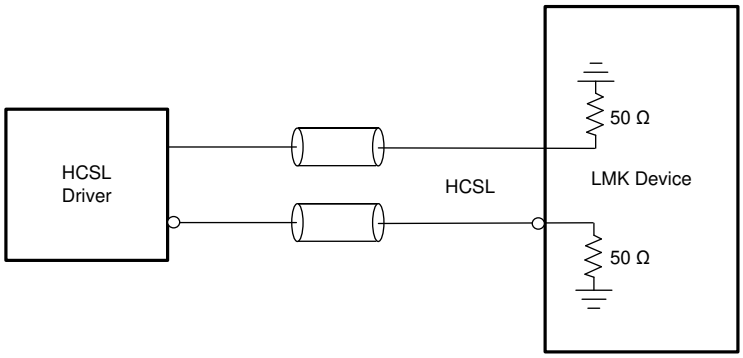



**Figure 9-14. HCSL (Load Terminated) to Reference (INx)**

| Driver | $R_B$ (Ω) |
|---|---|
| LVDS | open |
| CML* | open |
| LVPECL | 120 |
| HCSL | 50 |

*CML driver has 50-Ω pull-up

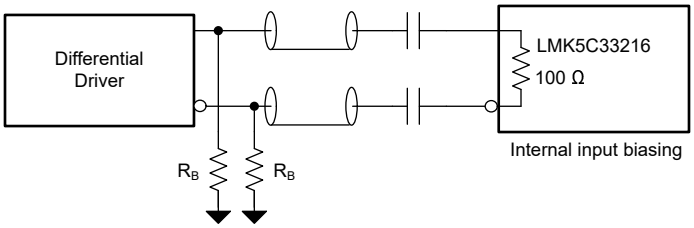



**Figure 9-15. AC-Coupled Differential to Reference (INx)**

### 9.3.4 Reference Input Mux Selection

For the DPLL block, the reference input mux selection can be done automatically using an internal state machine with a configurable input priority scheme, or manually through software register control or hardware pin control. The input mux can select IN0 or IN1 for LMK5C33216. The priority for all inputs can be assigned through registers. The priority ranges from 0 to 7, where 0 = ignore (never select), 1 = first priority, 2 = second priority and 7 = 7th priority. When all inputs are configured with the same priority setting, IN0 will be given first priority (IN0 → IN1). The selected input can be monitored through the status pins or register.

#### *9.3.4.1 Automatic Input Selection*

There are two automatic input selection modes that can be set by register: Auto Revertive and Auto Non-Revertive.

- *Auto Revertive:* In this mode, the DPLL automatically selects the valid input with the highest configured priority. If a clock with higher priority becomes valid, the DPLL will automatically switch over to that clock immediately.
- *Auto Non-Revertive:* In this mode, the DPLL automatically selects the highest priority input that is valid. If a higher priority input because valid, the DPLL will not switch-over until the currently selected input becomes invalid.

#### *9.3.4.2 Manual Input Selection*

There are two manual input selection modes that can be set by a register: Manual with Auto-Fallback and Manual with Auto-Holdover. In either manual mode, the input selection can be done through register control (Register DPLLx_MAN_REF_SEL) or hardware pin control (GPIOs).

- *Manual with Auto-Fallback:* In this mode, the manually selected reference is the active reference until it becomes invalid. If the reference becomes invalid, the DPLL will automatically fallback to the highest priority input that is valid or qualified. If no prioritized inputs are valid, the DPLL will enter holdover mode (if tuning word history is valid) or free-run mode. The DPLL will exit holdover mode when the selected input becomes valid.
- *Manual with Auto-Holdover:* In this mode, the manually selected reference is the active reference until it becomes invalid. If the reference becomes invalid, the DPLL will automatically enter holdover mode (if tuning word history is valid) or free-run mode. The DPLL will exit holdover mode when the selected input becomes valid.

The reference input selection flowchart is shown in Figure 9-16.

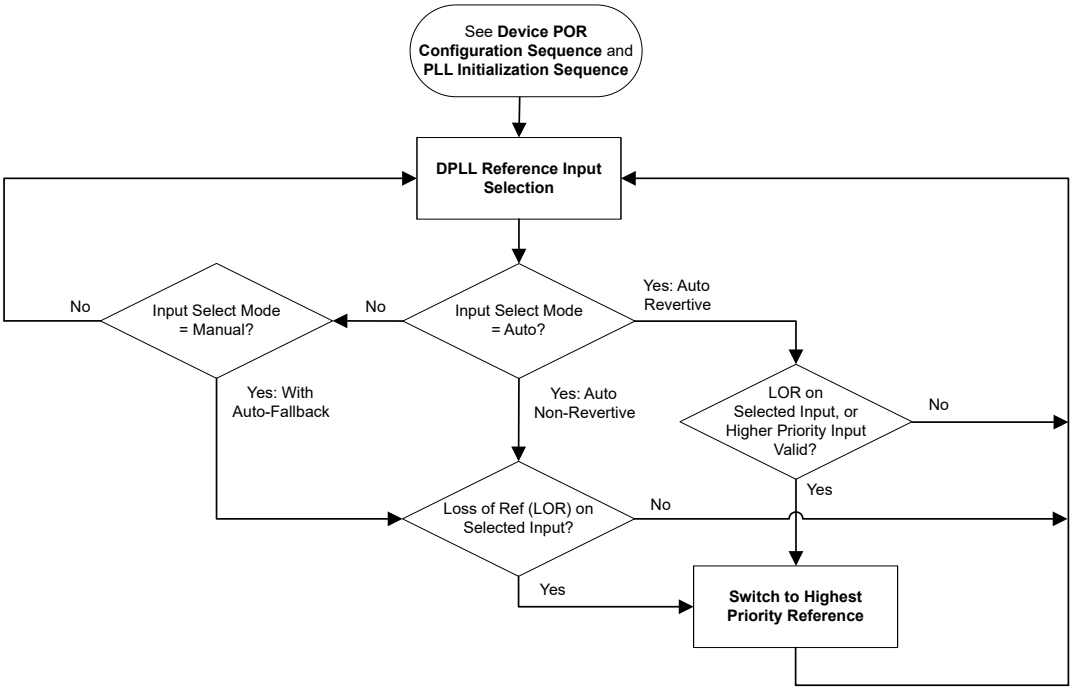



**Figure 9-16. DPLL Reference Input Selection Flowchart**

Also see Figure 9-36, Figure 9-37, and Figure 9-38.

### 9.3.5 Hitless Switching

The DPLL supports hitless switching through TI's proprietary phase cancellation scheme or phase slew control scheme. When hitless switching is disabled, a phase hit equal to the phase offset between the two inputs will be propagated to the output at a rate determined by the filtering of the DPLL bandwidth.

determined by the filtering of the DPLL bandwidth

#### *9.3.5.1 Hitless Switching with Phase Cancellation*

When hitless switching with phase cancellation is enabled, it will prevent a phase transient (phase hit) from propagating to the outputs when the two switched inputs have a fixed phase offset and are frequency-locked. The inputs are frequency-locked when they have same exact frequency (0-ppm offset), or have frequencies that are integer-related and can each be divided to a common frequency by integers. The hitless switching specifications ($t_{HITLESS}$ and $f_{HITLESS}$) are valid for reference inputs with no wander. In the case where two inputs are switched but are not frequency-locked, the output smoothly transitions to the new frequency with reduced transient.

#### *9.3.5.2 Hitless Switching With Phase Slew Control*

When DPLLx_PHS1_EN is selected, it enables Phase Slew Control during holdover exit. It will make the output phase transient (phase hit) as DPLLx_PHS1_THRESH and DPLLx_PHS1_TIMER defined when the DPLL switches from APLL-only mode or holdover mode to DPLL Lock Acquisition mode, or hitless switching with two inputs are not frequency-locked. When both Phase Cancellation function and Phase Slew Control function are disabled, a phase hit equal to the phase offset between XO and selected input or between the two inputs at the moment of switching will be propagated to the output at a rate determined by the DPLL fastlock bandwidth. In the case where two inputs are switched but are not frequency-locked Phase Slew Control function can achieve, the output smoothly transitions to the new frequency as the rate the user defined.

#### 9.3.5.3 Hitless Switching With 1-PPS Inputs

Hitless switching between 1-PPS inputs is supported when zero-delay mode (ZDM) synchronization is disabled, but the switchover event should only occur after the DPLL has acquired lock. If a switchover occurs before the DPLL has locked initially, the switchover will not be hitless and the DPLL will take an indeterminate amount of time to lock. In this case, a soft-reset should be issued for the DPLL to lock to the selected input. In an application, the system host can monitor the DPLL lock status through a STATUS pin or bit to determine when the DPLL has locked before allowing a switchover between 1-PPS inputs. The DPLL lock time is governed by the DPLL bandwidth (typically 10 mHz for a 1-PPS input).

Hitless switching between 1-PPS inputs is not supported when ZDM synchronization is enabled.

### 9.3.6 Gapped Clock Support on Reference Inputs

The DPLL supports locking to an input clock that has missing periods and is referred to as a gapped clock. Gapping severely increases the jitter of a clock, so the DPLL provides the high input jitter tolerance and low loop bandwidth necessary to generate a low-jitter periodic output clock. The resulting output will be a periodic non-gapped clock with an average frequency of the input with its missing cycles. The gapped clock width cannot be longer than the reference clock period after the R divider ($R_{IN0/IN1}$ / $f_{IN0/IN1}$). The reference input monitors should be configured to avoid any flags due to the worst-case clock gapping scenario to achieve and maintain lock. Reference switchover between two gapped clock inputs may violate the hitless switching specification if the switch occurs during a gap in either input clock.

### 9.3.7 Input Clock and PLL Monitoring, Status, and Interrupts

The following section describes the input clock and PLL monitoring, status, and interrupt features. The reference input frequency detector and phase valid detector can not be used at the same time.

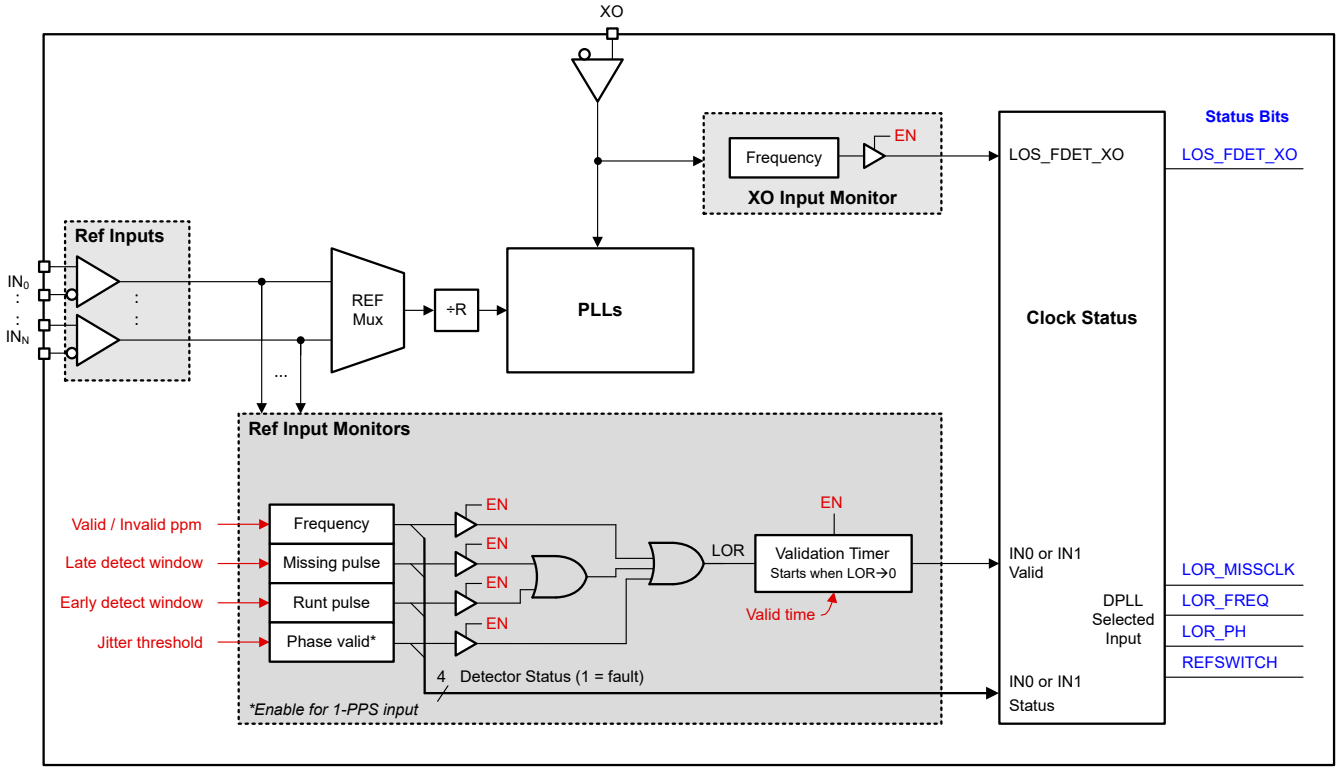



**Figure 9-17. Clock Monitors for Reference and XO Inputs**

#### 9.3.7.1 XO Input Monitoring

The XO input has a coarse frequency monitor to help qualify the input before it is used to lock the APLLs.

The XO frequency detector clears its LOS_FDET_XO flag when the input frequency is detected within the supported range of 10 MHz to 100 MHz. The XO frequency monitor uses a RC-based detector and cannot precisely detect if the XO input clock has sufficient frequency stability to ensure successful VCO calibration during the PLL start-up when the external XO clock has a slow or delayed start-up behavior. See Section 10.1.6 for more information.

The XO frequency detector can be bypassed by setting the XO_FDET_BYP bit (shown as $\overline{EN}$ in Figure 9-17) so that the XO input is always considered valid by the PLL control state machine. The user can observe the LOS_FDET_XO status flag through the status pins and status bit. Setting XO_FDET_BYP bit will bypass the detect, but will not reflect any change to LOS_FDET_XO status flag.

#### *9.3.7.2 Reference Input Monitoring*

Each DPLL reference clock input is independently monitored for input validation before it is qualified and available for selection by the DPLL. The reference monitoring blocks include frequency, missing pulse, and runt pulse monitors. For a 1-PPS input, the phase valid monitor is supported, while the frequency, missing pulse, and runt pulse monitors are not supported and must be disabled. A validation timer sets the minimum time for all enabled reference monitors to be clear of flags before an input is qualified.

The enablement and valid threshold for all reference monitors and validation timers are programmable per input. The reference monitors and validation timers are optional to enable, but are critical to achieve reliable DPLL lock and optimal transient performance during holdover or switchover events, and are also used to avoid selection of an unreliable or intermittent clock input. If a given detector is not enabled, it will not set a flag and will be ignored. The status flag of any enabled detector can be observed through the status pins for any reference input (selected or not selected). The status flags of the enabled detectors can also be read through the status bits for the selected input of the DPLL.

##### 9.3.7.2.1 Reference Validation Timer

The validation timer sets the amount of time required for each reference to be clear of flags from all enabled input monitors before the reference is qualified and valid for selection. The validation timer and enable settings are programmable.

##### 9.3.7.2.2 Frequency Monitoring

The precision frequency detector measures the frequency offset or error (in ppm) of all input clocks relative to the XO input's frequency, which is considered as the "0-ppm reference clock" for frequency comparison. The valid and invalid ppm frequency thresholds are configurable through the registers. The monitor will clear the LOR_FREQ flag when the relative input frequency error is less than the valid ppm threshold. Otherwise, the monitor will set the LOR_FREQ flag when the relative input frequency error is greater than the invalid ppm threshold. The ppm delta between the valid and invalid thresholds provides hysteresis to prevent the LOR_FREQ flag from toggling when the input frequency offset is crossing these thresholds.

A measurement accuracy (ppm) and averaging factor are used in computing the frequency detector register settings. A higher measurement accuracy (smaller ppm) or higher averaging factor will increase the measurement delay to set or clear the flag, which allow more time for the input frequency to settle, and can also provide better measurement resolution for an input with high drift or wander. Note that higher averaging reduces the maximum frequency ppm thresholds that can be configured.

##### 9.3.7.2.3 Missing Pulse Monitor (Late Detect)

The missing pulse monitor uses a window detector to validate input clock pulses that arrive within the nominal clock period plus a programmable late window threshold ($T_{LATE}$). When an input pulse arrives before $T_{LATE}$, the pulse is considered valid and the missing pulse flag will be cleared if set. When an input pulse does not arrive before $T_{LATE}$ (due to a missing or late pulse), the missing pulse flag will be set to disqualify the input.

Typically, $T_{LATE}$ should be set higher than the input's longest clock period (including cycle-to-cycle jitter), or higher than the gap width for a gapped clock. The missing pulse monitor can act as a coarse frequency detector with faster detection than the ppm frequency detector. The missing pulse monitor is supported for input frequencies between 2 kHz and $f_{VCO}/12$ and should be disabled when outside this range.

The missing pulse and runt pulse monitors operate from the same window detector block for each reference input. The status flags for both these monitors are combined by logic-OR gate and can be observed through status pin. The window detector flag for the selected DPLL input can also be observed through the corresponding MISSCLK status bit.

#### 9.3.7.2.4 Runt Pulse Monitor (Early Detect)

The runt pulse monitor uses a window detector to validate input clock pulses that arrive within the nominal clock period minus a programmable early window threshold ($T_{EARLY}$). When an input pulse arrives after $T_{EARLY}$, the pulse is considered valid and the runt pulse flag will be cleared. When an early or runt input pulse arrives before $T_{EARLY}$, the monitor will set the flag immediately to disqualify the input.

Typically, $T_{EARLY}$ should be set lower than the input's shortest clock period (including cycle-to-cycle jitter). The early pulse monitor can act as a coarse frequency detector with faster detection than the ppm frequency detector. The early pulse monitor is supported for input frequencies between 2 kHz and $f_{VCO}/12$ and should be disabled when outside of this range.

It is required to enable missing clock detect to user early clock detect. Early clock detect cannot be enabled alone.

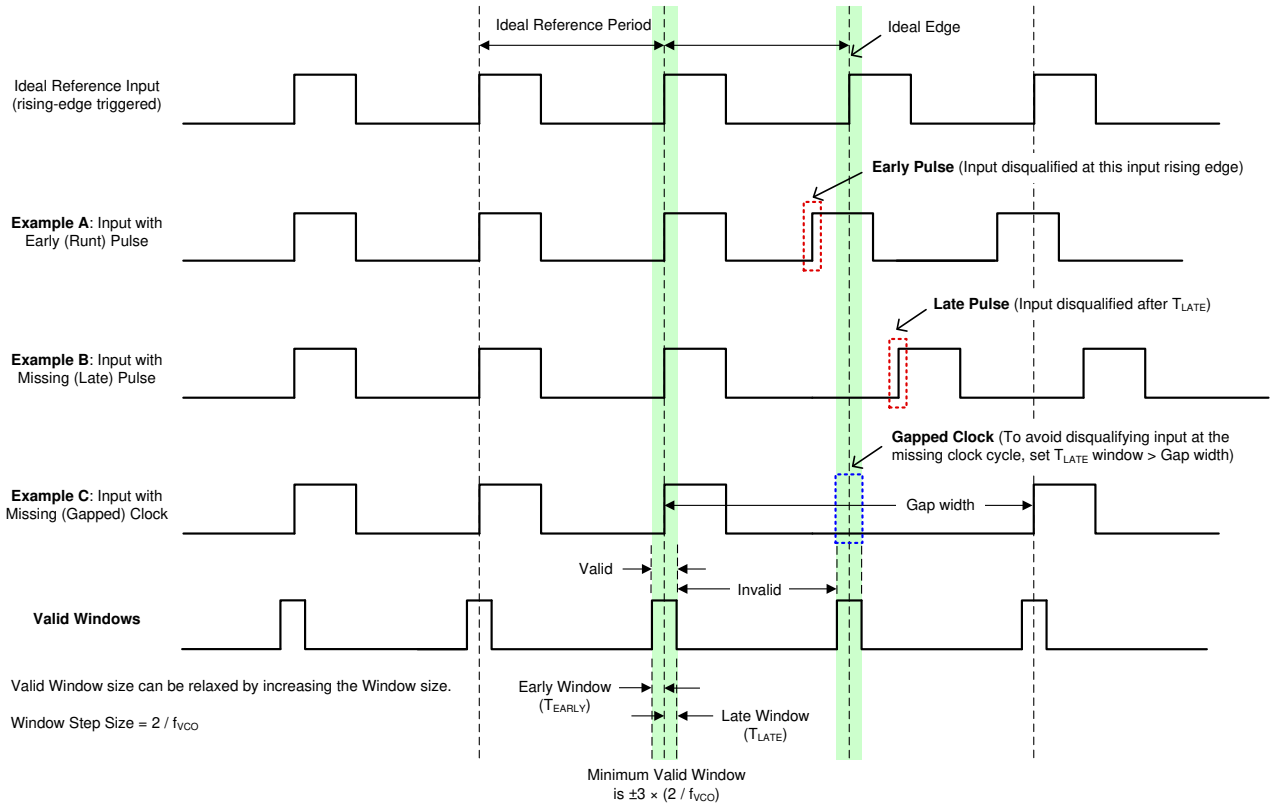



**Figure 9-18. Early and Late Window Detector Examples**

#### 9.3.7.2.5 Phase Valid Monitor for 1-PPS Inputs

The phase valid monitor is designed specifically for 1-PPS input validation because the frequency and window detectors do not support this low frequency. The phase valid monitor uses a window detector to validate 1-PPS input pulses that arrive within the nominal clock period ($T_{IN}$) plus a programmable jitter threshold ($T_{JIT}$). When the input pulse arrives within the counter window ($T_V$), the pulse is considered valid and the phase valid flag will be cleared. When the input pulse does not arrive before $T_V$ (due to a missing or late pulse), the flag will be set immediately to disqualify the input. $T_{JIT}$ should be set higher than the worst-case input cycle-to-cycle jitter.

*The phase valid register settings also are valid for 1-PPS ppm error threshold detect. Notice the $T_{JIT}$ also impacts the worst case ppm error allowed.* For example: High_Jitter_Freq = 1/($T_{IN}$ - $T_{JIT}$), then Max input allowable ppm error = (High_Jitter_Freq - Expected_Freq) / Expected_Freq * 1e6.

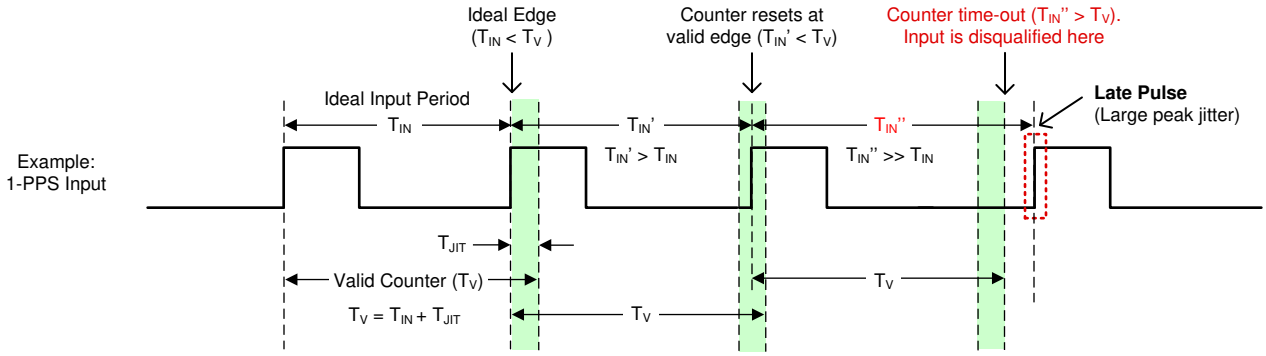



**Figure 9-19. 1-PPS Input Window Detector Example**

### *9.3.7.3 PLL Lock Detectors*

The loss-of-lock (LOL) status is available for APLL1, APLL2, and DPLL1, DPLL2, and DPLL3. The APLLs are monitored for loss-of-frequency lock only. The DPLL is monitored for both loss-of-frequency lock (LOFL) and loss-of-phase lock (LOPL). The DPLL lock threshold and loss-of-lock threshold are programmable for both LOPF and LOFL detectors.

The DPLL frequency lock detector will clear its LOFL flag when the DPLL's frequency error relative the selected reference input is less than the lock ppm threshold. Otherwise, it will set the LOFL flag when the DPLL's frequency error is greater than the unlock ppm threshold. The ppm delta between the lock and unlock thresholds provides hysteresis to prevent the LOFL flag from toggling when the DPLL frequency error is crossing these thresholds.

A measurement accuracy (ppm) and averaging factor are used in computing the frequency lock detector register settings. A higher measurement accuracy (smaller ppm) or higher averaging factor will increase the measurement delay to set or clear the LOFL flag. Higher averaging may be useful when locking to an input with high wander or when the DPLL is configured with a narrow loop bandwidth. Note that higher averaging reduces the maximum frequency ppm thresholds that can be configured.

The DPLL phase lock detector will clear its LOPL flag when the phase error of the DPLL is less than the phase lock threshold. Otherwise, the lock detector will set the LOPL flag when the phase error is greater than the phase unlock threshold.

Users can observe the APLL and DPLL lock detector flags through the status pins and the status bits.

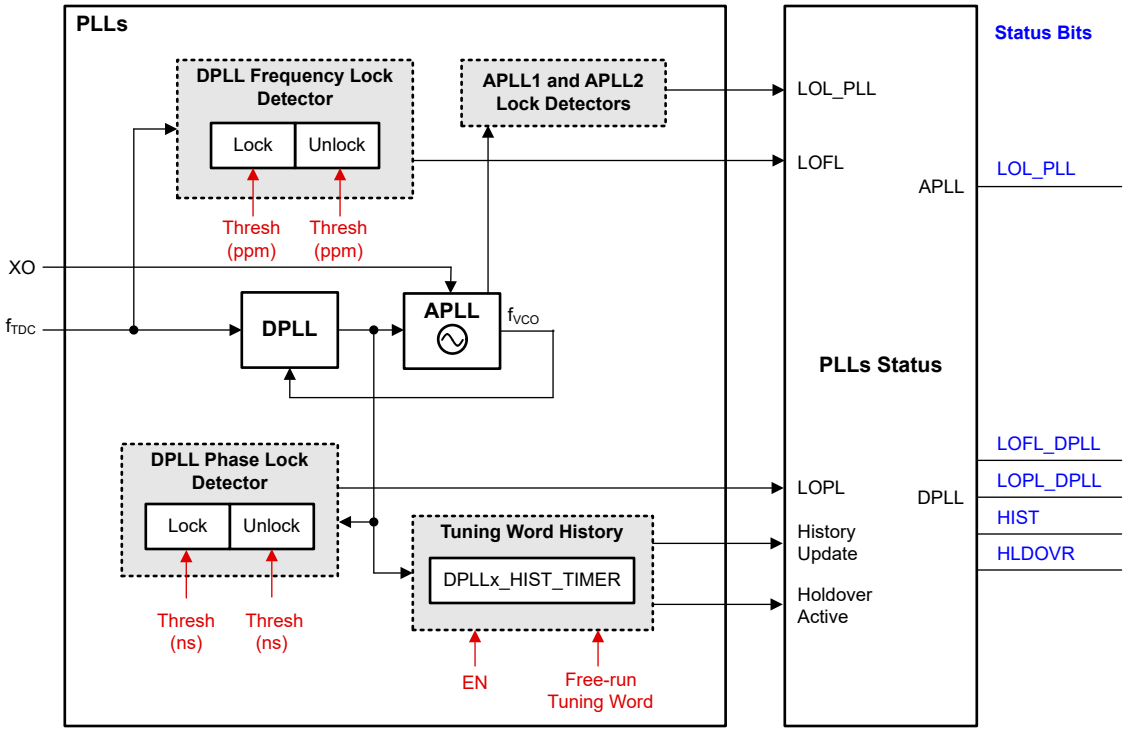



**Figure 9-20. PLL Lock Detectors and History Monitor**

### 9.3.7.4 Tuning Word History

The DPLL domain has a tuning word history monitor block that determines the initial output frequency accuracy upon entry into holdover. Once in holdover the stability of the reference clock (on XO input) determines the long-term stability and accuracy of the output frequency. The tuning word can be updated from one of three sources depending on the DPLL operating mode:

1. Locked Mode: from the output of the digital loop filter when locked
2. Holdover Mode: from the final output of the history monitor
3. Free Run Mode: from the free-run tuning word register (user defined)

When the history monitor is enabled and the DPLL is locked, the device averages the reference input frequency by accumulating history from the digital loop filter output during a programmable averaging time ($T_{AVG}$) set by DPLLx_HIST_TIMER. Once the input becomes invalid, the final tuning word value is stored to determine the initial holdover frequency accuracy. Generally, a longer $T_{AVG}$ time will produce a more accurate initial holdover frequency.

Because history data could be corrupted if a tuning word update occurs while the input clock is failing and before it is detected by the input monitors the most recent collected average is ignored. So the actual history used will be between greater than $T_{AVG}$ but less than 2 × $T_{AVG}$. Any in progress accumulation is ignored.

The tuning word history is initially cleared after a device hard reset or soft reset. After the DPLL locks to a new reference, the history monitor waits for the first $T_{AVG}$ timer to expire before storing the first tuning word value and begins to accumulate history. The history monitor will not clear the previous history value during reference switchover or holdover exit. The history can be manually cleared or reset by toggling the history enable bit (DPLLx_HIST_EN = 1 → 0 → 1), if needed.

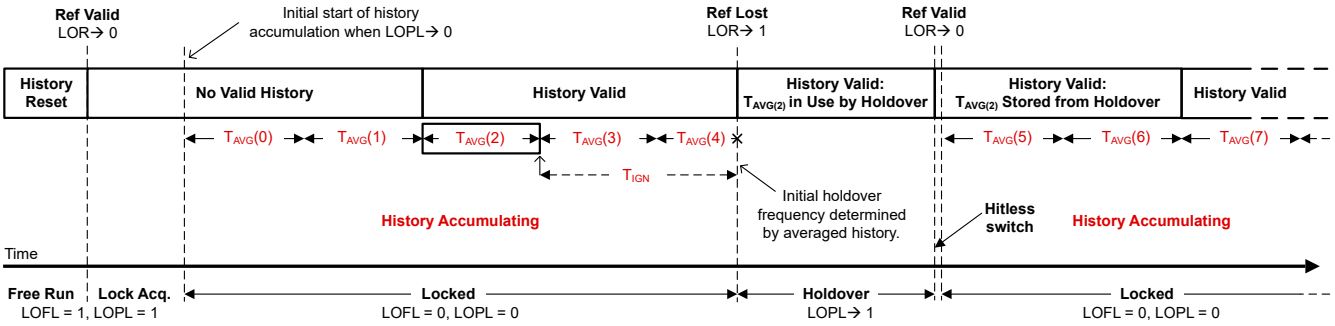



**Figure 9-21. Tuning Word History Windows**

When no tuning word history exists, the free-run tuning word value (DPLLx_FREE_RUN) is used and determines the initial holdover output frequency accuracy.

### 9.3.7.5 Status Outputs

The GPIO pins can be configured to output various status signals and interrupt flag for device diagnostic and debug purposes. The status signal, output driver type, and output polarity settings are programmable.

### 9.3.7.6 Interrupt

Any GPIO pin can be configured as a device interrupt output pin. The interrupt logic configuration is set through registers. When the interrupt logic is enabled, the interrupt output can be triggered from any combination of interrupt status indicators, including LOS for the XO, LOR for the selected DPLL input, LOL for APLL1, APLL2, and the DPLL, and holdover and switchover events for the DPLL. When the interrupt polarity is set high, a rising edge on the live status bit will assert its interrupt flag (sticky bit). Otherwise, when the polarity is set low, a falling edge on the live status bit will assert its interrupt flag. Any individual interrupt flag can be masked so it does not trigger the interrupt output. The unmasked interrupt flags are combined by the AND/OR gate to generate the interrupt output, which can be selected on either status pin.

When a system host detects an interrupt from the device, the host can read the interrupt flag or *sticky* registers to identify which bits were asserted to resolve the fault conditions in the system. After the system faults have been resolved, the host can clear the interrupt output by writing 1 to the self clearing INT_CLR field.

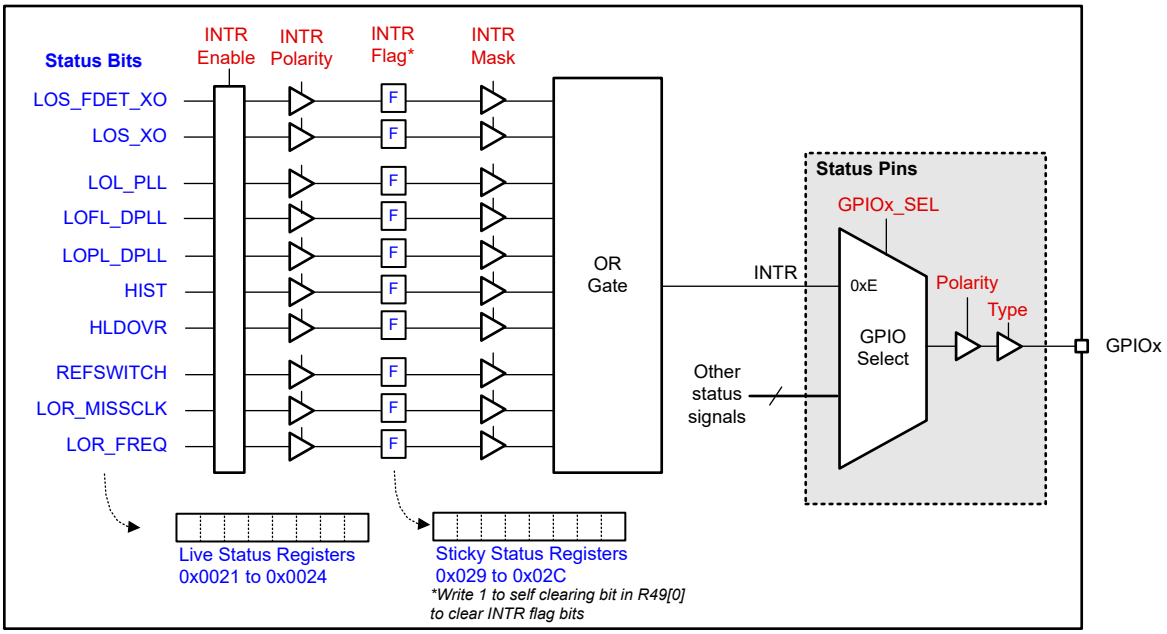



**Figure 9-22. Status and Interrupt**

### 9.3.8 PLL Relationships

Figure 9-23 shows the PLL architecture implemented in the LMK5C33216. The PLLs can be configured in the different PLL modes described in Section 9.2.1.

In each APLL, the denominator can be fixed 40-bit or programmable 24-bit. When an APLL works with a DPLL in a loop, APLL must use fixed 40-bit. When the APLL works in an independent loop, like APLL1 and APLL3 in Figure 9-6 or APLLs in Figure 9-7, 24-bit programmable denominator is recommended to enable 0-ppm error on output frequencies compared to source output.

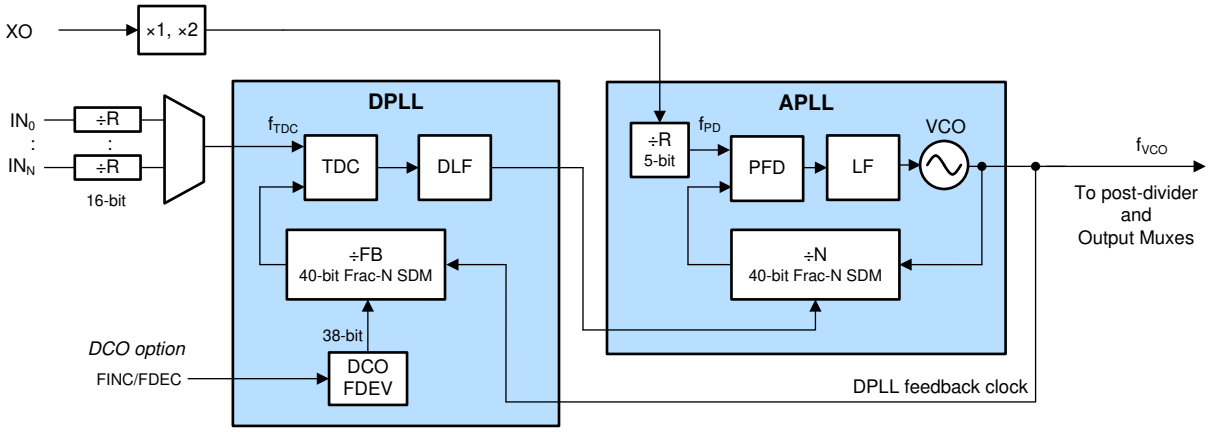



**Figure 9-23. PLL Architecture**

#### *9.3.8.1 PLL Frequency Relationships*

The following equations provide the APLL and DLL frequency relationships required to achieve closed-loop operation. The TICS Pro programming software can be used to generate valid divider settings based on the desired frequency plan.

Note that any divider in the following equations refer to the actual divide value (or range) and not its programmable register value.

When DPLL operation is enabled, the calculated DPLL frequency and APLL frequency must be nominally the same. It may not be possible for the APLL frequency to operate at the exact DPLL frequency when the APLL N divider 40-bit fixed denominator is selected, however the DPLL adjustments to the paired APLL will correct to the actual clock output frequency desired.

When the APLL operates independent of its paired DPLL, which tracks a reference cascaded from another APLL, it is advisable to select the programmable 24-bit fractional denominator to ensure that clock output frequencies from the cascaded APLL will have 0-ppm frequency error relative to the source PLL.

When using ZDM (zero delay mode) for a PLL, the clock output divider must be accounted for in the VCO frequency calculations.

#### 9.3.8.1.1 APLL Phase Detector Frequency

Equation 1 calculates the phase detector frequency which is used to find the VCO frequency in the APLL VCO Frequency calculation in Equation 2.

$$f_{PD} = f_{XO} \times D_{XO} / R_{XO} \quad (1)$$

where

- $f_{PD}$ = APLL phase detector frequency
- $f_{XO}$: APLL reference is XO frequency or cascaded refrence frequency from another APLL.
- $D_{XO}$: XO input doubler (0 = disabled, 1 = enabled)
- $R_{XO}$: APLL XO Input R divider value (1 to 32)

#### 9.3.8.1.2 APLL VCO Frequency

The APLL phase locks the APLL VCO to the APLL reference using the applied APLL numerator and is calculated using Equation 2.

$$f_{VCO} = f_{PD} \times (INT_{APLL} + NUM_{APLL} / DEN_{APLL}) \quad (2)$$

- $f_{VCO}$: VCO frequency
- $INT_{APLL}$: APLL N divider integer value (12 bits, 1 to $2^{12} – 1$)
- $NUM_{APLL}$: APLL N divider numerator value (40 bits, 0 to $2^{40} – 1$, or 24 bits, 0 to $2^{24} – 1$ )
- $DEN_{APLL}$: APLL N divider denominator value (fixed $2^{40}$, or programmable 1 to $2^{24}$)
  - Avoid integer boundary spurs by keeping the NUM/DEN ratio away from an integer value.
  - $0.125 < NUM_{APLL} / DEN_{APLL} < 0.875$ (In DPLL Mode, avoid 0.5)

#### 9.3.8.1.3 DPLL TDC Frequency

Equation 3 calculates the TDC frequency which is used to find the VCO frequency in the DPLL VCO Frequency calculation in Equation 5. Two different TDC frequencies are possible for each DPLL to enable switching between non-integer related frequencies while keeping the TDC rate high.

$$f_{TDC} = f_{INx} \times D_{INx} / R_{INx} \quad (3)$$

$$f_{TDC} = f_{INy} \times D_{INy} / R_{INy} \quad (4)$$

where

- $f_{TDC}$: DPLL TDC input frequency (see Equation 3)
- $f_{INx}$ or $f_{INy}$: INx or INy input frequency or cascaded refrence frequency from another APLL.
- $R_{INx}$ or $R_{INy}$: INx or INy R divider value (16 bits, 1 to $2^{16} – 1$)
- $D_{INx}$ or $D_{INy}$: INx or INy input doubler (0 = disabled and 1 = enabled)

#### 9.3.8.1.4 DPLL VCO Frequency

The DPLL phase locks the APLL VCO to the DPLL VCO frequency by updating the actual APLL numerator value and is calculated using Equation 5. Each DPLL can have two different values for DPLL N to allow locking to the same VCO frequency using two different TDC frequencies. DPLLx_REF#_FB_SEL register selects which DPLL N value is used.

$$f_{VCO} = f_{TDC} \times (INT_{DPLL} + NUM_{DPLL} / DEN_{DPLL}) \quad (5)$$

where

- $INT_{DPLL}$: DPLL FB divider integer value (33 bits, 1 to $2^{33} – 1$)
- $NUM_{DPLL}$: DPLL FB divider numerator value (40 bits, 0 to $2^{40} – 1$)
- $DEN_{DPLL}$: DPLL FB divider denominator value (40 bits, 1 to $2^{40}$)
- N: $INT_{DPLL} + NUM_{DPLL} / DEN_{DPLL}$

#### 9.3.8.1.5 Clock Output Frequency

Each APLL has a post divider which will provide a VCO post divider frequency calculated in Equation 6, Equation 7, or Equation 8. The final output frequency is calculated by dividing from the VCO post divider frequency and the output divide as calculated in Equation 9. For each output, the output frequency depends on the selected APLL clock source and output divider value.

$$\textbf{APLL1 selected: } f_{POST\_DIV} = f_{VCO1} / Pn_{APLL1} \quad (6)$$

$$\textbf{APLL2 selected: } f_{POST\_DIV} = f_{VCO2} / Pn_{APLL2} \quad (7)$$

$$\textbf{APLL3 selected: } f_{POST\_DIV} = f_{VCO3} / Pn_{APLL3} \quad (8)$$

$$\textbf{OUT[0:15]: } f_{OUTx} = f_{POST\_DIV} / OD_{OUTx} \quad (9)$$

where

- $f_{POST\_DIV}$: Output mux source frequency (APLL1, APLL2 or APLL3 post-divider clock)
- $Pn_{APLL1}$: APLL1 primary "P1" or secondary "P2" post-divide value (2 to 7)
- $Pn_{APLL2}$: APLL2 primary "P1" post-divide value (2 to 13) or secondary "P2" post-divide value (2 to 3)
- $Pn_{APLL3}$: APLL3 post-divide value (1 to 7)
- $f_{OUTx}$: Output clock frequency (x = 0 to 15)
- $OD_{OUTx}$: OUTx output bypass or divider value. All outputs have a 12-bit divider with values 1 to ($2^{12}$ - 1). All outputs except OUT2, OUT3, OUT14, and OUT15 have the option to follow the 12-bit divider with a 20-bit SYSREF divider that can be used to produce 1-PPS or other frequencies below 1 Hz when the SYSREF output is set for continuous output.

### *9.3.8.2 Analog PLLs (APLL1, APLL2, APLL3)*

Each APLL has a 40-bit fractional-N divider to support high-resolution frequency synthesis and very low phase noise and jitter, has the ability to tune its VCO frequency through sigma-delta modulator (SDM) control in DPLL mode. In cascaded mode, each APLL has the ability to lock its VCO frequency to another VCO frequency.

In free-run mode, APLL3 uses the XO input as an initial reference clock to its VCO3. APLL3's PFD compares the fractional-N divided clock with its reference clock and generates a control signal. The control signal is filtered by the APLL3 loop filter to generate VCO3's control voltage to set its output frequency. The SDM modulates the N divider ratio to get the desired fractional ratio between the PFD input and the VCO3 output. APLL1 or APLL2 operates similar to APLL3. User can select the reference from either the VCO3 clock or XO clock.

In DPLL mode, the APLL fractional SDM is controlled by the DPLL loop to pull the VCO frequency into lock with the DPLL reference input. For example, as Figure 9-6, if DPLL1 or DPLL2 is disabled, the respective APLL1 or APLL2 derives its reference from VCO3, then VCO1 or VCO2 will be effectively locked to the DPLL3 reference input, assuming there is no synthesis error introduced by the fractional N divide ratio of APLL1 or APLL2.

### *9.3.8.3 APLL Reference Paths*

#### 9.3.8.3.1 APLL XO Doubler

The APLL XO doubler can be enabled to double the PFD frequency for the APLL reference. Enabling the XO doubler adds minimal noise and can be useful to increase the PFD frequency to optimize phase noise, jitter, and fractional spurs. The flat portion of the APLL phase noise can improve when the PFD frequency is increased.

#### 9.3.8.3.2 APLL XO Reference (R) Divider

Each APLL has a 5-b XO reference (R) divider that can be used to meet the maximum APLL PFD frequency specification. It can also be used to ensure the APLL fractional-N divide ratio (NUM/DEN) is between 0.125 to 0.875 (avoid 0.5), which is recommended to support the DPLL frequency tuning range. Otherwise, the R divider can be bypassed (divide by 1).

### 9.3.8.4 APLL Phase Frequency Detector (PFD) and Charge Pump

APLL1 has programmable charge pump settings of 1.6, 3.2, 4.8, or 6.4 mA. APLL2 or APLL3 has programmable charge pump settings from 0 to 5.8 mA in 0.4-mA steps. Best performance from APLL3 is achieved with a charge pump currents of 0.8 mA or higher.

### 9.3.8.5 APLL Feedback Divider Paths

The VCO output of each APLL is fed back to its PFD block through the fractional feedback (N) divider. The VCO output is also fed back to the DPLL feedback path in DPLL mode. Each VCO output also can supply as an XO input for other APLLs through a fixed feedback divider.

#### 9.3.8.5.1 APLL N Divider with SDM

The APLL fractional N divider includes a 12-b integer portion (INT), a 40-b numerator portion (NUM), a fixed 40-b or a programmable 24-b denominator portion (DEN), and a sigma-delta modulator. The INT and NUM are programmable. When an APLL works with a DPLL in a loop, APLL can use fixed 40-bit for very high frequency resolution on the VCO clock. When the APLL works in an independent loop, like APLL1 and APLL2 in Figure 9-6or APLLs in Figure 9-7, 24-bit programmable denominator is recommended. The total APLL N divider value is: N = INT + NUM / $2^{40}$ or INT + NUM / $2^{24}$ .

In APLL free-run mode, the PFD frequency and total N divider for APLL determine the VCO frequency, which can be computed with 24-b denominator by Equation 2.

### 9.3.8.6 APLL Loop Filters (LF1, LF2, LF3)

APLL3 supports a programmable loop bandwidth from 100 Hz to 10 kHz (typical range), and APLL1 or APLL2 supports a programmable loop bandwidth from 100 kHz to 1 MHz (typical range). The loop filter components can be programmed to optimize the APLL bandwidth depending on the reference input frequency and phase noise. The LF1, LF2, and LF3 pins each require an external "C2" capacitor to ground. See the suggested values for the LF1, LF2, and LF3 capacitors in Section 6.

Figure 9-24 shows the APLL loop filter structure between the PFD/charge pump output and VCO control input.

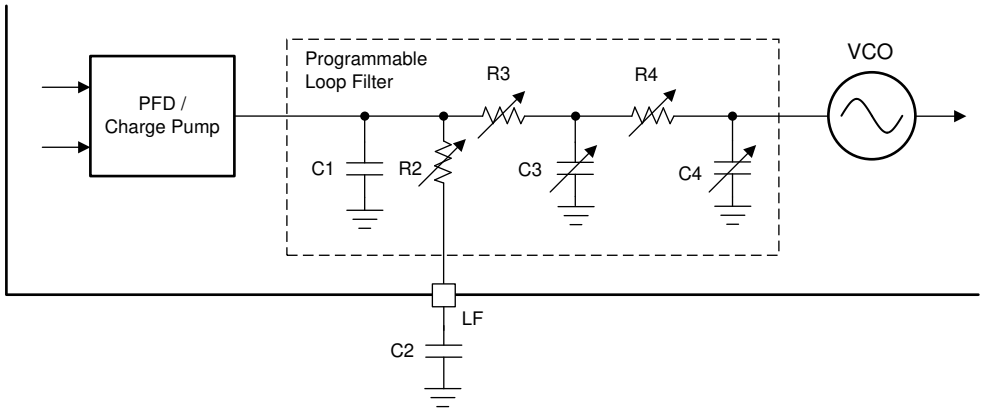



**Figure 9-24. Loop Filter Structure of Each APLL**

### 9.3.8.7 APLL Voltage Controlled Oscillators (VCO1, VCO2, VCO3)

Each APLL contains a fully-integrated VCO, which takes the voltage from its loop filter and converts this into a frequency. VCO1 uses a standard-performance LC VCO with a wider tuning range of 4800 MHz to 5350 MHz. VCO2 uses a high-performance LC VCO with a wider tuning range of 5600 MHz to 5950 MHz to cover other additional unrelated clock frequencies, if needed. VCO3 uses proprietary BAW resonator technology with a very high quality factor to deliver the lowest phase jitter and has a tuning range of 2457.6 MHz ± 50 ppm.

#### 9.3.8.7.1 VCO Calibration

Each APLL VCO must be calibrated to ensure that the PLL can achieve lock and deliver optimal phase noise performance. VCO calibration establishes an optimal operating point within the VCO tuning range. VCO calibration is executed automatically during initial PLL start-up after device power-on, hard-reset, or soft-reset once the XO input is detected by its input monitor. To ensure successful calibration and APLL lock, it is critical for the XO clock to be stable in amplitude and frequency before the start of calibration; otherwise, the calibration can fail and prevent PLL lock and output clock start-up. Before VCO calibration and APLL lock, the output drivers are typically held in the mute state (configurable per output) to prevent spurious output clocks.

A VCO calibration can be triggered manually for a single APLL by toggling a PLL enable cycle (APLLx_EN bit = 0 → 1) through host programming. This may be needed after the APLL N divider value (VCO frequency) is changed dynamically through programming.

### *9.3.8.8 APLL VCO Clock Distribution Paths*

APLL1 has two VCO post-dividers. The primary VCO1 post-divider clock (P1: ÷2 to ÷7) is distributed for OUT0, OUT1, OUT2, OUT3, OUT14, and OUT15 in LMK5C33216. The secondary VCO1 post-divider clock (P2: ÷2 to ÷7) are distributed for OUT0, OUT1, OUT2, and OUT3 in LMK5C33216.

APLL2 has two VCO2 post-dividers to provide more flexible clock frequency planning. The primary VCO2 post-divider clock (P1: ÷2 to ÷13) is distributed to all outputs, and secondary post-divider clock (P2: ÷2 to ÷3) is distributed to OUT4 and OUT6 for CML output.

APLL3 has one VCO post-divider. The VCO3 post-divider clock (÷1 to ÷7) is distributed for OUT0, OUT1, OUT4 to OUT15 in LMK5C33216.

Each VCO post-divider supports an independently programmable divider.

### *9.3.8.9 DPLL Reference (R) Divider Paths*

Each reference input clock has its own 16-b reference divider to the DPLL TDC block. The R divider output of the selected reference sets the TDC input frequency. To support hitless switching between inputs with different frequencies, the R dividers can be used to divide the clocks to a single common frequency to the DPLL TDC input.

### *9.3.8.10 DPLL Time-to-Digital Converter (TDC)*

The TDC input compares the phase of the R divider clock of the selected reference input and the DPLL feedback divider clock from VCO. The TDC output generates a digital correction word corresponding to the phase error which is processed by the DPLL loop filter.

### *9.3.8.11 DPLL Loop Filter (DLF)*

The DPLL supports a programmable loop bandwidth from 10 mHz to 4 kHz and can achieve jitter peaking below 0.1 dB (typical). The low-pass jitter transfer characteristic of the DPLL attenuates its reference input noise with up to 60-dB/decade roll-off above the loop bandwidth.

The DPLL loop filter output controls the fractional SDM of APLL to steer the VCO frequency into lock with the selected DPLL reference input.

### *9.3.8.12 DPLL Feedback (FB) Divider Path*

The DPLL feedback path has a programmable prescaler (33 bits, 1 to $2^{33}$-1) and a fractional feedback (FB) divider. The programmable DPLL FB divider includes a 33-b integer portion (INT), 40-b numerator portion (NUM), and 40-b denominator portion (DEN). The total DPLL FB divider value is: $FB_{DPLL}$ = INT + NUM / DEN.

In DPLL mode, the TDC frequency and total DPLL feedback divider and prescalers determine the VCO frequency, which can be computed by Equation 5.

### 9.3.9 Output Clock Distribution

The output clock distribution blocks include eight output muxes, eleven output dividers, and sixteen programmable output drivers in LMK5C33216. The output dividers support output synchronization (SYNC) to allow phase synchronization between two or more output channels. Also, the channel OUT0, OUT4, or OUT10 has an optional zero-delay mode (ZDM) synchronization feature to support deterministic input-to-output phase alignment (typically for 1-PPS clocks) with programmable offset. OUT0 may provide ZDM feedback to any DPLL, OUT4 for DPLL2, and OUT10 for DPLL3.

### 9.3.10 Output Channel Muxes

All output channels share eight (LMK5C33216) output muxes. Each output mux for the OUT0 and OUT1 channels can individually select a source among XO, the PLL1 VCO clocks (P1 or P2), the PLL2 VCO clock (P1), the PLL3 VCO clock, and the references Mux clock. Either OUT2 or OUT3 has one output Mux respectively, which can source from PLL1 VCO clocks (P1 or P2), the PLL2 VCO clock (P1). Either OUT14 or OUT15 has one output Mux respectively, which can source from the PLL1 VCO clocks (P1), the PLL2 VCO clock (P1) and the PLl3 VCO clocks (P1). OUT4 to OUT7 share one Mux, OUT8 to OUT13 share one Mux. These two Muxes can source from the PLL2 VCO clock (P1) and the PLL3 VCO clock. OUT4 and OUT6 also can source from the PLL2 VCO clock (P2) directly.

### 9.3.11 Output Dividers (OD)

There are one or more output dividers after each output mux. Each channel in OUT[0:1] has an individual 12-bit channel divider cascaded an optional 20-bit SYSREF divider. Each channel in OUT[2:3] and OUT[14:15] has an individual 12-bit output divider. The OUT[4:5] channel has a single 12-bit output divider cascaded an optional SYSREF divider that is similar to the OUT[6:7] channel output divider, as well as OUT[8:9], OUT[10:11] or OUT[12:13]. The output dividers are used to generate the final clock output frequency from the source selected by the output mux.

Each 12-bit channel divider (CD) can support output frequencies from 86 kHz to 1000 MHz (or up to the maximum frequency supported by the configured output driver type). It is possible to configure the PLL post-divider (P) and output channel divider (CD), bypass SYSREF divider (SD) to achieve higher clock frequencies, but the output swing of the driver may fall out of specification.

OUT4 and OUT6 can source from PLL2 VCO clock (P2) directly, bypass the output channel Mux and output dividers, and output normal swing or high swing CML clocks up to 3000 MHz.

The OUT0 or OUT1 channel combines a 12-bit output channel divider (CD) and a 20-bit SYSREF divider to support output frequencies from 1 Hz (1 PPS) to 1000 MHz. From VCO to output, the total divide value is the product of the PLL post-divider (P), output channel divider (CD)and SYSREF divider (SD) values (P × CD × SD).

Each output divider is powered from the same VDDO_x supply used for the clock output drivers. The output divider can be powered down if not used to save power. For each output group in OUT[2:3], OUT[4:5], OUT[6:7], OUT[8:9], OUT[10:11], OUT[12:13], or OUT[14:15], the output divider is automatically powered down when both output drivers are disabled. For OUT0 or OUT1 channel, the output divider is automatically powered down when its output driver is disabled.

### 9.3.12 SYSREF

LMK5C33216 can support JEDEC JESD204B or JESD204C SYSREF clocks. Except OUT[2:3] and OUT[14:15], each of all other output channel dividers can be cascaded an individual SYSREF divider. Set flexible SYSREF divider values to generate the same frequency SYSREFs or different frequency SYSREFs based on application requirements.

### 9.3.13 Output Delay

LMK5C33216 have the ability to tune output clock phase with delay function. In each channel divider path, there is a programmable static offset digital delay. With the SYSREF divider selected, the output clock can have additional programmable static offset digital delay, SYSREF digital delay and analog delay.

### 9.3.14 Clock Outputs (OUTx_P/N)

Each clock output can be individually configured as a differential driver (LVDS/HSDS/LVPECL). OUT4 or OUT6 can choose additional CML open collector mode. OUT0 or OUT1 has additional 1.8-V or 2.65-V LVCMOS drivers (two per pair). Otherwise, it can be disabled to save power if not used.

Each output channel has its own internal LDO regulator to provide excellent PSNR and minimize jitter and spurs induced by supply noise. The OUT0 and OUT1 channel (mux, divider, and drivers) are powered through a single output supply pin (VDDO_0_1), and similarly for the OUT2 and OUT3 channel (VDDO_2_3). OUT4 to OUT7 channels have their own output supply pin (VDDO_4_TO_7). OUT8 to OUT13 channels have their own output supply pin (VDDO_8_TO_13). OUT14 and OUT15 channels have their own output supply pin (VDDO_14_15). Each output supply pin should be powered by 3.3 V and always connected to the supply even if not used. CMOS output voltage levels are determined by internal programming of the CMOS output LDO to support either 1.8-V or 2.65-V LVCMOS.

For differential modes, the output clock specifications (such as output swing, phase noise, and jitter) are not sensitive to the VDDO_x voltage because of the channel's internal LDO regulator. LVDS/HSDS/LVPECL drivers have the capability to program output voltage swing and common mode. CML driver can support either normal output voltage swing or high output voltage swing. When an output channel is left unpowered, the channel's output(s) will not generate any clocks.

**Table 9-3. Output Driver Modes**

| OUT_x_MODE[2:0] | OUTPUT FORMAT(1) |
|---|---|
| 0x0 | Disabled (powered-down) |
| 0x1 | LVDS |
| 0x2 | LVPECL |
| 0x3 | HSDS |
| 0x4 | CMOS |
| 0x5 | CML Open Collector |

(1) LVCMOS formats are only available on OUT0 and OUT1. CML Open Collector type format is only available on OUT4 and OUT6.

#### *9.3.14.1 Differential Output*

The programmable differential output driver can be programmed to achieve $V_{OD}$ swing compatible with LVDS, CML, LVPECL, and other differential receivers, respectively, across a 100-Ω differential termination. The differential output drivers can all be DC coupled or AC coupled.

The LVDS and HSDS differential drivers have internal biasing **so external pullup or pulldown resistors should not be applied.** External pulldown resistors are needed for LVPECL driver format. External pullup inductors and/or resistors are required for the open collector CML outputs.

The device has the ability to adjust DC offsets at the clock outputs for LVPECL, LVDS, and HSDS output formats. The range of DC common modes supported does vary some for each output type, due to internal output buffer structure limitations. DC common mode output voltages have a step size of around 100 mV. Some of the lower DC common mode voltages (0.4 to 0.6 V) may only be possible for LVPECL configured outputs. The ability to be able to DC couple was directly aimed at SYSREF output modes to support pulsed mode operation. Typically the differential output should be interfaced through external AC-coupling to a differential receiver with proper input termination and biasing for most clocking applications.

The differential multi-format drivers are available on all output channels (LVPECL, LVDS, HSDS formats) and can work up to 1 GHz. There will be minimal time delay offset change over temperature for all of the differential multi-format driver output modes, since they are all derived from roughly the same output buffer critical speed paths.

Open collector CML output modes of up to 2975 MHz are only supported on output channels 4 and 6, either in bypass mode from the VCO3 or VCO2 divide by 2 or 3 straight to those outputs.

#### 9.3.14.2 LVCMOS Output

The LVCMOS driver has two outputs per pair. Each output on P and N can be configured for normal polarity, inverted polarity, or disabled as Hi-Z or static low level. The LVCMOS output high level ($V_{OH}$) is determined by the internal programmable LDO regulator voltage of 1.8 V or 2.65 V for rail-to-rail LVCMOS output voltage swing. LVCMOS mode is only supported on channel outputs 0 and 1 and is primarily there to support ASIC or processor clock which don't require stringent phase noise floor requirements.

Because an LVCMOS output clock is an unbalanced signal with large voltage swing, it can be a strong aggressor and couple noise onto other jitter-sensitive differential output clocks. If an LVCMOS clock is required from an output pair, configure the pair with both outputs enabled but with opposite polarity (+/– or –/+) and leave the unused output floating with no trace connected.

#### 9.3.14.3 Output Auto-Mute During LOL

Each output driver can automatically mute its clock when the selected output mux clock source is invalid, as configured by its MUTE enable field. The source can be invalid based on the LOL status of each PLL by configuring the APLL and DPLL mute control bits (MUTE_APLLx_LOCK, MUTE_DPLLx_LOCK, MUTE_DPLLx_PHLOCK). When auto-mute is disabled or bypassed (OUT_x_y_MUTE_EN = 0), the output clock can have incorrect frequency or be unstable before and during the VCO calibration.

### 9.3.15 Glitchless Output Clock Start-Up

When APLL auto-mute is enabled, the outputs will start up in synchronous fashion without clock glitches once APLL lock is achieved after any the following events: device power-on, exiting hard-reset, exiting soft-reset, or deasserting output SYNC.

### 9.3.16 Clock Output Interfacing and Termination

Figure 9-25 to Figure 9-29 show the recommended output interfacing and termination circuits. Unused clock outputs can be left floating and powered down by programming.

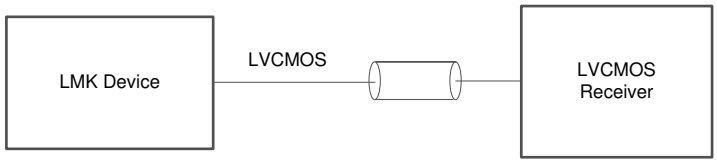



**Figure 9-25. 1.8-V or 2.65-V LVCMOS Output to LVCMOS Receiver**

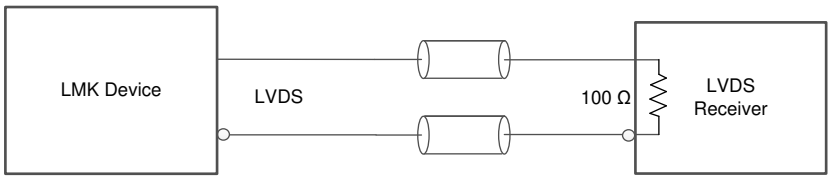



**Figure 9-26. LVDS/HSDS Output DC coupling to LVDS Receiver**

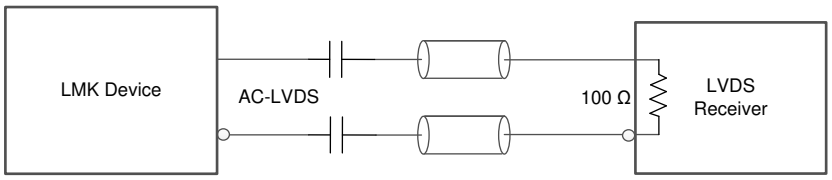



**Figure 9-27. LVDS/HSDS Output AC coupling to LVDS Receiver with Internal Termination/Biasing**

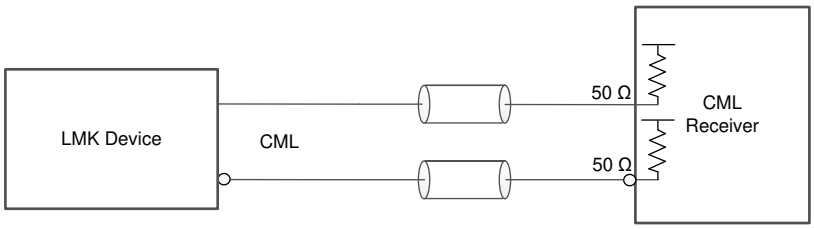



**Figure 9-28. CML Open Collector Output to CML Receiver**

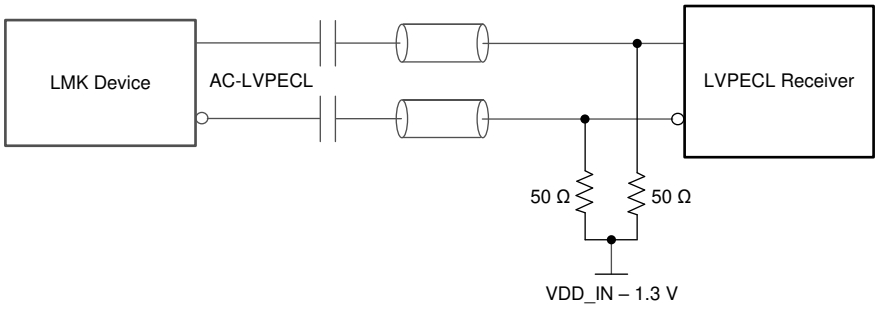



**Figure 9-29. LVPECL Output AC coupling to LVPECL Receiver With External Termination/Biasing**

### 9.3.17 Output Synchronization (SYNC)

Output SYNC can be used to phase-align two or more output clocks with a common rising edge by allowing the output dividers to exit reset on the same PLL output clock cycle. Any output dividers selecting the same PLL output can be synchronized together as a SYNC group by triggering a SYNC event through the hardware pin or software bit.

The following requirements must be met to establish a SYNC group for two or more output channels:

- Output dividers have their respective sync enable bit set (OUT_x_y_DIV_SYNC_EN = 1).
- SYSREF dividers have their additional respective sync enable bit set (OUT_x_y_SR_DIV_SYNC_EN = 1), work with above set (OUT_x_y_DIV_SYNC_EN = 1)
- Output dividers have their output mux selecting the same PLL output.
- The PLL (post-divider) output has its sync enable bit set (for example, PLL1_PRI_DIV_SYNC_EN = 1).
- SYNC_EN = 1

A SYNC event can be asserted by either a GPIOx pin programmed for SYNC input with GPIOx_MODE = 31 or the SYNC_SW register bit (active high). When SYNC is asserted, the SYNC-enabled dividers are held in reset and clock outputs are low. When SYNC is deasserted, the outputs from a common PLL will start with their initial clock phases synchronized or aligned. SYNC can also be used to set a low state on any SYNC-enabled outputs

to prevent output clocks from being distributed to downstream devices until they are configured and ready to accept the incoming clock.

Output channels with their sync disabled (OUT_x_y_DIV_SYNC_EN = 0) will not be affected by a SYNC event and will continue normal output operation as configured. VCO post-divider clocks must be enabled for synchronization to ensure the dividers they drive are synchronized accurately. However, any output deriving a clock from a reset VCO post-divider will not be valid during SYNC, even if the channel divider is not selected for SYNC. VCO post-dividers not selected for synchronization do not stop running during the SYNC so they can continue to source output channels that do not require synchronization. Output dividers with divide-by-1 (divider bypass mode) are not gated during the SYNC event.

**Table 9-4. Output Synchronization**

| GPIOx as SYNC PIN GPIOx_MODE = 31 | | SYNC_SW R21[6] | OUTPUT DIVIDER AND DRIVER STATE |
|---|---|---|---|
| GPIOx_POL = 0 | GPIOx_POL = 1 | | |
| 1 | 0 | 1 | Output driver(s) muted and output divider(s) reset |
| 1 → 0 | 0 → 1 | 1 → 0 | SYNCed outputs are released with synchronized phase |
| 0 | 1 | 0 | Normal output driver/divider operation as configured |

### 9.3.18 Zero-Delay Mode (ZDM) Synchronization

Zero-delay mode synchronization can be enabled to achieve *zero* phase delay between the selected DPLL reference input clock and the selected zero-delay feedback clock. OUT0 clock can feedback to any DPLL for zero-delay as shown in Figure 9-30. This is primarily used to achieve deterministic phase relationship between an input and some outputs, for example, 1-PPS input and 1-PPS output.

In addition to OUT0, for DPLL2, OUT4 may be used for ZDM. For DPLL3, OUT10 may be used for ZDM.

1-PPS phase alignment is able to re-establish with the phase slew control and ZDM. For 1-PPS and ZDM, hitless switching must be enabled to prevent the DPLL from becoming unlocked. After preforming hitless switching, the phase slew control can reduce the phase build out back to 0 at a controlled rate. Input to output phase error is user programmable using the DPLLx_PH_OFFSET field. To lock to a 1-PPS signal using ZDM mode, the output static delay or DPLLx_PH_OFFSET must be programmed to zero out the phase error between the 1 PPS input and 1 PPS feedback clock.

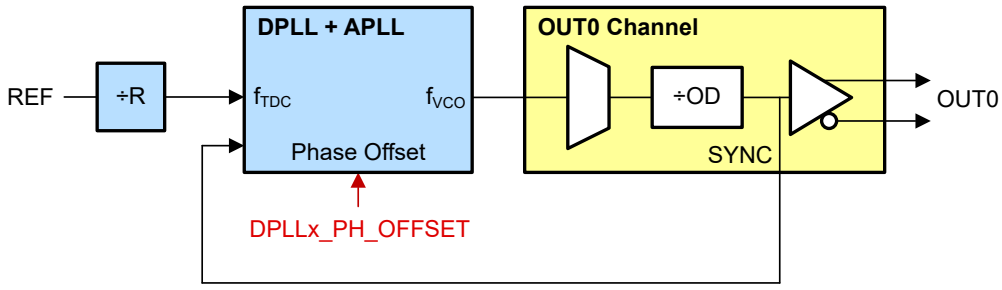



**Figure 9-30. DPLL ZDM Synchronization Between Reference Input and OUT0**

### 9.3.19 Time of Day (ToD) Counter

The Time of Day (ToD) counter allows the user to make a precise time measurement between two (or more) events. The events may be either a rising or falling edge of a GPIO pin or a falling edge of the SPI SCS pin. Any GPIO pin can be programmed for ToD Input. Rising or falling polarity can be chosen using the GPIO polarity invert register. After each ToD event, the counter values is captured and the application may read back a 40-bit value. The elapsed time is calculated based on the difference in the read back values. The accuracy of the measurement is better than 7.5 ns with a total measurement time over 59 minutes depending on exact configuration. It is necessary to read back at least the LSB of the TOD_CNTR to re-arm the ToD counter capture.

The ToD counter is clocked at a frequency based on PLL2 VCO frequency ÷ 20 or PLL3 VCO frequency ÷8. A time measurement is made by below steps.

1. Reset the ToD counter value. Recommended to reduce chance of counter roll-over between ToD capture events, but optional. If the reset is not done the user would need to detect roll-over of counter register which will complicate Equation 10 for elapsed time calculation.
2. Trigger ToD capture event and read back the ToD registers containing the stored counter value.
3. Trigger the ToD capture event a second time and read back the ToD registers containing the stored counter value.
4. The elapsed time can be found by equation Equation 10. The worst case error is twice the ToD counter clock period. Table 9-5 lists some common ToD clock frequencies/periods and roll-over times.

$$\text{Elapsed Time} = (\text{2nd captured ToD value} - \text{1st captured ToD value}) / \text{ToD Clock Rate} \quad (10)$$

The TOD_CNTR register is split across five registers.

**Table 9-5. Common ToD Clock Frequencies and Roll-over times**

| PLL Source | VCO Frequency | ToD Clock Frequency | ToD Clock Period (t) | Roll-over time |
|---|---|---|---|---|
| PLL3 | 2457.6 MHz | 307.2 MHz | ~3.225 ns | ~59.6 minutes |
| PLL2 | 5950 MHz | 297.5 MHz | ~3.361 ns | ~61.6 minutes |
| PLL2 | 5898.24 MHz | 294.912 MHz | ~3.391 ns | ~62.1 minutes |
| PLL2 | 5625 MHz | 281.25 MHz | ~3.556 ns | ~65.1 minutes |
| PLL2 | 5600 MHz | 280 MHz | ~3.571 ns | ~65.4 minutes |

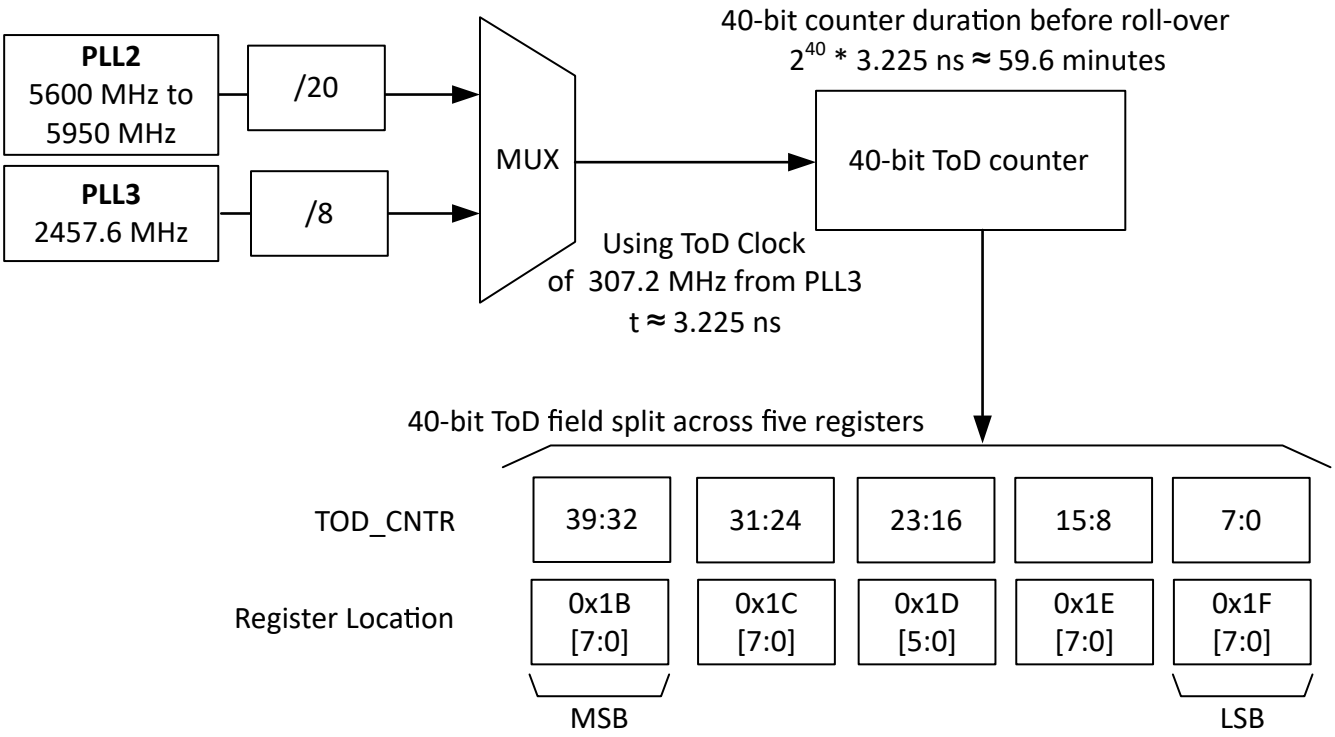



**Figure 9-31. ToD Clock and Counter**

Figure 9-32 illustrates the states of the Time of Day function.

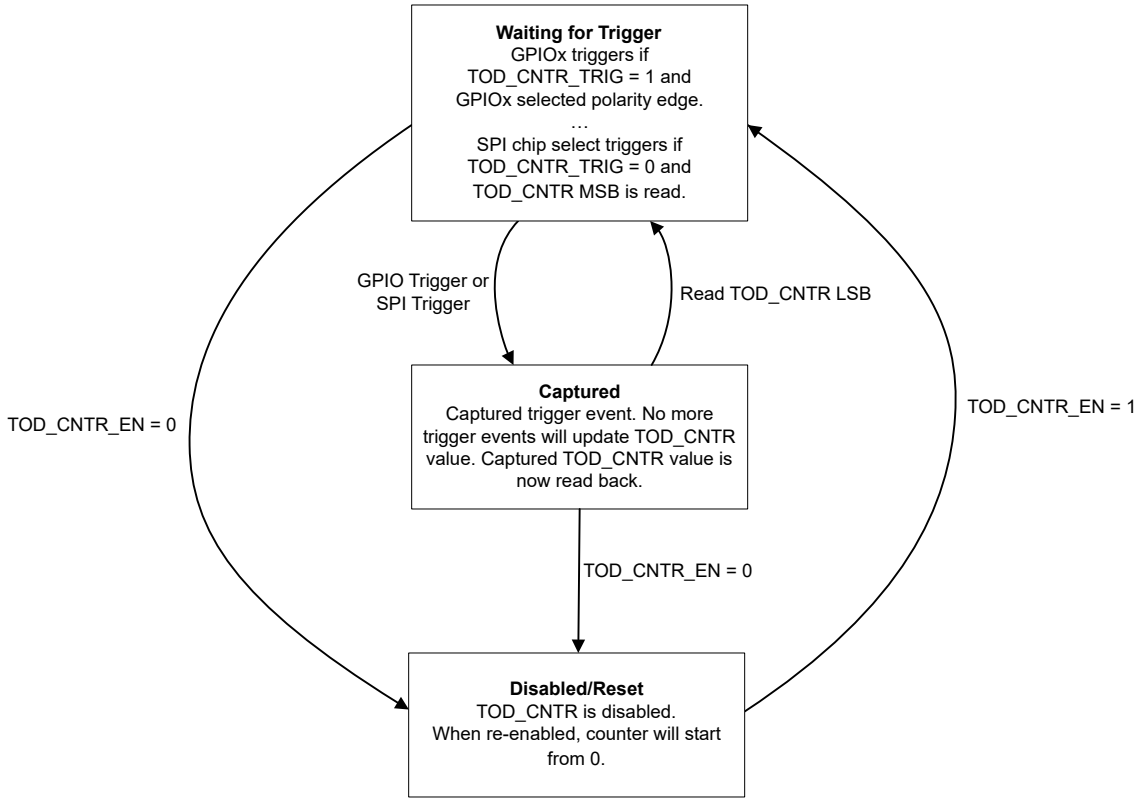



**Figure 9-32. State Diagram of ToD**

### *9.3.19.1 Configuring ToD Functionality*

1. Select the PLL to drive the ToD counter. PLL3 will offer the highest accuracy time measurement due to the highest ToD clock frequency, however PLL2 provides slightly longer roll-over times.
   - PLL3 source is selected by setting REF0_MISSCLK_VCOSEL to 0.
   - PLL2 source is selected by setting REF0_MISSCLK_VCOSEL to 1.
2. Select GPIO or SPI chip select as a trigger to capture the ToD counter value to TOD_CNTR field. Using a GPIO does not require any special timing for the SPI SCS pin. It is possible to use the GPIO pin for other purposes, then enable the ToD functionality when required.
   - GPIO trigger is selected by setting TOD_CNTR_TRIG to 1.
   - SPI chip select trigger is selected by setting TOD_CNTR_TRIG to 0.
3. Enable the time of day counter by setting TOD_CNTR_EN to 1.

### *9.3.19.2 SPI as a Trigger Source*

When TOD_CNTR_EN = 1, each SCS falling edge the ToD counter will be captured to the TOD_CNTR field. Subsequent to a SPI transaction which reads from the MSB of the TOD_CNTR field, no falling edge of SCS will capture the ToD counter to the TOD_CNTR field until the LSB of the TOD_CNTR field is read.

Figure 9-33 illustrates when the ToD is latched during single register reads and Figure 9-34 for a multibyte read.

Figure 9-33 shows ToD counter is captured every falling SCS edge until TOD_CNTR MSB is read.

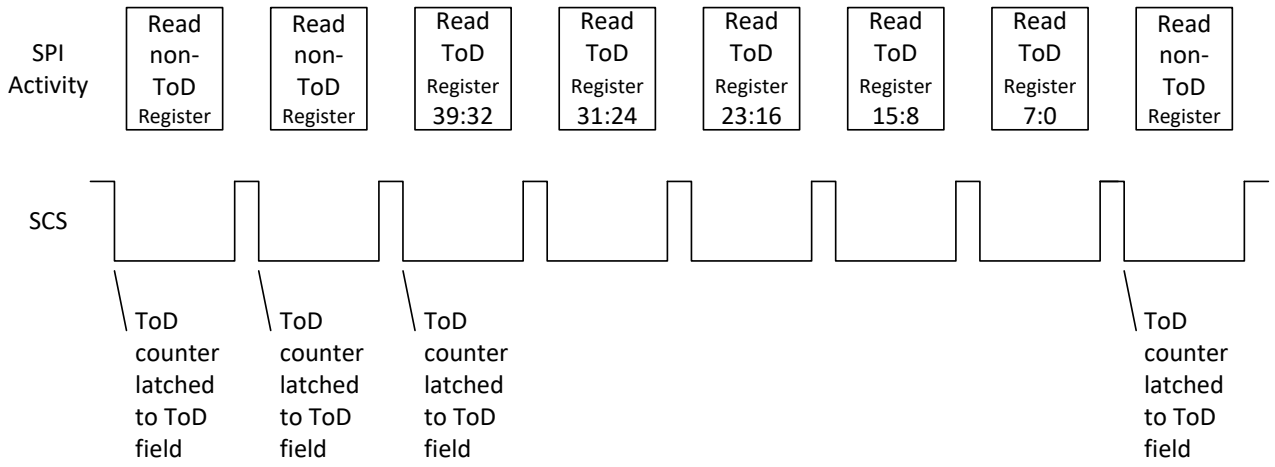



**Figure 9-33. ToD Single Byte Read**

Figure 9-34 ToD counter value can be captured and re-armed for capture during a single multibyte read, even if the first register read is not the TOD_CNTR registers.

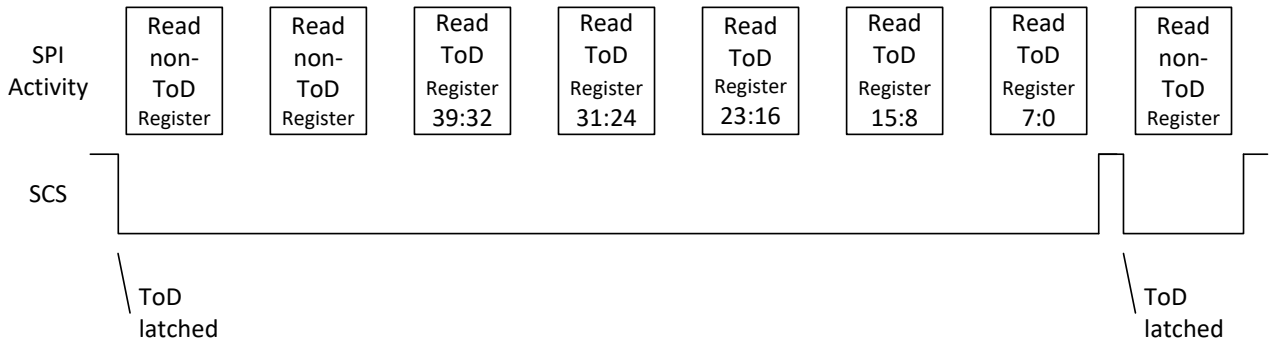



**Figure 9-34. ToD Multibyte Read**

#### *9.3.19.3 GPIO Pin as a ToD Trigger Source*

A rising edge of a GPIO pin selected for ToD functionality with GPIOx_MODE = 0x27 (TOD_TRIG_SEL) will capture the ToD counter value to the TOD_CNTR field upon an edge of the selected polarity (GPIOx_POL). No further updates to the TOD_CNTR field will be made by subsequent GPIO1 pin edges until the LSB of the TOD_CNTR field is read. Figure 9-35 illustrates the timing of using GPIO1 to capture ToD counter.

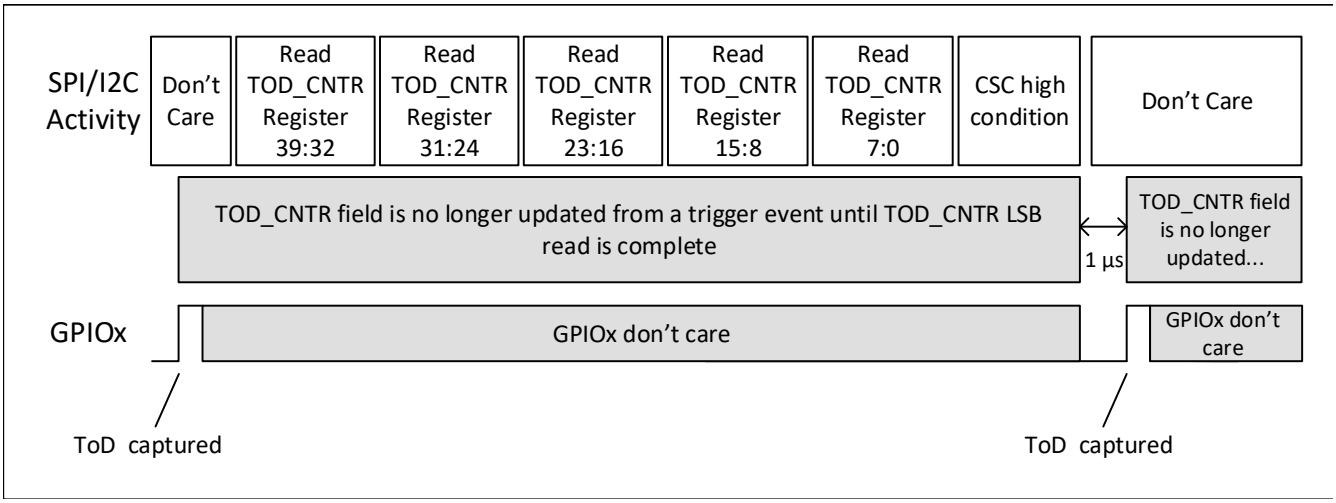



**Figure 9-35. ToD Counter Captured Using GPIO1**

#### 9.3.19.3.1 An Example: Making a time measurement using ToD and GPIO1 as trigger

1. Configure ToD registers as desired. In this example:
   - REF0_MISSCLK_VCOSEL is 0 so that VCO3 frequency / 8 is used for ToD clock rate
   - TOD_CNTR_TRIG = 1 for GPIO1 trigger
   - TOD_CNTR_CLR = 0 for normal operation
2. Set GPIO1_MODE = 0x27 (TOD_TRIG_SEL) and GPIO1_POL as desired, 0 in this example for active high input.
3. Provide rising edge on GPIO1 to capture current ToD counter value into the TOD_CNTR field.
4. Read and store the TOD_CNTR field for the first time.
   - Example: 1st_captured_TOD_value = 204 354.
5. Provide rising edge on GPIO1.
6. Read and store the TOD_CNTR field for the second time.
   - Example: 2nd_captured_TOD_value = 76 516 568
7. Calculate time delta using equation #1 with ToD clock rate of 307.2 MHz.
   - 248.412 155 ms = (76 516 568 - 204 354) / 307.2 MHz
   - Because the ToD clock rate is 307.2 MHz, the accuracy of the measurement is +/- 3.26 ns.

### *9.3.19.4 ToD Timing*

When TOD_CNTR_TRIG is 1 (GPIO pin):
- Timing accuracy of 1 ToD cycle + 2 ns requires a 20% to 80% rise time of less than or equal to 1 ns.
- GPIOx rising edge should not occur within 10 ns of rising SCS which sets TOD_CNTR_EN from 0 to 1.
- GPIOx should remain high for 10 ns.
- A new GPIOx trigger should not arrive within 1 µs of the rising edge of the SPI SCS after reading the LSB of the TOD_CNTR.

When TOD_CNTR_TRIG is 0 (SPI):
- Timing accuracy of 1 ToD cycle + 2 ns requires an 80% to 20% fall time of less than or equal to 1 ns.
- The ToD counter is captured to the TOD_CNTR registers at the falling edge of SPI SCS. No additional time to read back or pre-latching of register is required.

#### 9.3.19.5 Other ToD Behavior

The ToD counter continually counts up and periodically rolls over from $2^{40} – 1$ to 0.

- The user software must determine if the counter has rolled over in-between ToD reads. Accordingly it is recommended to reset the ToD counter by toggling the TOD_CNTR_EN bit before a prospective starting trigger event if known.

Since the REF0_MISSCLK_VCOSEL field also selects which VCO is used by all inputs for the early and missing reference clock validation, the early and missing input validation registers may need to be re-calculated if REF0_MISSCLK_VCOSEL is changed. Changing REF0_MISSCLK_VCOSEL or validation calculations during operation may result in references using the missing pulse or both missing and runt pulse detectors to be momentarily disqualified and send the DPLL into holdover.

While TOD_CNTR_EN = 0, the ToD counter is held in reset, which is 0. It is possible to make an absolute time measurement from the moment that TOD_CNTR_EN transitions from 0 to 1 to a future trigger event. However the accuracy of this measurement is less than performing a relative measurement caused by two GPIO or two SPI CSC triggers.

## 9.4 Device Functional Modes

### 9.4.1 Device Start-Up

The device can start up using $I^2C$ or SPI selected as the control interface depends on the 2-level input level sampled on the GPIO1 pin during power-on reset (POR). Internal register default settings after POR depend on the value of the ROM_PLUS_EE field stored in EEPROM.

- **GPIO1 = 0:** $I^2C$ communication interface selected
- **GPIO1 = 1:** SPI communication interface selected

After start-up, the $I^2C$ or SPI interface is enabled for register access to monitor the device status and control (or reconfigure) the device if needed. The register map configurations are the same for $I^2C$ and SPI.

The state of GPIO1 during POR determines:

- The serial interface ($I^2C$ or SPI) used for register access.
- The functionality of the SCS_ADD pin for device control and status.

The state of the EEPROM field EE_ROM_PAGE_SEL plus the GPIO0 and GPIO2 pins select the ROM page which will be used at start-up. If the field ROM_PLUS_EE is 0, then the device is started with just the ROM settings. If the field ROM_PLUS_EE is 1, then an EEPROM overlay is loaded and many fields controlling APLL and output clock configuration will be loaded from the EEPROM. This allows the user flexibility to select start-up clocks frequencies and output formats.

Figure 9-36 shows the device power-on reset configuration sequence.

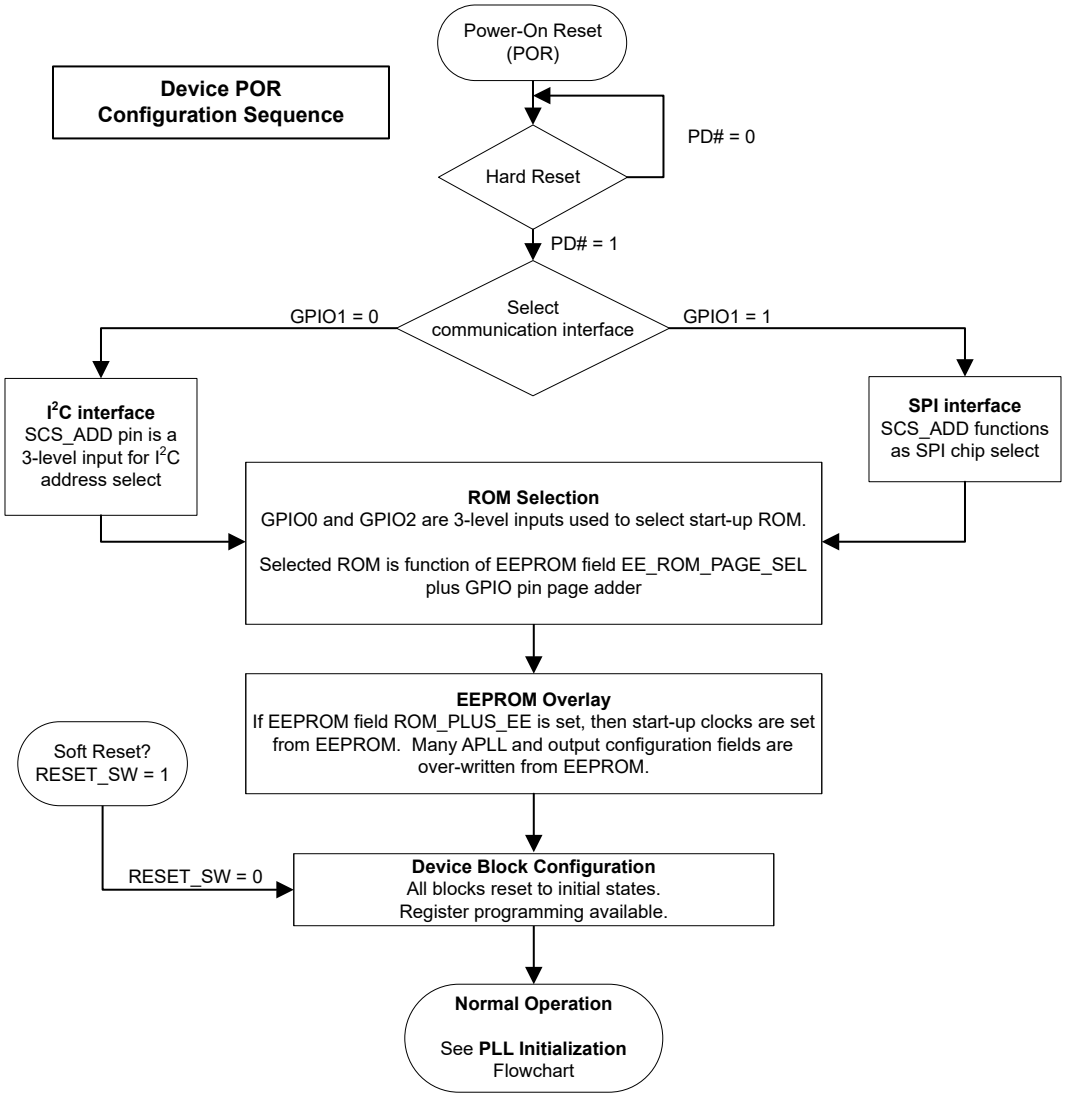



**Figure 9-36. Device POR Configuration Sequence**

Also see Figure 9-16, Figure 9-37, and Figure 9-38.

### *9.4.1.1 ROM Selection*

At POR the GPIO0 and GPIO2 pin state select a ROM page in conjunction with the EEPROM stored field EE_ROM_PAGE_SEL. The default EEPROM setting is EE_ROM_PAGE_SEL = 0. All register pages in the ROM image are factory-set in hardware (mask ROM) and are not software programmable. The table Table 9-6 lists the ROM selection options.

**Table 9-6. ROM page selection**

| GPIO2 ROM_ADD[1] | GPIO0 ROM_ADD[0] | ROM page with EE_ROM_PAGE_SEL = 0 |
|---|---|---|
| H | H | Low power mode. All PLLs off, all outputs off. |
| H | M | IN1 = 10 MHz SE 50-Ω termination, XO = 38.88 MHz. All outputs = 100 MHz LVDS from DPLL1 (OUT0 to 3, 14, 15) and DPLL2 (OUT4 to 13). |
| L | L | IN1 = 10 MHz CMOS, XO = 38.88 MHz, OUT2 = 125 MHz HSDS, OUT3 = 156.25 MHz LVDS, OUT10 = 122.88 MHz LVDS. |

#### *9.4.1.2 EEPROM Overlay*

An integrated EEPROM supports user customized output clocks on start-up when the ROM pages will not meet start-up clocking requirements.

At POR if the EEPROM field ROM_PLUS_EE = 1, after the ROM settings are loaded the EEPROM will overwrite APLL and clock output registers to provide the user programmed EEPROM start-up clocks. If the ROM based DPLL configuration is not valid, the APLLs will simply lock to the XO reference frequency until the DPLL is configured at which time the DPLL will validate the DPLL reference input and proceed to lock.

The factory default setting for the EEPROM field ROM_PLUS_EE = 0.

### 9.4.2 DPLL Operating States

The following sections describe the DPLL states of operation shown in Figure 9-37.

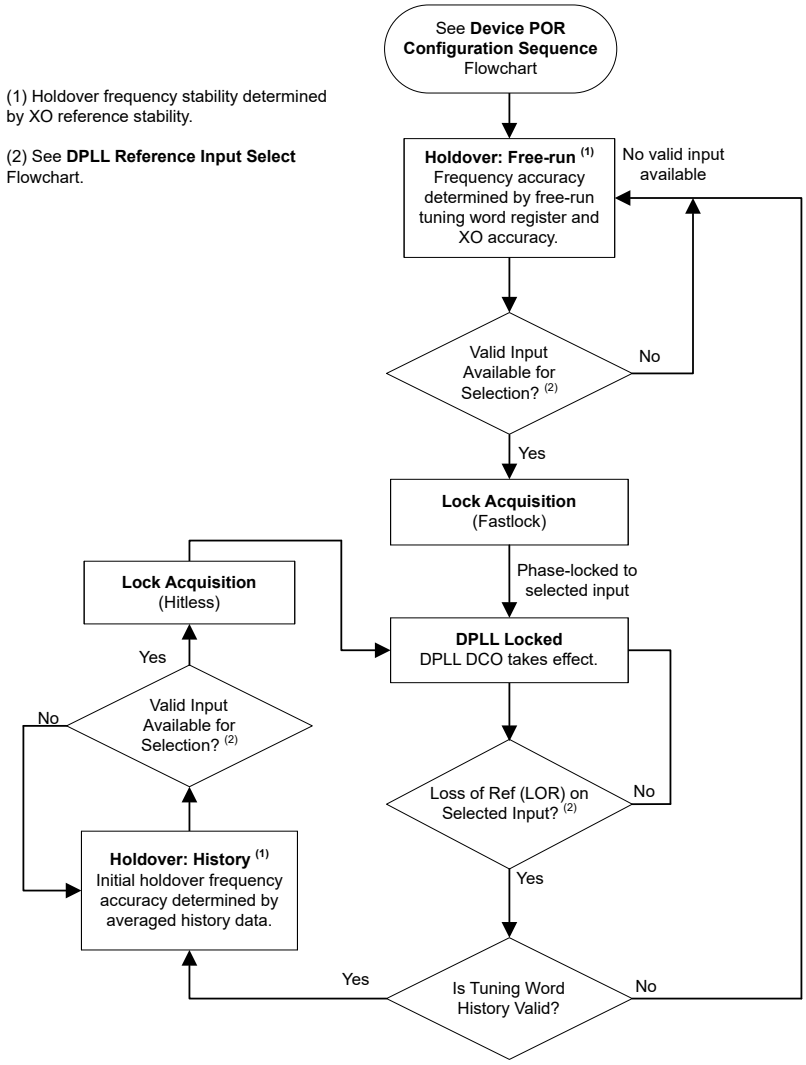



Diagram assumes holdover is enabled. Also see Figure 9-16, Figure 9-36, and Figure 9-38.

**Figure 9-37. DPLL Operating States**

#### 9.4.2.1 Free-Run

After device POR configuration and initialization, APLL will automatically lock to the XO clock once the XO input signal is valid. The output clock frequency accuracy and stability in free-run mode track the frequency accuracy and stability of the XO input. The reference inputs remain invalid (unqualified) during free-run mode. If the DPLL has locked, but not yet accumulated a valid history word and the reference is lost, then Free-Run is entered.

#### 9.4.2.2 Lock Acquisition

The DPLL constantly monitors its reference inputs for a valid input clock. When at least one valid input clock is detected, the PLL channel will exit free-run mode or holdover mode and initiate lock acquisition through the DPLL. The LMK5C33216 supports the Fastlock feature where the DPLL temporarily engages a wider loop bandwidth to reduce the lock time. Once the lock acquisition is done, the loop bandwidth is set to its normal configured loop bandwidth setting ($BW_{DPLL}$).

#### 9.4.2.3 DPLL Locked

Once the DPLL locks, the APLL output clocks are frequency and phase locked to the selected DPLL reference input clock. While the DPLL is locked, the APLL output clocks will not be affected by frequency drift on the XO input. The DPLL has a programmable frequency lock detector and phase lock detectors to indicate loss-of-frequency lock (LOFL) and loss-of-phase lock (LOPL) status flags, which can be observed through the status pins or status bits. Once frequency lock is detected (LOFL → 0), the tuning word history monitor (if enabled) will begin to accumulate historical averaging data used to determine the initial output frequency accuracy upon entry into holdover mode.

#### 9.4.2.4 Holdover

When a loss-of-reference (LOR) condition is detected and no valid input is available the DPLL enters holdover.

If history is disabled (DPLLx_HIST_EN = 0) the DPLL will use the 2s complement DPLLx_FREE_RUN[39:0] field which sets holdover frequency relative to the DPLL numerator. Short term frequency accuracy is based on the accuracy of the DPLLx_FREE_RUN field.

If history is enabled (DPLLx_HIST_EN = 1) but the tuning history is not yet valid, then the DPLLx_FREE_RUN field is used as if DPLLx_HIST_EN was disabled. If the tuning history is valid, the DPLL enters holdover using historical data to minimize holdover frequency error. See Section 9.3.7.4. In general, the longer the historical average time, the more accurate the initial holdover frequency assuming the 0-ppm reference clock (XO input) is drift-free. The stability of the XO reference clock determines the long-term stability and accuracy of the holdover output frequency.

Upon entry into holdover, the LOPL flag will be asserted (LOPL → 1). The LOFL flag reports DPLL frequency vs. reference frequency is in tolerance. In holdover LOFL will remain unchanged in holdover and not update until a valid reference is once again selected.

When a valid input becomes available for selection, the DPLL will exit holdover mode and automatically phase lock with the new input clock without any output glitches.

### 9.4.3 PLL Start-Up Sequence

Figure 9-38 shows the general sequence for PLL start-up after device configuration. This sequence also applies after a device soft-reset or individual PLL soft-reset. To ensure proper VCO calibration, it is critical for the external XO clock to be stable in amplitude and frequency prior to the start of VCO calibration otherwise the VCO calibration can fail and prevent start-up of the PLL and its output clocks.

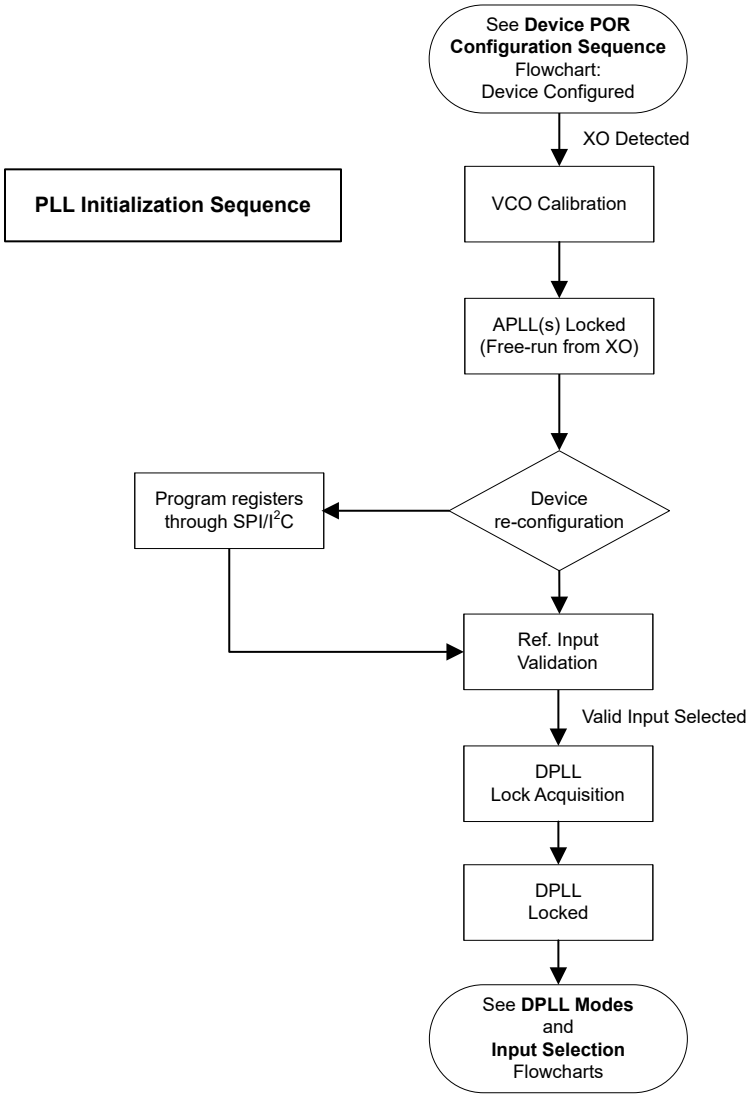



**Figure 9-38. PLL Initialization Sequence**

Also see Figure 9-16, Figure 9-36, and Figure 9-37.

### 9.4.4 Digitally-Controlled Oscillator (DCO) Frequency and Phase Adjustment

To support IEEE 1588 and other clock steering applications, the DPLL supports DCO mode to allow precise output clock frequency adjustment of less than 0.001 ppb/step. DCO may be implemented using DPLL DCO control or APLL DCO control. While the DPLL is operating in closed loop mode, DPLL DCO modifies the effective DPLL numerator. While the DPLL is in holdover or not used, APLL DCO adjusts the effective APLL numerator.

### 9.4.4.1 DPLL DCO Control

DCO mode can be enabled (DPLLx_FB_FDEV_EN = 1) when the DPLL is locked.

There are three methods to steer frequency when using the DPLL DCO.

- Register relative adjustment
  - Preset the deviation amount in DPLL_FDEV
  - Write an 8-bit register to enable increment/decrement by the deviation amount
- GPIO relative adjustment
  - Step/Direction GPIOx trigger
  - Adjust DPLLx_FB_NUM by programming a deviation amount for each step in pin set direction.
- Register absolute adjustment
  - Write the DPLLx_FB_NUM [39:0] based on the frequency control word (FCW)

The DCO frequency step size can be programmed through a 38-bit frequency deviation word register (DPLL_FDEV bits). The DPLL_FDEV value is an offset added to or subtracted from the current numerator value of the DPLL fractional feedback divider and determines the DCO frequency offset at the VCO output.

The DCO frequency increment (FINC) or frequency decrement (FDEC) updates can be controlled through software control (DPLLx_FB_FDEV_UPDATE) or user selectable pin control (GPIOx). DCO updates through software control are always available through $I^2C$ or SPI by writing to the DPLLx_FB_FDEV_UPDATE register bit. Writing a 0 will increment the DCO frequency by the programmed step size, and writing a 1 will decrement it by the step size. SPI can achieve faster DCO update rates than $I^2C$ because the SPI has faster write speed.

When DPLL pin control is selected (FDEV_TRIG_DPLLx and FDEV_DIR_DPLLx on GPIOs) a rising edge on the GPIO pin defined in FDEV_TRIG_DPLLx will apply a corresponding DCO update to the DPLL, another GPIO defined in FDEV_DIR_DPLLx will determine the direction of the FDEV trigger. FDEV_DIR_DPLLx = 0 means positive, FDEV_DIR_DPLLx = 1 means negative. In this way the GPIO pins will function as the FINC or FDEC input. The minimum positive pulse width applied to the trigger pins should be greater than 100 ns to be captured by the internal sampling clock. The DCO update rate should be limited to less than 5 MHz when using pin control.

When DCO control is disabled (DPLLx_FB_FDEV_EN = 0), the DCO frequency offset will be cleared and the VCO output frequency will be determined by the original numerator value of the DPLL fractional feedback divider.

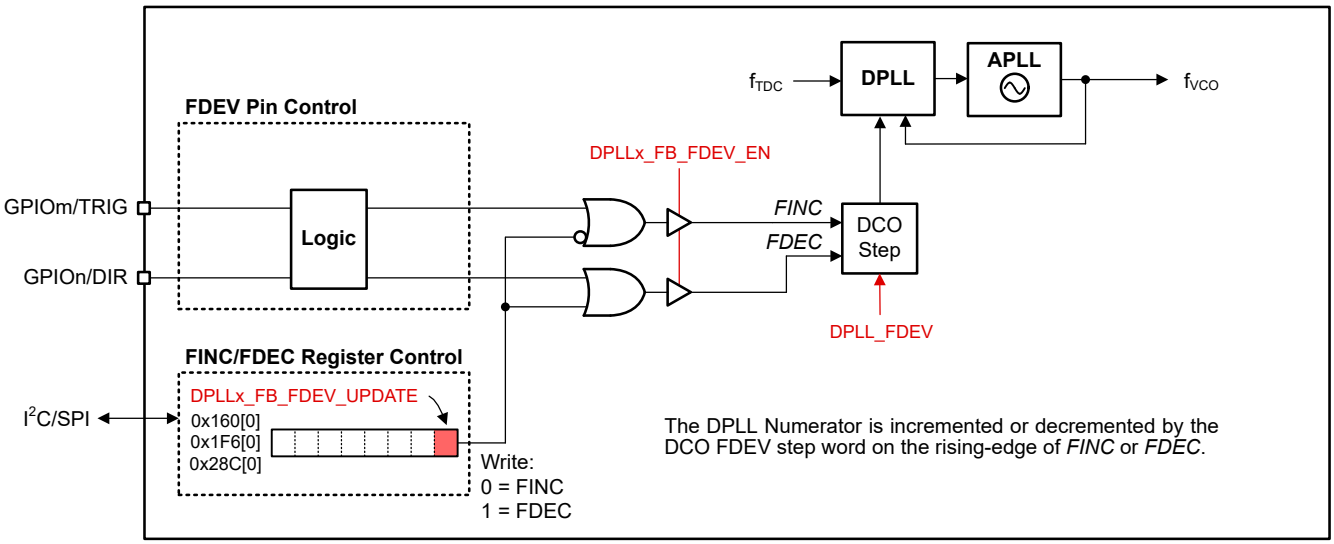



**Figure 9-39. DCO Mode Control Options**

#### 9.4.4.1.1 DPLL DCO Relative Adjustment Frequency Step Size

Equation 11 shows the formula to compute the DPLLx_FB_FDEV register value required to meet the specified DCO frequency step size in ppb (part-per-billion) when DCO mode is enabled for the DPLL.

$$DPLLx\_FB\_FDEV = (Reqd\_ppb / 10^9) \times DPLL_{DEN} \times f_{VCOx} / f_{TDCx} \quad (11)$$

where

- DPLLx_FB_FDEV: Frequency deviation value (0 to $2^{38}$- 1)
- Reqd_ppb: Required DCO frequency step size (in ppb)
- $DPLL_{DEN}$: DPLL FB divider denominator value (1 to $2^{40}$, register value of 0 = $2^{40}$)
- $f_{VCOx}$: VCOx frequency
- $f_{TDCx}$: TDCx frequency

#### 9.4.4.1.2 APLL DCO Frequency Step Size

To adjust APLL DCO, DPLLx_FREE_RUN field is written to. When DPLLx_HIST_EN = 1, the relative adjustements are performed. When DPLLx_HIST_EN = 0 the DPLLx_FREE_RUN value is used for the APLLx DCO numerator. The effective APLLx numerator can be read back from APLLx_NUM_STAT.

Equation 12 shows the formula to compute the DPLLx_FREE_RUN field value required to meet the specified DCO frequency step size in ppb (part-per-billion) when relative APLL DCO mode is enabled. DPLLx_FREE_RUN is a signed value and the actual programmed value for a negative number can be calculated as the 2s complement.

$$DPLLx\_FREE\_RUN = (Reqd\_ppb / 10^9) \times APLLx_{DEN} \times f_{VCOx} / f_{PDFx} \quad (12)$$

where

- DPLLx_FREE_RUN: Frequency deviation value (-$2^{39}$ to $2^{39}$- 1)
- Reqd_ppb: Required DCO frequency step size (in ppb)
- $APLLx_{DEN}$: APLL FB divider denominator value ($2^{40}$)
- $f_{VCOx}$: VCOx frequency
- $f_{PDFx}$: PLLx phase detector frequency

### 9.4.5 APLL Frequency Control

The device can also support APLL frequency and phase control through writing the 40-bit register DPLLx_FREE_RUN[39:0] while the DPLL is in holdover or not used. If the reference clock in a free-run mode or disabled, DPLL will disconnect with APLL, but we can still adjust frequency and phase accuracy.

To enable APLL DCO control, set DPLLx_LOOP_EN = 1, and PLLx_MODE = 1 for 40-bit fractional denominator. DPLLx_EN may be set = 0.

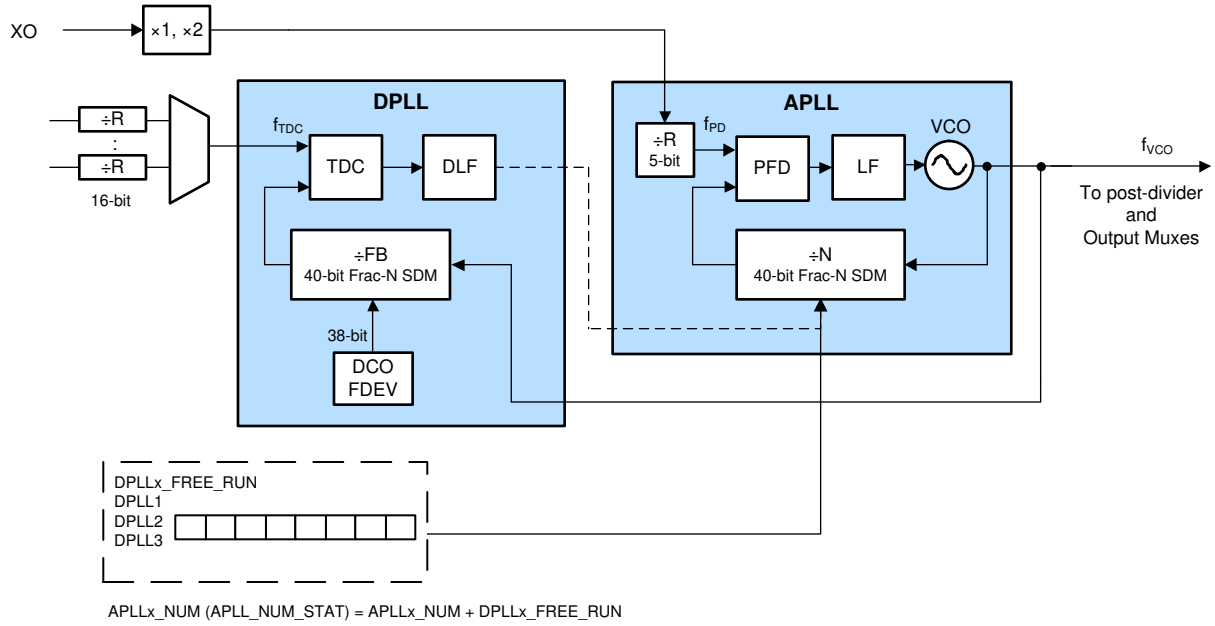



**Figure 9-40. APLL DCO Mode**

There are two alternative methods in adjusting the APLL DCO.

- Absolute frequency adjustment
  - Set DPLLx_HIST_EN = 0
  - Effective APLLx_NUM (APLLx_NUM_STAT) = APLLx_NUM + DPLLx_FREE_RUN
    - The APLLx_NUM_STAT is a read-only register and can be read back.
    - The DPLL loop filter block will modify the APLLx_NUM_STAT based on DPLLx_FREE_RUN value.
  - DPLLx_FREE_RUN is a 40-bit 2s complement number
- Relative frequency adjustment
  - Set DPLLx_HIST_EN = 1
  - DPLLx_FREE_RUN value is fed into the APLLx_NUM at a controlled rate defined by a step size register and step period register.
  - If another DPLLx_FREE_RUN write occurs before the LMK is complete in making the last adjustment, any remaining steps are lost and the new value begins to feed the APLL numerator.
  - A flag is set when the DPLLx_FREE_RUN word is fully fed into the effective APLLx_NUM (APLL_NUM_STAT).

### 9.4.6 Zero-Delay Mode Synchronization

The DPLL supports a zero-delay mode (ZDM) synchronization option to achieve a known and deterministic phase relationship between the selected DPLL reference input and OUT0, OUT4, or OUT10 clock depending on configuration and selected DPLL for ZDM. See Section 9.3.18.

## 9.5 Programming

### 9.5.1 Interface and Control

A system host device (MCU or FPGA) can use either $I^2C$ or SPI to access the register. The register configurations are the same for $I^2C$ and SPI. The device can be initialized, controlled, and monitored through register access during normal operation (when PD# is deasserted). Some device features can also be controlled and monitored through the external logic control and status pins. A 2-byte address and 1-byte data interface is used.

### 9.5.2 $I^2C$ Serial Interface

When (GPIO1 = 0), the device operates as an $I^2C$ client and supports bus rates of 100 kHz (standard mode) and 400 kHz (fast mode). Slower bus rates can work as long as the other $I^2C$ specifications are met. When operating with $I^2C$ communication interface the SCS_ADD pin selects one of three LSBs for the $I^2C$ device address. GPIO0 and GPIO2 input states determine device settings to load from ROM.

When using I2C communication the LMK5C33216 can support up to three different I2C addresses depending on the the state of the CSC_ADD pin on power-up, or any I2C address if the user re-programs the EEPROM. The five MSBs of the 7-bit I2C address are initialized from the EEPROM and the two LSBs are defined by the CSC_ADD pin state. The default EEPROM results in I2C addresses as shown in Table 9-7.

**Table 9-7. $I^2C$ Address**

| CSC_ADD Pin State | I2C Address LSB | I2C Address |
|---|---|---|
| Low | 0 | 0x64 |
| Vmid | 1 | 0x65 |
| High | 2 | 0x66 |

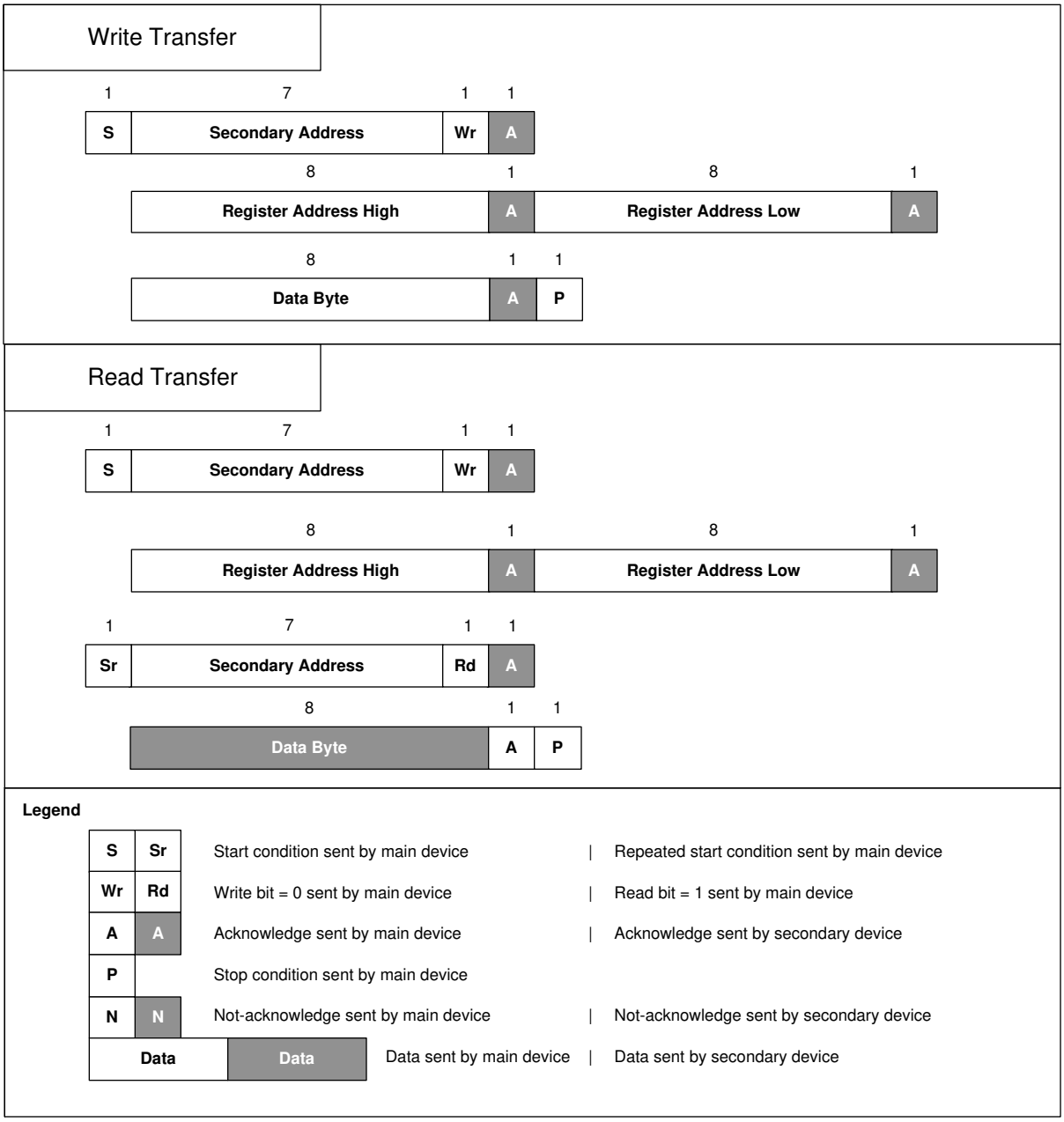



**Figure 9-41. I²C Byte Write and Read Transfers**

### 9.5.2.1 I²C Block Register Transfers

The device supports I²C block write and block read register transfers as shown in Figure 9-42.

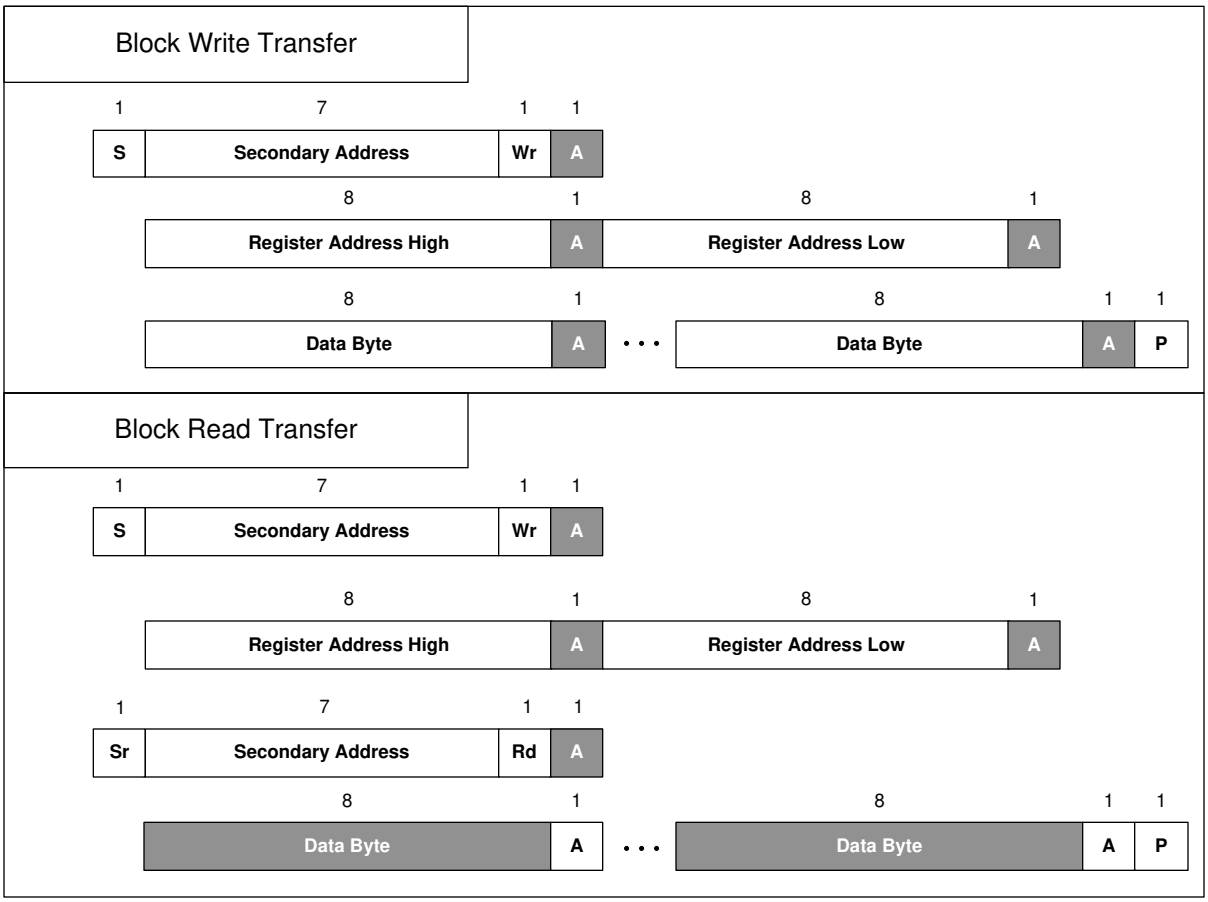



**Figure 9-42. I²C Block Register Transfers**

### 9.5.3 SPI Serial Interface

When SPI control interface is selected, the device uses a 3-wire SPI interface with SDIO, SCK, and SCS signals (SPI_3WIRE_DIS = 0). When using SPI interface SCS_ADD also can act as a time of day (ToD) trigger. When set SPI_3WIRE_DIS = 1, any GPIO may be selected as SDO to support readback with 4-wire SPI.

SPI and GPIO I/O are referenced to the 3.3-V power supply and the output drivers are 3.3-V LVCMOS compatible. The inputs are 1.8-V, 2.5-V, or 3.3-V LVCMOS compatible. When the SPI host is 3.3-V I/O, either 3-wire or 4-wire can be used without any voltage conversion. When the SPI host is not 3.3-V I/O complaint, the SDO signal from LMK5C33216 device should be divided to be compatible with the SPI host voltage level. The SDO pin may also be configured for open drain so the pullup resistors set the read back voltage as desired.

The host device must present data to the device MSB first. A message includes a transfer direction bit ( $\overline{W}$/R), a 15-bit address field (A14 to A0), and a 8-bit data field (D7 to D0) as shown in Figure 9-43. The $\overline{W}$/R bit is 0 for a SPI write and 1 for a SPI read.

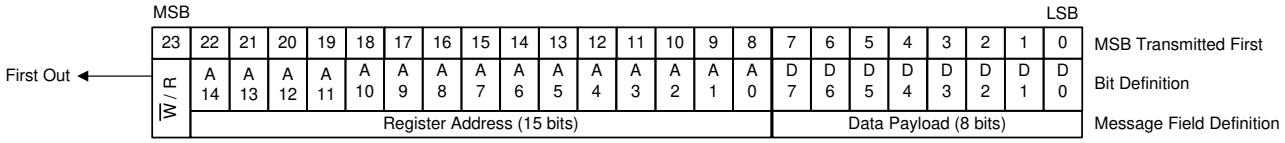



**Figure 9-43. SPI Message Format**

A message frame is initiated by asserting SCS low. The frame ends when SCS is deasserted high. The first bit transferred is the $\overline{W}$/R bit. The next 15 bits are the register address, and the remaining eight bits are data. On write transfers, data is committed in bytes as the final data bit (D0) is clocked in on the rising edge of SCK. If the write access is not an even multiple of eight clocks, the trailing data bits are not committed. On read transfers, data bits are clocked out from the SDO pin on the falling edges of SCK.

#### *9.5.3.1 SPI Block Register Transfer*

The LMK5C33216 supports a SPI block write and block read transfers. A SPI block transfer is exactly (2 + N) bytes long, where N is the number of data bytes to write or read. The host device (SPI host) is only required to specify the lowest address of the sequence of addresses to be accessed. The device will automatically increment the internal register address pointer if the SCS pin remains low after the host finishes the initial 24-bit transmission sequence. Each transfer of eight bits (a data payload width) results in the device automatically incrementing the address pointer (provided the SCS pin remains active low for all sequences).

### 9.5.4 Register Map Generation

The TICS Pro software tool for EVM programming has a step-by-step design flow to enter the user-selected clock design parameters, calculate the frequency plan, and generate the device register settings for the desired configuration. The register map data (registers hex dump in text format) can be exported to enable host programming of the device on start-up.

### 9.5.5 General Register Programming Sequence

For applications that use a system host to program the initial configuration after power up, this general procedure can be followed from the register map data generated and exported from TICS Pro:

1. Apply power to the device to start in $I^2C$ or SPI mode.
2. Write the register settings exported from TICS Pro while applying the following register mask (do not modify mask bits = 1):
   - Mask R23 = 0xFF (Device reset/control register)
3. Write 1 to R21[6] to assert SYNC. Clocks which should not be synced should have the SYNC functionality in their divider path disabled.
4. Write 1 to R23[6] to assert device soft-reset. This does not reset the register values.
5. Write 0 to R23[6] to exit soft-reset and begin the PLL start-up sequence.
6. Write 0 to R21[6] to de-assert SYNC and release all clocks to start-up synchronized.

# 10 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 10.1 Application Information

### 10.1.1 Device Start-Up Sequence

The device start-up sequence is shown in Figure 9-36 and Figure 9-38.

### 10.1.2 Power Down (PD#) Pin

The PD# pin (active low) can be used for device power down and used to initialize the POR sequence. When PD# is pulled low, the entire device is powered down and the serial interface is disabled. When PD# is pulled high, the device POR sequence is triggered to begin the device start-up sequence and normal operation as depicted in Figure 9-36. If the PD# pin is toggled to issue a momentary hard-reset, the negative pulse applied to the PD# pin should be greater than 200 ns to be captured by the internal digital system clock.

**Table 10-1. PD# Control**

| PD# PIN STATE | DEVICE OPERATION |
|---|---|
| 0 | Device is disabled |
| 1 | Normal operation |

### 10.1.3 Strap Pins for Start-Up

At start-up, voltage level on GPIOs determine the operation mode of the device. GPIO1 selects SPI or $I^2C$ mode. GPIO2 and GPIO0 select ROM page.

### 10.1.4 ROM and EEPROM

Some applications need start-up clocks to operate their entire system at power on. Others may need only a valid clock for the logic device (CPU, ASIC, or FPGA) at power on which may then program the LMK5C33216 with custom settings if the default ROM configuration does not meet the application requirements. The LMK5C33216 provides ROM pages to support default output clocks on start-up and an EEPROM to allow customization of the start-up clocks if the ROM pages do not meet the application requirements. See ROM Selection and EEPROM Overlay for more information.

### 10.1.5 Power Rail Sequencing, Power Supply Ramp Rate, and Mixing Supply Domains

#### *10.1.5.1 Power-On Reset (POR) Circuit*

The LMK5C33216 integrates a built-in power-on reset (POR) circuit that holds the device in reset until all of the following conditions have been met:

- All $V_{DD}$ core supplies have ramped above 2.72 V
- PD# pin has ramped above 1.2 V (minimum $V_{IH}$)

#### *10.1.5.2 Powering Up From a Single-Supply Rail*

As long as all VDD and VDDO supplies are driven by the same 3.3-V supply rail that ramp in a monotonic manner from 0 V to 3.135 V, and the time between decision point 2 and stabilized supply voltage is less than 1 ms, then there is no requirement to add a capacitor on the PD# pin to externally delay the device power-up sequence. As shown in Figure 10-1, the PD# pin can be left floating or otherwise driven by a system host to meet the clock sequencing requirements in the system.

If time between decision point 2 and stabilized supply voltage is greater than 1 ms, then the PD# pin must be delayed. Refer to Power Up From Split-Supply Rails.

As described in Slow or Delayed XO Start-Up, it is necessary for the XO reference to be valid after PD# decision point 1 to ensure successful VCO1 and VCO2 calibration.

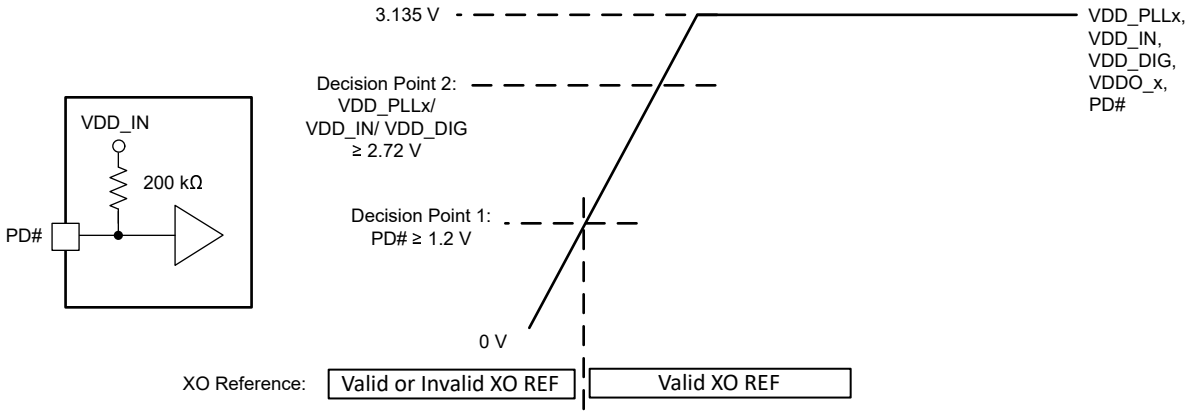



**Figure 10-1. Recommendation for Power Up From a Single-Supply Rail**

### *10.1.5.3 Power Up From Split-Supply Rails*

If VDD or VDDO supplies are driven from different supply sources, TI recommends to start the PLL calibration after all of the supplies have ramped above 3.135 V. This can be realized by delaying the PD# low-to-high transition. The PD# input incorporates a 200-kΩ resistor to VDD_IN and as shown in Figure 10-2. A capacitor from the PD# pin to GND can be used to form an RC time constant with the internal pullup resistor. This RC time constant can be designed to delay the low-to-high transition of PD# until all the core supplies have ramped above 3.135 V. It is recommended for VDDO supply pins to ramp before VDD supply pins.

Alternatively, the PD# pin can be driven high by a system host or power management device to delay the device power-up sequence until all supplies have ramped.

As described in Slow or Delayed XO Start-Up, it is necessary for the XO reference to be valid after PD# decision point 2 to ensure sucessful APLL1/VCO1 and APLL2/VCO2 calibration, or DPLL3 valid reference.

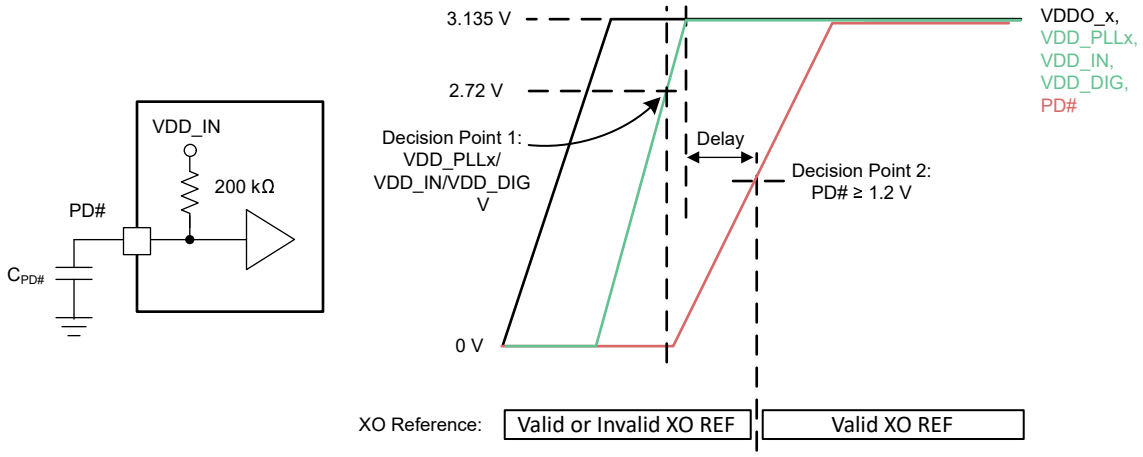



**Figure 10-2. Recommendation for Power Up From Split-Supply Rails**

#### *10.1.5.4 Non-Monotonic or Slow Power-Up Supply Ramp*

In case the VDD core supplies ramp with a non-monotonic manner or with a slow ramp time from 0 V to 3.135 V of over 100 ms, TI recommends to delay the VCO calibration until after all of the core supplies have ramped above 3.135 V. This could be achieved by delaying the PD# low-to-high transition with one of the methods described in Section 10.1.5.3.

If any core supply cannot ramp above 3.135 V before the PD# low-to-high transition, it is acceptable to issue a device soft-reset after all core supplies have ramped to manually trigger the VCO calibration and PLL start-up sequence.

### 10.1.6 Slow or Delayed XO Start-Up

Because the external XO clock input is used as the reference input for the APLL1/VCO1 and APLL2/VCO2 calibration, the XO input amplitude and frequency must be stable before the start of VCO calibration to ensure successful PLL lock and output start-up. If the XO clock is not stable prior to VCO calibration, the VCO calibration can fail and prevent PLL lock and output clock start-up.

If the XO clock has a slow start-up time or has glitches on power-up (due to a slow or non-monotonic power supply ramp, for example), TI recommends to delay the start of VCO calibration until after the XO is stable. This could be achieved by delaying the PD# low-to-high transition until after the XO clock has stabilized using one of the methods described in Section 10.1.5.3. It is also possible to issue a device soft-reset after the XO clock has stabilized to manually trigger the VCO calibration and PLL start-up sequence.

APLL3/VCO3 is factory calibrated and is not sensitive to an invalid XO reference start-up. Upon valid XO reference, APLL3/VCO3 will be able to acquire lock. When APLL3/VCO3 is used in conjunction with DPLL3, it is necessary for the XO to be valid before a DPLL3 reference is validated.

## 10.2 Typical Application

Figure 10-3 shows a reference schematic to help implement the LMK5C33216 and its peripheral circuitry. Power filtering examples are given for the core supply pins and independent output supply pins. Single-ended LVCMOS, LVDS, HSDS, LVPECL, and CML open collector clock interfacing examples are shown for the clock input and output pins. An external CMOS oscillator drives an AC-coupled voltage divider network as an example to interface the 3.3-V LVCMOS output to meet the input voltage swing specified for the XO input. The XO pin of the LMK5C33216 can accept 3.3V LVCMOS input. The required external capacitors are placed close to the LMK5C33216 and are shown with the suggested values. External pullup and pulldown resistor options at the logic I/O pins set the default input states. The $I^2C$ or SPI pins and other logic I/O pins can be connected to a host device (not shown) to program and control the LMK5C33216 and monitor its status.

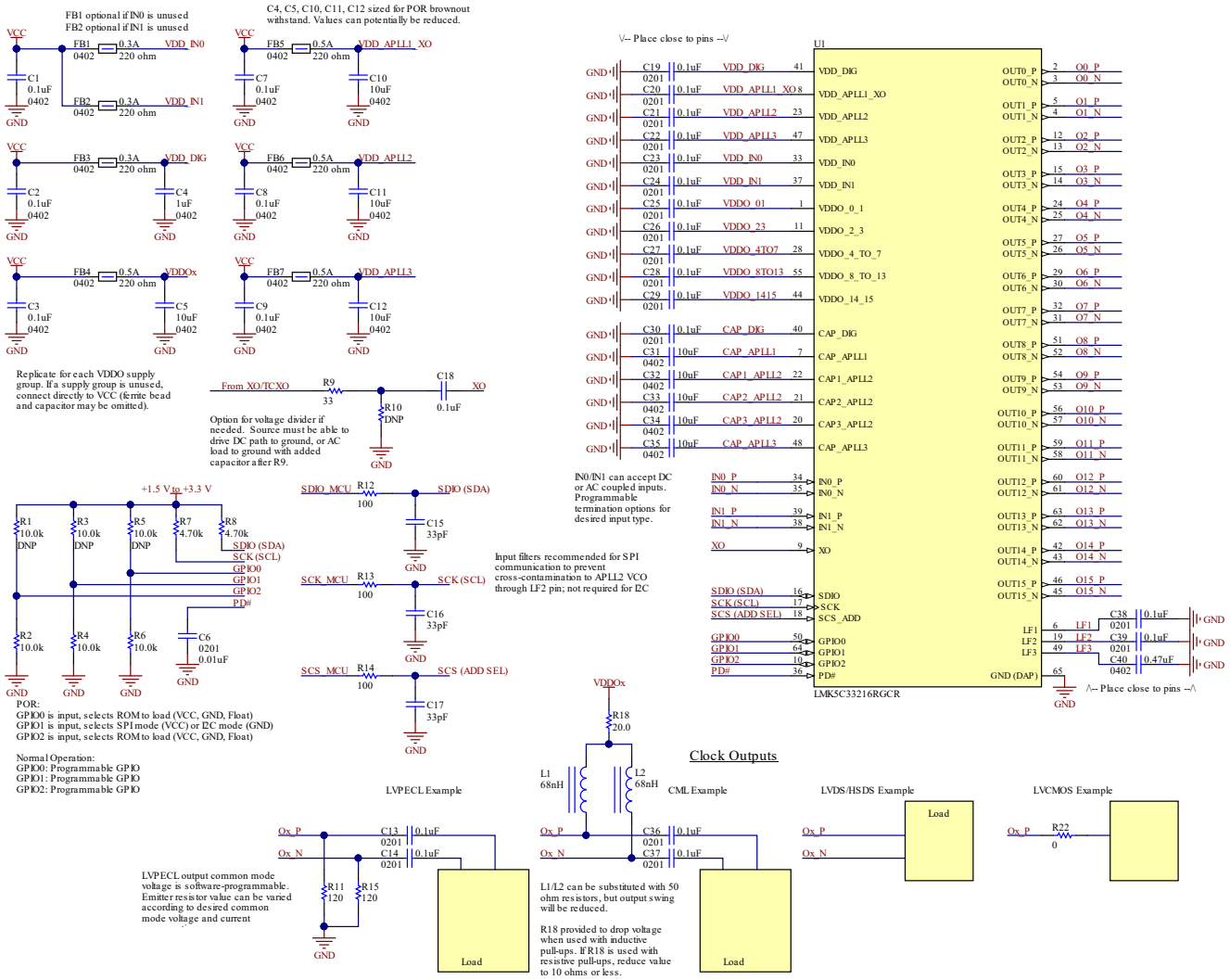



**Figure 10-3. Reference Schematic Example**

### 10.2.1 Design Requirements

In a typical application, consider the following design requirements or parameters to implement the overall clock solution:

1. Device initial configuration. The device should be configured as either host programmed (MCU or FPGA) or factory pre-programmed.
2. Device interface, set GPIO1 as desired for $I^2C$ or SPI communications interface.
3. XO frequency, signal type, and frequency accuracy and stability. Consider a high-stability TCXO or OCXO for the XO input if any of the following is required:
   - Standard-compliant frequency stability (such as SyncE, SONET/SDH, IEEE 1588)
   - Lowest possible close-in phase noise at offsets ≤ 100 Hz
   - Narrow DPLL bandwidth ≤ 10 Hz
4. For each DPLL/APLL domain, determine the following:
   - Input clocks: frequency, buffer mode, priority, and input selection mode
   - APLL reference: another VCO with Cascaded mode, or XO for Non-cascaded mode
   - Output clocks: frequency, buffer mode
   - DPLL loop bandwidth and maximum TDC frequency
   - If the DCO Mode or Zero-Delay Mode is required
5. Input clock and PLL monitoring options
6. Status outputs and interrupt flag
7. Power supply rails

### 10.2.2 Detailed Design Procedure

In a typical application, TI recommends the following steps:

1. Use the device GUI in the TICS Pro programming software for a step-by-step design flow to enter the design parameters, calculate the frequency plan for each PLL domain, and generate the register settings for the desired configuration. The register settings can be exported (registers hex dump in txt format) to enable host programming.
   - A host device can program the register settings through the serial interface after power-up and issue a soft-reset (by SWRST bit) to start the device. Set SW_SYNC before, and clear after SWRST.
2. Tie the GPIO1 pin to ground to select the $I^2C$ communications interface, or pull up GPIO1 high to VDD_DIG through an external resistor to select the SPI communications interface. Determine the logic I/O pin assignments for control and status functions. See Figure 9-36.
   - Connect $I^2C$/SPI and logic I/O pins (1.8-V compatible levels) to the host device pins with the proper I/O direction and voltage levels.
3. Select an XO frequency by following Section 9.3.1.
   - Choose an XO with target phase jitter performance that meets the frequency stability and accuracy requirements required for the output clocks during free-run or holdover.
   - For a 3.3-V LVCMOS driver, LMK5C33216 can accept it directly. Power the XO from a low-noise LDO regulator or optimize its power filtering to avoid supply noise-induced jitter on the XO clock.
   - **TICS Pro:** Configure the XO frequency to match the XO port input.

4. Wire the clock I/O for each PLL domain in the schematic and use TICS Pro to configure the device settings as follows:
   - Reference inputs: Follow the LVCMOS or differential clock input interface examples in Figure 10-3 or Section 9.3.3.
     - **TICS Pro:** For DPLL mode, configure the reference input buffer modes to match the reference clock driver interface requirements. See Table 9-2.
   - **TICS Pro:** For DPLL mode, configure the DPLL input selection modes and input priorities. See Section 9.3.4.
   - **TICS Pro:** Configure each APLL reference from other VCO domain (Cascaded mode) or XO clock (Non-cascaded mode).
     –
   - **TICS Pro:** Configure each output with the required clock frequency and PLL domain. TICS Pro can calculate the VCO frequencies and divider settings for the PLL and outputs. Consider the following output clock assignment guidelines to minimize crosstalk and spurs:
     - OUT[0:1] bank can select any PLL clocks, XO, and references.
     - OUT[2:3] bank is preferred for PLL1 or PLL2 clocks.
     - OUT[4:7] bank is preferred for PLL2 or PLL3 clocks.
     - OUT[8:13] bank is preferred for PLL3 or PLL2 clocks.
     - OUT[14:15] bank is preferred for PLL1, PLL2, or PLL3 clocks.
     - Group identical output frequencies (or harmonic frequencies) on adjacent channels, and use the output pairs with a single divider (for example, OUT2/3 or OUT14/15) when possible to minimize power.
     - Separate clock outputs when the difference of the two frequencies, $|f_{OUTx} – f_{OUTy}|$, falls within the jitter integration bandwidth (for example, 12 kHz to 20 MHz). Any outputs that are potential aggressors should be separated by at least four static pins (power pin, logic pin, or disabled output pins) to minimize potential coupling. If possible, separate these clocks by the placing them on opposite output banks, which are on opposite sides of the chip for best isolation.
     - Avoid or isolate any LVCMOS output (strong aggressor) from other jitter-sensitive differential output clocks. If an LVCMOS output is required, use dual complementary LVCMOS mode (+/- or -/+) with the unused LVCMOS output left floating with no trace.
     - If not all outputs pairs are used in the application, consider connecting an unused output to a pair of RF coaxial test structures for testing purposes (such as SMA, SMP ports).
   - **TICS Pro:** Configure the output drivers.
     - Configure the output driver modes to match the receiver clock input interface requirements. See Table 9-3.
     - Configure any output SYNC groups that need their output phases synchronized. See Section 9.3.17.
     - Configure the output auto-mute modes, and APLL and DPLL mute options. See Section 9.3.14.3.
   - Clock output Interfacing: Follow the single-ended or differential clock output interface examples in Figure 10-3 or Section 9.3.16.
     - Differential outputs can be AC-coupled and terminated and biased at the receiver inputs, or DC-coupled with proper receivers
     - LVCMOS outputs have internal source termination to drive 50-Ω traces directly. LVCMOS $V_{OH}$ level is determined by internal LDO programmed voltage (1.8 V or 2.65 V).
   - **TICS Pro:** Configure the DPLL loop bandwidth.
     - Below the loop bandwidth, the reference noise is added to the TDC noise floor and the XO/TCXO/OCXO noise. Above the loop bandwidth, the reference noise will be attenuated with roll-off up to 60 dB/decade. The optimal bandwidth depends on the relative phase noise between the reference input and the XO. APLL's loop bandwidth can be configured to provide additional attenuation of the reference input, TDC, and XO phase noise above APLL's bandwidth.
   - **TICS Pro:** Configure the maximum TDC frequency to optimize the DPLL TDC noise contribution for the desired use case.

  - *Wired*: A 400 kHz maximum TDC rate is commonly specified. This supports SyncE and other use cases using a narrow loop bandwidth (≤10 Hz) with a TCXO/OCXO/XO to set the frequency stability and wander performance.
  - *Wireless*: A 26 MHz maximum TDC rate is commonly specified for lowest in-band TDC noise contribution. This supports wireless and other use cases where close-in phase noise is critical.
- **TICS Pro:** If clock steering is needed (such as for IEEE 1588 PTP), enable DCO mode for the DPLL loop and enter the frequency step size (in ppb). The FDEV step register will be computed according to Section 9.4.4.1.2. Enable the FDEV_TRIG and FDEV_DIR pin control on the GPIO pins if needed.
- **TICS Pro:** If deterministic input-to-output clock phase is needed for 1-PPS input and 1-PPS output (on OUT0 or OUT1), enable the ZDM as required on OUT0, OUT4, or OUT10. See Section 9.3.18.

5. **TICS Pro:** Configure the reference input monitoring options for each reference input. Disable the monitor when not required or when the input operates beyond the monitor's supported frequency range. See Section 9.3.7.2.
   - *Frequency monitor*: Set the valid and invalid thresholds (in ppm).
   - *Missing pulse monitor*: Set the late window threshold ($T_{LATE}$) to allow for the longest expected input clock period, including worst-case cycle-to-cycle jitter. For a gapped clock input, set $T_{LATE}$ based on the number of allowable missing clock pulses.
   - *Runt pulse monitor*: Set the early window threshold ($T_{EARLY}$) to allow for the shortest expected input clock period, including worst-case cycle-to-cycle jitter.
   - *1-PPS Phase validation monitor*: Set the phase validation jitter threshold, including worst-case input cycle-to-cycle jitter.
   - *Validation timer*: Set the amount of time the reference input must be qualified by all enabled input monitors before the input is valid for selection.
6. **TICS Pro:** Configure the DPLL lock detect and tuning word history monitoring options for each channel. See Section 9.3.7.3 and Section 9.3.7.4.
   - *DPLL frequency lock and phase lock detectors*: Set the lock and unlock thresholds for each detector.
7. **TICS Pro:** Configure each status output pin and interrupt flag as needed. See Section 9.3.7.5 and Section 9.3.7.6.
   - Select the desired status signal selection, status polarity, and driver mode (3.3-V LVCMOS or open-drain). Open-drain requires an external pullup resistor.
   - If the Interrupt is enabled and selected as a status output, configure the flag polarity and the mask bits for any interrupt source, and the combinational OR gate, as needed.
8. Consider the following guidelines for designing the power supply:
   - Outputs with identical frequency or integer-related (harmonic) frequencies can share a common filtered power supply.
     - Example: 156.25-MHz and 312.5-MHz outputs on OUT[4:5] and OUT[6:7] can share a filtered VDDO supply, while 100-MHz, 50-MHz, and 25-MHz outputs on OUT[0:1] and OUT[2:3] can share a separate VDDO supply.
   - See Section 10.1.5.

## 10.3 Do's and Don'ts

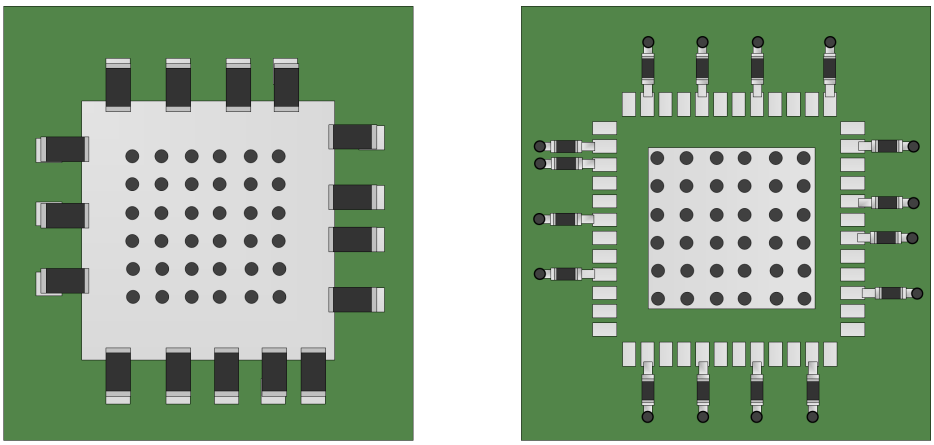
- Power all the VDD pins with proper supply decoupling and bypassing connect as shown in Figure 10-3.
- Power down unused blocks through registers to minimize power consumption.
- Use proper source or load terminations to match the impedance of input and output clock traces for any active signals to/from the device.
- Leave unused clock outputs floating and powered down through register control.
- Leave unused clock inputs floating.
- If needed, external biasing resistors (10-kΩ pullup to 3.3 V or 10-kΩ pulldown) can be connected on each GPIO pin to select device operation mode during POR.
- Consider routing each GPIO pin to a test point or high-impedance input of a host device to monitor device status outputs.
- Consider using a LDO regulator to power the external XO/TCXO/OCXO source.

  - High jitter and spurious on the oscillator clock are often caused by high spectral noise and ripple on its power supply.
- Include dedicated header to access the $I^2C$ or SPI interface of the device, as well as a header pin for ground.
  - This can enabled off-board programming for device bring-up, prototyping, and diagnostics using the TI USB2ANY interface and TICS Pro software tools.

# 11 Power Supply Recommendations

## 11.1 Power Supply Bypassing

Figure 11-1 shows two general placements of power supply bypass capacitors on either the back side or the component side of the PCB. If the capacitors are mounted on the back side, 0402 components can be employed. For component side mounting, use 0201 body size capacitors to facilitate signal routing. A combination of component side and back side placement can be used. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low-impedance connection to the ground plane.




(**Does not** indicate actual location of the device supply pins)

**Figure 11-1. Generalized Placement of Power Supply Bypass Capacitors**

# 12 Layout

## 12.1 Layout Guidelines

- Isolate input, XO/OCXO/TCXO and output clocks from adjacent clocks with different frequencies and other nearby dynamic signals.
- Consider the XO/OCXO/TCXO placement and layout in terms of the supply/ground noise and thermal gradients from nearby circuitry (for example, power supplies, FPGA, ASIC) as well as system-level vibration and shock. These factors can affect the frequency stability/accuracy and transient performance of the oscillator.
- Avoid impedance discontinuities on controlled-impedance 50-Ω single-ended (or 100-Ω differential) traces for clock and dynamic logic signals.
- Place bypass capacitors close to the VDD and VDDO pins on the same side as the IC, or directly below the IC pins on the opposite side of the PCB. Larger decoupling capacitor values can be placed further away.
- Place external capacitors close to the CAP_x and LFx pins.
- Use multiple vias to connect wide supply traces to the respective power islands or planes if possible.
- Use at least a 6×6 through-hole via pattern to connect the IC ground/thermal pad to the PCB ground planes.
- See the Land Pattern Example, Solder Mask Details, and Solder Paste Example in Section 14.

## 12.2 Layout Example

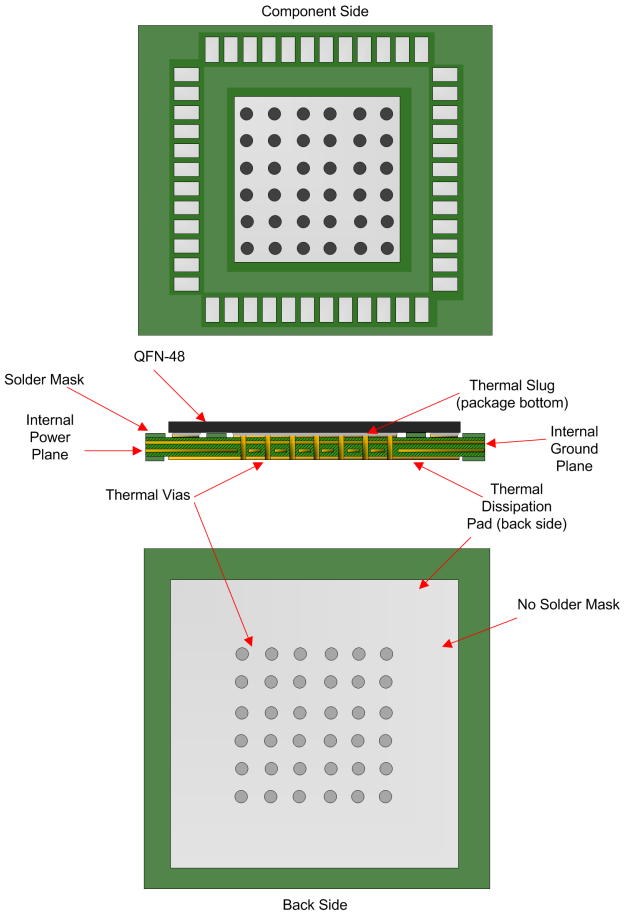



**Figure 12-1. General PCB Ground Layout for Thermal Reliability (8+ Layers Recommended) - TBD**

## 12.3 Thermal Reliability

The LMK5C33216 is a high-performance device. To ensure good electrical and thermal performance, TI recommends to design a thermally-enhanced interface between the IC ground/thermal pad and the PCB ground using at least a 6×6 through-hole via pattern connected to multiple PCB ground layers as shown in Figure 12-1.

### 12.3.1 Support for PCB Temperature up to 105°C

The device can maintain a safe junction temperature below the recommended maximum value of 135°C even when operated on a PCB with a maximum board temperature ($T_{PCB}$) of 105 °C. This can shown by the following example calculation, which assumes the total device power ($P_{TOTAL}$) computed with all blocks enabled using the typical current consumption from the Section 7.5 (VDD = 3.3 V) and the thermal data in Section 7.4 with no airflow.

$$T_J = T_{PCB} + (\Psi_{JB} \times P_{TOTAL}) = \mathbf{130.2\ °C} \quad (13)$$

where

- $T_{PCB}$ = 105 °C
- $\Psi_{JB}$ = 6.3 °C/W
- $P_{TOTAL} = P_{CORE} + P_{OUTPUT}$ = 4.0 W
  - $P_{CORE}$ = (38 + 5.5 + 5.5 + 186 + 227 + 172) mA × 3.3 V = 2.1 W
    - All DPLLs, APLLs and all Inputs enabled
  - $P_{OUTPUT}$ = 575 mA × 3.3 V = 1.9 W
    - All output channels enabled

# 13 Device and Documentation Support

## 13.1 Documentation Support

### 13.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *LMK5C33216EVM User's Guide*

## 13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 13.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 13.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 13.5 Glossary

**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.

## 13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

# 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LMK5C33216RGCR | Active | Production | VQFN (RGC) \| 64 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | K5C33216 |
| LMK5C33216RGCR.A | Active | Production | VQFN (RGC) \| 64 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | K5C33216 |
| LMK5C33216RGCR.B | Active | Production | VQFN (RGC) \| 64 | 2500 \| LARGE T&R | - | Call TI | Call TI | -40 to 85 | |
| LMK5C33216RGCT | Active | Production | VQFN (RGC) \| 64 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | K5C33216 |
| LMK5C33216RGCT.A | Active | Production | VQFN (RGC) \| 64 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | K5C33216 |
| LMK5C33216RGCT.B | Active | Production | VQFN (RGC) \| 64 | 250 \| SMALL T&R | - | Call TI | Call TI | -40 to 85 | |
| LMK5C33216RGCTG4 | Active | Production | VQFN (RGC) \| 64 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | K5C33216 |
| LMK5C33216RGCTG4.A | Active | Production | VQFN (RGC) \| 64 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 85 | K5C33216 |
| LMK5C33216RGCTG4.B | Active | Production | VQFN (RGC) \| 64 | 250 \| SMALL T&R | - | Call TI | Call TI | -40 to 85 | |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

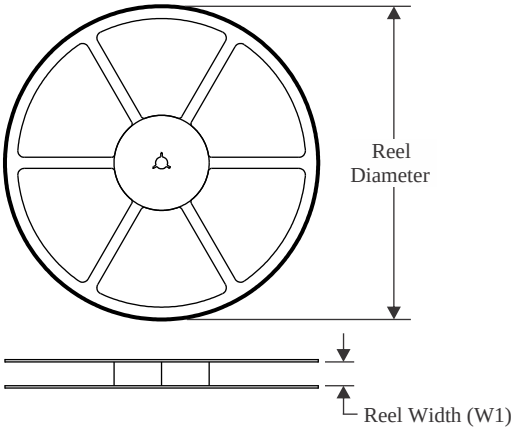
**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

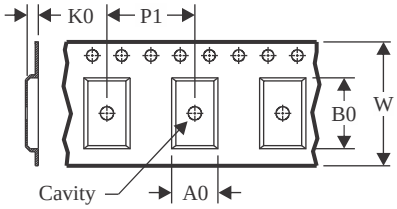
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

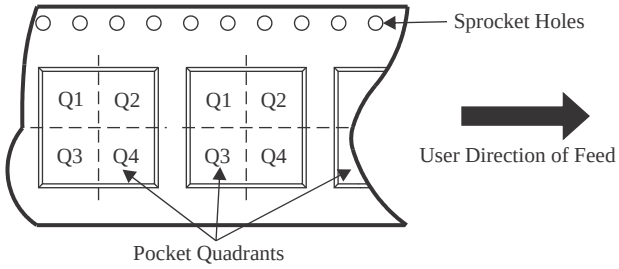



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

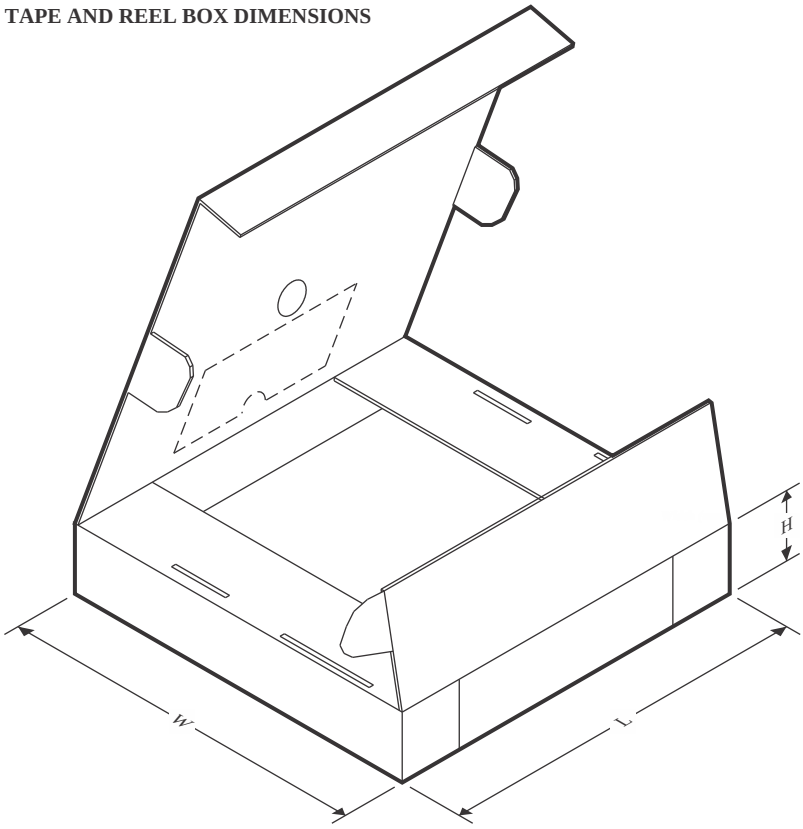
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LMK5C33216RGCR | VQFN | RGC | 64 | 2500 | 330.0 | 16.4 | 9.3 | 9.3 | 1.1 | 12.0 | 16.0 | Q2 |
| LMK5C33216RGCT | VQFN | RGC | 64 | 250 | 180.0 | 16.4 | 9.3 | 9.3 | 1.1 | 12.0 | 16.0 | Q2 |
| LMK5C33216RGCTG4 | VQFN | RGC | 64 | 250 | 180.0 | 16.4 | 9.3 | 9.3 | 1.1 | 12.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LMK5C33216RGCR | VQFN | RGC | 64 | 2500 | 367.0 | 367.0 | 38.0 |
| LMK5C33216RGCT | VQFN | RGC | 64 | 250 | 210.0 | 185.0 | 35.0 |
| LMK5C33216RGCTG4 | VQFN | RGC | 64 | 250 | 210.0 | 185.0 | 35.0 |

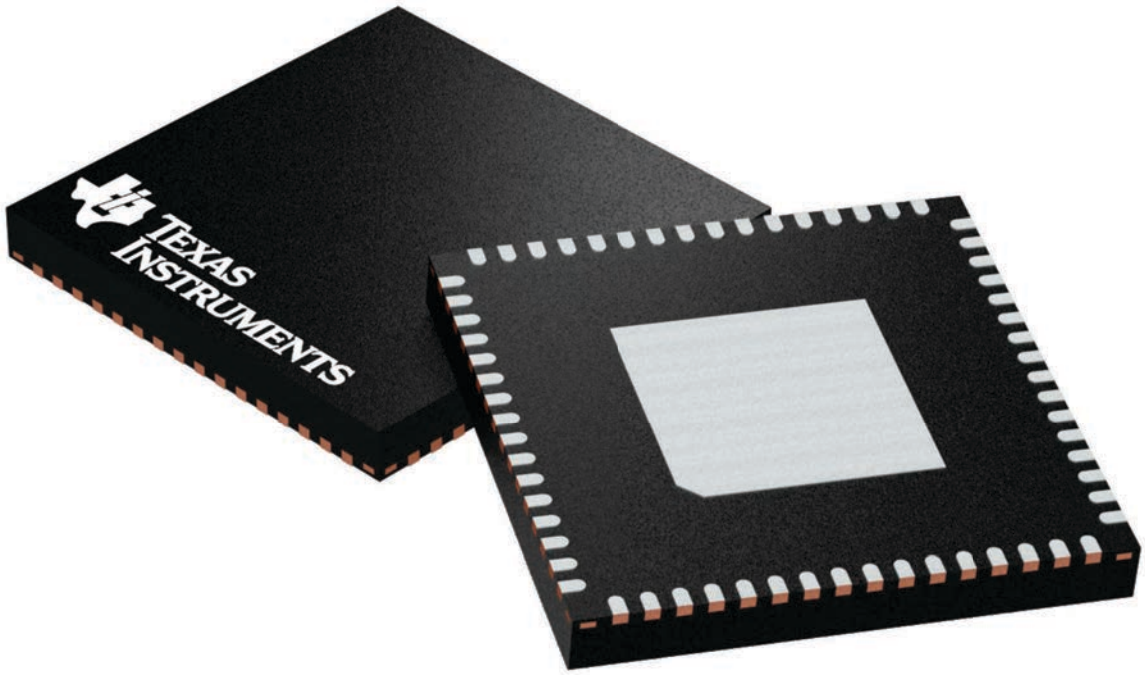
# GENERIC PACKAGE VIEW

## RGC 64

## VQFN - 1 mm max height

**9 x 9, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

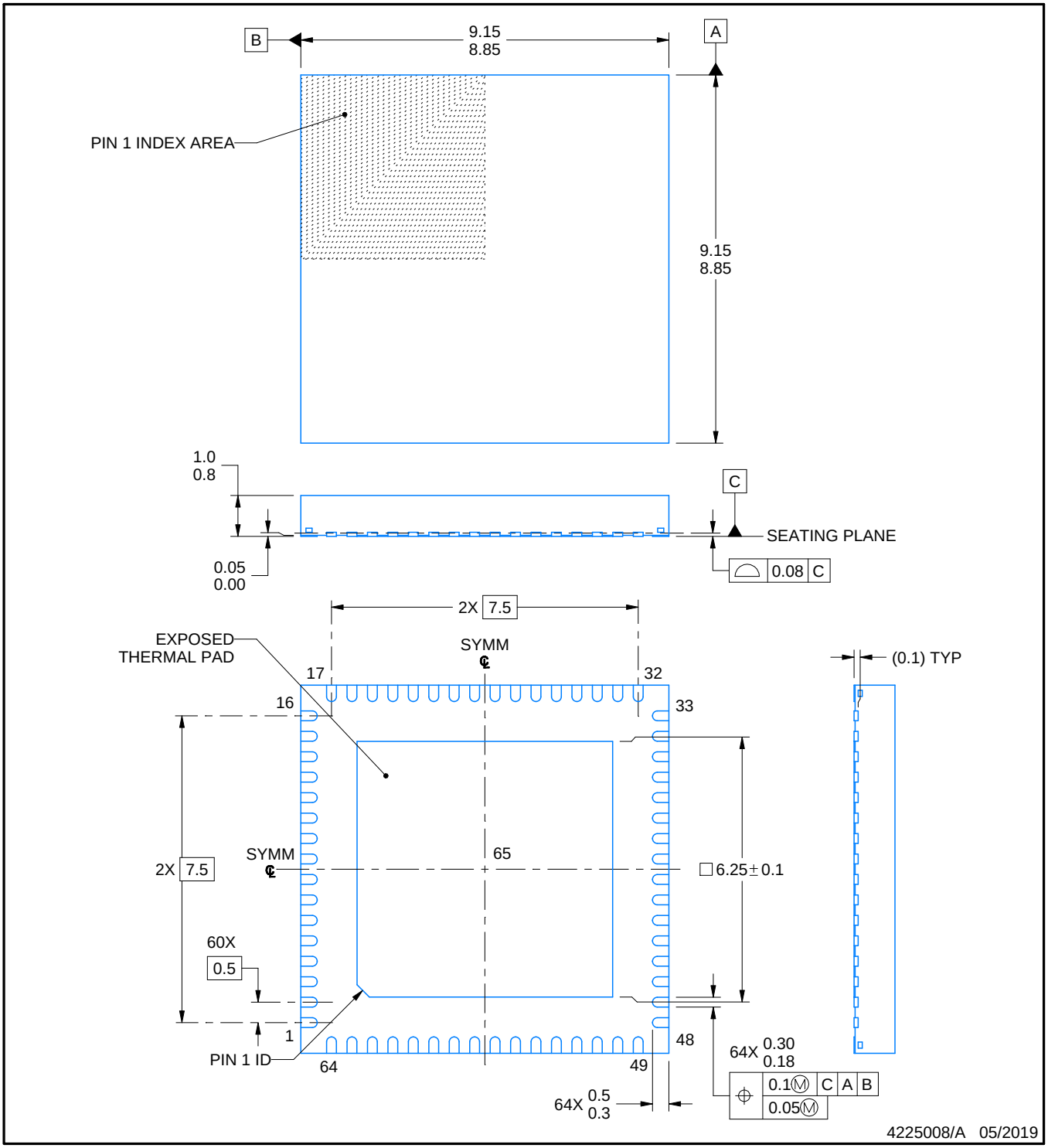
4224597/A

# RGC0064E

# PACKAGE OUTLINE

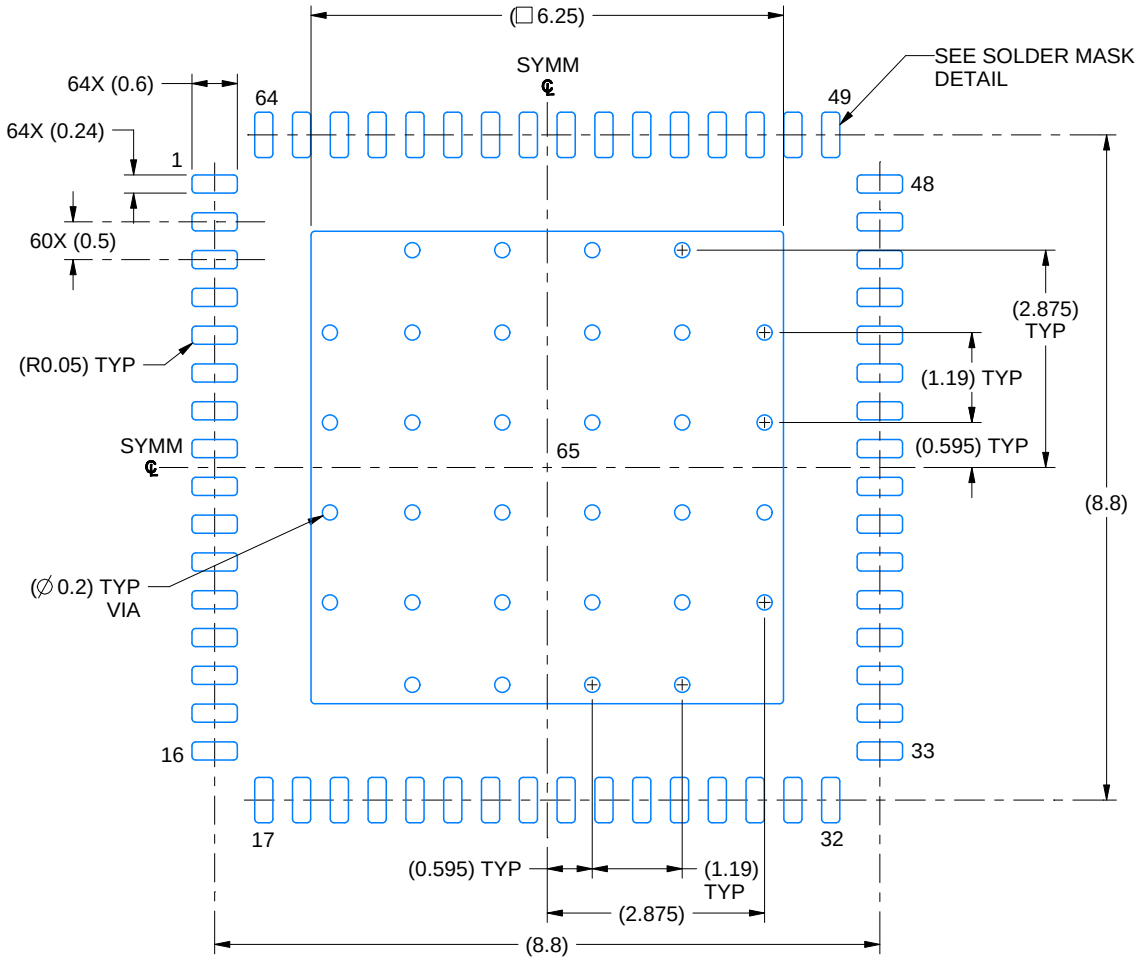
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

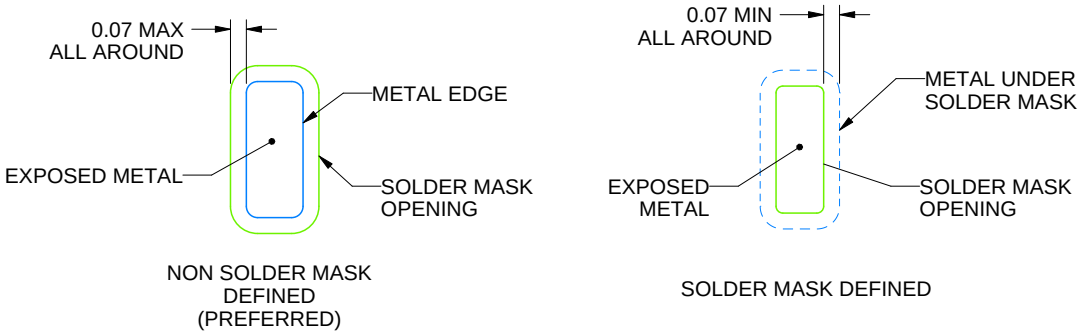



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

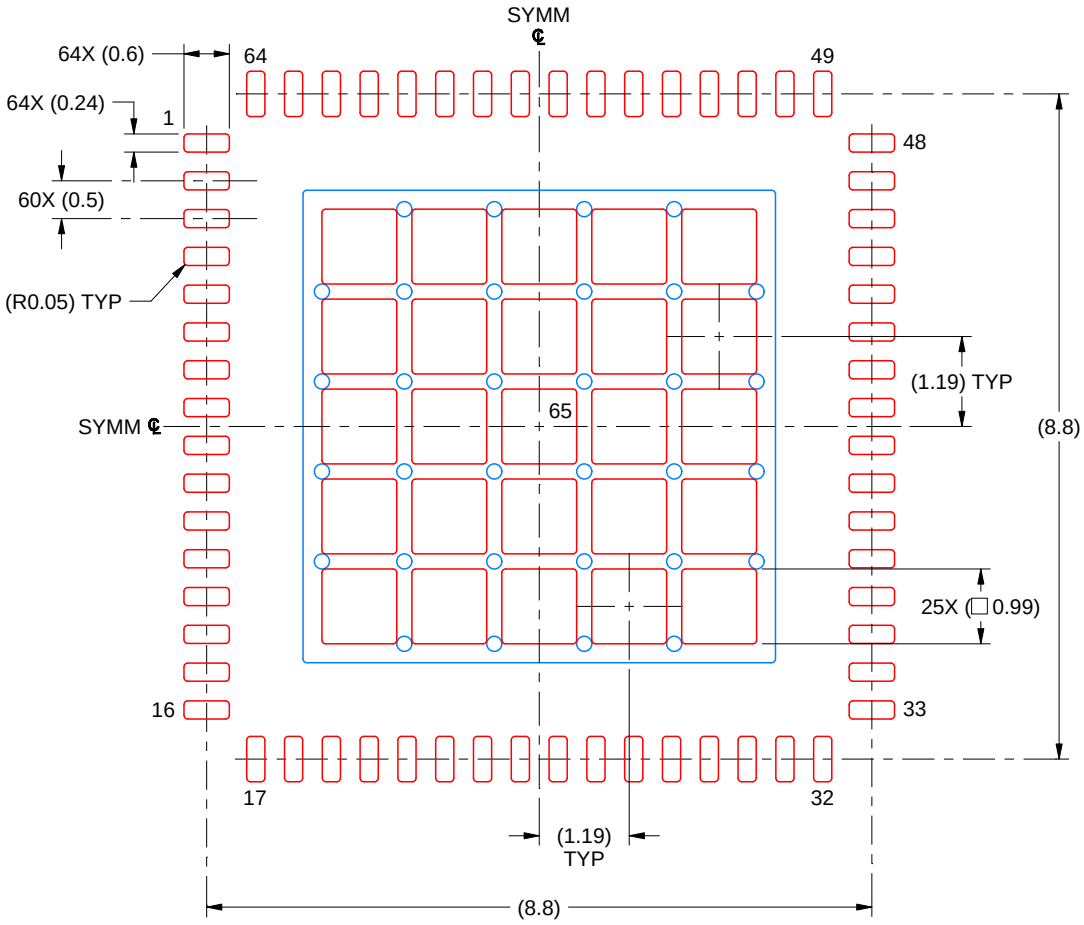



SOLDER MASK DETAILS

4225008/A 05/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
63% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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