LP5816 4-Channel I²C Interface RGBW LED Driver

1 Features

- Operating voltage range
  - V_{CC} range: 2.5V to 5.5V
  - Logic pins compatible with 1.8V, 3.3V, and 5V
  - Output voltage up to 5.5V
- 4 constant current sinks with high precision
  - 0.1mA to 51mA per channel
  - Device-to-device error: ±8% (max.)
  - Channel-to-channel error: ±3% (max.)
  - Ultra-low headroom voltage: 135mV (max.) at 25.5mA; 275mV (max.) at 51mA
- Ultra-low power consumption
  - Shutdown: I_{SD} = 0.1μA (typ.)
  - Standby: I_{STB} = 22μA (typ.)
  - Active:
    - I_{NOR} = 0.15mA (typ.) when disable output channel
    - I_{NOR} = 0.23mA (typ.) when LED current = 25.5mA
- Analog dimming (current gain control)
  - Global 1-bit Maximum Current (MC): 25.5mA or 51mA
  - Individual 8-bits Dot Current (DC) setting
- PWM dimming up to audible-noise-free 23kHz
  - Individual 8-bits PWM dimming resolution
  - Linear or exponential dimming curves
- 400kHz (max.) I²C interface
- ESD: 4kV HBM, 1.5kV CDM
- Package
  - 1.6mm*2.1mm SOT583-8 with 0.5mm pitch
  - 1.36mm*0.8mm DSBGA-8 with 0.35mm pitch
- –40°C to 125°C operating temperature range

2 Applications

LED animation and indication for:

- Personal Electronics
  - Virtual Reality (VR) Headset
  - Gaming Controller and Peripherals
  - Electronic and Robotic Toys
  - Smart Speaker
  - Wireless Speaker
  - Solid State Drive (SSD)
  - Electronic Smart Lock
  - Headsets/Headphones and Earbuds
  - GPS Personal Navigation Device
- WLAN/Wi-Fi Access Point
- Video Doorbell
- Video Conference System

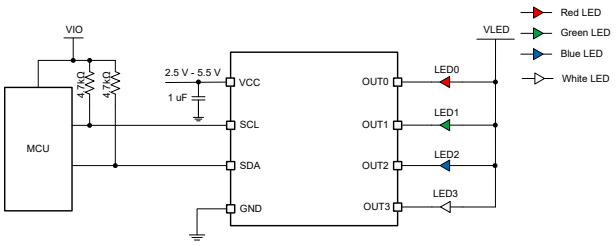
3 Description

The LP5816 is a 4-channel RGBW LED driver. The device has ultra-low operation current with 0.1μA (typical) in shutdown mode, 0.1mA (typical) when enable device and 0.2mA (typical) when illuminate LEDs.

Both analog dimming and PWM dimming methods are adopted to achieve powerful dimming performance. The output current of each LED can be adjusted with 256 steps from 0.1mA to 25.5mA or 0.2mA to 51mA. The 8-bits PWM generator enables smooth and audible-noise-free dimming control for LED brightness.

Package Information

PART NUMBER	PACKAGE	PACKAGE SIZE (NOM)
LP5816DRLR	SOT583 (8)	1.6mm × 2.1mm
LP5816YCHR	DSBGA (8)	1.36mm × 0.8mm



LP5816 Simplified Schematic

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Device Comparison....3
5 Pin Configuration and Functions....4
6 Specifications....5
6.1 Absolute Maximum Ratings....5
6.2 ESD Ratings....5
6.3 Recommended Operating Conditions....5
6.4 Thermal Information....5
6.5 Electrical Characteristics....6
6.6 Timing Requirements....7
6.7 Timing Diagrams....8
6.8 Typical Characteristics....8
7 Detailed Description....11
7.1 Overview....11
7.2 Functional Block Diagram....11
7.3 Feature Description....12
7.4 Device Functional Modes....15
7.5 Programming....17
7.6 Register Maps....19
8 Application and Implementation....27
8.1 Application Information....27
8.2 Typical Application....27
8.3 Power Supply Recommendations....32
8.4 Layout....32
9 Device and Documentation Support....33
9.1 Documentation Support....33
9.2 Receiving Notification of Documentation Updates....33
9.3 Support Resources....33
9.4 Trademarks....33
9.5 Electrostatic Discharge Caution....33
9.6 Glossary....33
10 Revision History....33
11 Mechanical, Packaging, and Orderable Information....34

4 Device Comparison

PART NUMBER	PACKAGE (1)	MATERIAL	LED NUMBER	AUTO ANIMATIO	INSTANT BLINKING	I²C ADDRESS	SOFTWARE COMPATIBLE
LP5816	SOT583-8	LP5814DRLR	4	Yes	No	0x2C	Yes
	DSBGA-8	LP5814YCHR					
	DSBGA-8	LP5814IYCHR			Yes		
LP5815	SOT583-8	LP5815DRLR	3			0x2D	
	DSBGA-8	LP5815YCHR					
LP5816	SOT583-8	LP5816DRLR	4	No	No	0x2C	
	DSBGA-8	LP5816YCHR					
LP5817	SOT583-8	LP5817DRLR	3			0x2D	
	DSBGA-8	LP5817YCHR					

(1) For the most up-to-date packaging information refer to the Section 11.

5 Pin Configuration and Functions

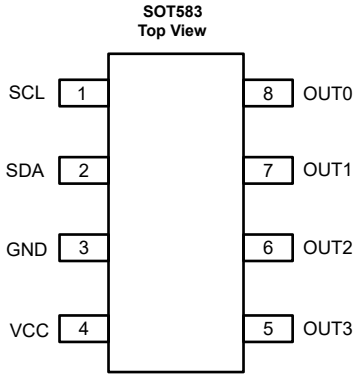


Figure 5-1. LP5816 DRL Package 8-Pin SOT583 Top View

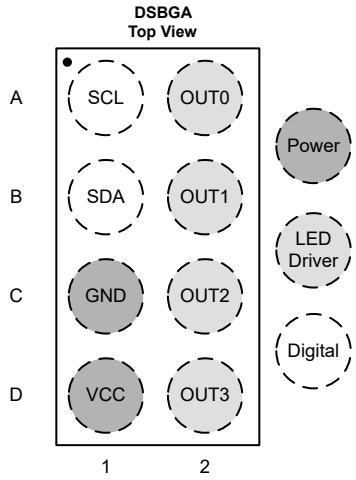


Figure 5-2. LP5816 YCH Package 8-Pin DSBGA Top View

Table 5-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	DRL	YCH		
SCL	1	A1	I	I^2C serial interface clock input.
SDA	2	B1	I/O	I^2C serial interface data input/output.
GND	3	C1	P	Ground.
VCC	4	D1	P	Power supply of the device. A 1 µF capacitor is recommended to be connected between this pin with GND and be placed as close to the device as possible.
OUT3	5	D2	O	Constant current sink output 3.
OUT2	6	C2	O	Constant current sink output 2.
OUT1	7	B2	O	Constant current sink output 1.
OUT0	8	A2	O	Constant current sink output 0.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range at terminals	VCC, SCL, SDA, OUT0, OUT1, OUT2, OUT3	–0.3	6	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Input voltage range	2.5		5.5	V
C_{IN}	Effective input capacitance range	1	4.7		µF
OUT0, OUT1, OUT2, OUT3	Voltage on OUT0, OUT1, OUT2, OUT3 pins	0		5.5	V
SCL, SDA	Voltage on SCL, SDA pins	0		5.5	V
T_A	Ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LP5816 DRL (SOT583) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	118.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	27.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Unless specified otherwise, typical characteristics apply over the full ambient temperature range (–40°C < T_A < +85°C), V_{CC} = 3.6V, C_{IN} = 1µF.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply						
V_{CC}	Input voltage range		2.5		5.5	V
V_{CC_UVLO}	Under-voltage lockout threshold	V_{CC} rising	2.2	2.3	2.4	V
		V_{CC} falling	2	2.1	2.2	V
I_{SD}	Shutdown current into VCC pin	V_{CC} = 3.6V		0.1	0.3	µA
I_{STB}	Standby current into VCC pin	V_{CC} = 3.6V, CHIP_EN = 0 (bit)		22	26	µA
I_{NOR}	Normal operation current into VCC pin	V_{CC} = 3.6V, CHIP_EN = 1 (bit), OUT0_EN = OUT1_EN = OUT2_EN = OUT3_EN = 0 (bit)		0.15	0.17	mA
I_{NOR}	Normal operation current into VCC pin	V_{CC} = 3.6V, CHIP_EN = 1 (bit), OUT0_EN = OUT1_EN = OUT2_EN = OUT3_EN = 1 (bit), I_{OUT0} = I_{OUT1} = I_{OUT2} = I_{OUT3} = 25.5mA (MAX_CURRENT = 0 (bit), OUTx_DC = FFh, OUTx_MANUAL_PWM = FFh)		0.23	0.29	mA
LED Driver Output						
I_{CS}	Constant current sink output range	V_{CC} = 3.6V, VLED = 5V, MAX_CURRENT = 0 (bit), OUTx_MANUAL_PWM = FFh (100% ON)	0.1		25.5	mA
		V_{CC} = 3.6V, VLED = 5V, MAX_CURRENT = 1 (bit), OUTx_MANUAL_PWM = FFh (100% ON)	0.2		51	mA
I_{CS_LKG}	Constant current sink leakage current	V_{CC} = 3.6V, OUTx = 1V, OUTx_MANUAL_PWM = 0 (0%)		0.1	1	µA
I_{ERR_D2D}	Device to device current error, I_{ERR_D2D} = (I_{AVE}-I_{SET})/I_{SET}×100%	All LEDs turn ON. Current set to 25.5mA (MAX_CURRENT = 0 (bit), OUTx_DC = FFh, OUTx_MANUAL_PWM = FFh)	–8		8	%
		All LEDs turn ON. Current set to 51mA (MAX_CURRENT = 1 (bit), OUTx_DC = FFh, OUTx_MANUAL_PWM = FFh)	–8		8	%
I_{ERR_C2C}	Channel to Channel current error I_{ERR_C2C} = (I_{OUTX}-I_{AVE})/I_{AVE}×100%	All LEDs turn ON. Current set to 25.5mA (MAX_CURRENT = 0 (bit), OUTx_DC = FFh, OUTx_MANUAL_PWM = FFh)	–3		3	%
		All LEDs turn ON. Current set to 51mA (MAX_CURRENT = 1 (bit), OUTx_DC = FFh, OUTx_MANUAL_PWM = FFh)	–2		2	%
V_{HR}	LED driver output headroom voltage	All LEDs turn ON. Current set to 25.5mA (MAX_CURRENT = 0 (bit), OUTx_DC = FFh, OUTx_MANUAL_PWM = FFh), V_{CC} = 3.6V			0.135	V
		All LEDs turn ON. Current set to 51mA (MAX_CURRENT = 1 (bit), OUTx_DC = FFh, OUTx_MANUAL_PWM = FFh), V_{CC} = 3.6V			0.275	V
		All LEDs turn ON. Current set to 25.5mA (MAX_CURRENT = 0 (bit), OUTx_DC = FFh, OUTx_MANUAL_PWM = FFh), V_{CC} = 2.5V			0.15	V
		All LEDs turn ON. Current set to 51mA (MAX_CURRENT = 1 (bit), OUTx_DC = FFh, OUTx_MANUAL_PWM = FFh), , V_{CC} = 2.5V			0.3	V
f_{LED_PWM}	PWM dimming frequency			23		kHz
f_{OSC}	Internal oscillator frequency			6		MHz

Unless specified otherwise, typical characteristics apply over the full ambient temperature range (–40°C < T_A < +85°C), V_{CC} = 3.6V, C_{IN} = 1µF.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic Interface						
V_{IH_LOGIC}	High level input voltage of SDA, SCL		1.4			V
V_{IL_LOGIC}	Low level input voltage of SDA, SCL				0.4	V
V_{OL_LOGIC}	Low level output voltage of SDA				0.4	V
Protection						
T_{SD}	Thermal shutdown threshold for LED driver part	T_J rising		150		°C
T_{SD_HYS}	Thermal shutdown hysteresis	T_J falling below T_{SD}		15		°C

6.6 Timing Requirements

Unless specified otherwise, typical characteristics apply over the full ambient temperature range (–40°C < TA < +85°C), V_{CC} = 3.6V, C_{IN} = 1µF.

I^2C Timing Requirements		MIN	NOM	MAX	UNIT
Standard-mode					
f_{SCL}	SCL clock frequency	0		100	kHz
1	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4			µs
2	LOW period of the SCL clock	4.7			µs
3	HIGH period of the SCL clock	4			µs
4	Set-up time for a repeated START condition	4.7			µs
5	Data hold time	0			µs
6	Data set-up time	250			ns
7	Rise time of both SDA and SCL signals			1000	ns
8	Fall time of both SDA and SCL signals			300	ns
9	Set-up time for STOP condition	4			µs
10	Bus free time between a STOP and START condition	4.7			µs
C_b	Capacitive load for each bus line			400	pF
Fast-mode					
f_{SCL}	SCL clock frequency	0		400	kHz
1	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.6			µs
2	LOW period of the SCL clock	1.3			µs
3	HIGH period of the SCL clock	0.6			µs
4	Set-up time for a repeated START condition	0.6			µs
5	Data hold time	0			µs
6	Data set-up time	100			ns
7	Rise time of both SDA and SCL signals			300	ns
8	Fall time of both SDA and SCL signals			300	ns
9	Set-up time for STOP condition	0.6			µs
10	Bus free time between a STOP and START condition	1.3			µs
C_b	Capacitive load for each bus line			400	pF

6.7 Timing Diagrams

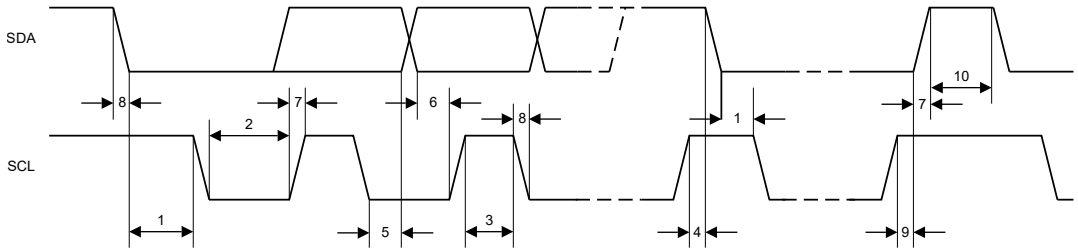


Figure 6-1. I²C Timing Parameters

6.8 Typical Characteristics

Unless specified otherwise, typical characteristics apply over the full ambient temperature range (–40°C < T_A < +85°C), V_{CC} = 3.6V, C_{IN} = 1µF

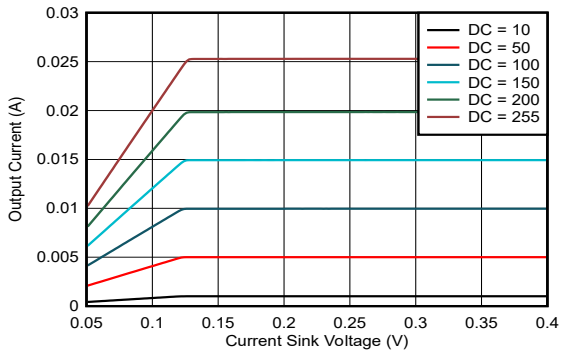


Figure 6-2. Current Sinks Voltage vs Current (MC = 0, VCC = 2.5V)

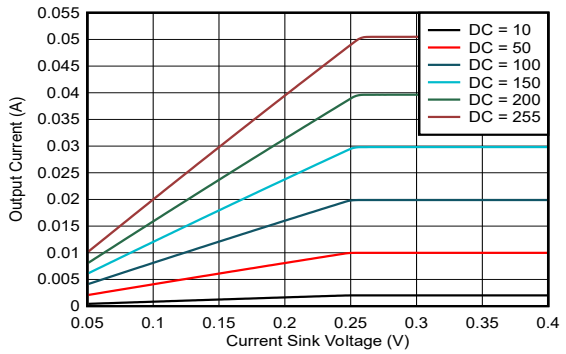


Figure 6-3. Current Sinks Voltage vs Current (MC = 1, VCC = 2.5V)

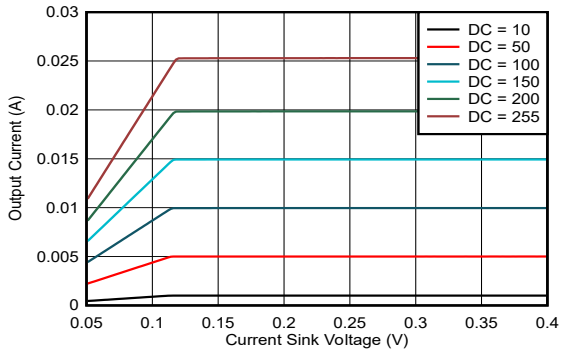


Figure 6-4. Current Sinks Voltage vs Current (MC = 0, VCC = 3.6V)

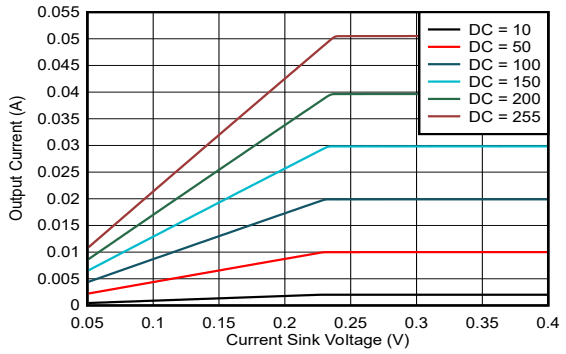


Figure 6-5. Current Sinks Voltage vs Current (MC = 1, VCC = 3.6V)

6.8 Typical Characteristics (continued)

Unless specified otherwise, typical characteristics apply over the full ambient temperature range (–40°C < T_A < +85°C), V_{CC} = 3.6V, C_{IN} = 1µF

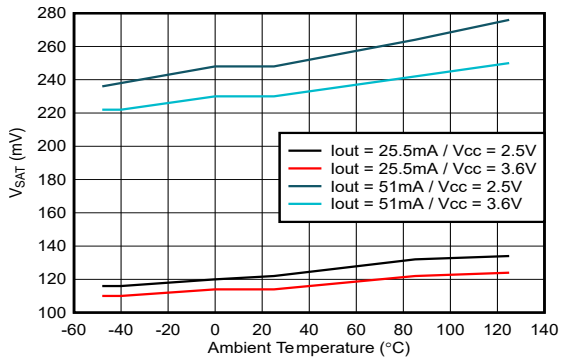


Figure 6-6. V_{SAT} vs Temperature

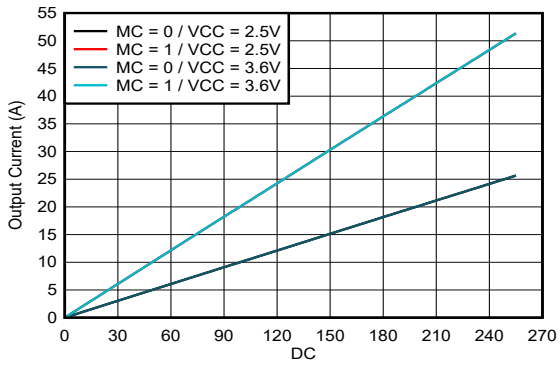


Figure 6-7. DC vs Current

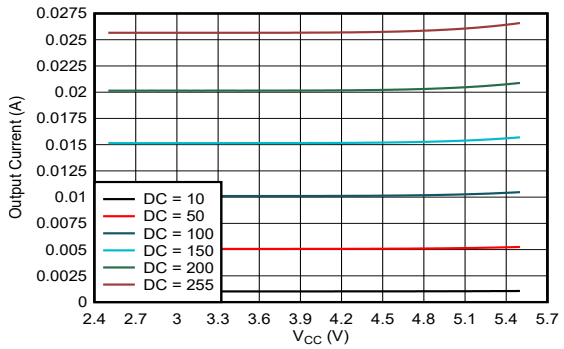


Figure 6-8. V_{CC} vs Current (MC = 0)

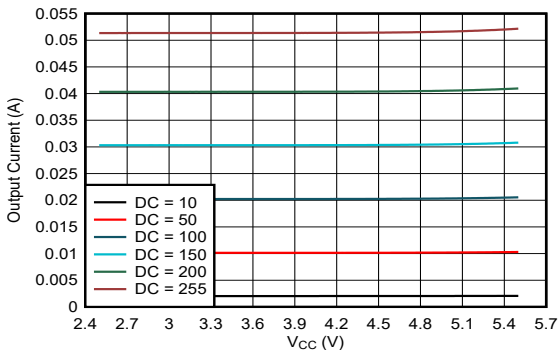


Figure 6-9. V_{CC} vs Current (MC = 1)

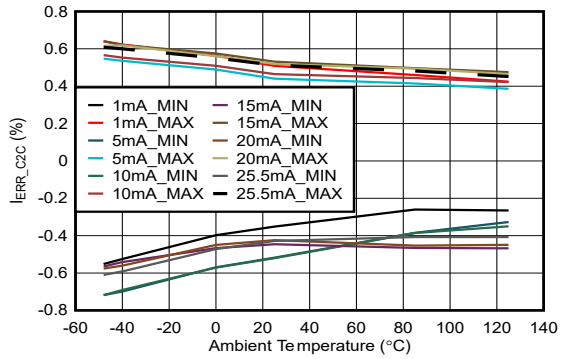


Figure 6-10. Channel-to-Channel Current Accuracy vs Temperature (MC = 0, VCC = 2.5V)

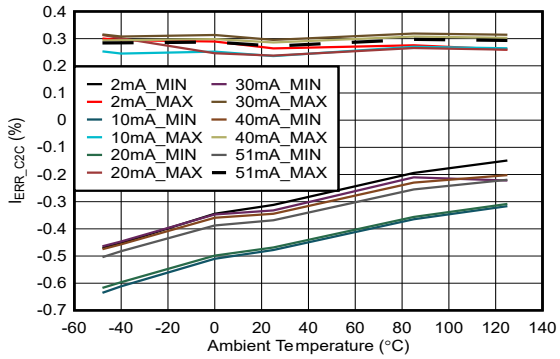


Figure 6-11. Channel-to-Channel Current Accuracy vs Temperature (MC = 1, VCC = 2.5V)

6.8 Typical Characteristics (continued)

Unless specified otherwise, typical characteristics apply over the full ambient temperature range (–40°C < T_A < +85°C), V_{CC} = 3.6V, C_{IN} = 1µF

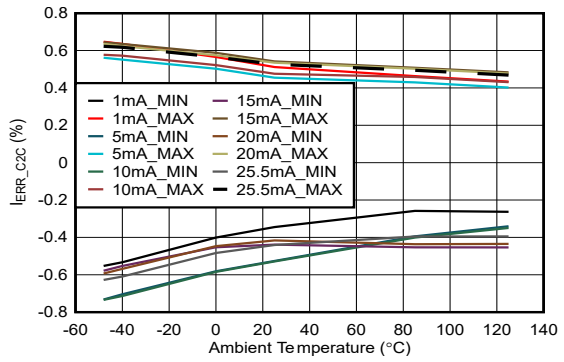


Figure 6-12. Channel-to-Channel Current Accuracy vs Temperature (MC = 0, VCC = 3.6V)

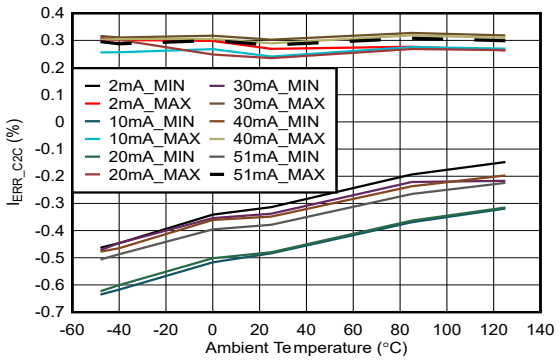


Figure 6-13. Channel-to-Channel Current Accuracy vs Temperature (MC = 1, VCC = 3.6V)

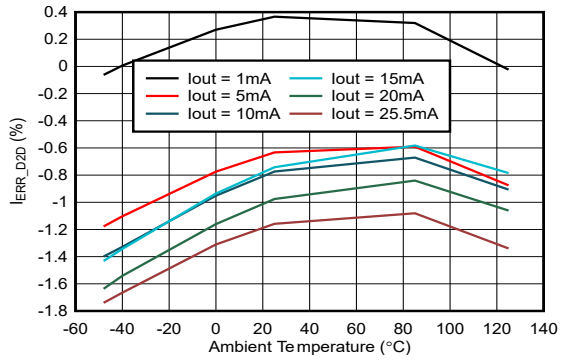


Figure 6-14. Device-to-Device Current Accuracy vs Temperature (MC = 0, VCC = 2.5V)

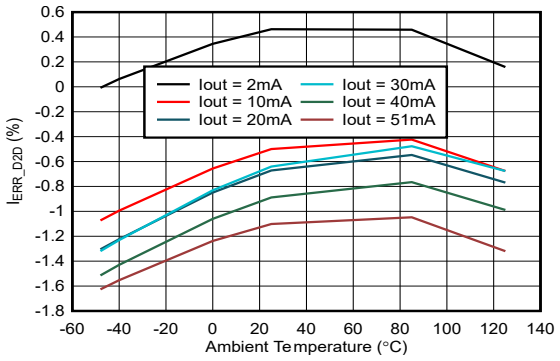


Figure 6-15. Device-to-Device Current Accuracy vs Temperature (MC = 1, VCC = 2.5V)

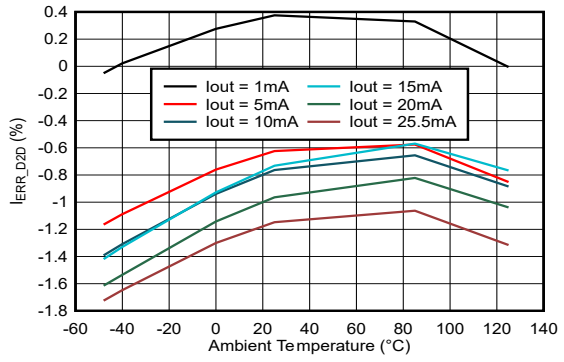


Figure 6-16. Device-to-Device Current Accuracy vs Temperature (MC = 0, VCC = 3.6V)

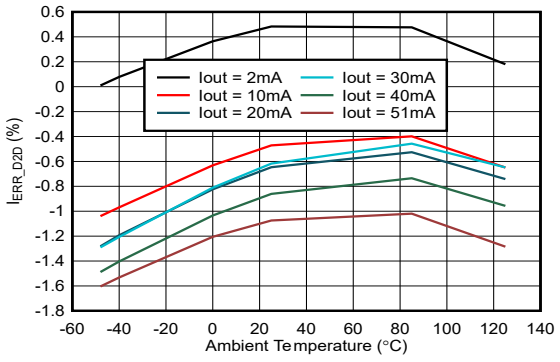


Figure 6-17. Device-to-Device Current Accuracy vs Temperature (MC = 1, VCC = 3.6V)

7 Detailed Description

7.1 Overview

The LP5816 is a 4 channel RGBW LED driver. The maximum output current of each channel is up to 51mA and can be adjusted by 256 steps from 0 to the full current. Besides the annalog dimming, every channel supports 8-bit PWM dimming.

The LP5816 features ultra-low shutdown current that is about 0.1uA. Two approaches are provided to control the LP5816 enter shutdown mode, sending shutdown command or constantly pulling down SCL, which improves the flexibility in system design for different application requirements.

7.2 Functional Block Diagram

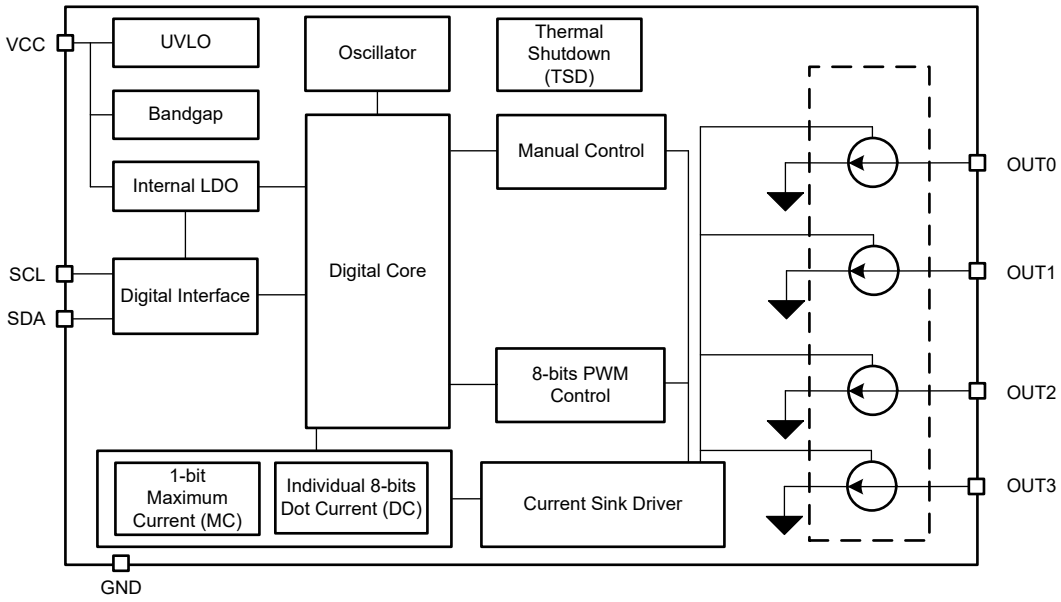


Figure 7-1. LP5816 Function Block

7.3 Feature Description

7.3.1 Analog Dimming

There are two methods to control the current gain of each output channel.

- Global 1-bit Maximum Current (MC) control for all channels without external resistor
- Individual 8-bit Dot Current (DC) control for each channel

The maximum output current I_{OUT_max} of each channel can be programmed by the 1 bit MAX_CURRENT. When the device is powered on, the default value of MC is 0h, which is 25.5mA.

Table 7-1. Maximum Current (MC) Bit Setting

1-bit Maximum Current (MC)		I_{OUT_MAX} (mA)
Binary	Decimal	
0 (default)	0 (default)	25.5 (default)
1	1	51

The LP5816 can individually adjust the analog output current of each channel by using Dot Current (DC) function. The brightness deviation among the LED bins can be miminized to achieve uniform display performance through the DC setting. The DC is programmed in an 8-bit depth, so the analog current can be adjusted with 256 steps from 0 to 100% of I_{OUT_MAX}. The default value of all DC is 0h, which is not current output.

Table 7-2. Dot Current (DC) Bits Setting

8-bits Dot Current (DC) Register		Ratio of I_{OUT_MAX}
Binary	Decimal	
0000 0000 (default)	0 (default)	0% (default)
0000 0001	1	0.39%
0000 0010	2	0.78%
---	---	---
1000 0000	128	50.2%
---	---	---
1111 1101	253	99.2%
1111 1110	254	99.6%
1111 1111	255	100%

By configuring the MC and DC, the analog output current of each channel can be calculated as Equation 1:

$$I_{OUT}\left(mA\right) = I_{OUT\_MAX} \times \frac{DC}{255} \quad (1)$$

The average output current of each channel can be caculated asEquation 2:

$$I_{AVE}\left(mA\right) = I_{OUT\_MAX} \times \frac{DC}{255} \times D_{PWM} \quad (2)$$

- D_{PWM} is the PWM duty.

7.3.2 PWM Dimming

The LP5816 supports 8-bit PWM dimming with 23kHz frequency. The device integrates an internal 6MHz oscillator to generate the PWM clock.

The PWM output value of each channel is controlled by the OUT0_MANUAL_PWM, OUT1_MANUAL_PWM, OUT2_MANUAL_PWM and OUT3_MANUAL_PWM separately.

If OUT0_FADE_EN, OUT1_FADE_EN, OUT2_FADE_EN and OUT3_FADE_EN bit in DEV_CONFIG2 register is set as 0, the output PWM value updates immeditaly to the latest received PWM set value.

If OUT0_FADE_EN, OUT1_FADE_EN, OUT2_FADE_EN and OUT3_FADE_EN bit in DEV_CONFIG2 register is set as 1, the fade in or out function is enabled, the output PWM ramps up or down smoothly to the latest received PWM value within the time period defined by OUT_FADE_TIME automatically.

The LP5816 allows users to configure the dimming scale as exponential curve or linear curve for each channel separately through the OUT0_EXP_EN, OUT1_EXP_EN, OUT2_EXP_EN and OUT3_EXP_EN in DEV_CONFIG3 register. A human-eye-friendly visual performance can be achieved by using the internal exponential scale. The linear scale has great linearity between PWM duty cycle and PWM setting value, which provides flexible approach for external controlled gamma correction algorithm. The 8-bit linear and exponential curves are shown as Figure 7-2.

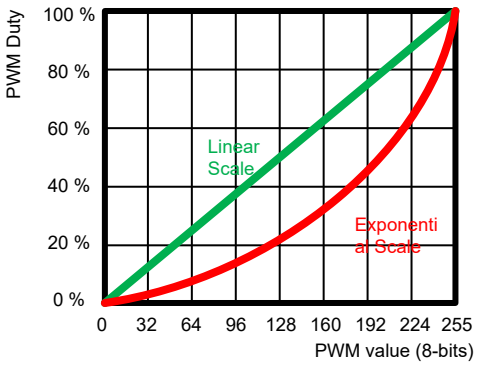


Figure 7-2. Linear and Exponential PWM Dimming Curves

7.3.3 Sloper

In manual control mode, output fade in or out is supported when LED0_FADE_EN, LED1_FADE_EN, LED2_FADE_EN and LED3_FADE_EN bit in DEV_CONFIG2 register is set as 1. Sloper is the basic element to achieve autonomous fade in and fade out animations. The output can achieve 256 steps fade in or fade out effects from 'PWM_Start' to 'PWM_End' within a specified time period T as shown in Figure 7-3. Exponential dimming curve can also be supported in the sloper.

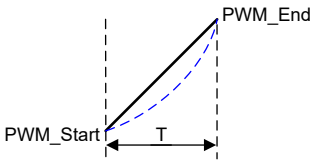


Figure 7-3. Sloper Curve Demonstration

The programable time T is selectable from 0 to around 8s with 16 levels shown in Table 7-3.

Table 7-3. Programable Time Options

Register Value	0h	1h	2h	3h	4h	5h	6h	7h	8h	9h	Ah	Bh	Ch	Dh	Eh	Fh
Time (Typ.)	0s	0.05s	0.1s	0.15s	0.2s	0.25s	0.3s	0.35s	0.4s	0.45s	0.5s	1s	2s	4s	6s	8s

7.3.4 Protections

7.3.4.1 UVLO

The LP5816 has an internal comparator that monitors the voltage at VCC. When V_{CC} is below V_{CC_UVLO}, the device resets and keeps in Power On Reset (POR) state. When V_{CC} ramps above V_{CC_UVLO}, the device enters INITIALIZATION mode and the POR flag is set. The POR flag needs manual clear by setting POR_CLR bit when CHIP_EN = 1.

7.3.4.2 Thermal Shutdown

The LP5816 implements a thermal shutdown mechanism to protect the device from damage due to overheating. When the junction temperature of the device rises to 155°C (typical), the device turns off all output channels. The TSD flag is set to indicate thermal shutdown is triggered. The LP5816 releases thermal shutdown when the junction temperature reduces to 140°C (typical). The TSD flag needs manual clear by setting TSD_CLR bit when CHIP_EN = 1.

7.4 Device Functional Modes

The Figure 7-4 shows the function modes of the LED driver.

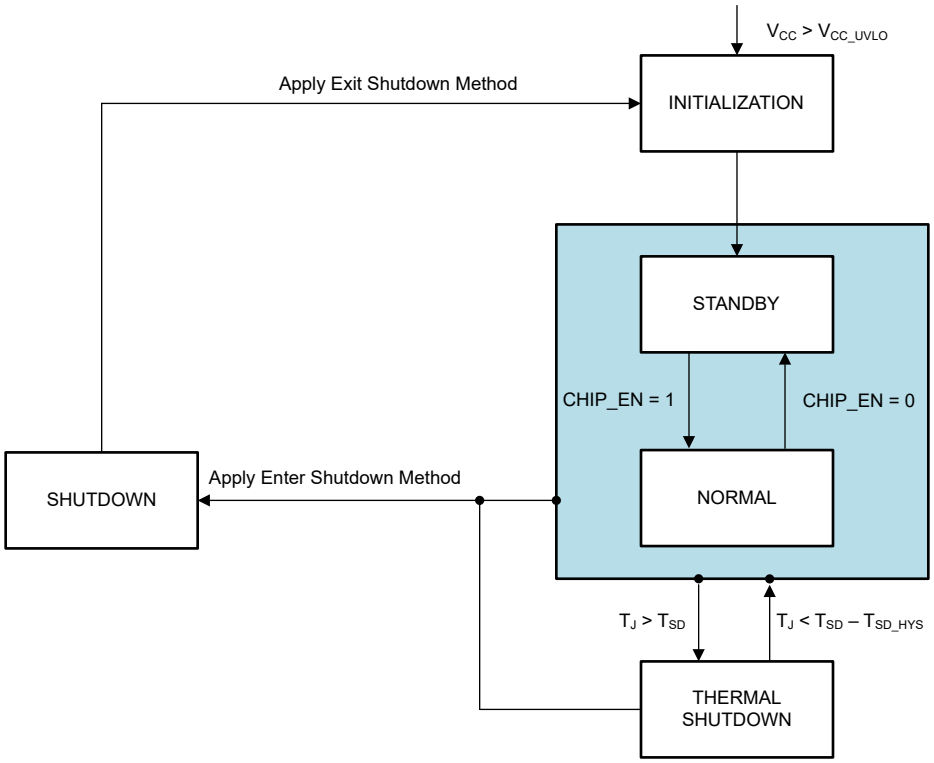


Figure 7-4. Functional Modes

7.4.1 Initialization Mode

The LP5816 enters INITIALIZATION mode when VCC voltage ramps above the V_{CC_UVLO} or exits from SHUTDOWN mode. The LP5816 reset all registers to default value in INITIALIZATION mode. The POR flag is set to 1 after exiting from INITIALIZATION mode to indicate the reset history.

7.4.2 Standby and Normal Mode

The LP5816 enters STANDBY mode when CHIP_EN = 0 or NORMAL mode when CHIP_EN = 1 after exiting from INITIALIZATION mode or THERMAL SHUTDOWN mode.

While staying in STANDBY or NORMAL mode,

- when Enter Shutdown Method is applied, the LP5816 enters SHUTDOWN mode. The Enter Shutdown Method is described in Shutdown Mode.
- when the junction temperature of the LP5816 rises above the thermal shutdown threshold T_{SD}, the LP5816 turns off all output channels and enters THERMAL SHUTDOWN mode.

7.4.3 Shutdown Mode

The LP5816 supports shutdown mode to minimize the power consumption from VCC. The qusicent current from VCC decreases to 0.1 uA (typical) in SHUTDOWN mode. The LP5816 provides two pairs of methods to control the device enter and exit SHUTDOWN mode.

- Figure 7-5 shows the method 1
  - **Enter shutdown**, send Shutdown_command by writing 0x33 to register 0xD though I^2C communication.
  - **Exit shutdown**, toggle SDA 8 times to generate 8 falling edges while keeping SCL as high. The supported maximum toggle frequency for SDA is 100kHz.

- Figure 7-6 shows the method 2
  - **Enter shutdown**, pull down SCL for 100ms while keeping SDA as high.
  - **Exit shutdown**, pull up SCL to generate one rising edge regardless of SDA state.

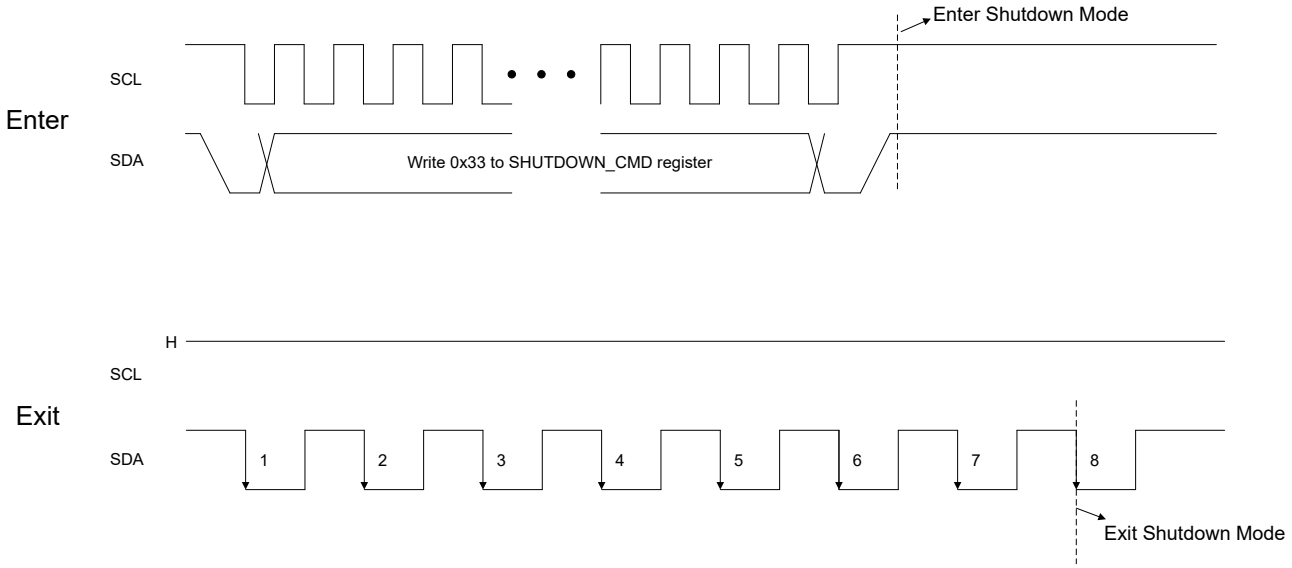


Figure 7-5. Enter and Exit Shutdown Mode Method Pair 1

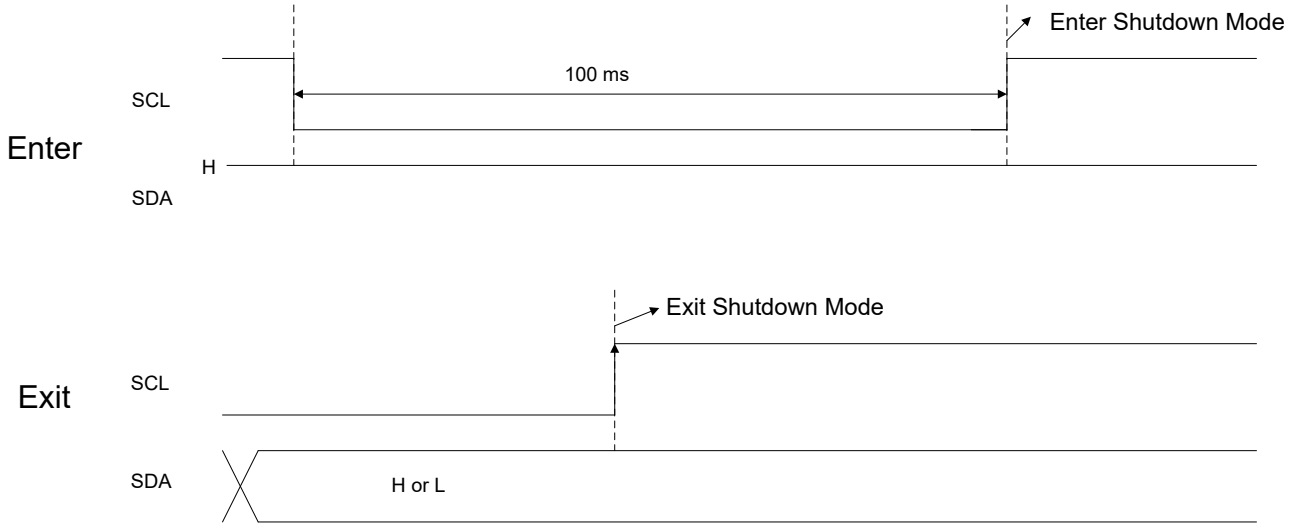


Figure 7-6. Enter and Exit Shutdown Mode Method Pair 2

7.4.4 Thermal Shutdown Mode

All output channels are turned off while the LP5816 staying in THERMAL SHUTDOWN mode. The I2C interface is still active and the LP5816 enters SHUTDOWN mode when Enter Shutdown Method is applied.

When the junction temperature of LP5816 falles blow the thermal shutdown threshold, the LP5816 enters STANDBY mode when CHIP_EN = 0 or NORMAL mode when CHIP_EN = 1 after exiting from THERMAL SHUTDOWN mode. The TSD flag needs manual clear through setting TSD_CLR bit when CHIP_EN = 1.

7.5 Programming

The LP5816 is compatible with I²C standard specification. The device supports standard mode (100kHz maximum) and fast mode (400kHz maximum). The device chip address is 0x2C.

7.5.1 I²C Data Tansactions

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when clock signal is LOW. START and STOP conditions classify the beginning and the end of the data transfer session. A START condition is defined as the SDA signal transitioning from and the end of the data transfer session. A START condition is defined as the SDA signal transitioning from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The bus leader always generates START and STOP conditions. The bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the bus leader can generate repeated START conditions. First START and repeated START conditions are functionally equivalent.

Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the leader. The leader releases the SDA line (HIGH) during the acknowledge clock pulse. The device pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The device generates an acknowledge after each byte has been received.

There is one exception to the acknowledge after every byte rule. When the leader is the receiver, the receiver must indicate to the transmitter an end of data by not acknowledging (negative acknowledge) the last byte clocked out of the follower. This negative acknowledge still includes the acknowledge clock pulse (generated by the leader), but the SDA line is not pulled down.

7.5.2 I²C Data Format

The address and data bits are transmitted MSB first with 8-bits length format in each cycle. Each transmission is started with Address Byte 1, which are divided into 7 bits of the chip address and 1 read/write bit. The 8 bits of register address are put in Address Byte 2. The device supports both independent mode and broadcast mode. The auto-increment feature allows writing / reading several consecutive registers within one transmission. If not consecutive, a new transmission must be started.

Table 7-4. I²C Data Format

Address Byte1	Chip Address							R/W
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Independent	0	1	0	1	1	0	0	R: 1 W: 0
Broadcast	0	1	1	0	1	0	0	
Address Byte2	Register Address							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	7th bit	6th bit	5th bit	4th bit	3rd bit	2nd bit	1st bit	0 bit

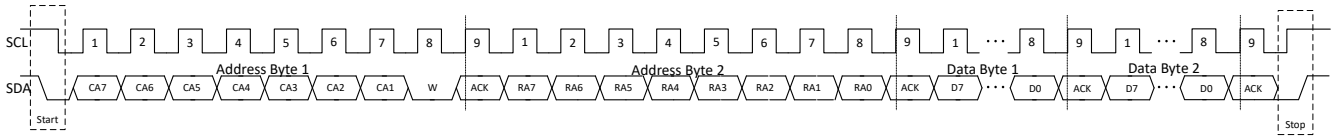


Figure 7-7. I²C Write Timming

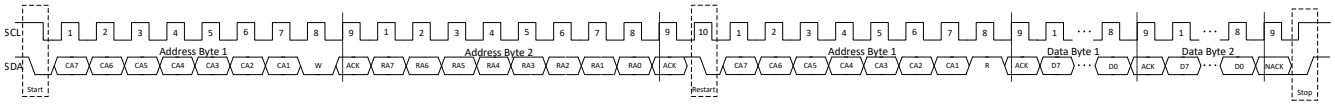


Figure 7-8. I²C Read Timming

7.5.3 Command Description

The LP5816 has 3 dedicated software commands, Shutdown_command, Reset_command and Update_command.

- Send **Shutdown_command** is one of the 2 methods to make the device enter SHUTDOWN mode as described in Shutdown Mode .
- Send **Reset_command** to reset all registers to default value.
- Send **Update_command** to make the modified value in the device configuration registers as shown in Table 7-5 to take effect. The LP5816 responds to the Update_command only when CHIP_EN = 1.

Table 7-5. Update_command Control Registers

Register Address	Register Acronym
0x01 to 0x04	DEV_CONGIF*x*, *x* = 0, 1, 2, 3

7.6 Register Maps

Table 7-6. Register Maps

Address	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0h	CHIP_EN	RESERVED							CHIP_EN
1h	DEV_CONFIG0	RESERVED							MAX_CURRENT
2h	DEV_CONFIG1	RESERVED				OUT3_EN	OUT2_EN	OUT1_EN	OUT0_EN
3h	DEV_CONFIG2	LED_FADE_TIME				OUT3_FADE_EN	OUT2_FADE_EN	OUT1_FADE_EN	OUT0_FADE_EN
4h	DEV_CONFIG3	OUT3_EXP_EN	OUT2_EXP_EN	OUT1_EXP_EN	OUT0_EXP_EN	RESERVED			
Dh	SHUTDOWN_CMD	SHUTDOWN							
Eh	RESET_CMD	RESET							
Fh	UPDATE_CMD	UPDATE							
13h	FLAG_CLR	RESERVED						TSD_CLR	POR_CLR
14h	OUT0_DC	OUT0_DC							
15h	OUT1_DC	OUT1_DC							
16h	OUT2_DC	OUT2_DC							
17h	OUT3_DC	OUT3_DC							
18h	OUT0_MANUAL_PWM	OUT0_MANUAL_PWM							
19h	OUT1_MANUAL_PWM	OUT1_MANUAL_PWM							
1Ah	OUT2_MANUAL_PWM	OUT2_MANUAL_PWM							
1Bh	OUT3_MANUAL_PWM	OUT3_MANUAL_PWM							
40h	FLAG	RESERVED						TSD	POR

Complex bit access types are encoded to fit into small table cells. Table 7-7 shows the codes that are used for access types in this section.

Table 7-7. Register Maps Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

7.6.1 CHIP_EN (Address = 0h) [Reset = 00h]

CHIP_EN is shown in Figure 7-9 and described in Table 7-8.

Return to the Summary Table.

Figure 7-9. CHIP_EN

7	6	5	4	3	2	1	0
RESERVED							CHIP_EN
R-0h							R/W-0h

Figure 7-9. CHIP_EN (continued)

Table 7-8. CHIP_EN Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	Reserved
0	CHIP_EN	R/W	0h	Device enable. 0x0 = Disable 0x1 = Enable

7.6.2 DEV_CONFIG0 (Address = 1h) [Reset = 00h]

DEV_CONFIG0 is shown in Figure 7-10 and described in Table 7-9.

Return to the Summary Table.

Figure 7-10. DEV_CONFIG0

7	6	5	4	3	2	1	0
RESERVED							MAX_CURRENT
R-0h							R/W-0h

Table 7-9. DEV_CONFIG0 Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0h	Reserved
0	MAX_CURRENT	R/W	0h	Max output current. 0x0 = 25.5mA 0x1 = 51mA

7.6.3 DEV_CONFIG1 (Address = 2h) [Reset = 00h]

DEV_CONFIG1 is shown in Figure 7-11 and described in Table 7-10.

Return to the Summary Table.

Figure 7-11. DEV_CONFIG1

7	6	5	4	3	2	1	0
RESERVED				OUT3_EN	OUT2_EN	OUT1_EN	OUT0_EN
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-10. DEV_CONFIG1 Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3	OUT3_EN	R/W	0h	OUT3 enable. 0x0 = Disable 0x1 = Enable
2	OUT2_EN	R/W	0h	OUT2 enable. 0x0 = Disable 0x1 = Enable
1	OUT1_EN	R/W	0h	OUT1 enable. 0x0 = Disable 0x1 = Enable
0	OUT0_EN	R/W	0h	OUT0 enable. 0x0 = Disable 0x1 = Enable

7.6.4 DEV_CONFIG2 (Address = 3h) [Reset = 00h]

DEV_CONFIG2 is shown in Figure 7-12 and described in Table 7-11.

Return to the Summary Table.

Figure 7-12. DEV_CONFIG2

7	6	5	4	3	2	1	0
LED_FADE_TIME				OUT3_FADE_EN	OUT2_FADE_EN	OUT1_FADE_EN	OUT0_FADE_EN
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-11. DEV_CONFIG2 Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LED_FADE_TIME	R/W	0h	OUT fade sloper time. 0x0 = 0s 0x1 = 0.05s 0x2 = 0.10s 0x3 = 0.15s 0x4 = 0.20s 0x5 = 0.25s 0x6 = 0.30s 0x7 = 0.35s 0x8 = 0.40s 0x9 = 0.45s 0xA = 0.50s 0xB = 1.00s 0xC = 2.00s 0xD = 4.00s 0xE = 6.00s 0xF = 8.00s
3	OUT3_FADE_EN	R/W	0h	OUT3 fade in and out enable. 0x0 = Disable 0x1 = Enable
2	OUT2_FADE_EN	R/W	0h	OUT2 fade in and out enable. 0x0 = Disable 0x1 = Enable
1	OUT1_FADE_EN	R/W	0h	OUT1 fade in and out enable. 0x0 = Disable 0x1 = Enable
0	OUT0_FADE_EN	R/W	0h	OUT0 fade in and out enable. 0x0 = Disable 0x1 = Enable

7.6.5 DEV_CONFIG3 (Address = 4h) [Reset = 00h]

DEV_CONFIG3 is shown in Figure 7-13 and described in Table 7-12.

Return to the Summary Table.

Figure 7-13. DEV_CONFIG3

7	6	5	4	3	2	1	0
OUT3_EXP_EN	OUT2_EXP_EN	OUT1_EXP_EN	OUT0_EXP_EN	RESERVED			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			

Table 7-12. DEV_CONFIG3 Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT3_EXP_EN	R/W	0h	OUT3 exponential PWM dimming enable. 0x0 = Disable 0x1 = Enable

Table 7-12. DEV_CONFIG3 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	OUT2_EXP_EN	R/W	0h	OUT2 exponential PWM dimming enable. 0x0 = Disable 0x1 = Enable
5	OUT1_EXP_EN	R/W	0h	OUT1 exponential PWM dimming enable. 0x0 = Disable 0x1 = Enable
4	OUT0_EXP_EN	R/W	0h	OUT0 exponential PWM dimming enable. 0x0 = Disable 0x1 = Enable
3-0	RESERVED	R	0h	Reserved

7.6.6 SHUTDOWN_CMD (Address = Dh) [Reset = 00h]

SHUTDOWN_CMD is shown in Figure 7-14 and described in Table 7-13.

Return to the Summary Table.

Figure 7-14. SHUTDOWN_CMD

7	6	5	4	3	2	1	0
SHUTDOWN							
W-0h							

Table 7-13. SHUTDOWN_CMD Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SHUTDOWN	W	0h	0x33 = Enter shutdown mode

7.6.7 RESET_CMD (Address = Eh) [Reset = 00h]

RESET_CMD is shown in Figure 7-15 and described in Table 7-14.

Return to the Summary Table.

Figure 7-15. RESET_CMD

7	6	5	4	3	2	1	0
RESET							
W-0h							

Table 7-14. RESET_CMD Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESET	W	0h	0xCC = Reset all the registers to default value

7.6.8 UPDATE_CMD (Address = Fh) [Reset = 00h]

UPDATE_CMD is shown in Figure 7-16 and described in Table 7-15.

Return to the Summary Table.

Figure 7-16. UPDATE_CMD

7	6	5	4	3	2	1	0
UPDATE							
W-0h							

Table 7-15. UPDATE_CMD Field Descriptions

Bit	Field	Type	Reset	Description
7-0	UPDATE	W	0h	0x55 = Update all device configuration registers value

7.6.9 FLAG_CLR (Address = 13h) [Reset = 00h]

FLAG_CLR is shown in Figure 7-17 and described in Table 7-16.

Return to the Summary Table.

Figure 7-17. FLAG_CLR

7	6	5	4	3	2	1	0
RESERVED						TSD_CLR	POR_CLR
R-0h						W1C-0h	W1C-0h

Table 7-16. FLAG_CLR Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1	TSD_CLR	W1C	0h	Write 1 to clear TSD flag.
0	POR_CLR	W1C	0h	Write 1 to clear POR flag.

7.6.10 OUT0_DC (Address = 14h) [Reset = 00h]

OUT0_DC is shown in Figure 7-18 and described in Table 7-17.

Return to the Summary Table.

Figure 7-18. OUT0_DC

7	6	5	4	3	2	1	0
OUT0_DC							
R/W-0h							

Table 7-17. OUT0_DC Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT0_DC	R/W	0h	OUT0 DC setting.

7.6.11 OUT1_DC (Address = 15h) [Reset = 00h]

OUT1_DC is shown in Figure 7-19 and described in Table 7-18.

Return to the Summary Table.

Figure 7-19. OUT1_DC

7	6	5	4	3	2	1	0
OUT1_DC							
R/W-0h							

Table 7-18. OUT1_DC Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT1_DC	R/W	0h	OUT1 DC setting.

7.6.12 OUT2_DC (Address = 16h) [Reset = 00h]

OUT2_DC is shown in Figure 7-20 and described in Table 7-19.

Return to the Summary Table.

Figure 7-20. OUT2_DC

7	6	5	4	3	2	1	0
OUT2_DC							
R/W-0h							

Table 7-19. OUT2_DC Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT2_DC	R/W	0h	OUT2 DC setting.

7.6.13 OUT3_DC (Address = 17h) [Reset = 00h]

OUT3_DC is shown in Figure 7-21 and described in Table 7-20.

Return to the Summary Table.

Figure 7-21. OUT3_DC

7	6	5	4	3	2	1	0
OUT3_DC							
R/W-0h							

Table 7-20. OUT3_DC Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT3_DC	R/W	0h	OUT3 DC setting.

7.6.14 OUT0_MANUAL_PWM (Address = 18h) [Reset = 00h]

OUT0_MANUAL_PWM is shown in Figure 7-22 and described in Table 7-21.

Return to the Summary Table.

Figure 7-22. OUT0_MANUAL_PWM

7	6	5	4	3	2	1	0
OUT0_MANUAL_PWM							
R/W-0h							

Table 7-21. OUT0_MANUAL_PWM Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT0_MANUAL_PWM	R/W	0h	OUT0 manual PWM setting. 0x00 = 0% ... 0x80 = 50% ... 0xFF = 100%

7.6.15 OUT1_MANUAL_PWM (Address = 19h) [Reset = 00h]

OUT1_MANUAL_PWM is shown in Figure 7-23 and described in Table 7-22.

Return to the Summary Table.

Figure 7-23. OUT1_MANUAL_PWM

7	6	5	4	3	2	1	0
OUT1_MANUAL_PWM							
R/W-0h							

Table 7-22. OUT1_MANUAL_PWM Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT1_MANUAL_PWM	R/W	0h	OUT1 manual PWM setting. 0x00 = 0% ... 0x80 = 50% ... 0xFF = 100%

7.6.16 OUT2_MANUAL_PWM (Address = 1Ah) [Reset = 00h]

OUT2_MANUAL_PWM is shown in Figure 7-24 and described in Table 7-23.

Return to the Summary Table.

Figure 7-24. OUT2_MANUAL_PWM

7	6	5	4	3	2	1	0
OUT2_MANUAL_PWM							
R/W-0h							

Table 7-23. OUT2_MANUAL_PWM Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT2_MANUAL_PWM	R/W	0h	OUT2 manual PWM setting. 0x00 = 0% ... 0x80 = 50% ... 0xFF = 100%

7.6.17 OUT3_MANUAL_PWM (Address = 1Bh) [Reset = 00h]

OUT3_MANUAL_PWM is shown in Figure 7-25 and described in Table 7-24.

Return to the Summary Table.

Figure 7-25. OUT3_MANUAL_PWM

7	6	5	4	3	2	1	0
OUT3_MANUAL_PWM							
R/W-0h							

Table 7-24. OUT3_MANUAL_PWM Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT3_MANUAL_PWM	R/W	0h	OUT3 manual PWM setting. 0x00 = 0% ... 0x80 = 50% ... 0xFF = 100%

7.6.18 FLAG (Address = 40h) [Reset = 00h]

FLAG is shown in Figure 7-26 and described in Table 7-25.

Return to the Summary Table.

Figure 7-26. FLAG

7	6	5	4	3	2	1	0
RESERVED						TSD	POR
R-0h						R-0h	R-0h

Table 7-25. FLAG Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1	TSD	R	0h	TSD flag. 0x0 = TSD is not triggered 0x1 = TSD is triggered
0	POR	R	0h	POR flag. 0x0 = POR is not triggered 0x1 = POR is triggered

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LP5816 is a 4 channel RGBW LED driver. The device has ultra-low operation current at active mode and only consumes 0.25mA when LED current is set at 25mA. In battery powered applications like e-tag, ear bud, e-cigarettes, VR headset, RGB mouse, smart speaker, and other hand-held devices, LP5816 can provide premium LED lighting effects with low power consumption and small package.

8.2 Typical Application

8.2.1 Application

Figure 8-1 shows an example of typical application, which uses one LP5816 to drive RGBW LEDs through I^2C communication.

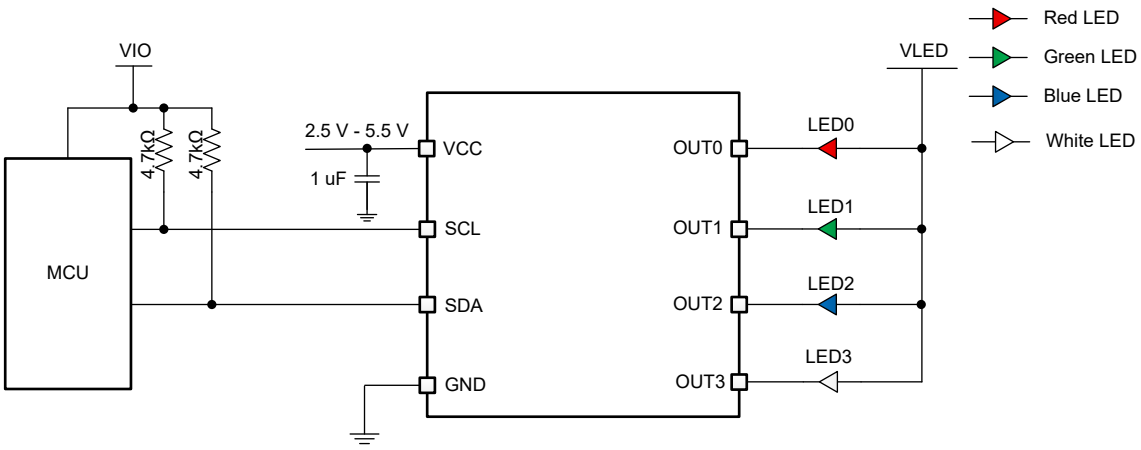


Figure 8-1. Typical Application - LP5816 Driving RGBW LEDs

8.2.2 Design Parameters

Design Parameters shows the typical design parameters of Application.

Table 8-1. Design Parameters

PARAMETER	VALUE
Input voltage	3.6V to 4.2V by one Li-on battery cell
RGBW LED count	1
LED maximum average current (red, green, blue, white)	51mA, 40.8mA, 40.8mA, 40.8mA
LED PWM frequency	23kHz
LED PWM duty cycle (red, green, blue, white)	100%, 80%, 40%, 20%

8.2.3 Detailed Design Procedure

This section showcases the detailed design procedures for LP5816 including components selection and how to light on LED.

8.2.3.1 Program Procedure

After VCC powering up, enable the device by setting CHIP_EN = 1. Set the maximum current for each output. Then set the device configuration registers to enbale the output and select the dimming mode for each output. Finally, Send UPDATE_CMD to make the prior configuration settings take effect. After that, set the PWM value to adjust the output brightness.

The detailed program procedure is illustrated in Figure 8-2.

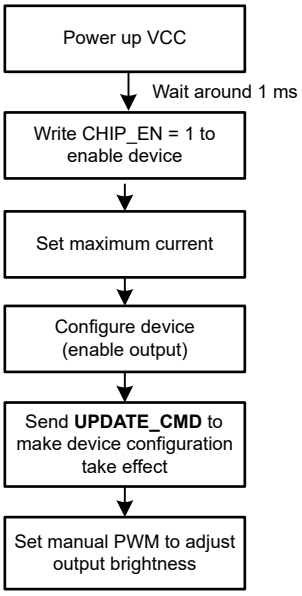


Figure 8-2. Program Procedure

8.2.3.2 Programming Example

To get the design parameters in Section 8.2.2, the following program steps can be referred.

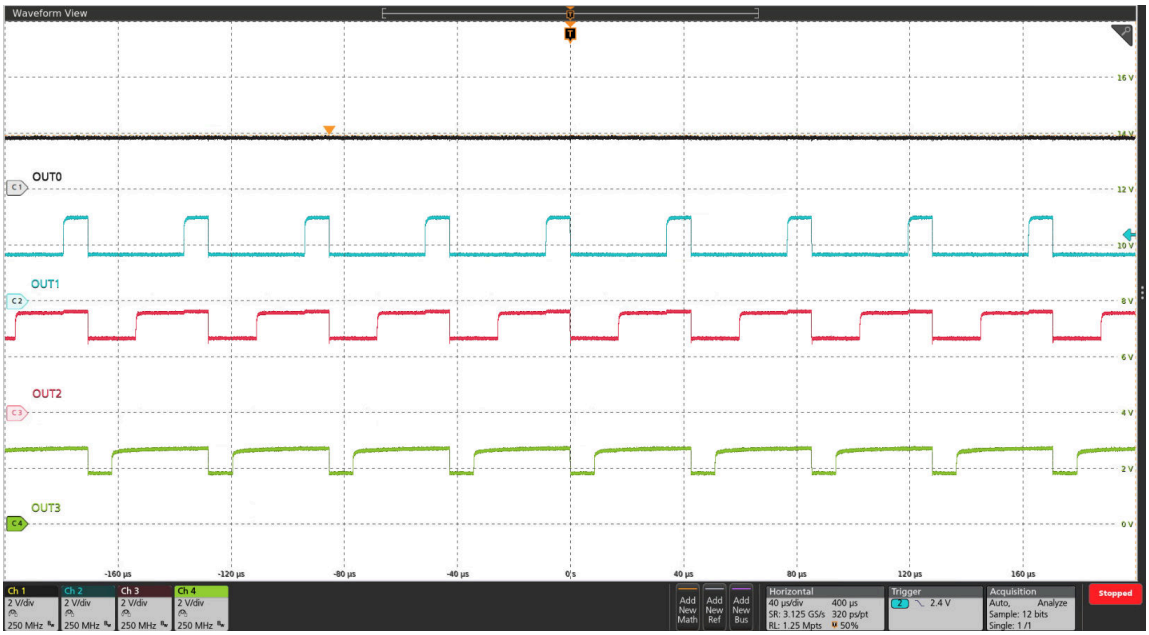
After VCC powering up and wait around 1ms,

1. Set CHIP_EN = 1 to enable the device(**Write 01h to register 00h**)
2. Set MAX_CURRENT = 1h to set 51mA maximum output LED current (**Write 01h to register 01h**)
3. Set 51mA maximum current for red LEDs, 40.8mA maximum current for green, blue and white LEDs (**Write FFh to registers 14h, write CCh to registers 15h, 16h and 17h**)
4. Enable all 4 LEDs (**Write 0Fh to register 02h**)
5. Send **UPDATE_CMD** to make above step2 and step4 configurations take effect (**Write 55h to register 0Fh**)
6. Set red, green, blue and white LEDs PWM duty cycle as 100%, 80%, 40% and 20% (**Write FFh to register 18h, write CCh to register 19h, write 66h to register 1Ah, write 33h to register 1Bh**)

After this step, the red, green, blue and white LEDs are turned on with 100%, 80%, 40% and 20% PWM duty cycle.

8.2.4 Application Performance Plots

The following figures show the application performance plots.



OUT0 PWM 100% OUT1 PWM 80% OUT2 PWM 40% OUT3 PWM 20%

Figure 8-3. Current Sinks Waveforms of OUT0, OUT1, OUT2, OUT3

8.3 Power Supply Recommendations

The LP5816 is designed to operate from an input voltage supply range from 2.5V to 5.5V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance is required close to the ceramic bypass capacitors. A typical choice is a tantalum or aluminum electrolytic capacitor with a value of 100µF.

8.4 Layout

8.4.1 Layout Guidelines

The input capacitor needs not only to be close to the VCC pin, but also to the GND pin to reduce input supply ripple. For OUTx (x = 0, 1, 2, 3), low inductive and resistive path of switch load loop can help to provide a high slew rate. Therefore, path of adjecent outputs must be short and wide and avoid parallel wiring and narrow trace. For better thermal performance, TI suggest to make copper polygon connected with each pin bigger.

8.4.2 Layout Example

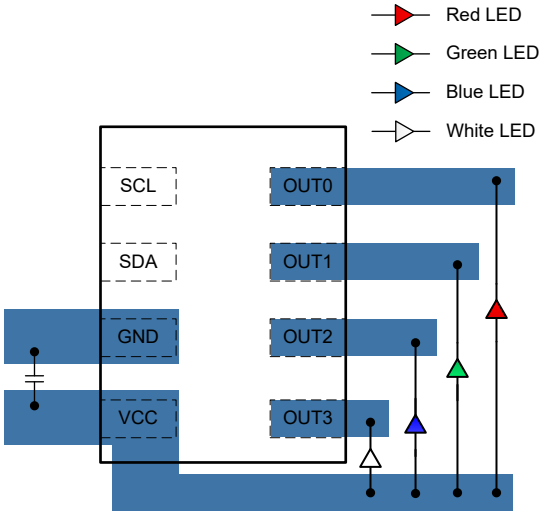


Figure 8-4. LP5816 DRL Package Layout Example

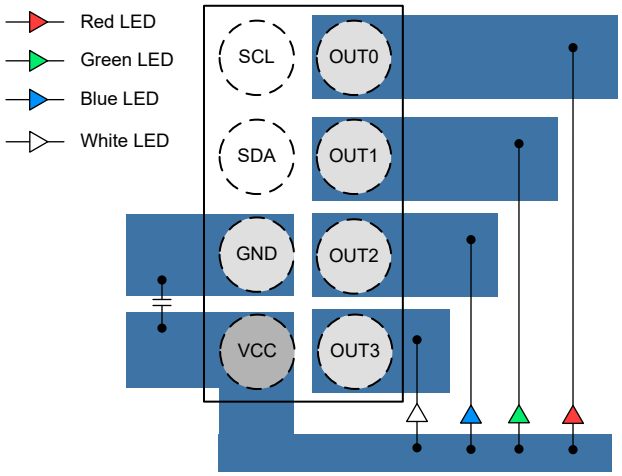


Figure 8-5. LP5816 YCH Package Layout Example

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

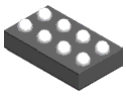
10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2025) to Revision A (April 2025)	Page
• Changed document status from "Advance Information" to "Production Data"	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

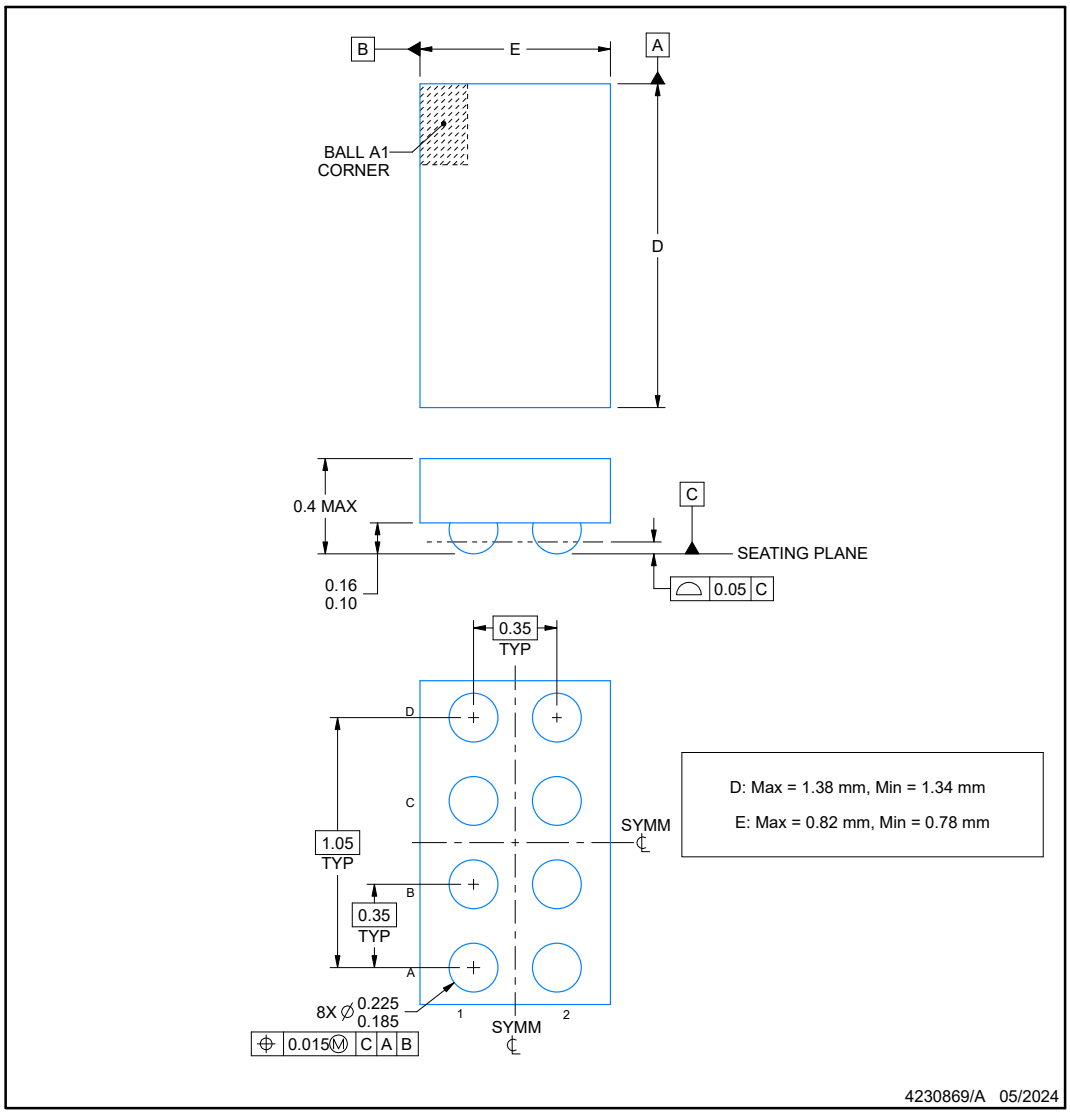


PACKAGE OUTLINE

YCH0008-C02

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

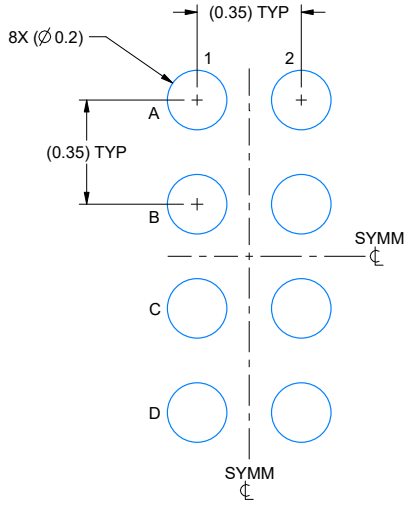
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

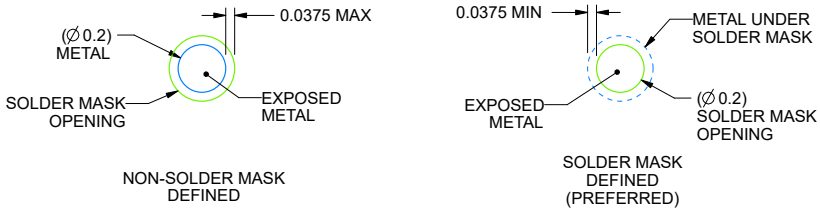
YCH0008-C02

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS
NOT TO SCALE

4230869/A 05/2024

NOTES: (continued)

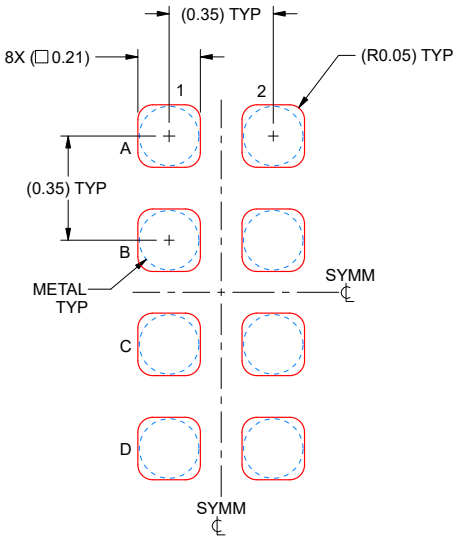
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YCH0008-C02

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

4230869/A 05/2024

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP5816DRLR	Active	Production	SOT-5X3 (DRL) | 8	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5816
LP5816DRLR.A	Active	Production	SOT-5X3 (DRL) | 8	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	5816
LP5816YCHR	Active	Production	DSBGA (YCH) | 8	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	H

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

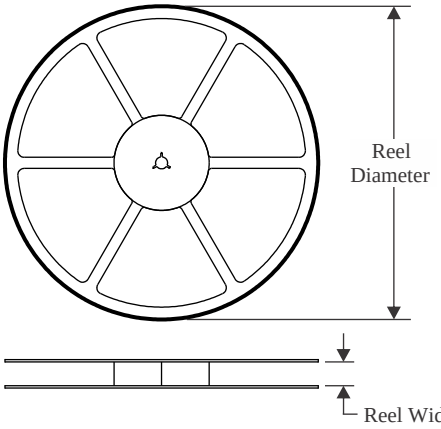
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

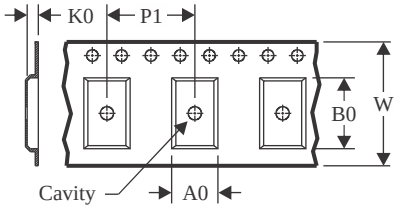
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

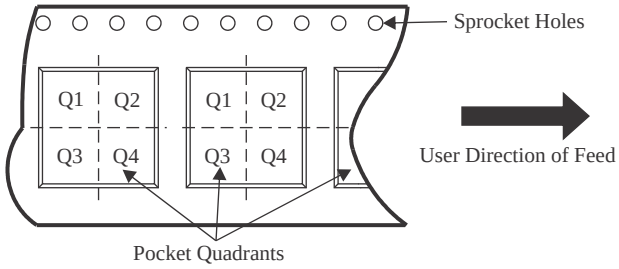


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

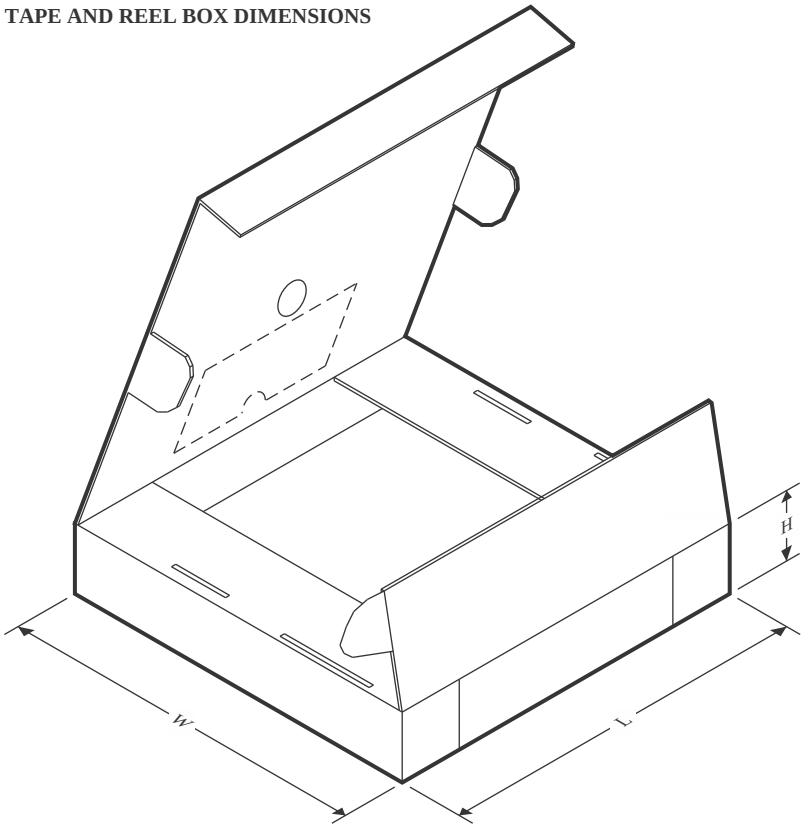
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5816DRLR	SOT-5X3	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3
LP5816YCHR	DSBGA	YCH	8	12000	180.0	8.4	0.92	1.48	0.43	2.0	8.0	Q1

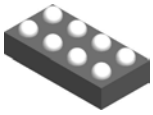
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5816DRLR	SOT-5X3	DRL	8	4000	210.0	185.0	35.0
LP5816YCHR	DSBGA	YCH	8	12000	182.0	182.0	20.0

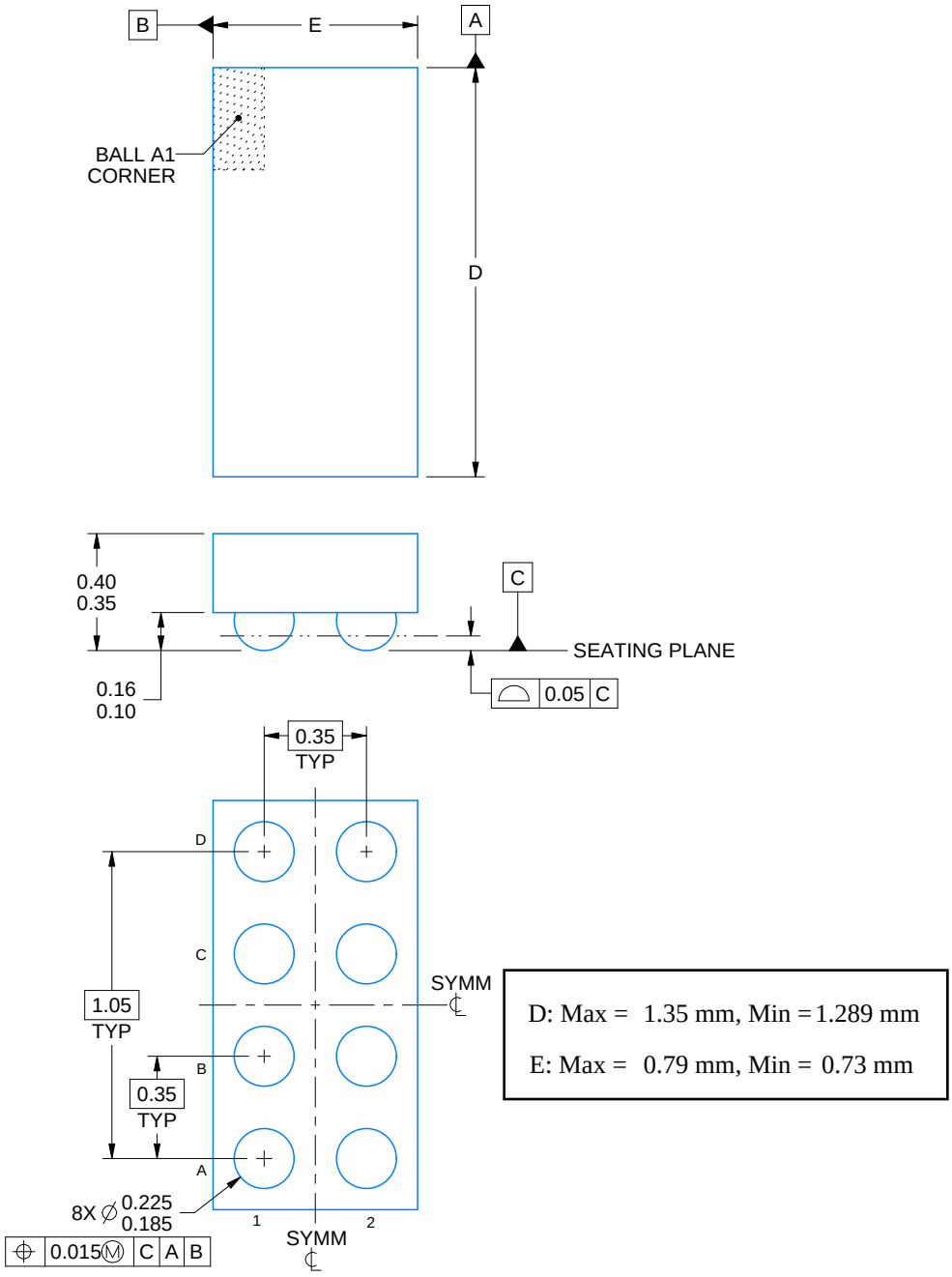
YCH0008



PACKAGE OUTLINE

DSBGA - 0.4 mm max height

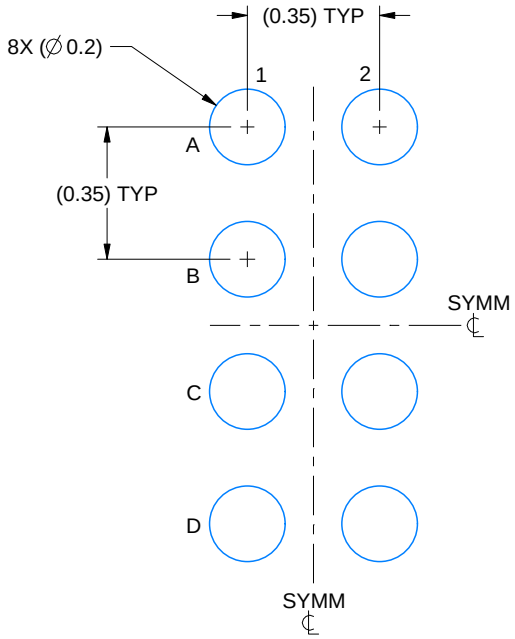
DIE SIZE BALL GRID ARRAY



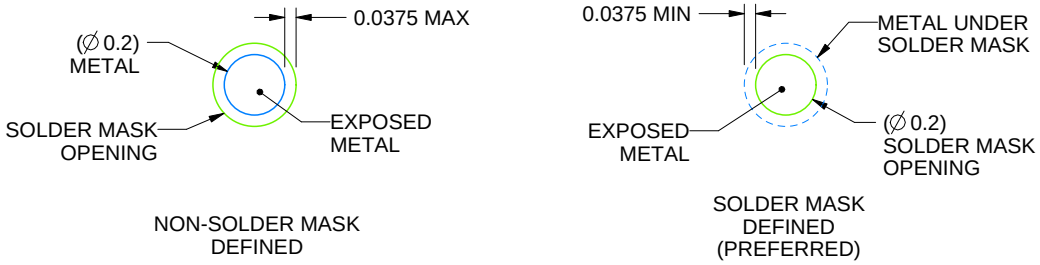
4225328/B 06/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X

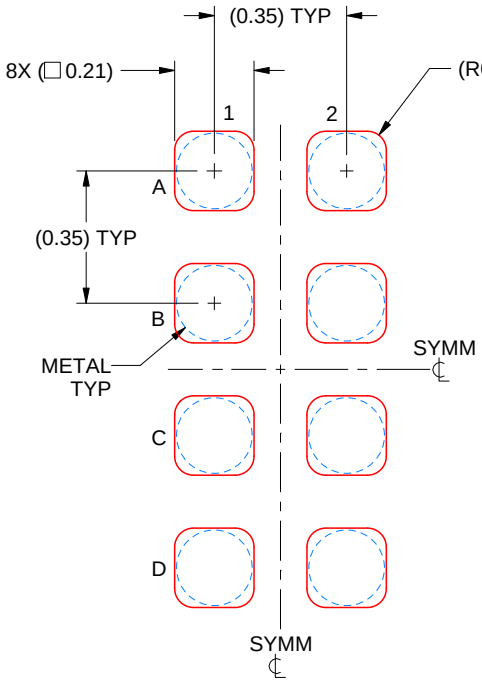


SOLDER MASK DETAILS
NOT TO SCALE

4225328/B 06/2023

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

4225328/B 06/2023

NOTES: (continued)

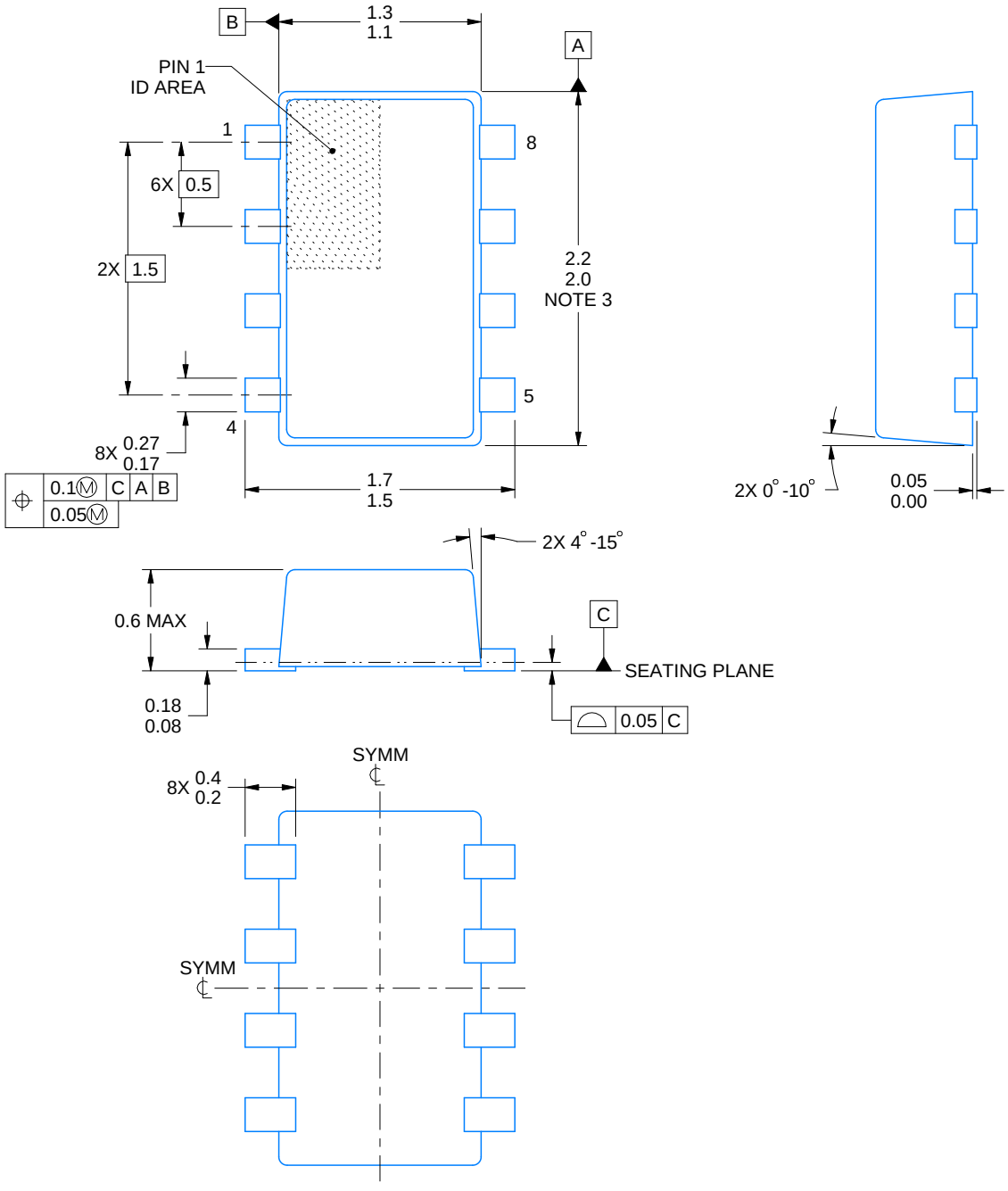
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



4224486/G 11/2024

NOTES:

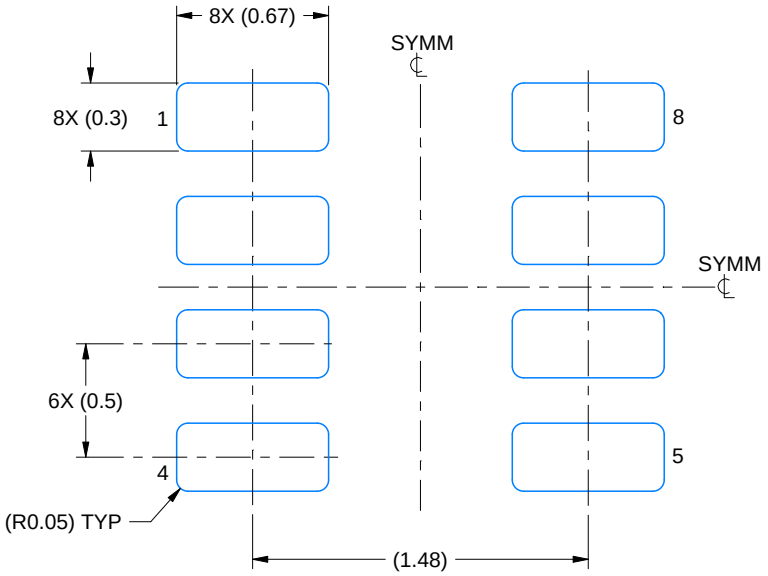
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC Registration MO-293, Variation UDAD

EXAMPLE BOARD LAYOUT

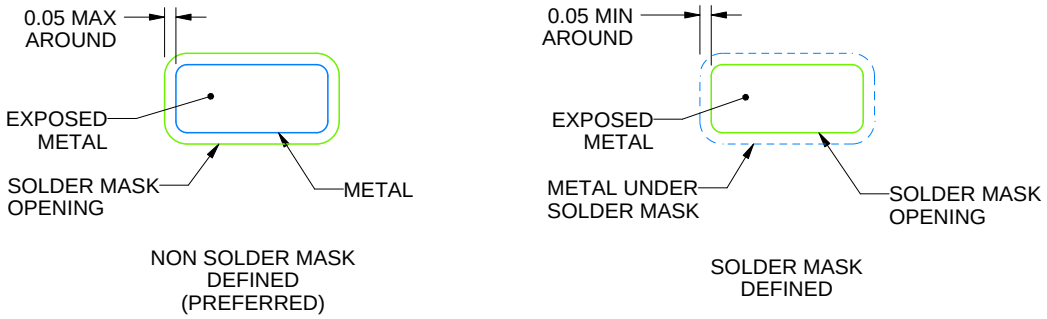
DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDERMASK DETAILS

4224486/G 11/2024

NOTES: (continued)

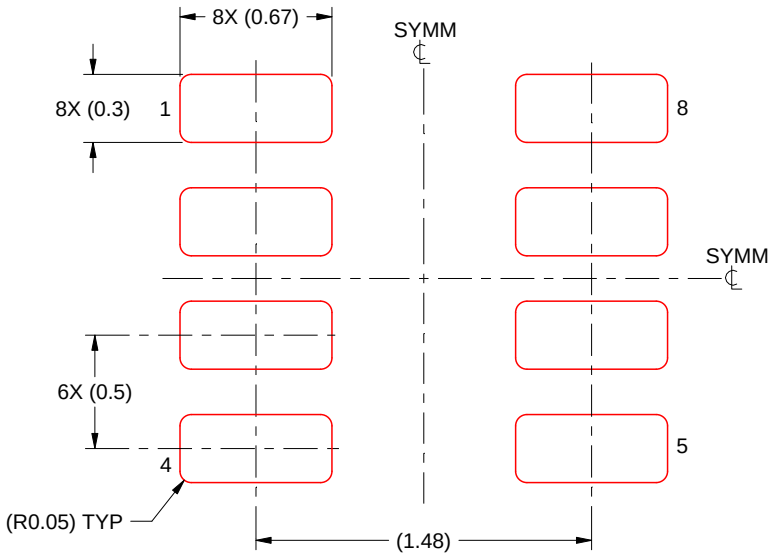
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4224486/G 11/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025