NE5532x, SA5532x Dual Low-Noise Operational Amplifiers

1 Features

- Equivalent Input Noise Voltage: 5nV/√Hz Typ at 1kHz
- Unity-Gain Bandwidth: 12MHz Typ
- Common-Mode Rejection Ratio: 100dB Typ
- High DC Voltage Gain: 100V/mV Typ
- High Slew Rate: 5V/μs Typ

2 Applications

- AV Receivers
- Embedded PCs
- Net books
- Video Broadcasting and Infrastructure: Scalable Platforms
- DVD Recorders and Players
- Multichannel Video Trans coders
- Pro Audio Mixers

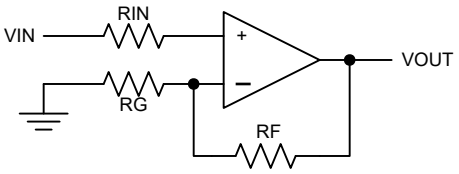
3 Description

The NE5532, NE5532A, SA5532, and SA5532A devices are high-performance operational amplifiers combining excellent dc and ac characteristics. These devices feature very low noise, high output-drive capability, high unity-gain and maximum-output-swing bandwidths, low distortion, high slew rate, input-protection diodes, and output short-circuit protection. These operational amplifiers are compensated internally for unity-gain operation. These devices have specified maximum limits for equivalent input noise voltage.

Device Information

PART NUMBER(1)	PACKAGE (PIN)	PACKAGE SIZE (NOM)(2)
NE5532x, SA5532x	SOIC (8)	4.90mm × 3.91mm
NE5532x, SA5532x	PDIP (8)	9.81mm × 6.35mm
NE5532x	SO (8)	6.20mm × 5.30mm

(1) For more information, see Section 10.
(2) The package size (length x width) is a nominal value and includes pins, where applicable



Simplified Schematic

Table of Contents

4 Pin Configuration and Functions

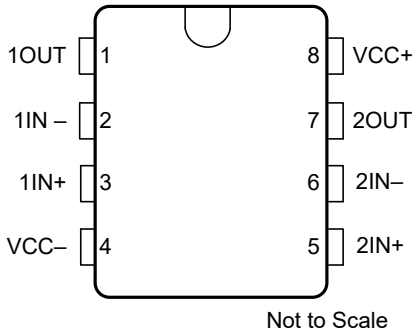


Figure 4-1. NE5532x, D Package, 8-Pin SOIC, P Package, 8-Pin PDIP, PS Package, 8-Pin SO SA5532x, D Package, 8-Pin SOIC, P Package, 8-Pin PDIP (Top View)

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN+	3	Input	Noninverting input
1IN–	2	Input	Inverting input
OUT1	1	Output	Output
2IN+	5	Input	Noninverting input
2IN–	6	Input	Inverting input
2OUT	7	Output	Output
VCC+	8	—	Positive supply
VCC–	4	—	Negative supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)	V_{CC+}	0	+18	V
		$V_{CC–}$	–18	0	V
	Input voltage, either input(2) (3)		–15	+15	V
	Input current(4)		–10	10	mA
	Duration of output short circuit(5)		Unlimited		
T_J	Operating virtual-junction temperature			+150	°C
T_{stg}	Storage temperature range		–60	+125	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Section 5.3 but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and $V_{CC–}$.
(3) The magnitude of the input voltage must never exceed the magnitude of the supply voltage.
(4) Excessive input current flows if a differential input voltage in exceeding approximately 0.6V is applied between the inputs, unless some limiting resistance is used.
(5) The output can be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to the maximum dissipation rating is not exceeded.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC+}	Supply voltage		5	15	V
$V_{CC–}$	Supply voltage		–5	–15	V
T_A	Operating free-air temperature	NE5532, NE5532A	0	70	°C
		SA5532, SA5532A	–40	+85	

5.4 Thermal Information

THERMAL METRIC(1)		NE5532, NE5532A, SA5532, and SA5532A			UNIT
		D	P	PS	
		8 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance (3) (2)	97	85	95	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics application report*.
(2) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A) / \theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

5.5 Electrical Characteristics

$V_{CC±}$ = ±15V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0	T_A = 25°C		0.5	4	mV
			T_A = Full range[2]			5	
I_{IO}	Input offset current	T_A = 25°C			10	150	nA
		T_A = Full range[2]				200	
I_{IB}	Input bias current	T_A = 25°C			200	800	nA
		T_A = Full range[2]				1000	
V_{ICR}	Common-mode input-voltage range			±12	±13		V
A_{VD}	Large-signal differential-voltage amplification	R_L ≥ 600Ω, V_O = ±10 V	T_A = 25°C	15	50		V/mV
			T_A = Full range[2]	10			
		R_L ≥ 2kΩ, V_O±10 V	T_A = 25°C	25	100		
			T_A = Full range[2]	15			
B_1	Unity-gain bandwidth				12		MHz
r_i	Input resistance			30	300		kΩ
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min		70	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC±}/\Delta V_{IO}$)	$V_{CC±}$ = ±9 V to ±15 V, V_O = 0		80	100		dB
I_{OS}	Output short-circuit current				38		mA
I_{CC}	Total supply current	V_O = 0, No load			6	16	mA

(1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified.
(2) Full temperature ranges are: –40°C to 85°C for the SA5532 and SA5532A devices, and 0°C to 70°C for the NE5532 and NE5532A devices.

5.6 Operating Characteristics

$V_{CC±}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	NE5532, SA5532			NE5532A, SA5532A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain			5			5		V/μs
V_n	Equivalent input noise voltage	f = 30Hz		8			8		nV/√Hz
		f = 1kHz		5			5		
I_n	Equivalent input noise current	f = 30Hz		2.7			2.7		pA/√Hz
		f = 1kHz		0.7			0.7		

5.7 Typical Characteristics

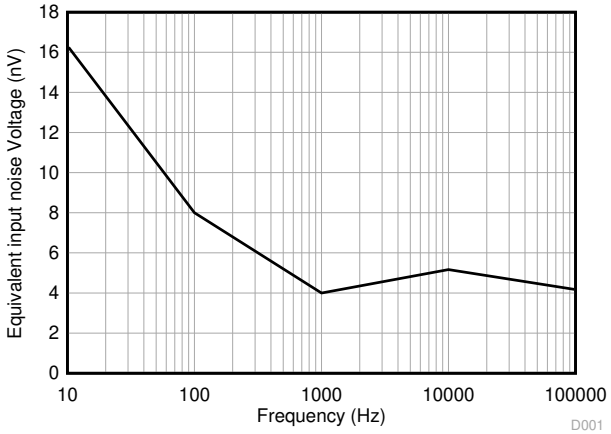


Figure 5-1. Equivalent Input Noise Voltage vs Frequency

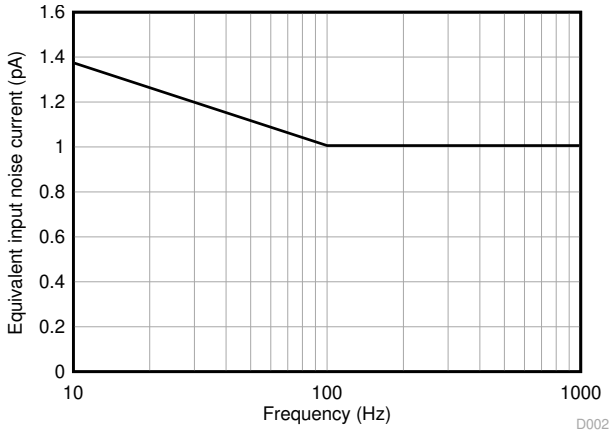


Figure 5-2. Equivalent Input Noise Current vs Frequency

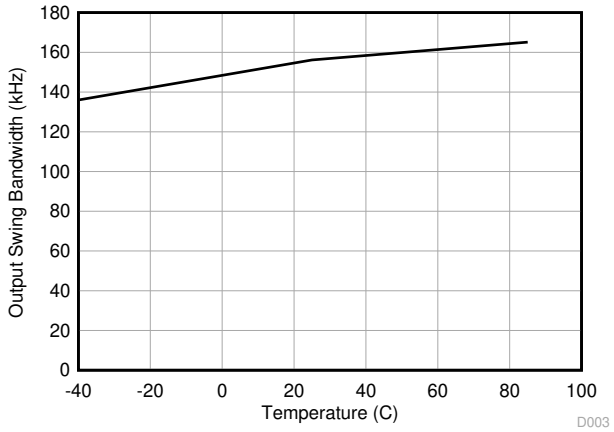


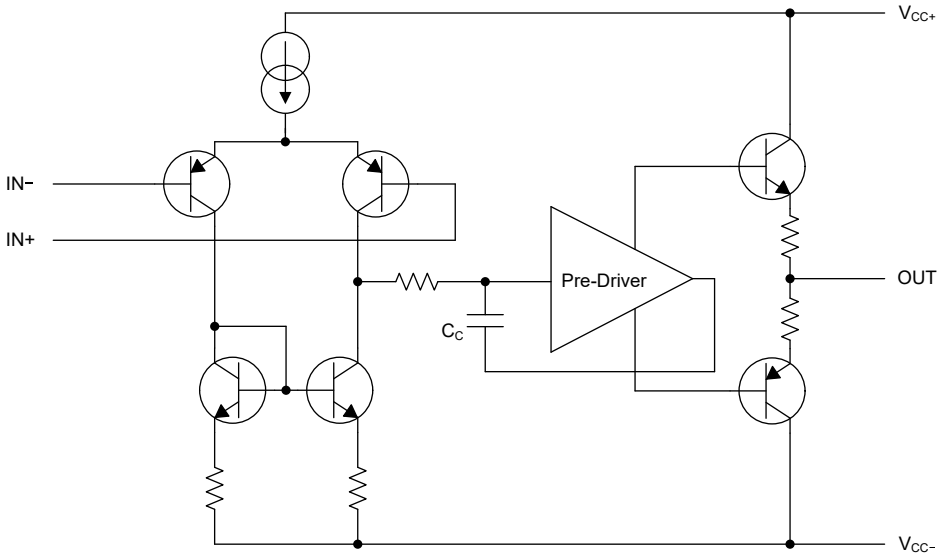
Figure 5-3. Output Swing Bandwidth vs Temperature at V_{CC} = ±10 V

6 Detailed Description

6.1 Overview

The NE5532, NE5532A, SA5532, and SA5532A devices are high-performance operational amplifiers combining excellent dc and ac characteristics. Devices feature very low noise, high output-drive capability, high unity-gain and maximum-output-swing bandwidths, low distortion, high slew rate, input-protection diodes, and output short-circuit protection. These operational amplifiers are compensated internally for unity-gain operation. These devices have specified maximum limits for equivalent input noise voltage.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain can be operated without greatly distorting the signal. The NE5532, NE5532A, SA5532, and SA5532A devices have a 10MHz unity-gain bandwidth.

6.3.2 Common-Mode Rejection Ratio

The common-mode rejection ratio (CMRR) of an amplifier is a measure of how well the device rejects unwanted input signals common to both input leads. CMRR is found by taking the ratio of the change in input offset voltage to the change in the input voltage and converting to decibels. The CMRR can be infinite, but in practice, amplifiers are designed to have ratio as high as possible. The CMRR of the NE5532, NE5532A, SA5532, and SA5532A devices is 100dB.

6.3.3 Slew Rate

The slew rate is the rate at which an operational amplifier can change output when there is a change on the input. The NE5532, NE5532A, SA5532, and SA5532A devices have a 9V/ms slew rate.

6.4 Device Functional Modes

The NE5532, NE5532A, SA5532, and SA5532A devices are powered on when the supply is connected. Each of these devices can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Typical Application

Some applications require differential signals. Figure 7-1 shows a simple circuit to convert a single-ended input of 2V to 10V into differential output of ±8V on a single 15V supply. The output range is intentionally limited to maximize linearity. The circuit is composed of two amplifiers. One amplifier acts as a buffer and creates a voltage, V_{OUT+}. The second amplifier inverts the input and adds a reference voltage to generate $V_{OUT–}$. Both V_{OUT+} and $V_{OUT–}$ range from 2V to 10V. The difference, V_{DIFF}, is the difference between V_{OUT+} and $V_{OUT–}$.

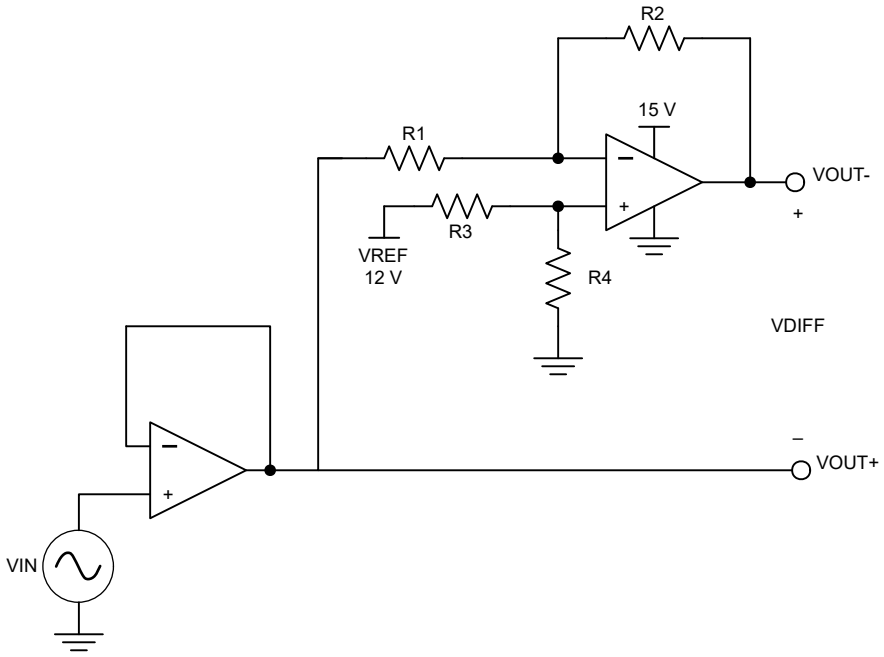


Figure 7-1. Schematic for Single-Ended Input to Differential Output Conversion

7.1.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 15V
- Reference voltage: 12V
- Input: 2V to 10V
- Output differential: ±8V

7.1.2 Detailed Design Procedure

The circuit in Figure 7-1 takes a single-ended input signal, V_{IN}, and generates two output signals, V_{OUT+} and V_{OUT-} using two amplifiers and a reference voltage, V_{REF}. V_{OUT+} is the output of the first amplifier and is a buffered version of the input signal, V_{IN} Equation 1. V_{OUT-} is the output of the second amplifier which uses V_{REF} to add an offset voltage to V_{IN} and feedback to add inverting gain. The transfer function for V_{OUT-} is Equation 2.

$$V_{OUT+} = V_{IN} \tag{1}$$

$$V_{out-} = V_{ref} \times \left(\frac{R_4}{R_{3+} R_4} \right) \times \left(1 + \frac{R_2}{R_1} \right) - V_{in} \times \frac{R_2}{R_1} \tag{2}$$

The differential output signal, V_{DIFF}, is the difference between the two single-ended output signals, V_{OUT+} and V_{OUT-}. Equation 3 shows the transfer function for V_{DIFF}. By applying the conditions that $R_1 = R_2$ and $R_3 = R_4$, the transfer function is simplified into Equation 6. Using this configuration, the maximum input signal is equal to the reference voltage and the maximum output of each amplifier is equal to the V_{REF}. The differential output range is $2 \times V_{REF}$. Furthermore, the common mode voltage is one half of V_{REF} (see Equation 7).

$$V_{DIFF} = V_{OUT+} - V_{OUT-} = V_{IN} \times \left(1 + \frac{R_2}{R_1} \right) - V_{REF} \times \left(\frac{R_4}{R_3 + R_4} \right) \left(1 + \frac{R_2}{R_1} \right) \tag{3}$$

$$V_{OUT+} = V_{IN} \tag{4}$$

$$V_{OUT-} = V_{REF} - V_{IN} \tag{5}$$

$$V_{DIFF} = 2 \times V_{IN} - V_{REF} \tag{6}$$

$$V_{cm} = \left(\frac{V_{OUT+} + V_{OUT-}}{2} \right) = \frac{1}{2} V_{REF} \tag{7}$$

7.1.2.1 Amplifier Selection

Linearity over the input range is key for good dc accuracy. The common mode input range and the output swing limitations determine the linearity. In general, an amplifier with rail-to-rail input and output swing is required. Bandwidth is a key concern for this design. Since the NE5532 has a bandwidth of 10MHz, this circuit can only be able to process signals with frequencies of less than 10MHz.

7.1.2.2 Passive Component Selection

Because the transfer function of V_{OUT-} is heavily reliant on resistors (R_1, R_2, R_3, and R_4), use resistors with low tolerances to maximize performance and minimize error. This design used resistors with resistance values of 36kΩ with tolerances measured to be within 2%. But, if the noise of the system is a key parameter, the user can select smaller resistance values (6kΩ or lower) to keep the overall system noise low. This maintains that the noise from the resistors is lower than the amplifier noise.

7.1.3 Application Curves

The measured transfer functions in Figure 7-2, Figure 7-3, and Figure 7-4 are generated by sweeping the input voltage from 0V to 12V. However, this design only uses between 2V and 10V for optimum linearity.

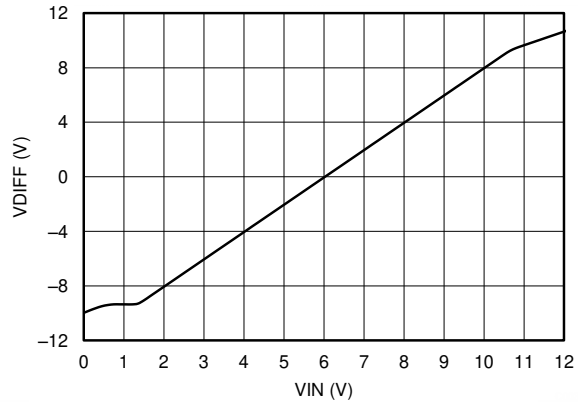


Figure 7-2. Differential Output Voltage vs Input Voltage

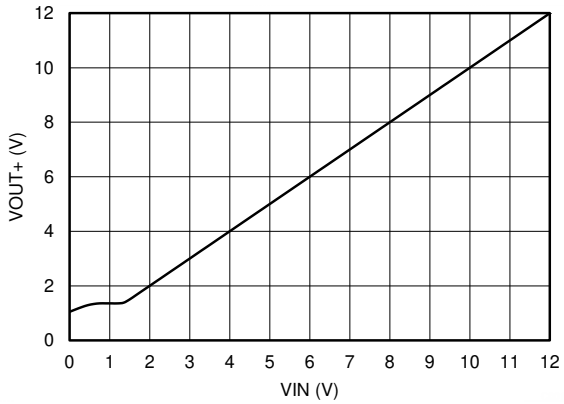


Figure 7-3. Positive Output Voltage Node vs Input Voltage

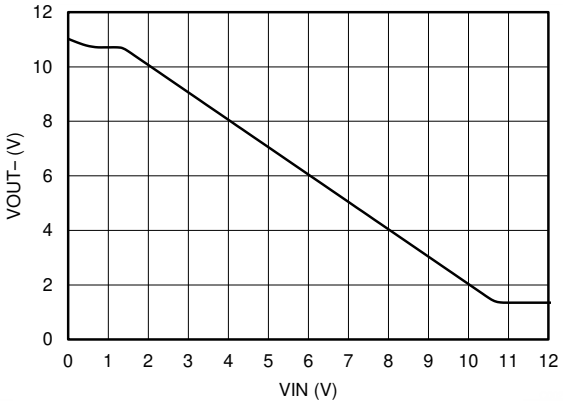


Figure 7-4. Positive Output Voltage Node vs Input Voltage

7.2 Power Supply Recommendations

The NE5532x and SA5532x devices are specified for operation over the range of ±5 to ±15 V; many specifications apply from 0°C to 70°C (NE5532x) and –40°C to +85°C (SA5532x). Section 5.7 presents parameters that exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages outside of the ±22 V range are able to permanently damage the device (see Section 5.1).

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see Section 7.3.1.

7.3 Layout

7.3.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.

  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCB are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to Circuit Board Layout Techniques, SLOA089.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If not possible to keep them separate, better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Section 7.3.2* .
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

7.3.2 Layout Example

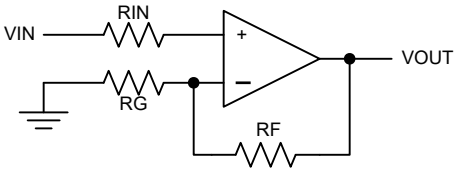


Figure 7-5. Operational Amplifier Schematic for Noninverting Configuration

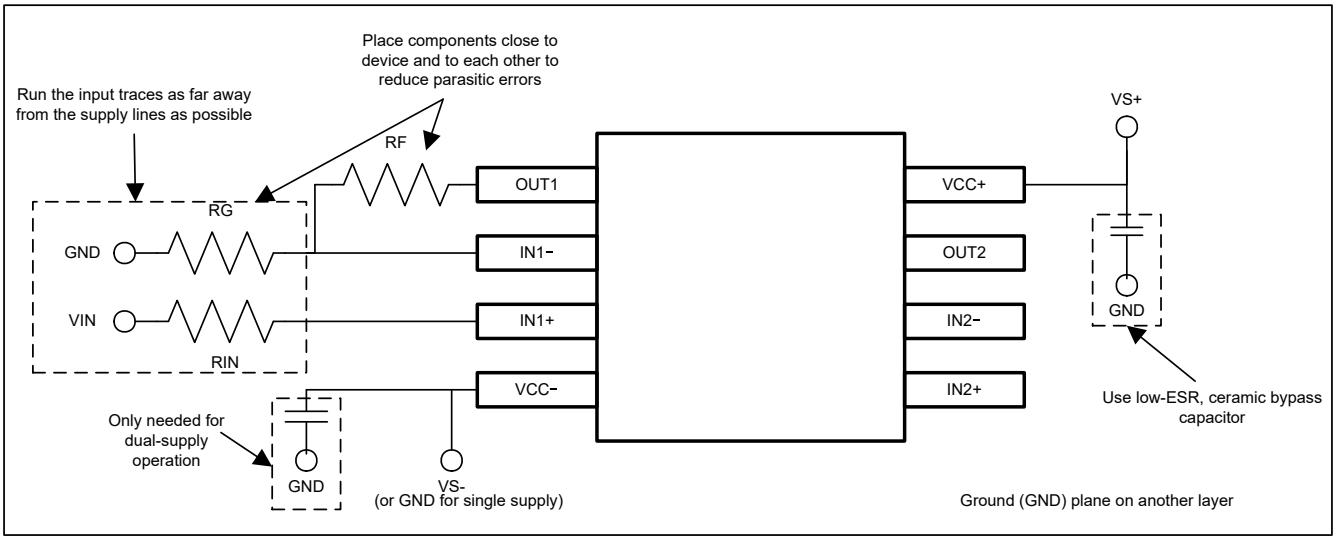


Figure 7-6. Operational Amplifier Board Layout for Noninverting Configuration

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

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8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

Changes from Revision J (January 2015) to Revision K (December 2025)	Page
• Changed Unity-gain bandwidth from 10MHz to 12MHz typ	1
• Changed High slew rate from 9V/µs to 5V/µs typ	1
• Removed peak to peak voltage swing	1
• Changed Supply voltage positive and negative from 22V to 18V	3
• Changed Input voltage positive and negative from –10V and +10V to –15V and +15V	3
• Changed Storage temperature range from –35°C and +150°C to –60°C and +125°C	3
• Changed HBM value from 2000V to 1000V	3
• Changed Unity gain bandwidth from 10MHz to 12MHz	4
• Removed Maximum peak-to-peak output voltage swing, Small-signal differential-voltage amplification, Maximum output-swing bandwidth, Output impedance, Crosstalk attenuation	4
• Changed Supply current value from 8mA to 6mA	4
• Removed Overshoot factor	4
• Changed Slew rate value from 9V/µs to 5V/µs	4

Changes from Revision I (April 2009) to Revision J (January 2015)	Page
• Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted *Ordering Information* table	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
NE5532ADR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532A
NE5532ADR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532A
NE5532ADR1G4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532A
NE5532ADR1G4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532A
NE5532AP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	NE5532AP
NE5532AP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	NE5532AP
NE5532APSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532A
NE5532APSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532A
NE5532APSRE4	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532A
NE5532D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	N5532
NE5532DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532
NE5532DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532
NE5532DRE4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532
NE5532DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532
NE5532DRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532
NE5532P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	NE5532P
NE5532P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	NE5532P
NE5532PE4	Active	Production	PDIP (P) | 8	50 | TUBE	-	Call TI	Call TI	0 to 70	
NE5532PSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532
NE5532PSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532
SA5532AD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	SA5532A
SA5532ADR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA5532A
SA5532ADR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA5532A
SA5532ADRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA5532A
SA5532ADRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA5532A
SA5532AP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SA5532AP
SA5532AP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SA5532AP
SA5532APE4	Active	Production	PDIP (P) | 8	50 | TUBE	-	Call TI	Call TI	-40 to 85	
SA5532D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	SA5532

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SA5532DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA5532
SA5532DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA5532
SA5532P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SA5532P
SA5532P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SA5532P

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

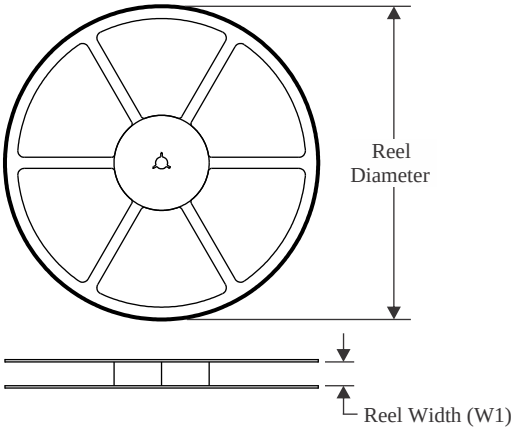
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

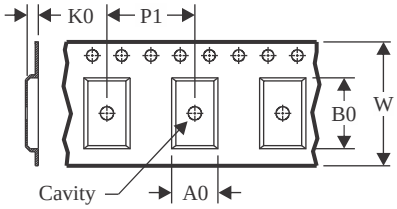
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

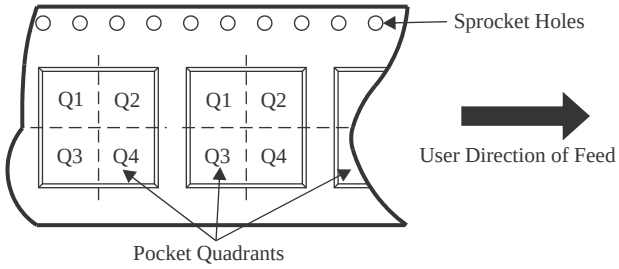


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

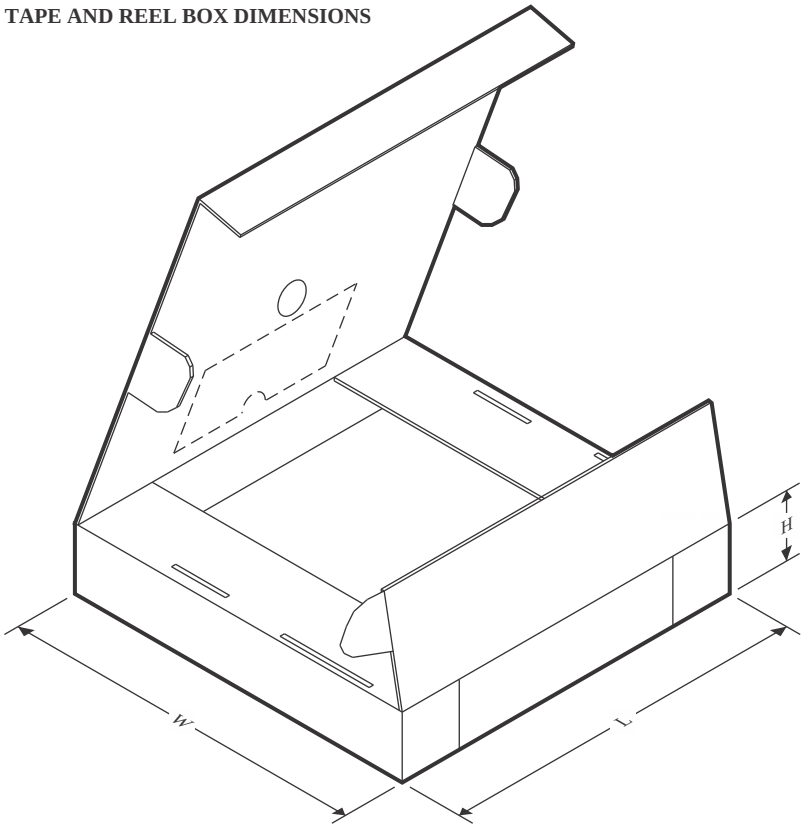
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
NE5532ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NE5532ADR1G4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NE5532APSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
NE5532DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NE5532DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NE5532PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SA5532ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SA5532ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SA5532DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

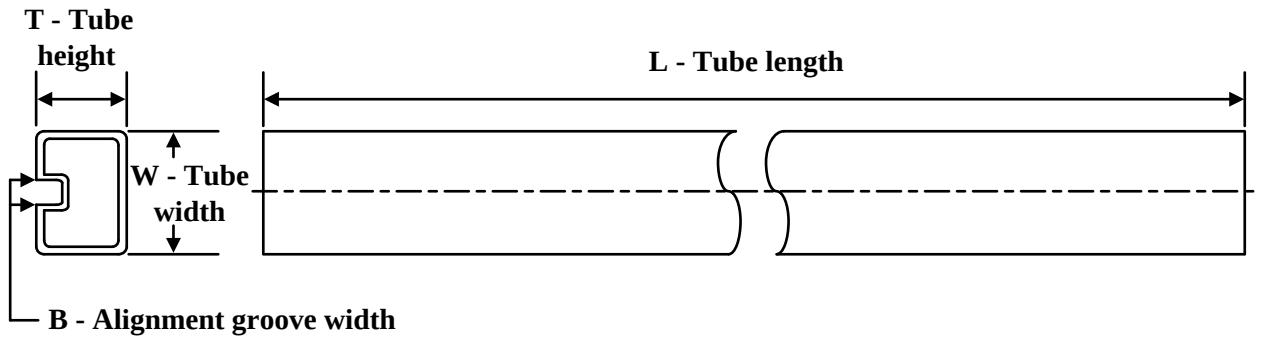
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

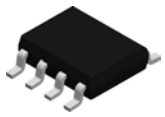
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
NE5532ADR	SOIC	D	8	2500	353.0	353.0	32.0
NE5532ADR1G4	SOIC	D	8	2500	353.0	353.0	32.0
NE5532APSR	SO	PS	8	2000	353.0	353.0	32.0
NE5532DR	SOIC	D	8	2500	353.0	353.0	32.0
NE5532DRG4	SOIC	D	8	2500	340.5	338.1	20.6
NE5532PSR	SO	PS	8	2000	353.0	353.0	32.0
SA5532ADR	SOIC	D	8	2500	353.0	353.0	32.0
SA5532ADRG4	SOIC	D	8	2500	353.0	353.0	32.0
SA5532DR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
NE5532AP	P	PDIP	8	50	506	13.97	11230	4.32
NE5532AP.A	P	PDIP	8	50	506	13.97	11230	4.32
NE5532P	P	PDIP	8	50	506	13.97	11230	4.32
NE5532P.A	P	PDIP	8	50	506	13.97	11230	4.32
SA5532AP	P	PDIP	8	50	506	13.97	11230	4.32
SA5532AP.A	P	PDIP	8	50	506	13.97	11230	4.32
SA5532P	P	PDIP	8	50	506	13.97	11230	4.32
SA5532P.A	P	PDIP	8	50	506	13.97	11230	4.32

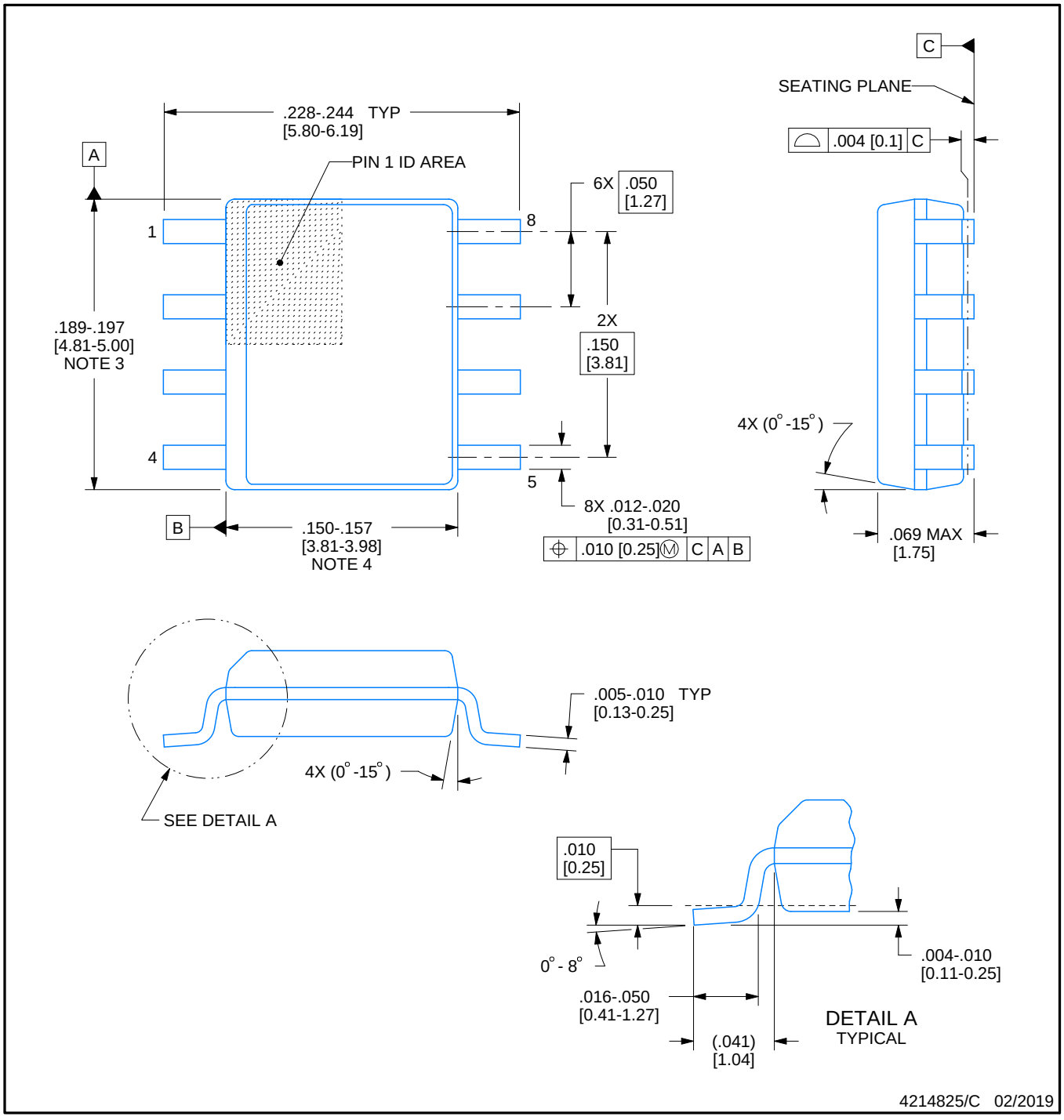


PACKAGE OUTLINE

D0008A

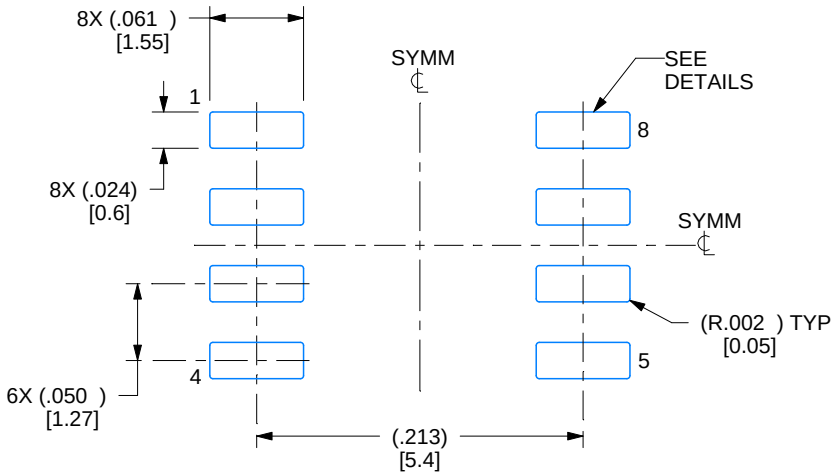
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

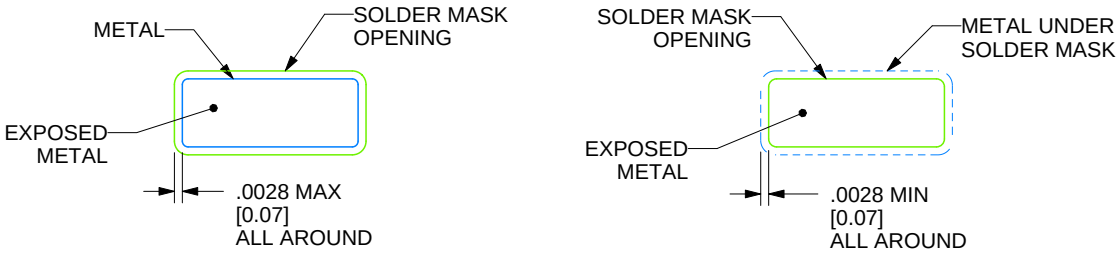


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

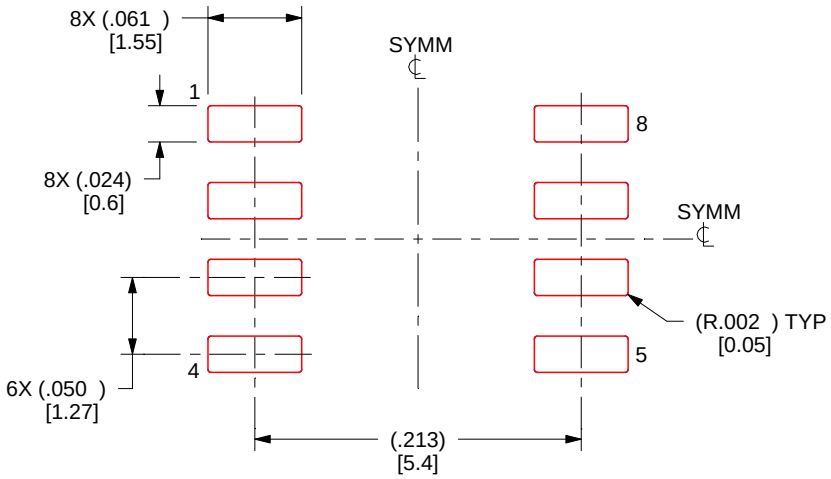
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

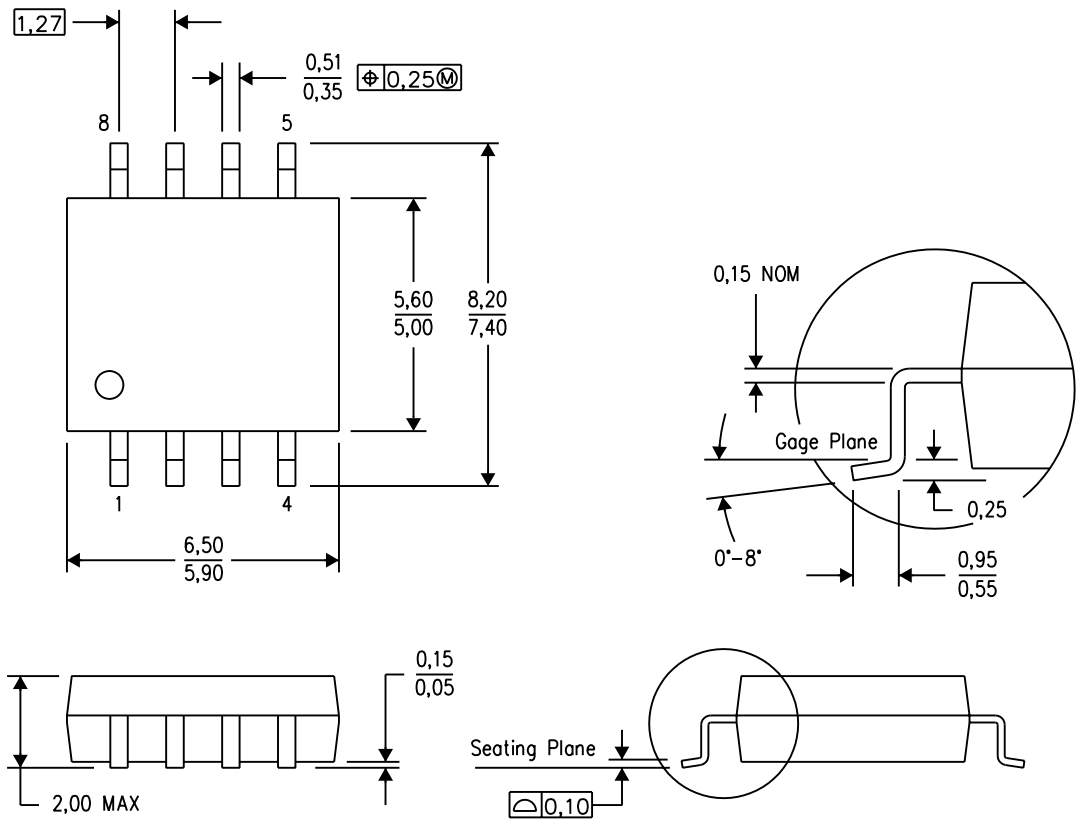
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

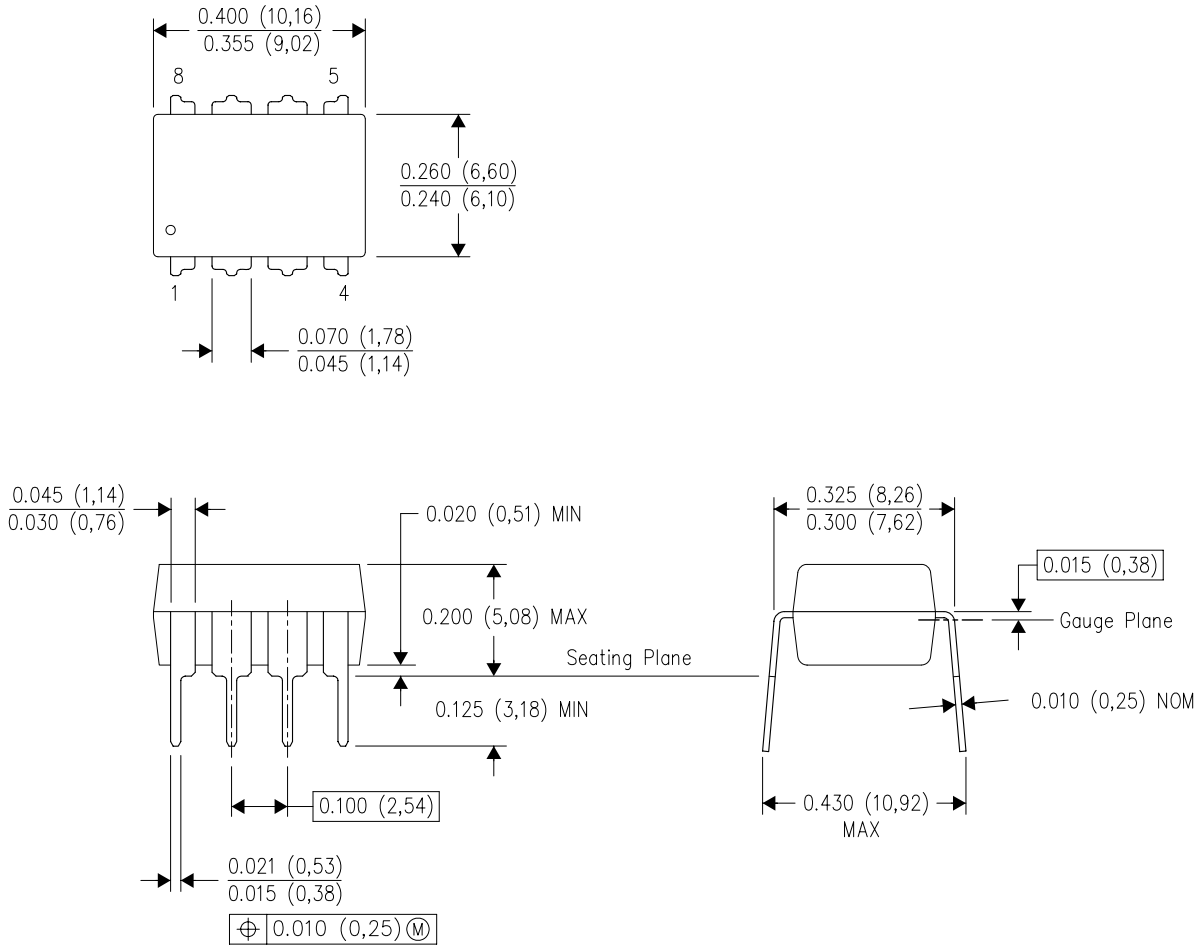
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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