

DS8830, SN55183, SN75183 DUAL DIFFERENTIAL LINE DRIVERS

SLLS093D – OCTOBER 1972 – REVISED APRIL 1998

- Single 5-V Supply
- Differential Line Operation
- Dual Channels
- TTL Compatibility
- Short-Circuit Protection of Outputs
- Output Clamp Diodes to Terminate Line Transients
- High-Current Outputs
- Quad Inputs
- Single-Ended or Differential AND/NAND Outputs
- Designed for Use With Dual Differential Drivers SN55182 and SN75182
- Designed to Be Interchangeable With National Semiconductor DS7830 and DS8830

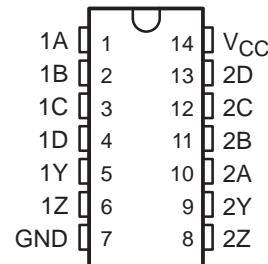
description

The DS8830, SN55183, and SN75183 dual differential line drivers are designed to provide differential output signals with high current capability for driving balanced lines, such as twisted pair, at normal line impedances without high power dissipation. These devices can be used as TTL expander/phase splitters, because the output stages are similar to TTL totem-pole outputs.

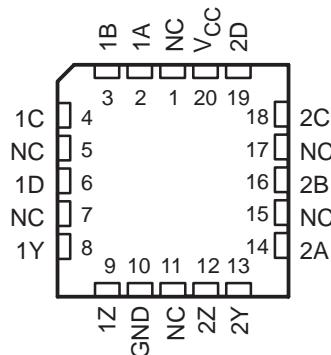
The driver is of monolithic single-chip construction, and both halves of the dual circuits use common power supply and ground terminals.

The SN55183 is characterized for operation over the full military temperature range of -55°C to 125°C . The DS8830 and SN75183 are characterized for operation from 0°C to 70°C .

SN55183 . . . J OR W PACKAGE
SN75183 . . . D OR N PACKAGE
DS8830 . . . N PACKAGE
(TOP VIEW)



SN55183 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

THE DS8830 AND SN55183 ARE NOT RECOMMENDED FOR NEW DESIGNS



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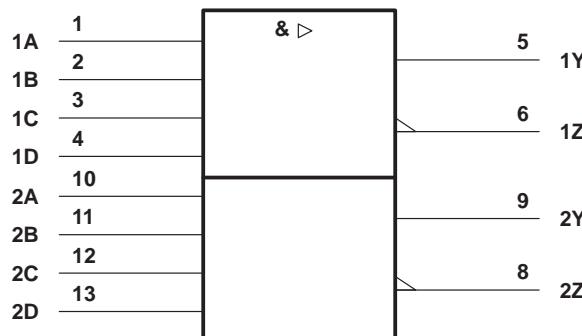
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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DS8830, SN55183, SN75183 DUAL DIFFERENTIAL LINE DRIVERS

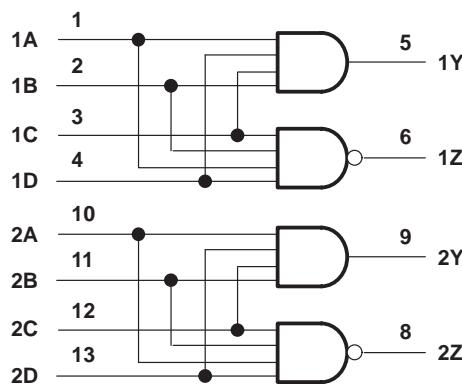
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

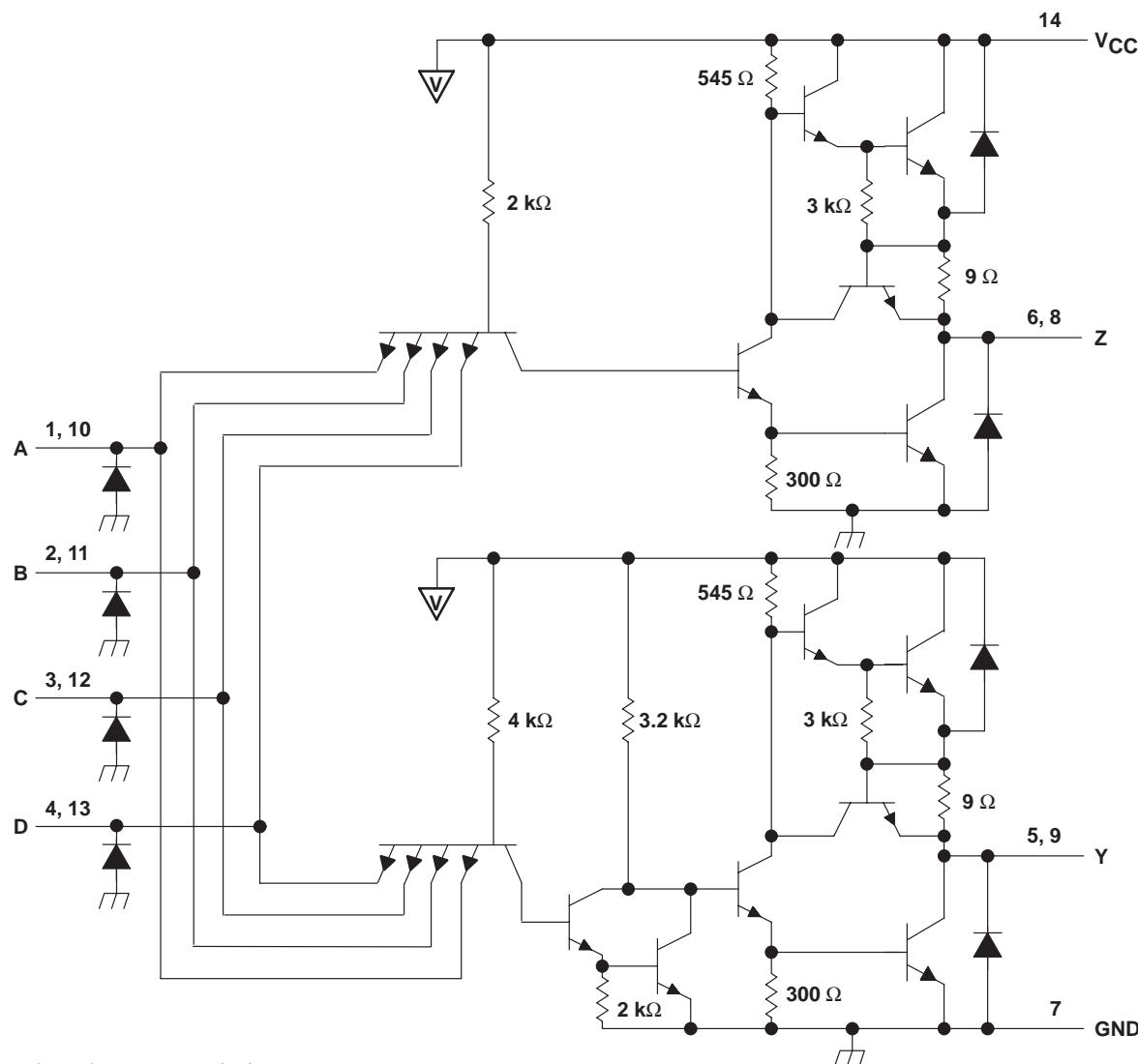
logic diagram (positive logic)



Positive logic: $y = ABCD$, $Z = \overline{ABCD}$

Pin numbers shown are for the D, J, N, and W packages.

schematic (each driver)



Resistor values shown are nominal.

Pin numbers shown are for the D, J, N, and W packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I	5.5 V
Duration of output short circuit (see Note 2)	1 s
Continuous total power dissipation	See Dissipation Rating Table
Storage temperature range, T_{STG}	–65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds: D or N package	260°C
Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds: J package	300°C
Case temperature for 60 seconds, T_C : FK package	260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Not more than one output should be shorted to ground at any one time.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ C$	$T_A = 70^\circ C$	$T_A = 125^\circ C$
			POWER RATING	POWER RATING
D	950 mW	7.6 mW/°C	608 mW	–
FK [‡]	1375 mW	11.0 mW/°C	880 mW	275 mW
J [‡]	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	–
W [‡]	1000 mW	8.0 mW/°C	640 mW	200 mW

[‡] In the FK, J, and W packages, SN55183 chips are alloy mounted and SN75183 chips are glass mounted.

recommended operating conditions

	SN55183	DS8830, SN75183			UNIT
		MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5 5.25
High-level input voltage, V_{IH}	2			2	V
Low-level input voltage, V_{IL}			0.8		V
High-level output current, I_{OH}			–40		mA
Low-level output current, I_{OL}			40		mA
Operating free-air temperature, T_A	–55		125	0	70 °C

electrical characteristics over recommended ranges of V_{CC} and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage Y (AND) outputs	$V_{IH} = 2\text{ V}$	$I_{OH} = -0.8\text{ mA}$	2.4		3.3	V
			$I_{OH} = -40\text{ mA}$	1.8			
V_{OL}	Low-level output voltage Y (AND) outputs	$V_{IL} = 0.8\text{ V}$	$I_{OL} = 32\text{ mA}$	0.2		0.4	V
			$I_{OL} = 40\text{ mA}$	0.22			
V_{OH}	High-level output voltage Z (NAND) outputs	$V_{IL} = 0.8\text{ V}$	$I_{OH} = -0.8\text{ mA}$	2.4		3.3	V
			$I_{OH} = -40\text{ mA}$	1.8			
V_{OL}	Low-level output voltage Z (NAND) outputs	$V_{IH} = 2\text{ V}$	$I_{OL} = 32\text{ mA}$	0.2		0.4	V
			$I_{OL} = 40\text{ mA}$	0.22			
I_{IH}	High-level input current	$V_{IH} = 2.4\text{ V}$		120		μA	
I_I	Input current at maximum input voltage	$V_{IH} = 5.5\text{ V}$		2		mA	
I_{IL}	Low-level input current	$V_{IL} = 0.4\text{ V}$		-4.8		mA	
I_{OS}	Short-circuit output current‡	$V_{CC} = 5\text{ V}, T_A = 125^\circ\text{C} \S$		-40	-100	-120	mA
I_{CC}	Supply current (average per driver)	$V_{CC} = 5\text{ V}, \text{ All inputs at } 5\text{ V}, \text{ No load}$		10		18	mA

† All typical values are at $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$.

‡ Not more than one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

§ $T_A = 125^\circ\text{C}$ is applicable to SN55183 only.

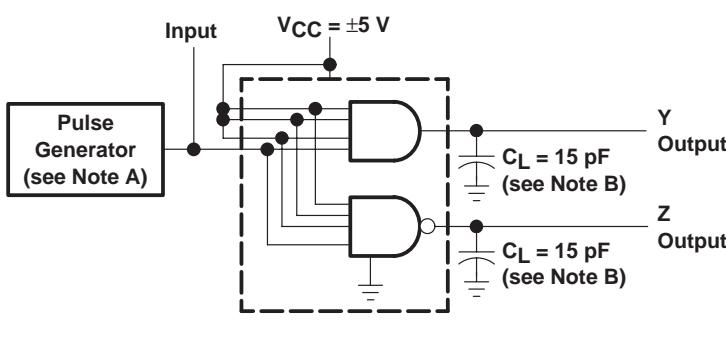
switching characteristics, $V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level Y output	AND gates	$C_L = 15\text{ pF}, \text{ See Figure 1(a)}$	8		12	ns
t_{PHL}	Propagation delay time, high- to low-level Y output	AND gates	$C_L = 15\text{ pF}, \text{ See Figure 1(a)}$	12		18	ns
t_{PLH}	Propagation delay time, low- to high-level Z output	NAND gates	$C_L = 15\text{ pF}, \text{ See Figure 1(a)}$	6		12	ns
t_{PHL}	Propagation delay time, high- to low-level Z output	NAND gates	$C_L = 15\text{ pF}, \text{ See Figure 1(a)}$	6		8	ns
t_{PLH}	Propagation delay time, low- to high-level differential output	Y output with respect to Z output, $R_L = 100\text{ \Omega}$ in series with 5000 pF, See Figure 1(b)		9		16	ns
t_{PHL}	Propagation delay time, high- to low-level differential output	Y output with respect to Z output, $R_L = 100\text{ \Omega}$ in series with 5000 pF, See Figure 1(b)		8		16	ns

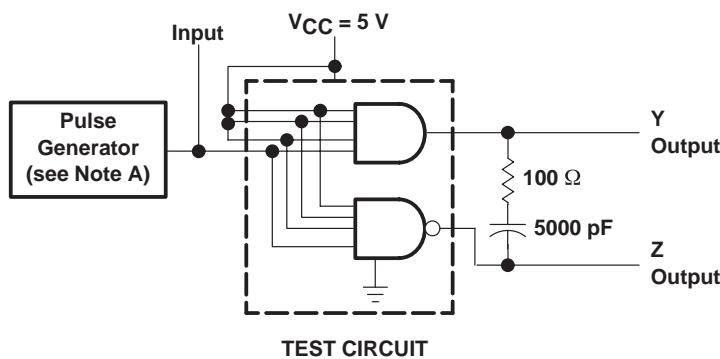
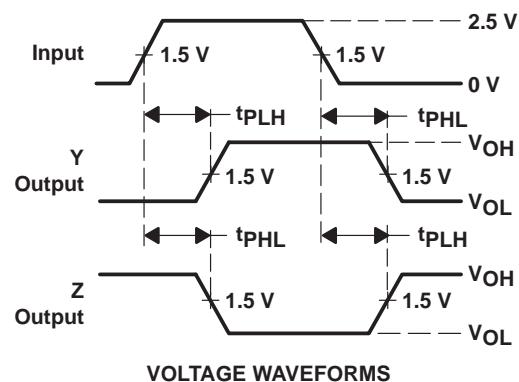
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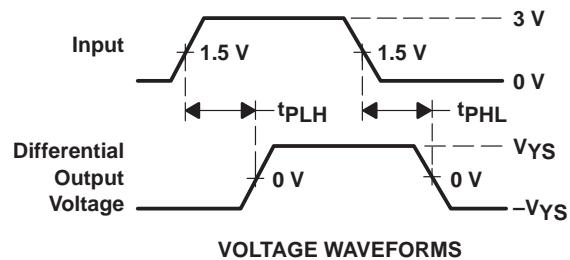
PARAMETER MEASUREMENT INFORMATION



(a) OUTPUTS Y AND Z



(b) DIFFERENTIAL OUTPUT



NOTES: A. The pulse generators have the following characteristics: $Z_O = 50 \Omega$, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$, $t_w = 0.5 \mu\text{s}$, $\text{PRR} \leq 1 \text{ MHz}$.
 B. C_L includes probe and jig capacitance.
 C. Waveforms are monitored on an oscilloscope with $r_i \geq 1 \text{ M}\Omega$.

Figure 1. Test Circuits and Voltage Waveforms

TYPICAL CHARACTERISTICS[†]

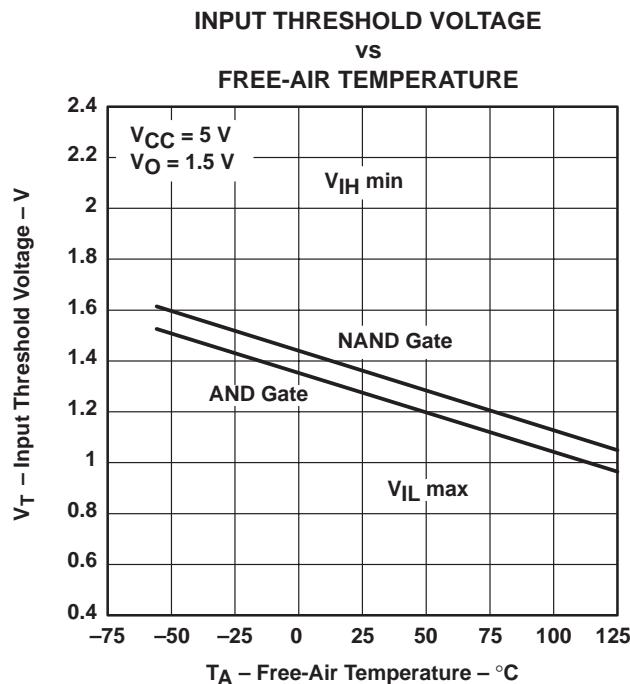


Figure 2

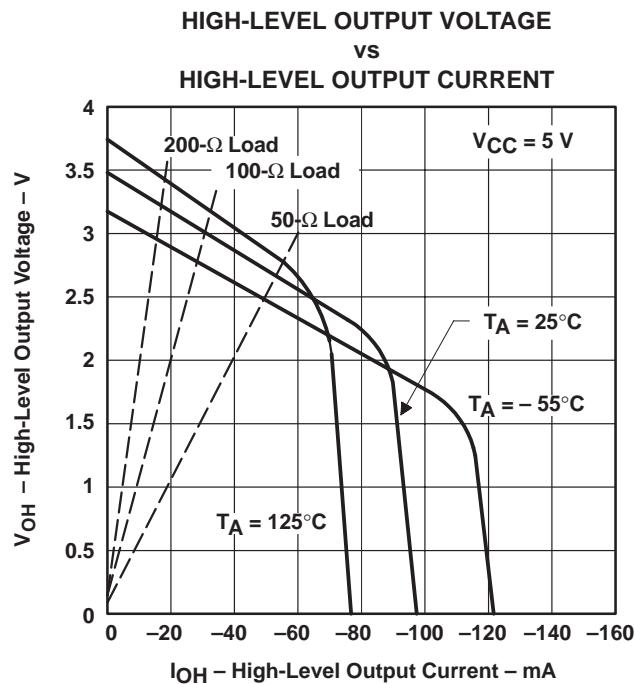


Figure 3

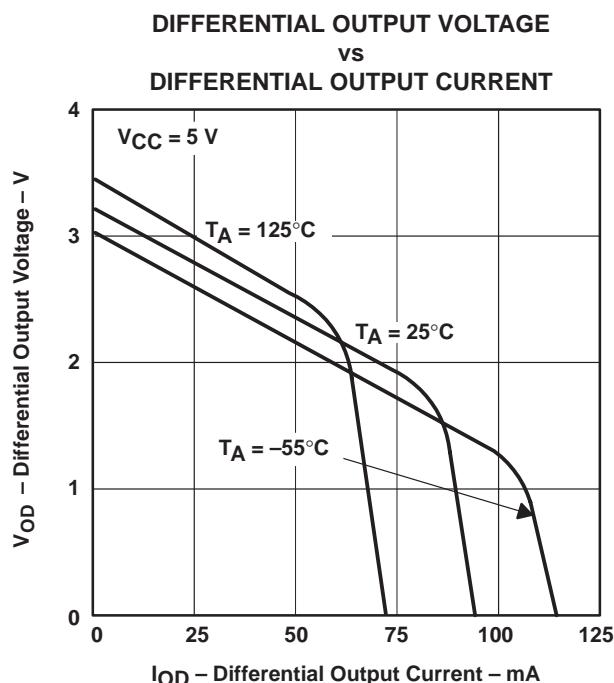


Figure 4

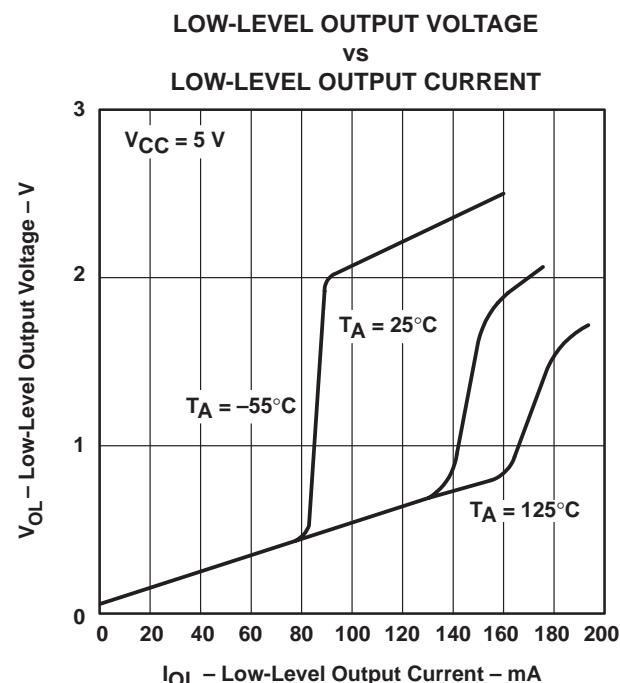


Figure 5

[†] Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

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TYPICAL CHARACTERISTICS[†]

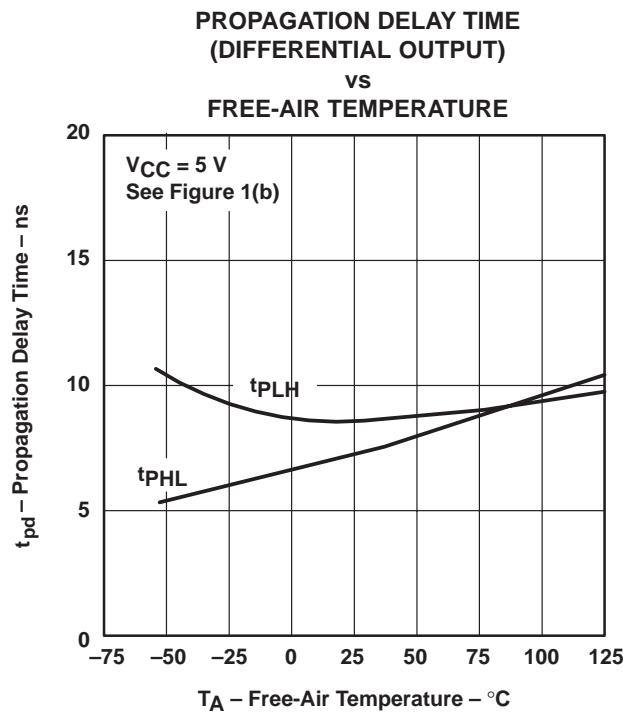


Figure 6

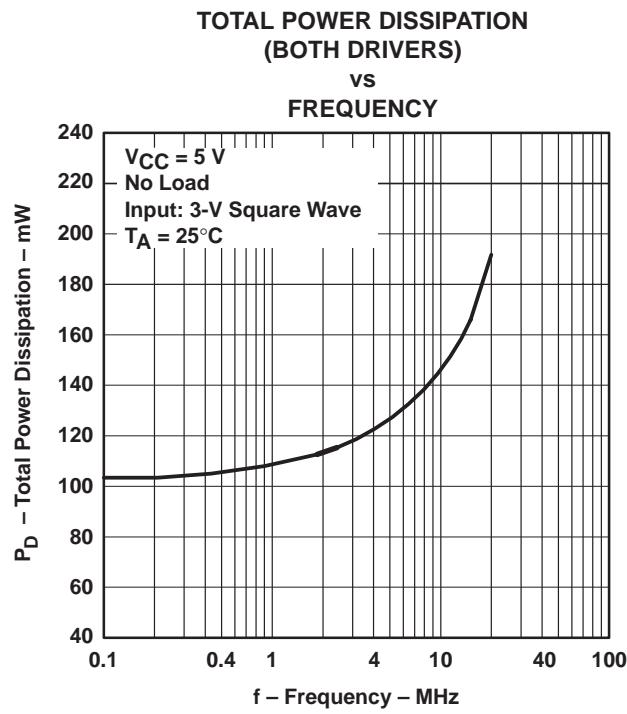
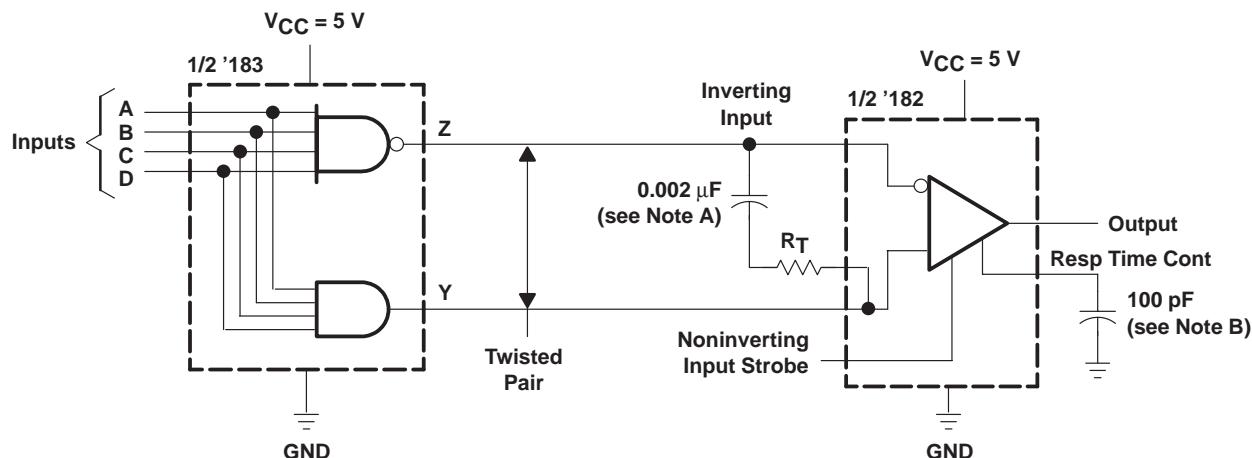


Figure 7

[†] Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

APPLICATION INFORMATION



NOTES: A. When the inputs are open circuited, the output is high. A capacitor may be used for dc isolation of the line-terminating resistor. At the frequency of operation, the impedance of the capacitor should be relatively small.

Example: let $f = 5 \text{ MHz}$
 $C = 0.002 \mu\text{F}$

$$Z_{(\text{circuit})} = \frac{1}{2\pi f C} = \frac{1}{2\pi(5 \times 10^6)(0.002 \times 10^{-6})}$$

$$Z_{(\text{circuit})} \approx 16\Omega$$

B. Use of a capacitor to control response time is optional.

Figure 8. Transmission of Digital Data Over Twisted-Pair Line

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
7900901CA	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7900901CA SNJ55183J
SN55183J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN55183J
SN55183J.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN55183J
SN75183D	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75183
SN75183D.A	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75183
SN75183N	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75183N
SN75183N.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75183N
SN75183NE4	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75183N
SN75183NSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75183
SN75183NSR.A	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75183
SNJ55183J	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7900901CA SNJ55183J
SNJ55183J.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7900901CA SNJ55183J

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

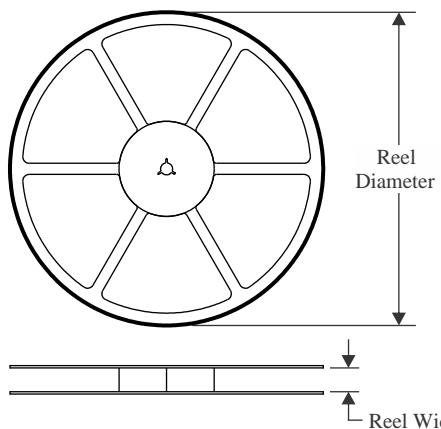
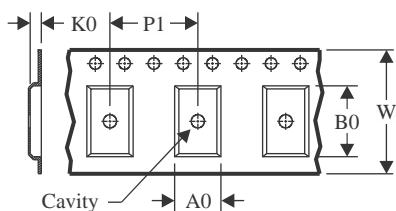
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN55183, SN75183 :

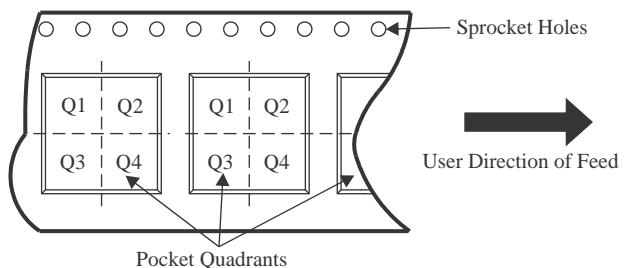
- Catalog : [SN75183](#)
- Military : [SN55183](#)
- Space : [SN55183-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

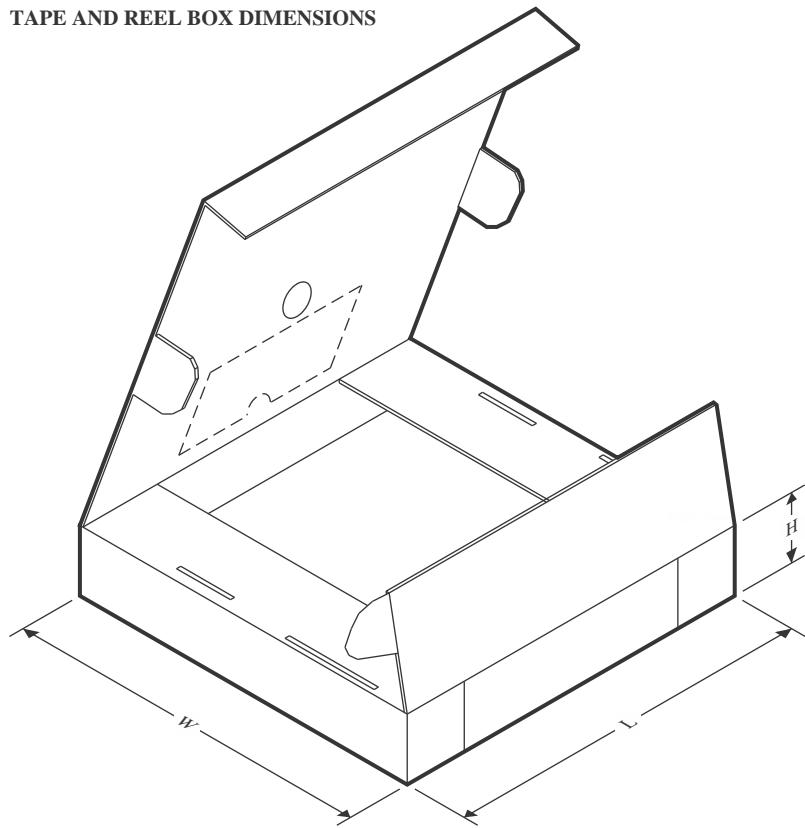
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


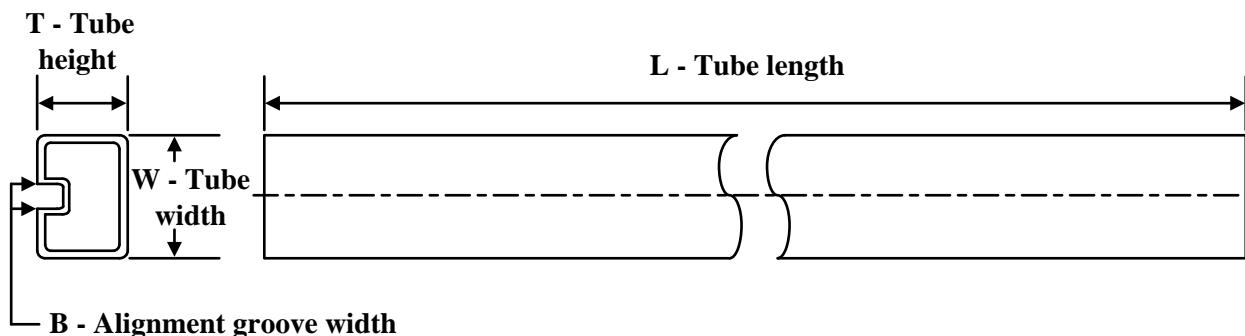
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75183NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75183NSR	SOP	NS	14	2000	353.0	353.0	32.0

TUBE


*All dimensions are nominal

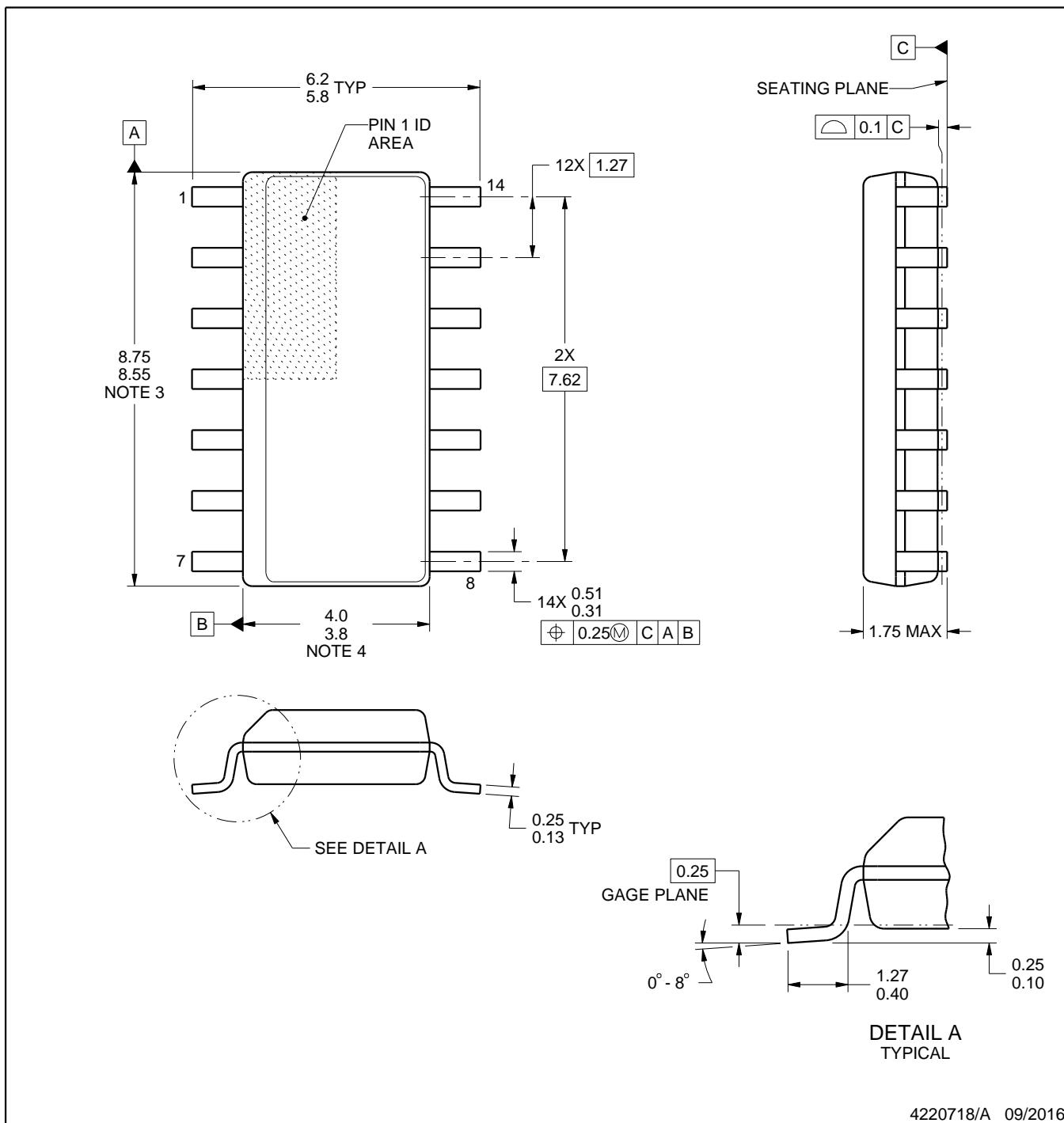
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75183D	D	SOIC	14	50	506.6	8	3940	4.32
SN75183D.A	D	SOIC	14	50	506.6	8	3940	4.32
SN75183N	N	PDIP	14	25	506	13.97	11230	4.32
SN75183N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN75183NE4	N	PDIP	14	25	506	13.97	11230	4.32

PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

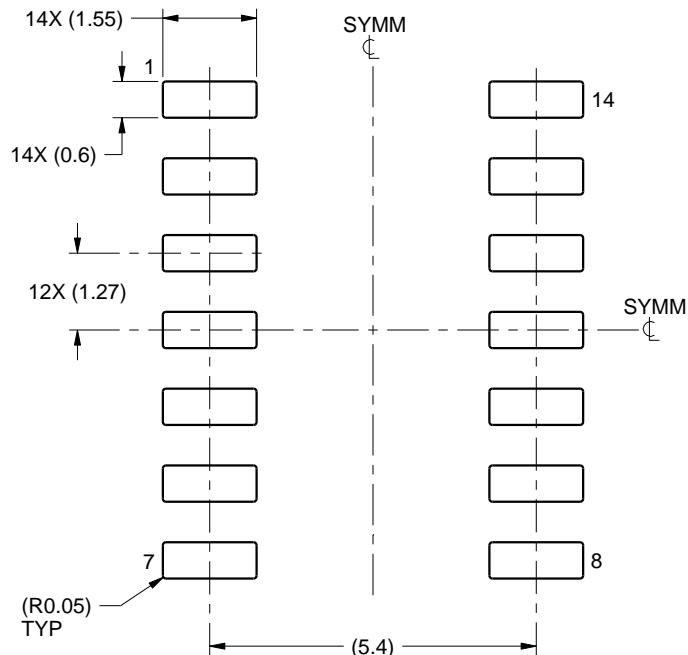
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

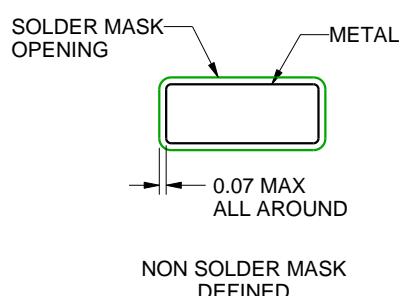
D0014A

SOIC - 1.75 mm max height

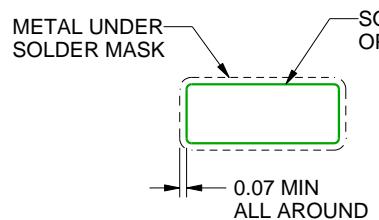
SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

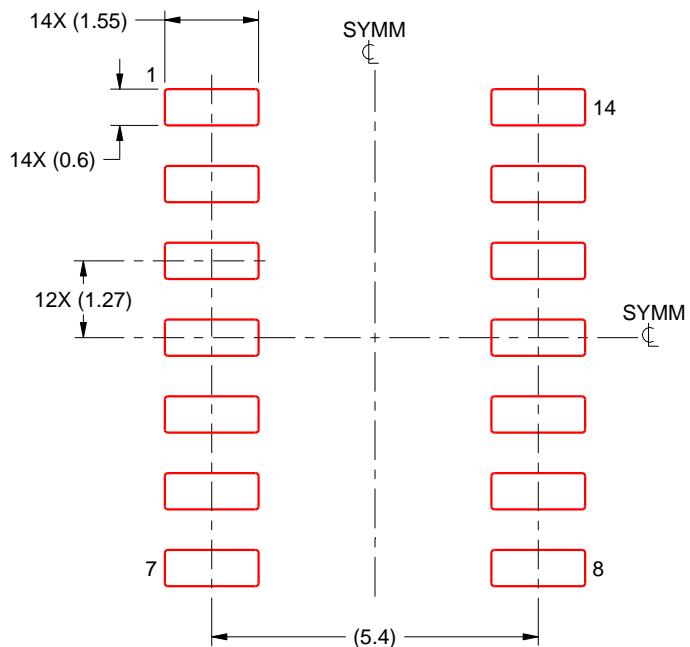
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



NOTES:

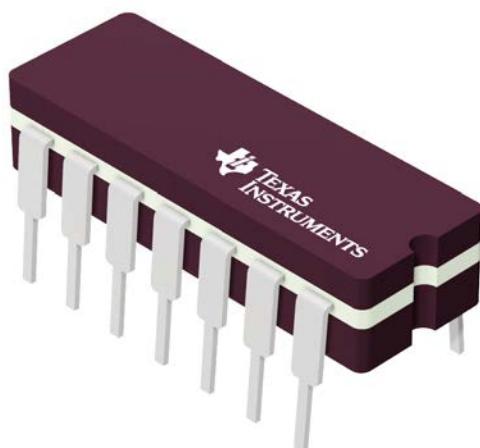
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

J 14

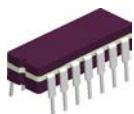
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

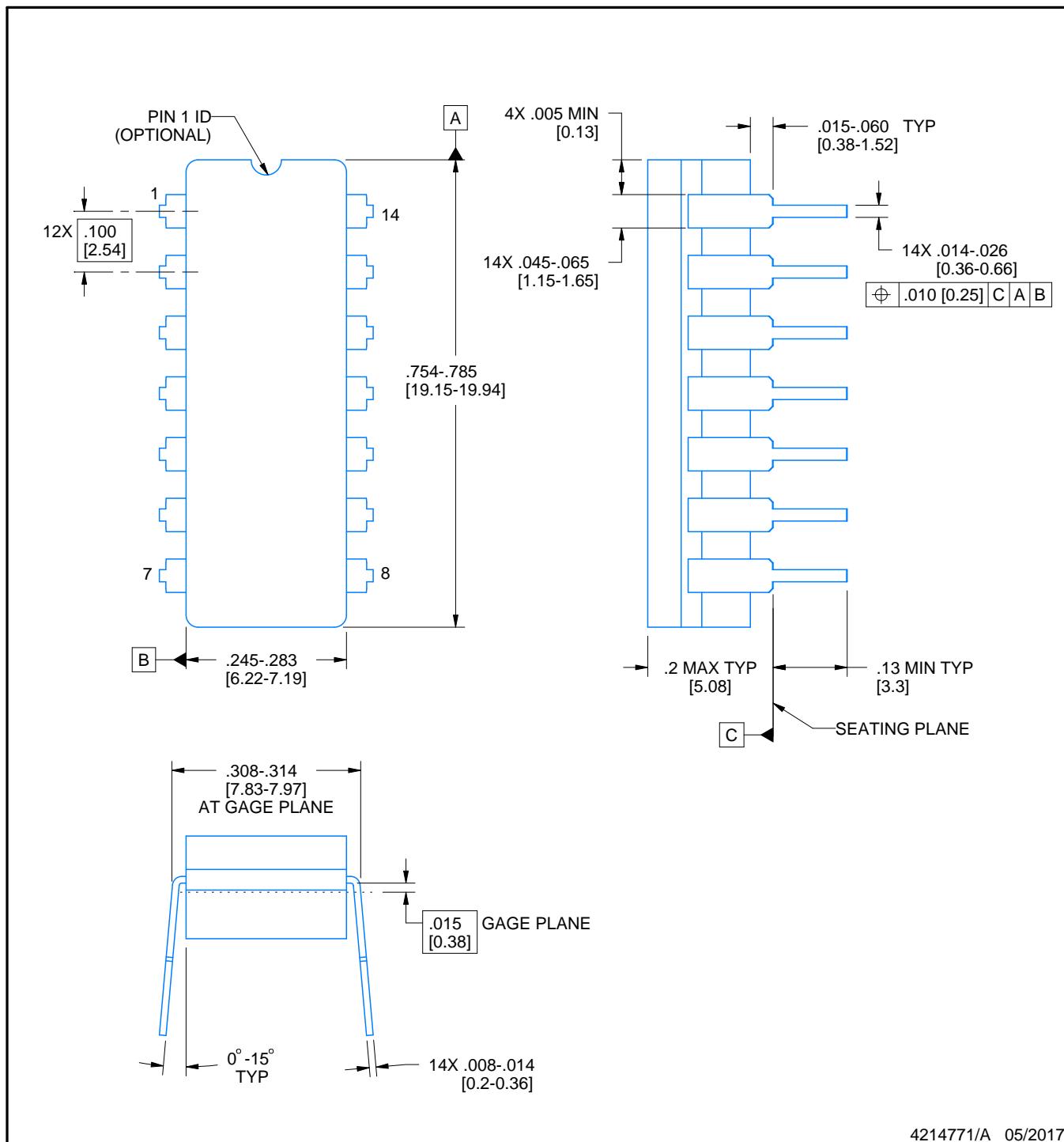


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

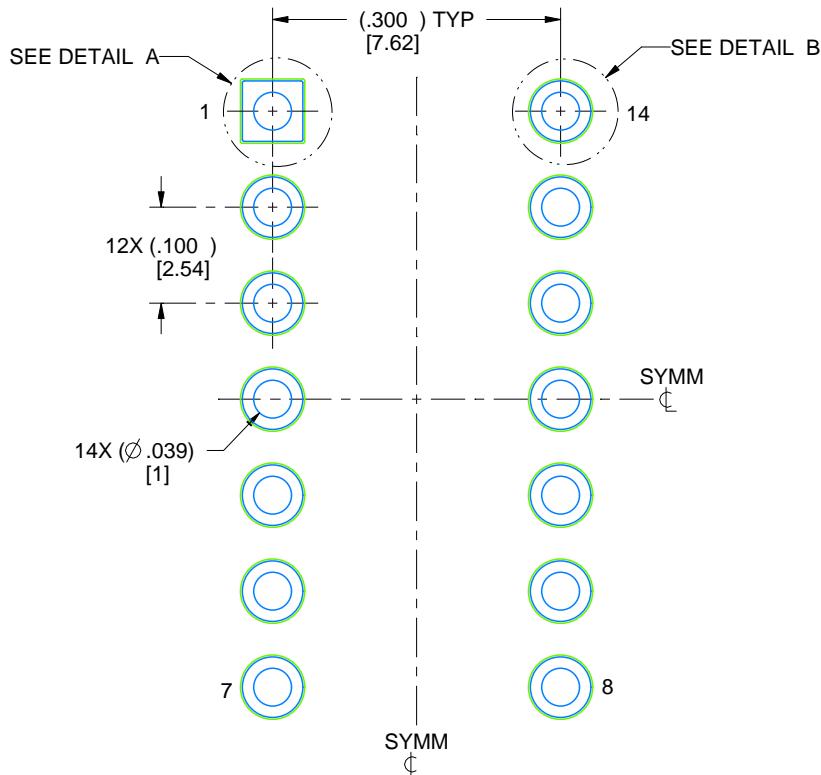
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

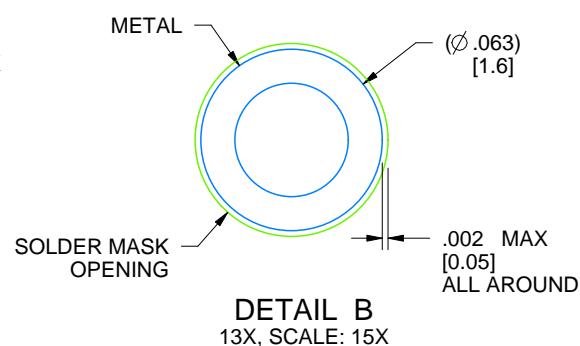
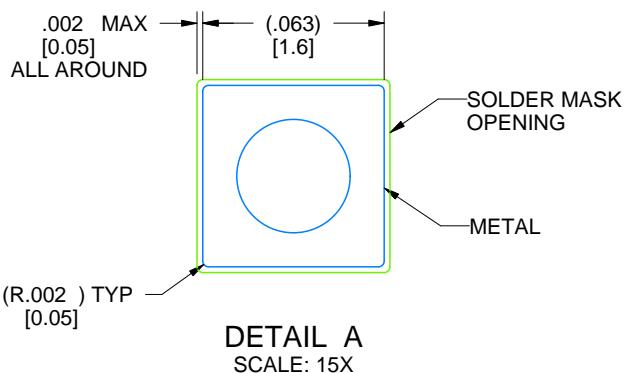
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

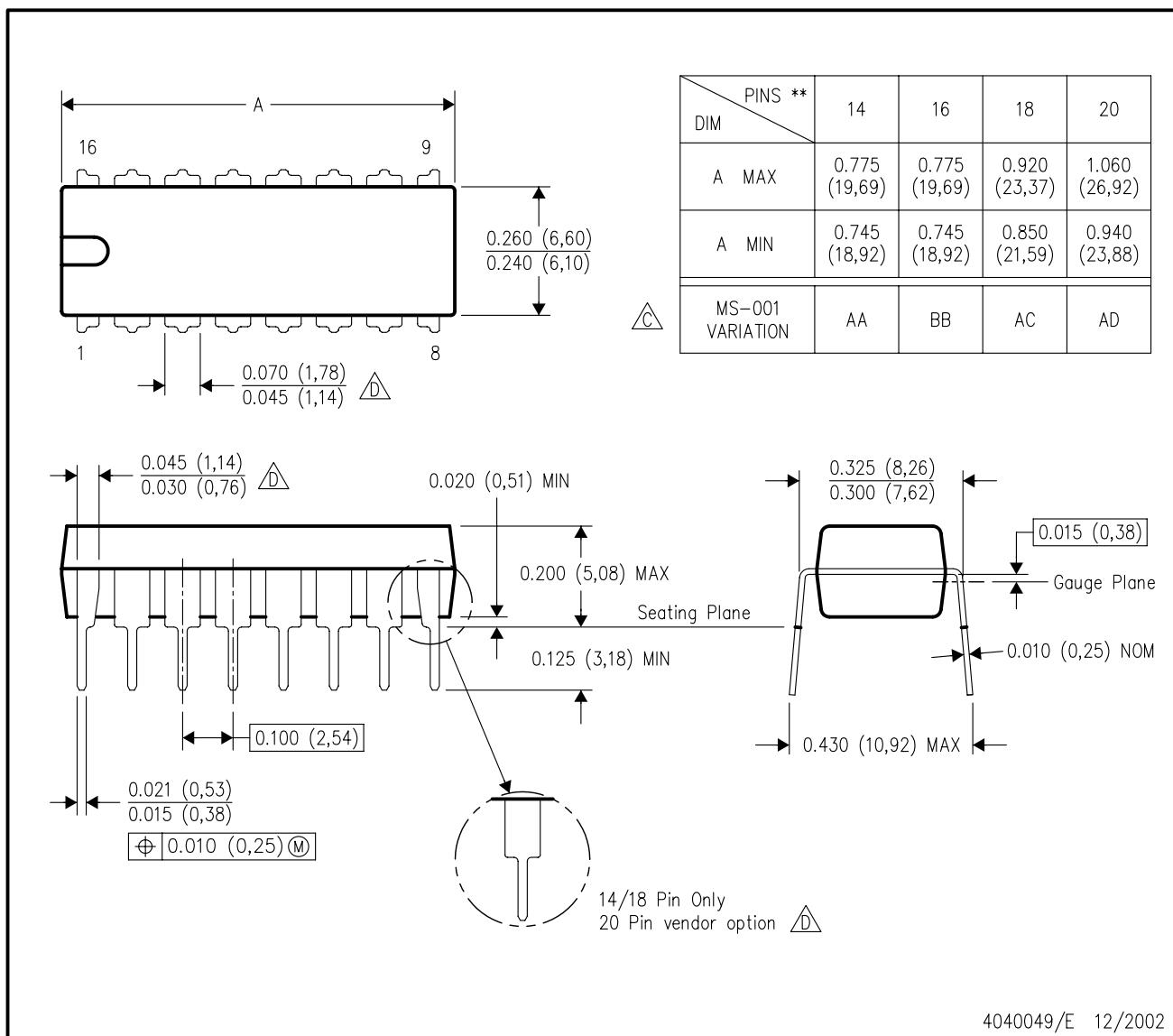


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N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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