QUAD HIGH-SPEED DIFFERENTIAL RECEIVER

Check for Samples: SN65LVDS349

FEATURES

- **Meets or Exceeds the Requirements of ANSI TIA/EIA-644A Standard**
- **Single-Channel Signaling Rates up to 560 Mbps**
- **-4 V to 5 V Common-Mode Input Voltage Range**
- **Flow-Through Architecture**
- **SN65LVDS349 Provides a Wide Common-Mode Range Replacement for the SN65LVDS048A or the DS90LV048A**

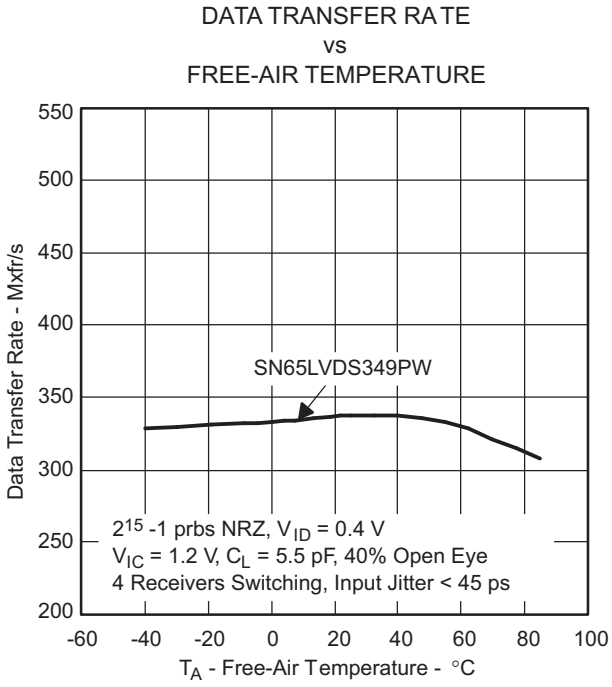
APPLICATIONS

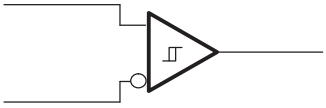
- **Logic Level Translator**
- **Point-to-Point Baseband Data Transmission Over 100-Ω Media**
- **ECL/PECL-to-LVTTL Conversion**
- **Wireless Base Stations**
- **Central Office or PABX Switches**

DESCRIPTION

The SN65LVDS349 is a high-speed, quadruple differential receiver with a wide common-mode input voltage range. This allows receipt of TIA/EIA-644 signals with up to 3-V of ground noise or a variety of differential and single-ended logic levels. The '349 is in a 16-pin package to match the industry-standard footprint of the DS90LV048. The '349 offers a flow-through architecture with all inputs on one side and outputs on the other to ease board layout and reduce crosstalk between receivers.

The LVDS349 provides 3x the standard's minimum common-mode noise voltage tolerance. The -4 V to 5 V common-mode range allows usage in harsh operating environments or accepts LVPECL, PECL, LVECL, ECL, CMOS, and LVCMOS levels without level shifting circuitry. See the Application Information Section for more details on the ECL/PECL to LVDS interface.





(One of four shown; failsafe circuit does not exist in LVDS349)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

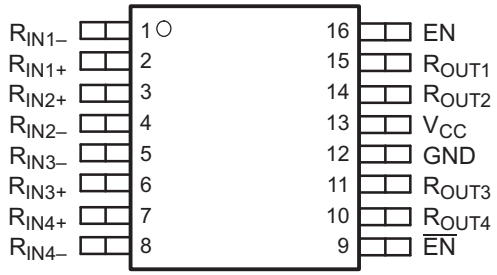
Precise control of the differential input voltage thresholds allows for inclusion of 50 mV of input-voltage hysteresis to improve noise rejection. The differential input thresholds are still no more than ±50 mV over the full input common-mode voltage range.

The receiver inputs can withstand ±15 kV human-body model (HBM), with respect to ground, without damage. This provides reliability in cabled and other connections where potentially damaging noise is always a threat.

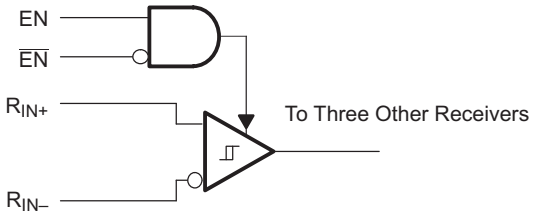
The intended application of these devices and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The SN65LVDS349 is characterized for operation from -40°C to 85°C.

SN65LVDS349
PW PACKAGE
(TOP VIEW)



FUNCTIONAL BLOCK DIAGRAM (one of four receivers shown)



A. Failsafe circuit does not exist in LVDS349

Table 1. AVAILABLE OPTIONS(1)

PART NUMBER(2)	PACKAGE TYPE	PACKAGE MARKING
SN65LVDS349PW	TSSOP	DL349

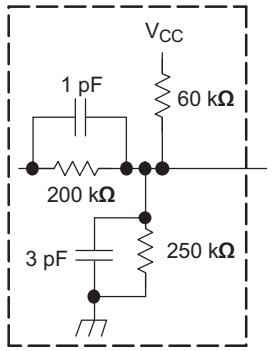
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on ti.com.
(2) Add the R suffix to the device type (e.g., SN65LVDS349PWR) for taped and reeled carrier.

Table 2. FUNCTION TABLE(1)

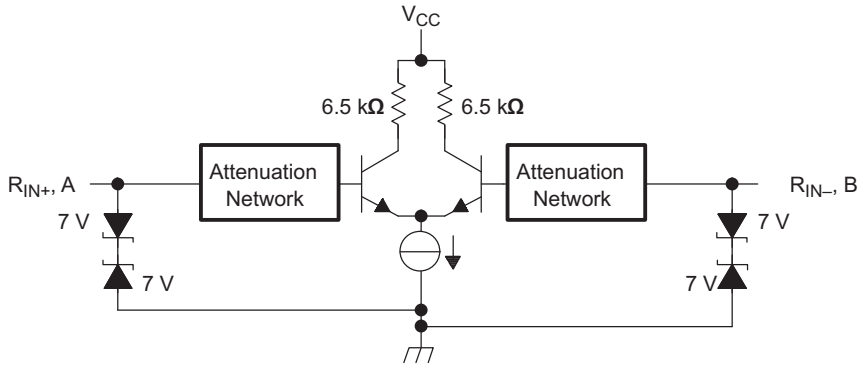
349 DEVICE			
INPUTS			OUTPUTS
$V_{ID} = V_{RIN+} - V_{RIN-}$	EN	$\overline{EN}$	R_{OUT}
$V_{ID} \geq 50$ mV	H	L or OPEN	H
-50 mV < V_{ID} < 50 mV	H	L or OPEN	?
$V_{ID} \leq$ -50 mV	H	L or OPEN	L
Open	H	L or OPEN	?(2)(3)
X	L or OPEN	X	Z
	X	H	Z

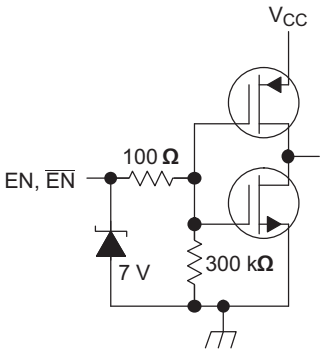
(1) This logic table is at dc condition.
(2) Outputs can toggle with inputs disconnected.
(3) ? indicates state is indeterminate

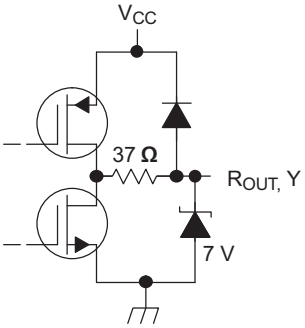
EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



Attenuation Network







ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

				UNIT
Supply voltage range(2), V_{CC},V_{CCA},V_{CCD1}, and V_{CCD2}				-0.5 V to 4 V
Voltage range	Enables, R_{OUT}, or Y			-0.5 V to 6 V
	R_{IN+}, R_{IN-}, A or B			-5 V to 6 V
Electrostatic discharge		Human body model(3)	A, B, R_{IN+}, R_{IN-} and GND	±15 kV
			All pins	±7 kV
		Charged-device model(4)	All pins	±500 V
Continuous power dissipation				See Dissipation Rating Table
Storage temperature range				-65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal (GND, AGND).
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

THERMAL INFORMATION

THERMAL METRIC(1)		SN65LVDS349 PW 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	111.9	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance (3)	33.3	
θ_{JB}	Junction-to-board thermal resistance (4)	52.4	
ψ_{JT}	Junction-to-top characterization parameter (5)	2.0	
ψ_{JB}	Junction-to-board characterization parameter (6)	51.2	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance (7)	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC},V_{CCA},V_{CCD1}, and V_{CCD2}	Supply voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage	Enables	2		5	V
V_{IL}	Low-level input voltage	Enables	0		0.8	V
	Magnitude of differential input voltage	$\|V_{ID}\|$ (LVDS349)	0.1		3	V
	Input voltage (any combination of common mode or input signals)		-4		5	V
T_A	Operating free-air temperature		-40		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{ITH1}	Positive-going differential input voltage threshold		See Figure 1 and Figure 2			50	mV
V_{ITH2}	Negative-going differential input voltage threshold		See Figure 1	-50			mV
$V_{ID(HYS)}$	Differential input voltage hysteresis, $V_{ITH1} – V_{ITH2}$				50		mV
V_{OH}	High-level output voltage		I_{OH} = -4 mA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 4 mA			0.4	V
I_{CC}	Supply current	LVDS349	Enabled, EN at V_{CC}, $\overline{EN}$ at 0 V, No load		16	20	mA
			Disabled, EN at 0 or $\overline{EN}$ at V_{CC}		1.1	4	
I_I	Input current (RIN+, RIN-, A or B inputs)	LVDS349	V_I = -4 V, Other input open	-75		0	µA
			0 V ≤ V_I ≤ 2.4 V, Other input 1.2 V	-20		0	
			V_I = 5 V, Other input open	0		40	
$I_{I(OFF)}$	Power-off input current (RIN+, RIN-, A or B inputs)	LVDS349	V_{CC} = 1.5 V, V_I = -4 V or 5 V, Other input open	-50		50	µA
			V_{CC} = 1.5 V, 0 V ≤ V_I≤ 2.4 V, Other input at 1.2 V	-20		20	
I_{ID}	Differential input current (I_{RIN+} - I_{RIN-}, or I_{IA} - I_{IB})	LVDS349	V_{ID} = 100 mV, V_{IC} = -3.9 V or 4.9 V	-4		4	µA
I_{IH}	High-level input current	Enables	V_{IH} = 2 V	0		10	µA
I_{IL}	Low-level input current	Enables	V_{IL} = 0.8 V	0		10	µA
I_{OZ}	High-impedance output current		V_O = 0 V	-10		10	µA
C_{IN}	Input capacitance, R_{IN+}, R_{IN-} input to GND or A or B input to AGND		V_I = 0.4 sin (4E6πft) + 0.5 V		5		pF

(1) All typical values are at 25°C and with a 3.3-V supply.

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 10 pF, See Figure 3	2.5	4	6	ns
t_{PHL}	Propagation delay time, high-to-low-level output		2.5	4	6	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHL1} - t_{pLH1} \rvert$)			200		ps
$t_{sk(o)}$	Output skew(2)			150		ps
$t_{sk(pp)}$	Part-to-part skew(3)				1	ns
t_r	Output signal rise time			1.2		ns
t_f	Output signal fall time			1		ns
t_r	Output signal rise time	C_L = 1 pF, See Figure 3		650		ps
t_f	Output signal fall time			400		ps
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	See Figure 4		5	9	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			5	9	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output			8	12	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			8	12	ns

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(o)}$ is the magnitude of the time difference between the t_{PHL} or t_{PLH} of all receivers of a single device with all of their inputs connected together.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

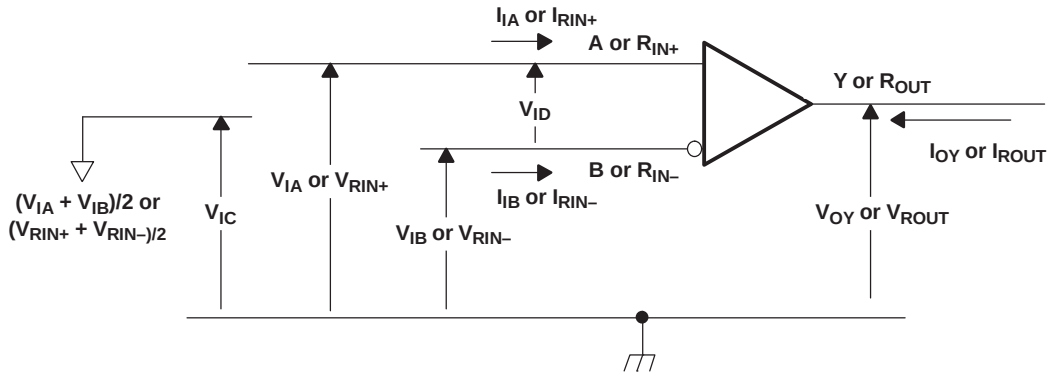
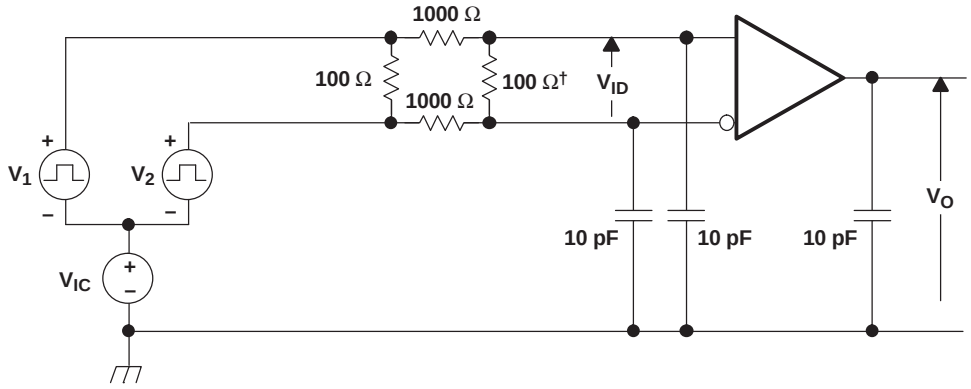
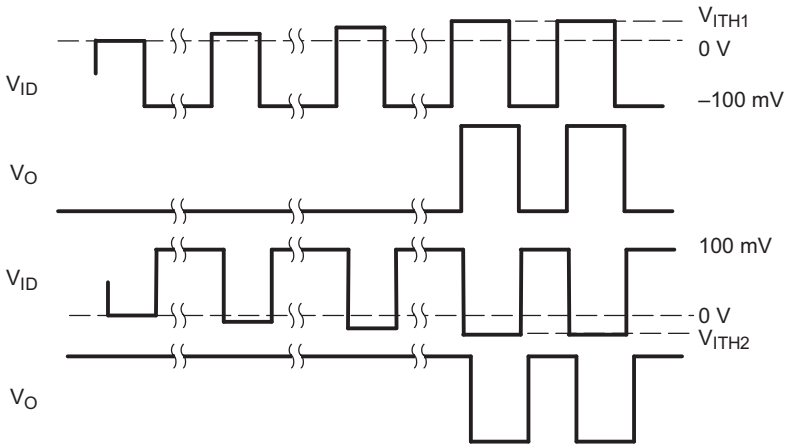


Figure 1. Voltage and Current Definitions



A. Fixture capacitance ±20%.

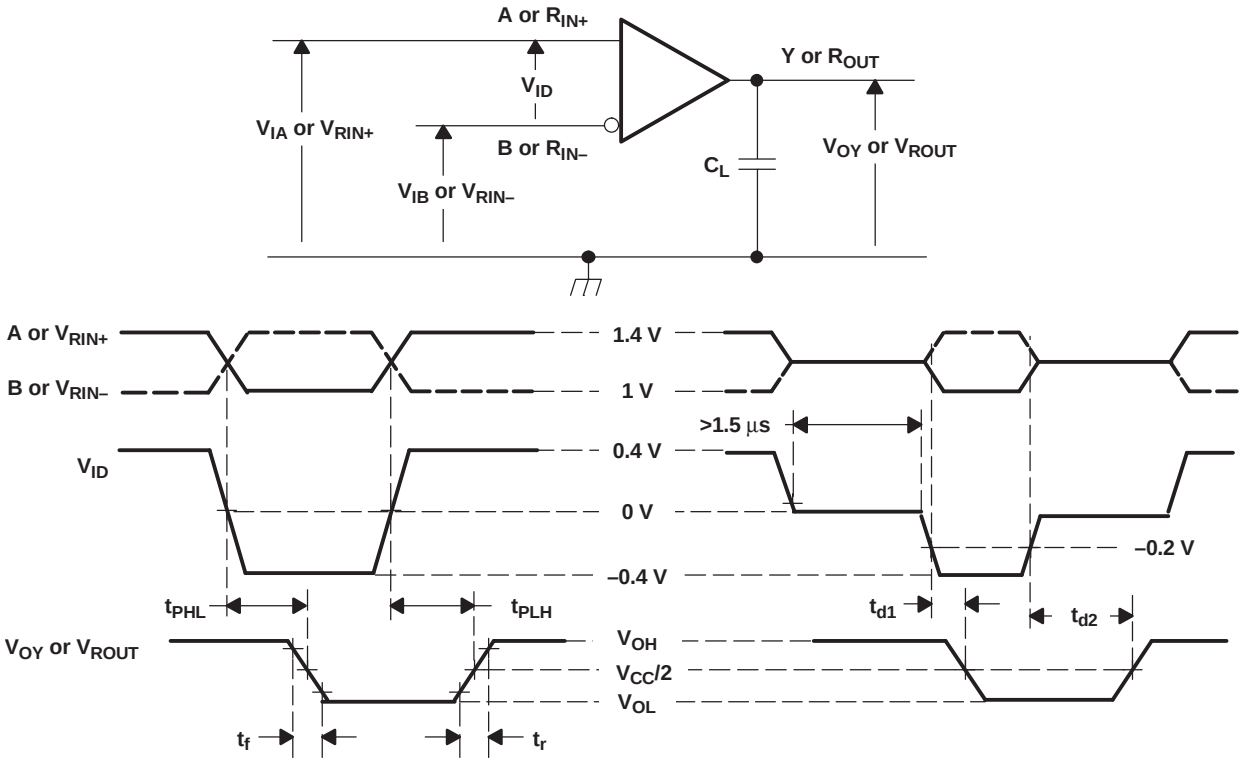
B. Resistors are metal film, 1% tolerance, and surface mount



A. Input signal of 3 MHz, duty cycle of 50±0.2%, and transition time of < 1 ns.

Figure 2. V_{ITH1} and V_{ITH2}, Input Voltage Threshold Test Circuit and Definitions

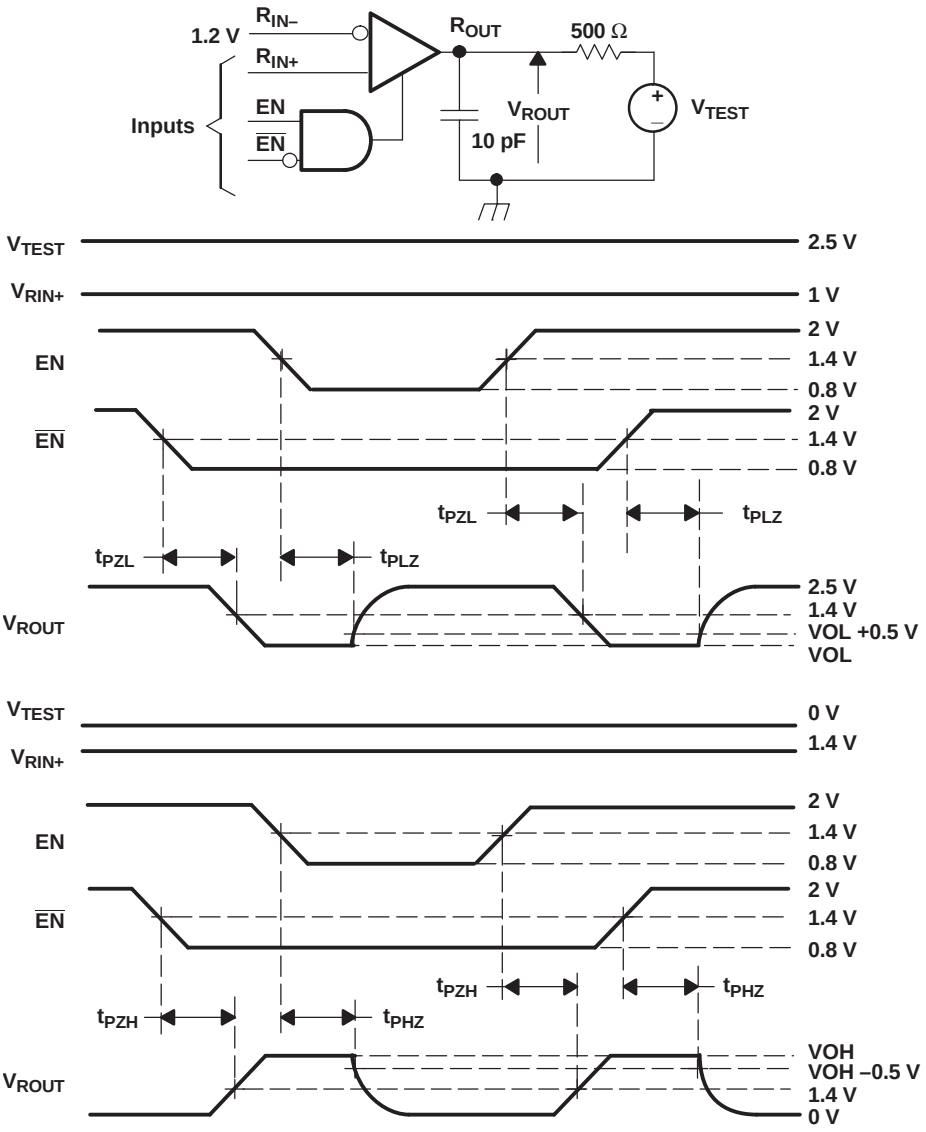
PARAMETER MEASUREMENT INFORMATION (continued)



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, signaling rate = 250 kHz, duty cycle = 50 ±2%, C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T and is ±20%.

Figure 3. Timing Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, signaling rate = 500 kHz, duty cycle = 50 ±2%, C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T and is ±20%.

Figure 4. Enable/Disable Time Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

LOW-TO-HIGH PROPAGATION DELAY vs FREE-AIR TEMPERATURE

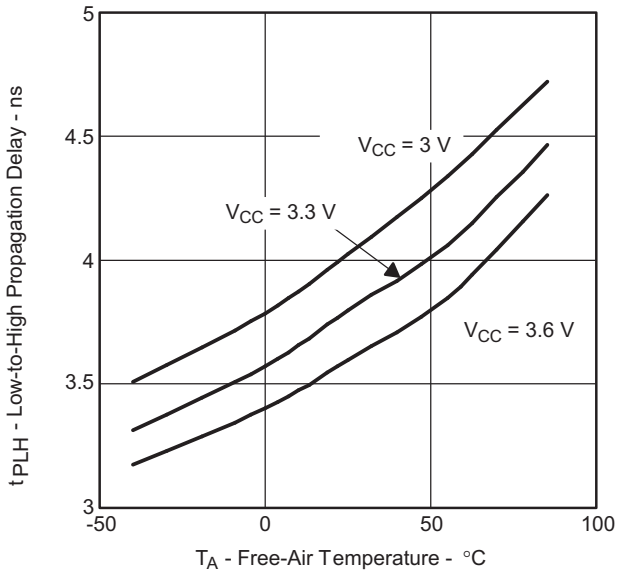


Figure 5.

HIGH-TO-LOW PROPAGATION DELAY vs FREE-AIR TEMPERATURE

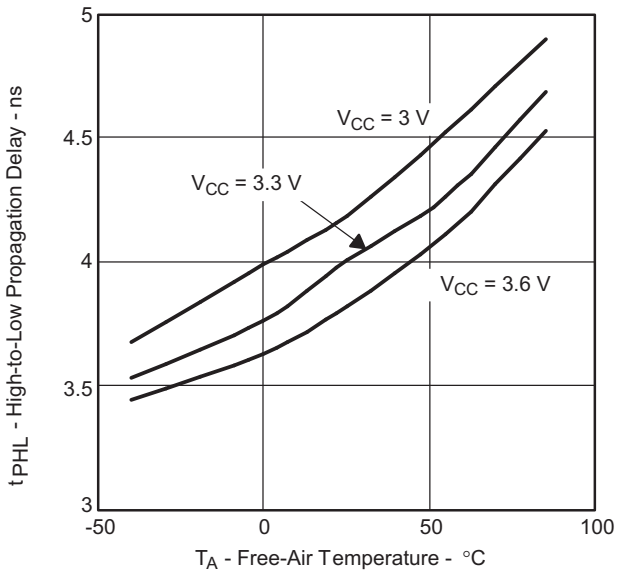


Figure 6.

LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

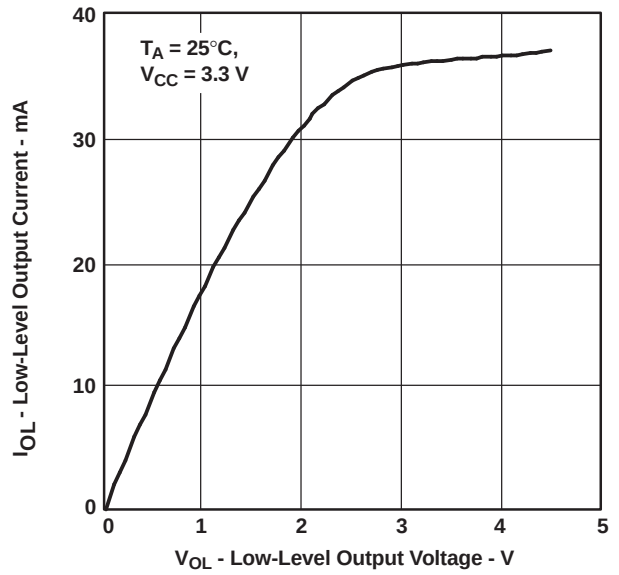


Figure 7.

HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

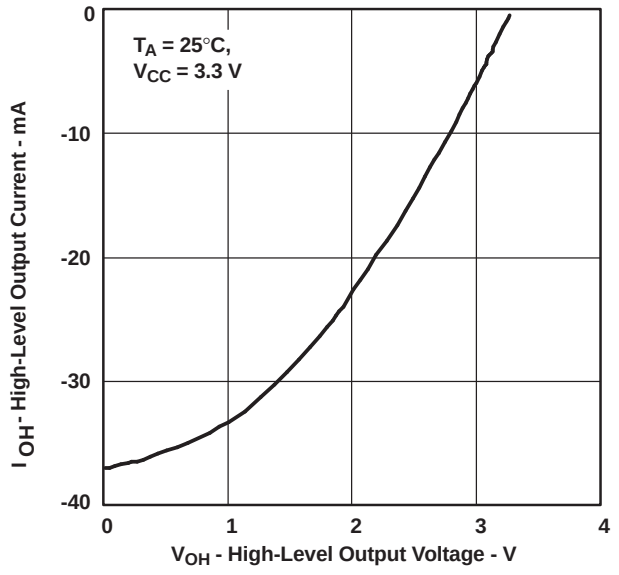


Figure 8.

TYPICAL CHARACTERISTICS (continued)

DATA TRANSFER RATE vs FREE-AIR TEMPERATURE

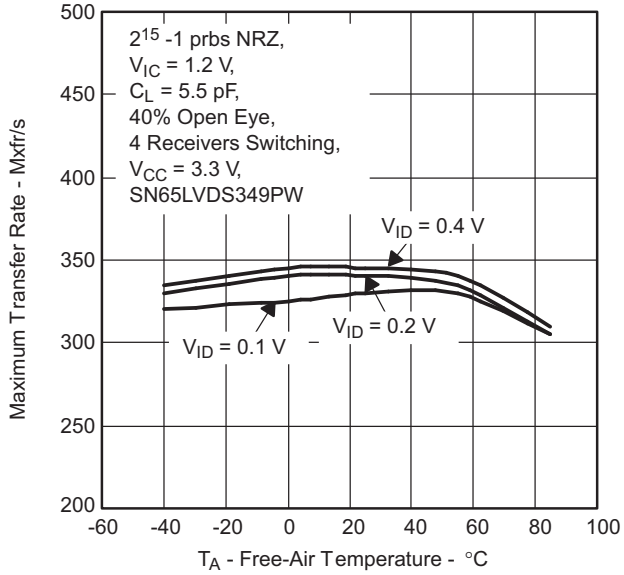


Figure 9.

RMS SUPPLY CURRENT vs SWITCHING FREQUENCY

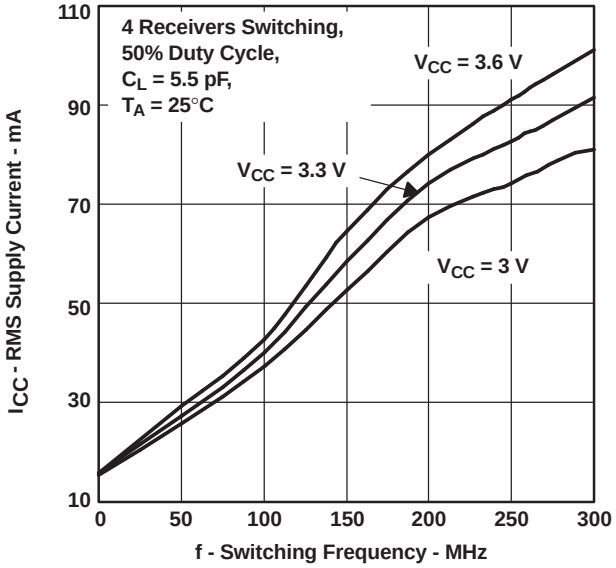


Figure 10.

2^{23} -1 prbs NRZ, T_A = 25°C, C_L = 5.5 pF, 4 Receivers Switching, V_{CC} = 3.3 V

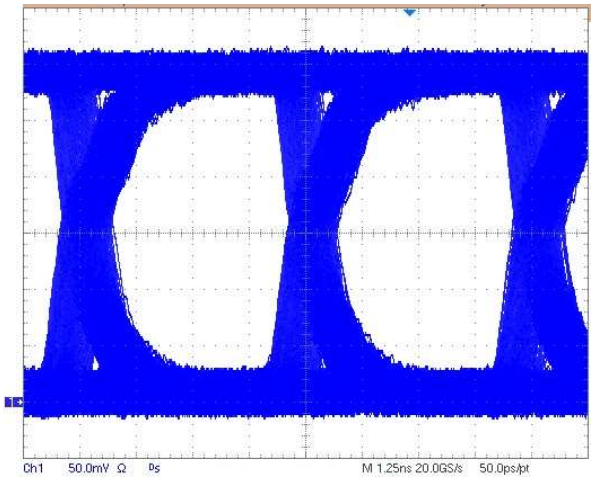


Figure 11. SN65LVDS349 Eye Pattern Running at 200 Mxfr/s

APPLICATION INFORMATION

IMPEDANCE MATCHING AND REFLECTIONS

A termination mismatch can result in reflections that degrade the signal at the load. A low source impedance causes the signal to alternate polarity at the load (oscillates) as shown in Figure 12. High source impedance results in the signal accumulating monotonically to the final value (stair step) as shown in Figure 13. Both of these modes result in a delay in valid signal and reduce the opening in the eye pattern. A 10% termination mismatch results in a 5% reflection ($r = Z_L - Z_O/Z_L + Z_O$), even a 1:3 mismatch absorbs half of the incoming signal. This shows that termination is important in the more critical cases, however, in a general sense, a rather large termination mismatch is not as critical when the differential output signal is much greater than the receiver sensitivity.

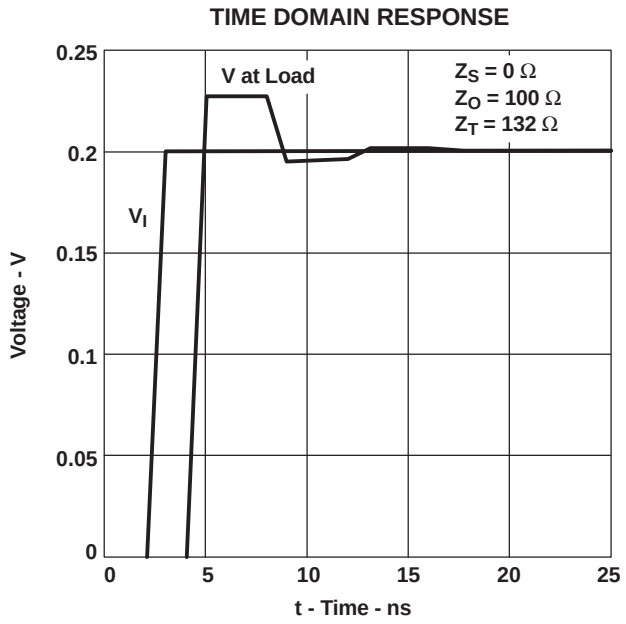


Figure 12. Low-Source Impedance

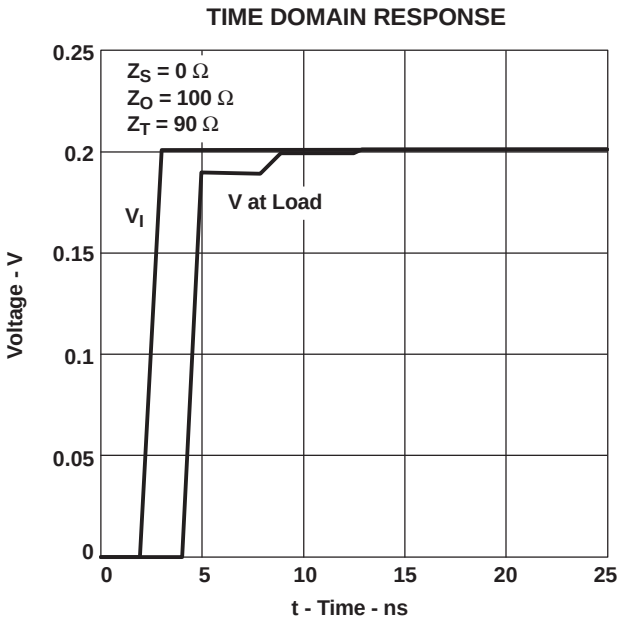


Figure 13. High-Source Impedance

For example, a 200-mV drive signal into a 100-Ω lossless transmission media with a termination resistor of 90 Ω to 132Ω results in ~227 mV to 189 mV into the receiver. This would typically be more than enough signal into a receiver with a sensitivity of ±50 mV assuming no other disturbance or attenuation on the line. The other factors, which reduce the signal margin, do affect this and therefore it is important to match the impedance as closely as possible to allow more noise immunity at the receiver.

ACTIVE FAILSAFE FEATURE

A differential line receiver commonly has a failsafe circuit to prevent it from switching on input noise. Current LVDS failsafe solutions require either external components with subsequent reductions in signal quality or integrated solutions with limited application.

In the SN65LVDS349, the failsafe circuit does not exist. Thus the output can switch if there is noise on the input lines.

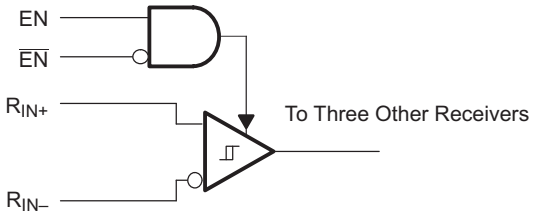


Figure 14. Failsafe Circuit Does Not Exist in the SN65LVDS349

ECL/PECL-to-LVTTL CONVERSION WITH TI LVDS RECEIVER

The various versions of emitter-coupled logic (i.e., ECL, PECL, and LVPECL) are often the physical layer of choice for system designers. Designers know that established technology is capable of high-speed data transmission. In the past, system requirements often forced the selection of ECL. Now technologies like LVDS provide designers with another alternative. While the total exchange of ECL for LVDS may not be a design option, designers have been able to take advantage of LVDS by implementing a small resistor divider network at the input of the LVDS receiver. TI has taken the next step by introducing a wide common-mode LVDS receiver (no divider network required) which can be connected directly to an ECL driver with only the termination bias voltage required for ECL termination (V_{CC} - 2 V).

Figure 15 shows the use of an LV/PECL driver driving 5 meters of CAT-5 cable and being received by TI's wide common-mode receiver and the resulting eye-pattern. The values for R3 are required in order to provide a resistor path to ground for the LV/PECL driver. With no resistor divider, R1 simply needs to match the characteristic load impedance of 50 Ω. The R2 resistor is a small value intended to minimize common-mode reflections.

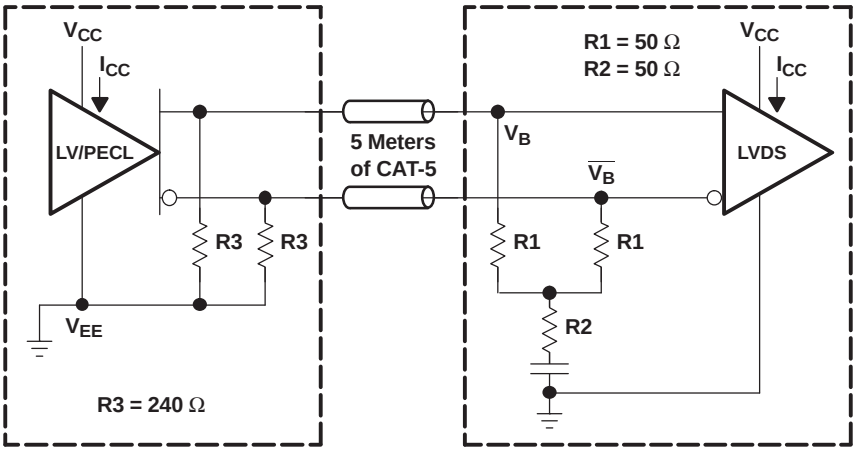


Figure 15. LVPECL or PECL to Remote Wide Common-Mode LVDS Receiver

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVDS349PW	Last Time Buy	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL349
SN65LVDS349PW.B	Last Time Buy	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL349
SN65LVDS349PWR	Last Time Buy	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL349
SN65LVDS349PWR.B	Last Time Buy	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL349
SN65LVDS349PWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL349
SN65LVDS349PWRG4.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL349

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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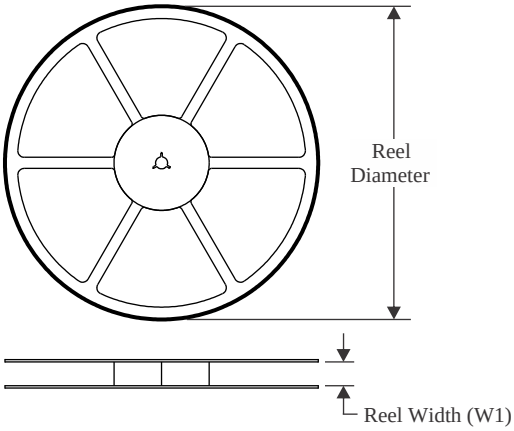
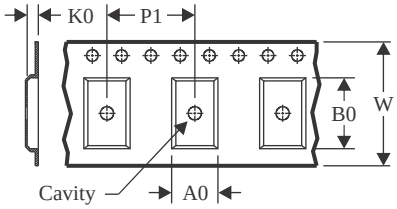
TAPE AND REEL INFORMATION

REEL DIMENSIONS

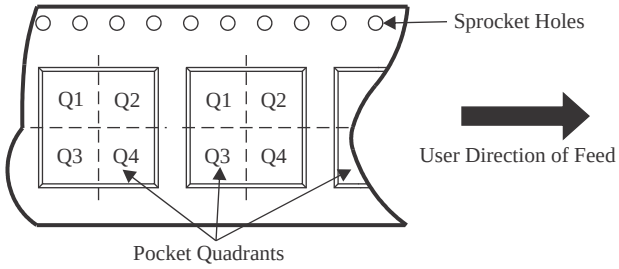


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

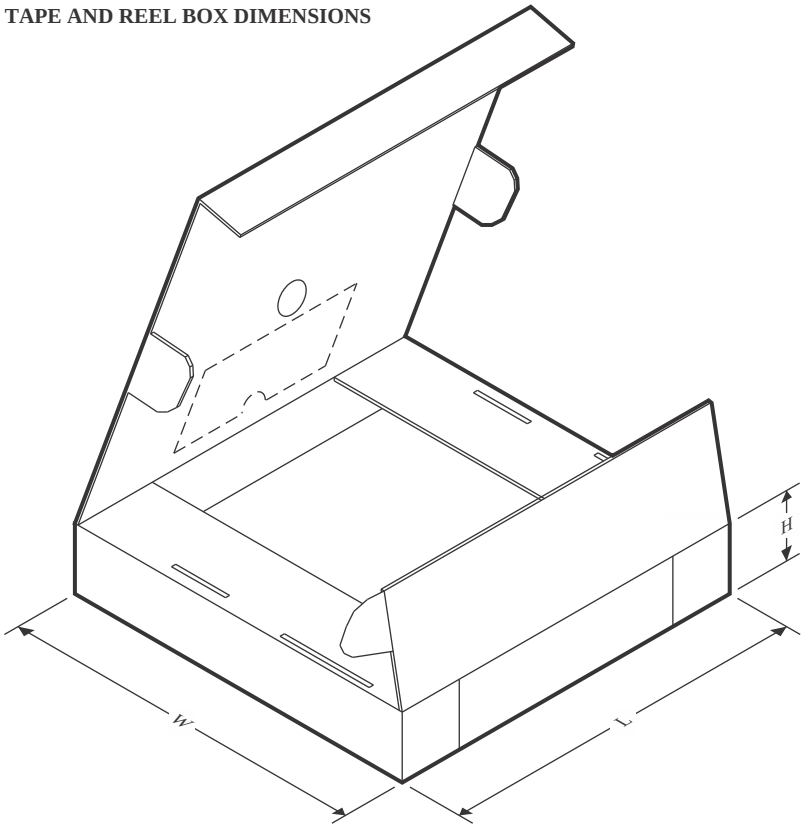
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS349PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65LVDS349PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

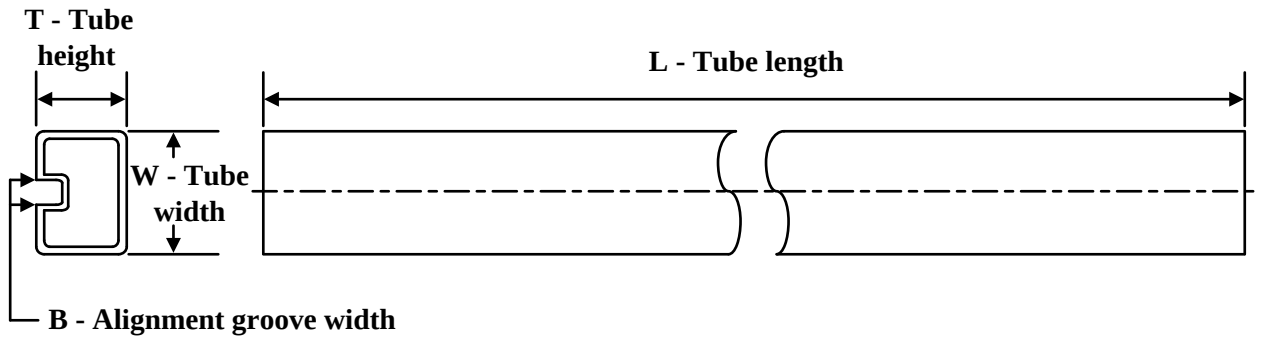
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS349PWR	TSSOP	PW	16	2000	350.0	350.0	43.0
SN65LVDS349PWRG4	TSSOP	PW	16	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

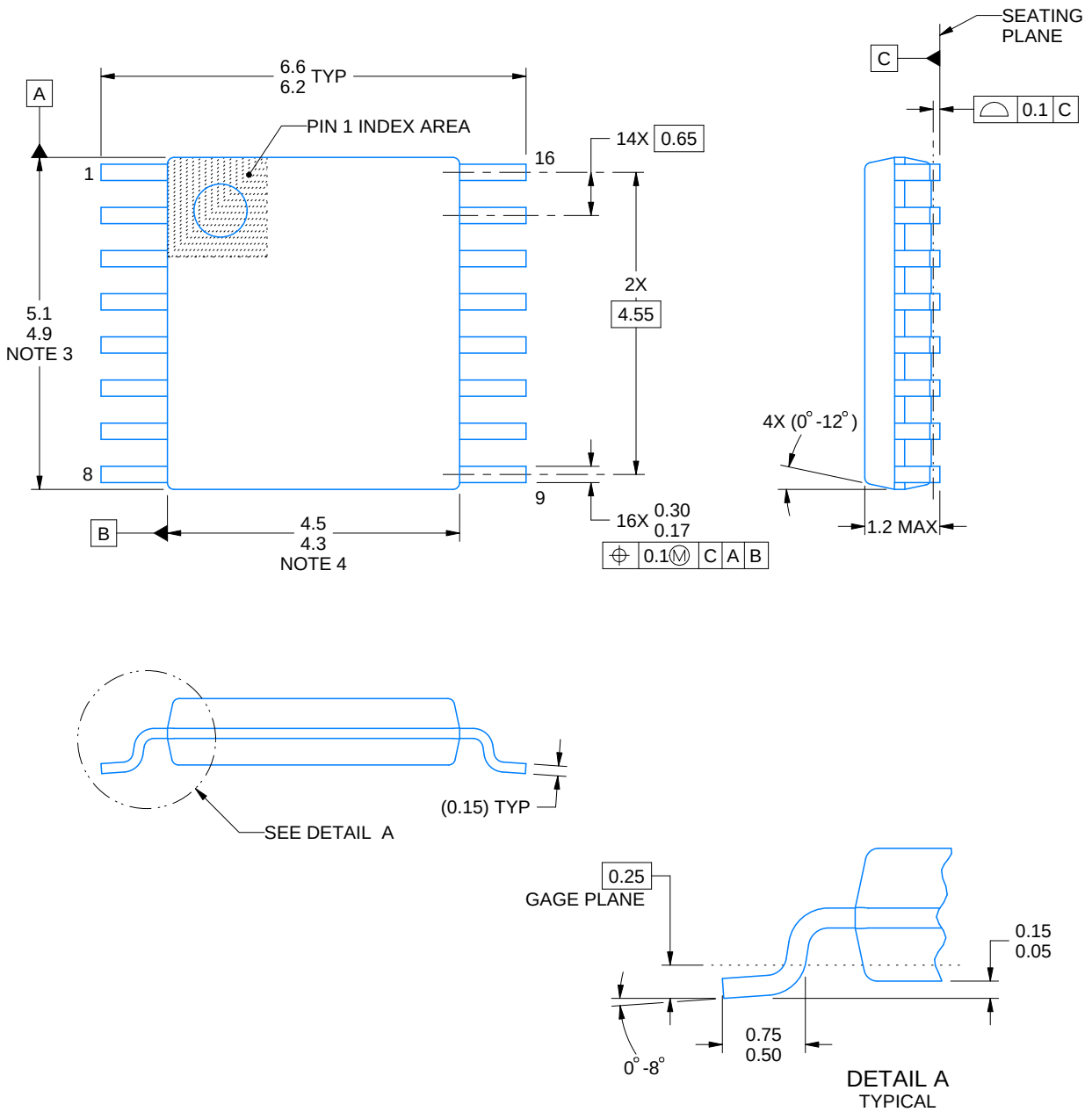
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LVDS349PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDS349PW.B	PW	TSSOP	16	90	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0016A

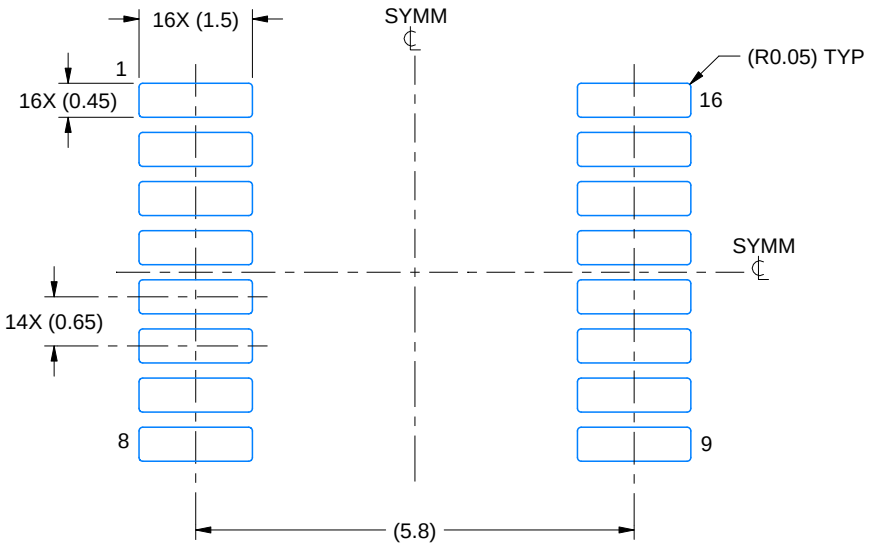
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

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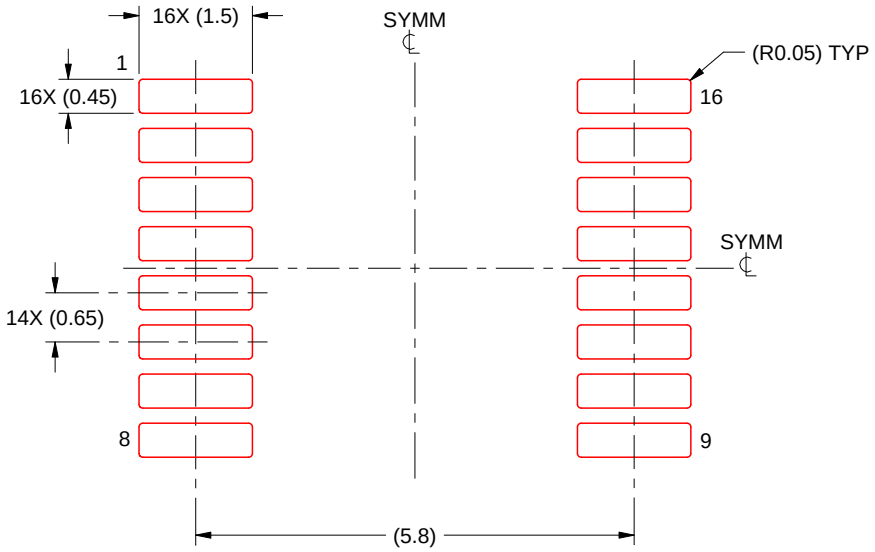
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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