

3.3 V ECL 1:2 Fanout Buffer

FEATURES

- 1:2 ECL Fanout Buffer
- Operating Range
 - PECL $V_{CC} = 3.0\text{ V}$ to 3.8 V With $V_{EE} = 0\text{ V}$
 - NECL: $V_{CC} = 0\text{ V}$ with $V_{EE} = -3.0$ to -3.8 V
- 5 ps Skew Between Outputs
- Support for Clock Frequencies $> 2.0\text{ GHz}$
- 265 ps Typical Propagation Delay
- Deterministic Output Value for Open Input Conditions or When Inputs = V_{EE}
- Built-in Temperature Compensation
- Drop in Compatible to MC10LVEL11, MC100LVEL11
- Built-In Input Pull Down Resistors

APPLICATIONS

- Data and Clock Transmission Over Backplane
- Signaling Level Conversion

DESCRIPTION

The SN65LVEL11 is a fully differential 1:2 ECL fanout buffer. The device includes circuitry to maintain a known logic level when inputs are in open condition. The SN65LVEL11 is functionally equivalent to SN65EL11 with improved performance. The SN65LVEL11 is housed in an industry standard SOIC-8 package and is also available in the TSSOP-8 package option.

PINOUT ASSIGNMENT

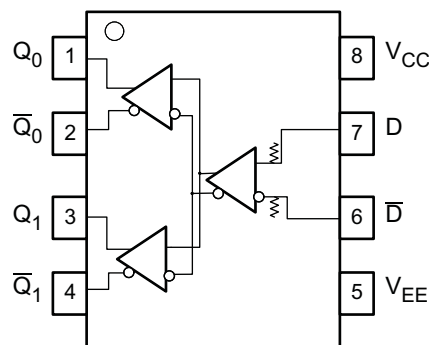


Table 1. Pin Description

PIN	FUNCTION
D, $\bar{D}$	PECL/ECL data inputs
Q_0 , $\bar{Q}_0$, Q_1 , $\bar{Q}_1$	PECL/ECL outputs
V_{CC}	Positive supply
V_{EE}	Negative supply

ORDERING INFORMATION⁽¹⁾

PART NUMBER	PART MARKING	PACKAGE	LEAD FINISH
SN65LVEL11D	SN65LVEL11	SOIC	NiPdAu
SN65LVEL11DGK	SN65LVEL11	SOIC-TSSOP	NiPdAu

(1) Leaded device options not initially available. Contact TI sales representative for further details.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

PARAMETER	CONDITION	VALUE	UNIT
Absolute PECL mode supply voltage, V_{CC}	$V_{EE} = 0\text{ V}$	6	V
Absolute NECL mode power supply, V_{EE}	$V_{CC} = 0\text{ V}$	–6	V
PECL mode input voltage	$V_{EE} = 0\text{ V}; V_I \leq V_{CC}$	6	V
NECL mode input voltage	$V_{CC} = 0\text{ V}; V_I \geq V_{EE}$	–6	V
Output current	Continuous	50	mA
	Surge	100	
Operating temperature range		–40 to 85	°C
Storage temperature range		–65 to 150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

POWER DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	POWER RATING $T_A < 25^\circ\text{C}$ (mW)	THERMAL RESISTANCE, JUNCTION TO AMBIENT NO AIRFLOW	DERATING FACTOR $T_A > 25^\circ\text{C}$ (mW/°C)	POWER RATING $T_A = 85^\circ\text{C}$ (mW)
SOIC	Low-K	719	139	7	288
	High-K	840	119	8	336
SOIC-TSSOP	Low-K	469	213	5	188
	High-K	527	189	5	211

THERMAL CHARACTERISTICS

PARAMETER		PACKAGE	VALUE	UNIT
θ_{JB}	Junction-to Board Thermal Resistance	SOIC	79	°C/W
		SOIC-TSSOP	120	
θ_{JC}	Junction-to Case Thermal Resistance	SOIC	98	°C/W
		SOIC-TSSOP	74	

KEY ATTRIBUTES

CHARACTERISTICS	VALUE
Internal input pull down resistor	75 k Ω
Moisture sensitivity level	Level 1
Flammability rating (Oxygen Index: 28 to 34)	UL 94 V-0 at 0.125 in
ESD-HBM	4 kV
ESD-machine model	200 V
ESD-charge device model	2 kV
Meets or exceeds JEDEC Spec EIA/JESD78 latchup test	

LVPECL DC CHARACTERISTICS⁽¹⁾ ($V_{CC} = 3.3\text{ V}$, $V_{EE} = 0.0\text{ V}$)⁽²⁾

CHARACTERISTICS		–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Power Supply Current		20	25		20	25		21	25	mA
V_{OH}	Output HIGH Voltage ⁽³⁾		2215	2420	2215	2286	2420	2215		2420	mV
V_{OL}	Output LOW Voltage ⁽³⁾		1470	1680	1470	1584	1680	1470		1680	mV
V_{IH}	Input High Voltage (Single-Ended)		2135	2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)		1490	1825	1490		1825	1490		1825	mV
V_{IHCMR}	Input HIGH voltage common mode range (Differential) ⁽⁴⁾										V
	$V_{pp} < 500\text{ mV}$		1.2	3.1	1.1		3.1	1.1		3.1	
	$V_{pp} > 500\text{ mV}$		1.4	3.1	1.3		3.1	1.3		3.1	
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW current										μA
	D		0.5			0.5			0.5		
	$\overline{D}$		–600			–600			–600		

- (1) Device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
- (2) Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $\pm 0.3\text{ V}$
- (3) Outputs are terminated through a 50 Ω resistor to $V_{CC} - 2.0\text{ V}$.
- (4) V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} min and 1 V.

LVPNECL DC CHARACTERISTICS⁽¹⁾ ($V_{EE} = -3.3\text{ V}$; $V_{CC} = 0.0\text{ V}$;) ⁽²⁾

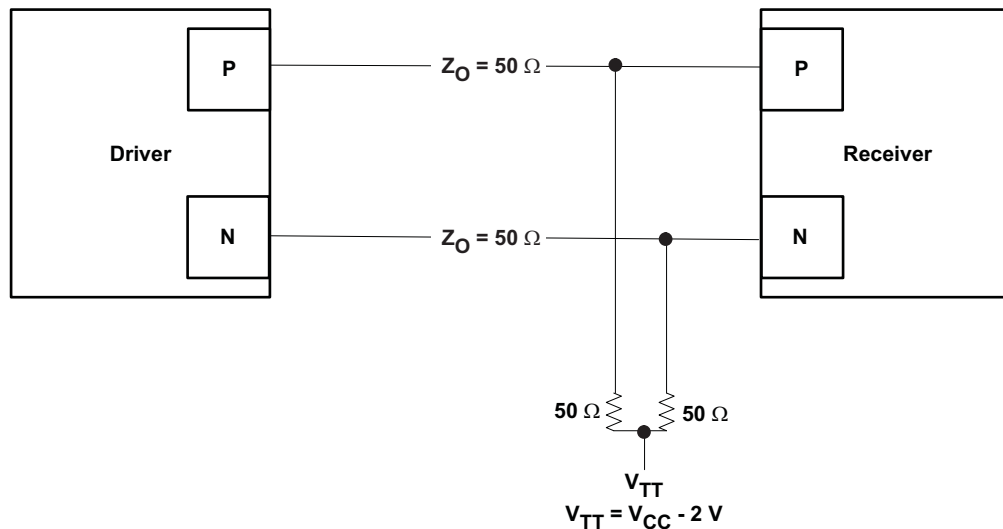
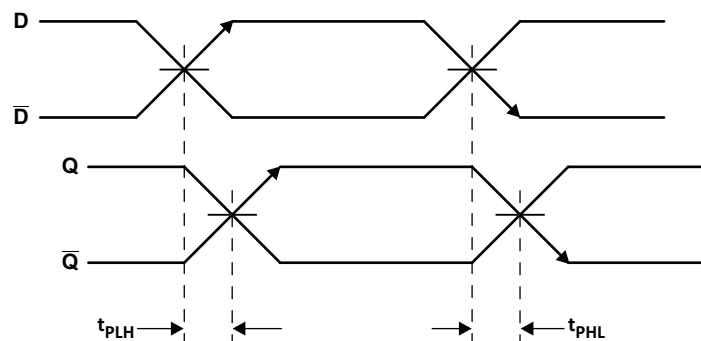
CHARACTERISTICS		–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{EE}	Power supply current		20	25		20	25		21	25	mA
V_{OH}	Output HIGH voltage ⁽³⁾		–1085	–880	–1085	–1013	–880	–1085		–880	mV
V_{OL}	Output LOW voltage ⁽³⁾		–1830	–1620	–1830	–1722	–1620	–1830		–1620	mV
V_{IH}	Input high voltage (Single-Ended)		–1165	–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW voltage (Single-Ended)		–1810	–1475	–1810		–1475	–1810		–1475	mV
V_{IHCMR}	Input HIGH voltage common mode range (Differential) ⁽⁴⁾										V
	$V_{pp} < 500\text{ mV}$		–2.1	–0.2	–2.2		–0.2	–2.2		–0.2	
	$V_{pp} > 500\text{ mV}$		–1.9	–0.2	–2.0		–0.2	–2.0		–0.2	
I_{IH}	Input HIGH current			150			150			150	μA
I_{IL}	Input LOW current										μA
	D		0.5			0.5			0.5		
	$\overline{D}$		–600			–600			–600		

- (1) Device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
- (2) Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $\pm 0.3\text{ V}$.
- (3) Outputs are terminated through a 50 Ω resistor to $V_{CC} - 2.0\text{ V}$.
- (4) V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} min and 1 V.

AC CHARACTERISTICS ⁽¹⁾($V_{CC} = 3.3\text{ V}$; $V_{EE} = 0.0\text{ V}$ or $V_{CC} = 0.0\text{ V}$; $V_{EE} = -3.3\text{ V}$) ⁽²⁾

CHARACTERISTIC		–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{MAX}	Max switching frequency ⁽³⁾ See Figure 6		2.9			2.7			2.4		GHz
t_{PLH}/t_{PHL}	Propagation delay to output	235		350	235		350	235		350	ps
t_{SKEW}	Within device skew ⁽⁴⁾		10	18		10	18		10	18	ps
	Device to device skew ⁽⁵⁾		10	25		10	25		10	25	ps
	Duty cycle skew ⁽⁶⁾		5	15		5	15		5	15	ps
t_{JITTER}	Random clock jitter (RMS)		0.2			0.2			0.2		ps
V_{PP}	Input swing ⁽⁷⁾	200		1000	200		1000	200		1000	mV
t_r/t_f	Output rise/fall times Q (20%–80%)	150		300	150		300	150		300	ps

- (1) Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
- (2) V_{EE} can vary $\pm 0.3\text{ V}$
- (3) Maximum switching frequency measured at output amplitude of 300 mVpp.
- (4) Within-device skew is defined as identical transitions on similar paths through a device.
- (5) Device-Device Skew is defined as identical transitions at identical V_{CC} levels.
- (6) Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.
- (7) $V_{PP(min)}$ is the minimum input swing for which AC parameters are assured.

Typical Termination for Output Driver

Figure 1. Termination for Output Driver

Figure 2. Propagation Delay

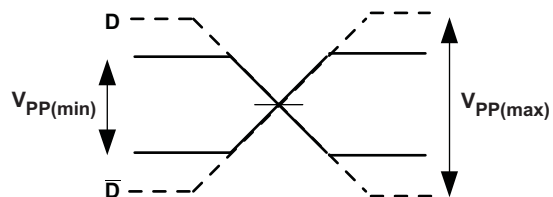


Figure 3. Input Voltage Swing

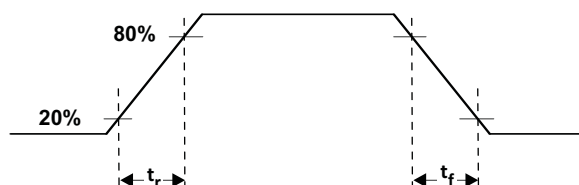


Figure 4. Output Rise and Fall Times

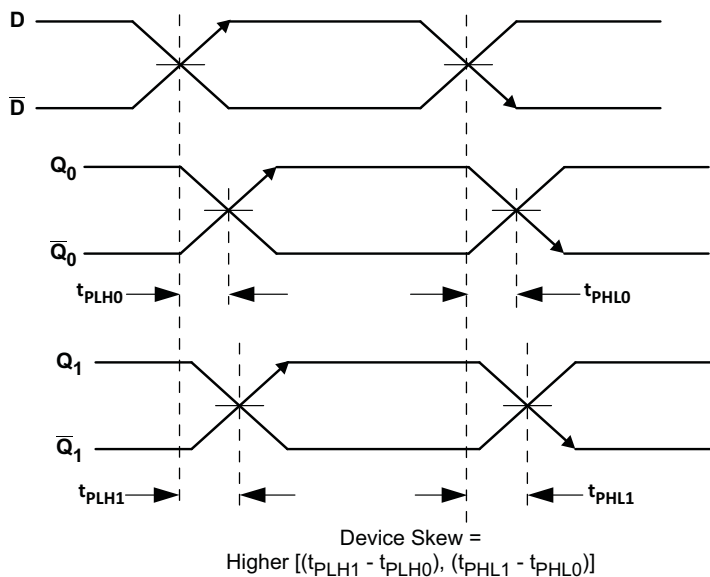


Figure 5. Device Skew

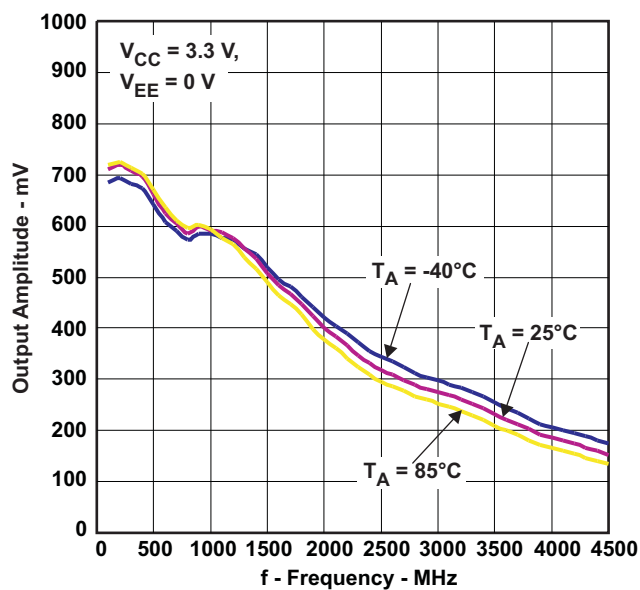


Figure 6. Output Amplitude vs Frequency

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVEL11D	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVEL11
SN65LVEL11D.B	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVEL11
SN65LVEL11DGK	Active	Production	VSSOP (DGK) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SINI
SN65LVEL11DGK.B	Active	Production	VSSOP (DGK) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SINI
SN65LVEL11DGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	Call TI Nipdau	Level-1-260C-UNLIM	-40 to 85	SINI
SN65LVEL11DGKR.B	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SINI
SN65LVEL11DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVEL11
SN65LVEL11DR.B	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVEL11

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

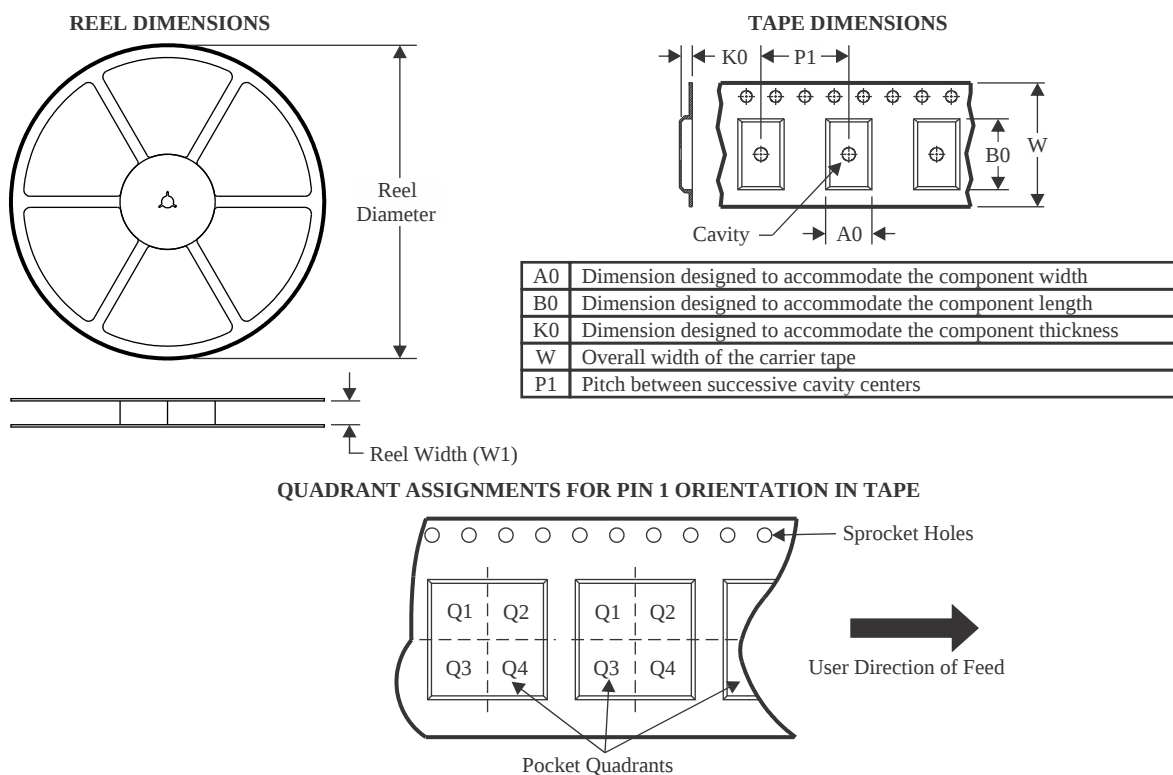
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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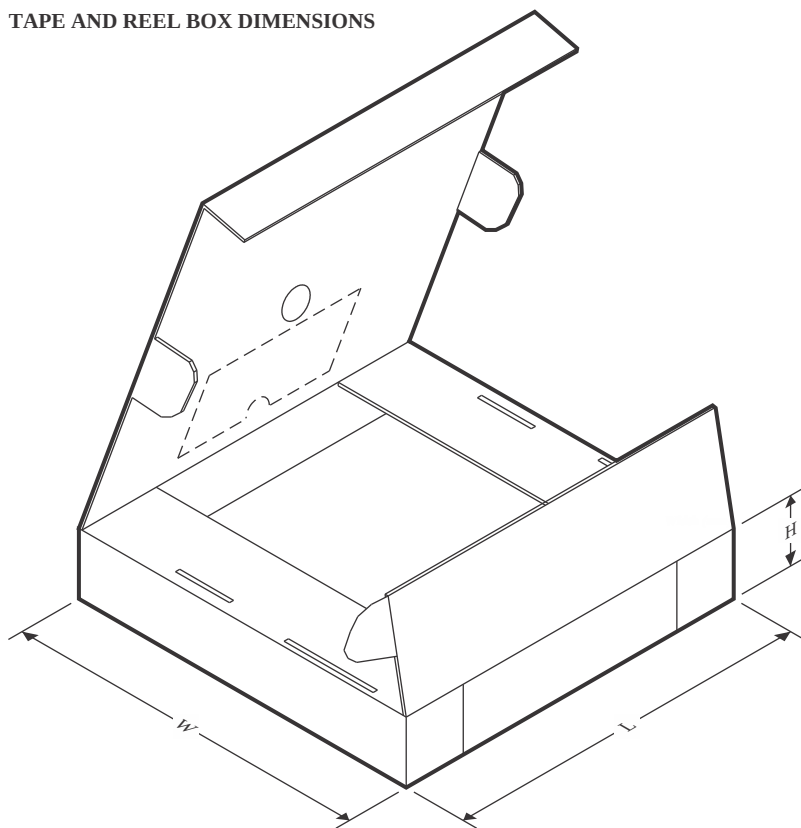
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVEL11DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

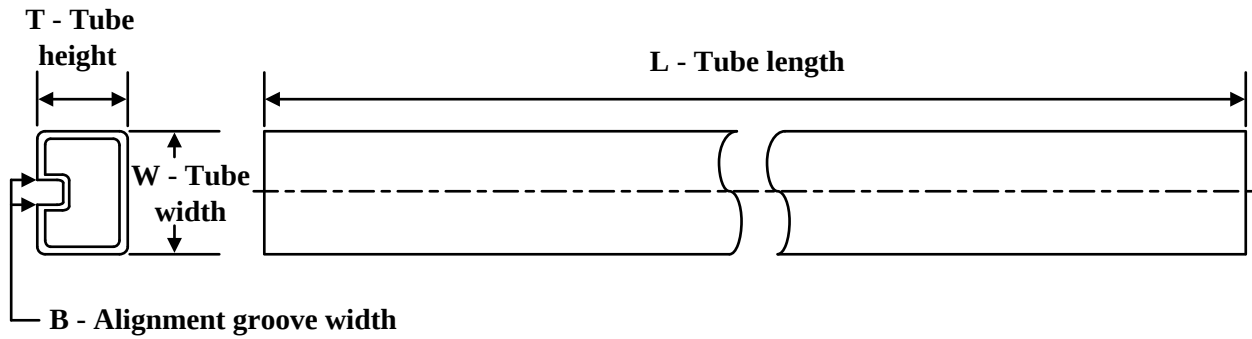
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVEL11DR	SOIC	D	8	2500	353.0	353.0	32.0

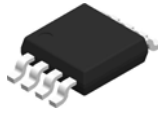
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65LVEL11D	D	SOIC	8	75	506.6	8	3940	4.32
SN65LVEL11D.B	D	SOIC	8	75	506.6	8	3940	4.32
SN65LVEL11DGK	DGK	VSSOP	8	80	330.2	6.6	3005	1.88
SN65LVEL11DGK.B	DGK	VSSOP	8	80	330.2	6.6	3005	1.88

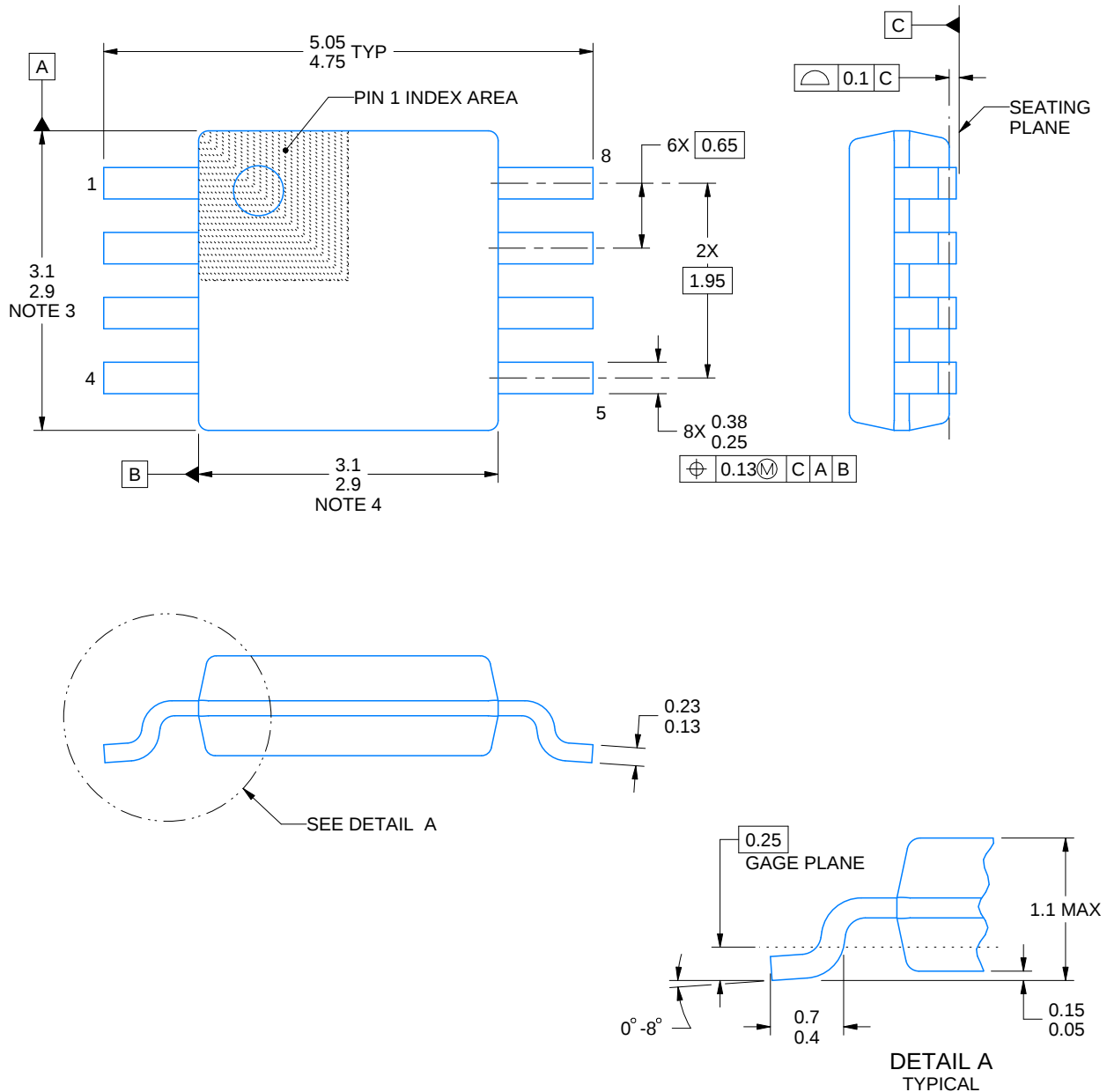
DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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NOTES:

PowerPAD is a trademark of Texas Instruments.

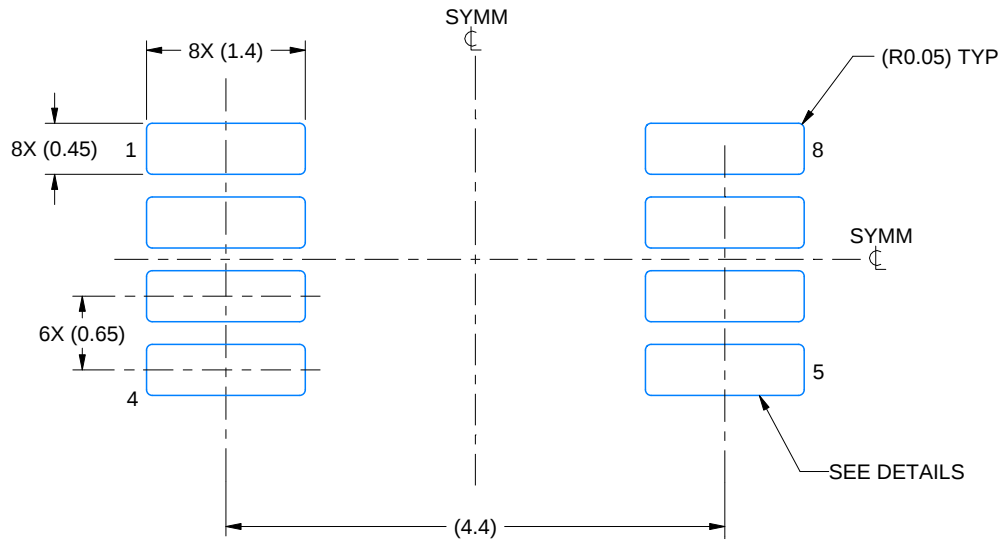
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

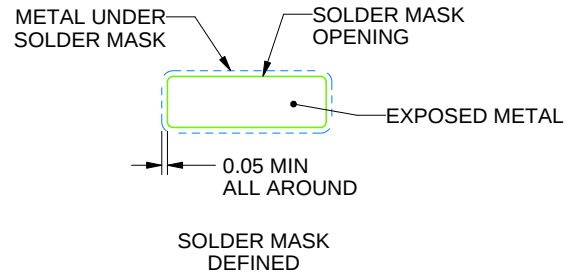
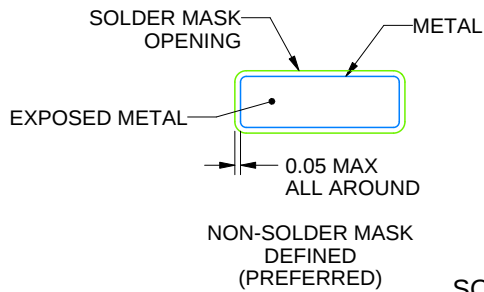
DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

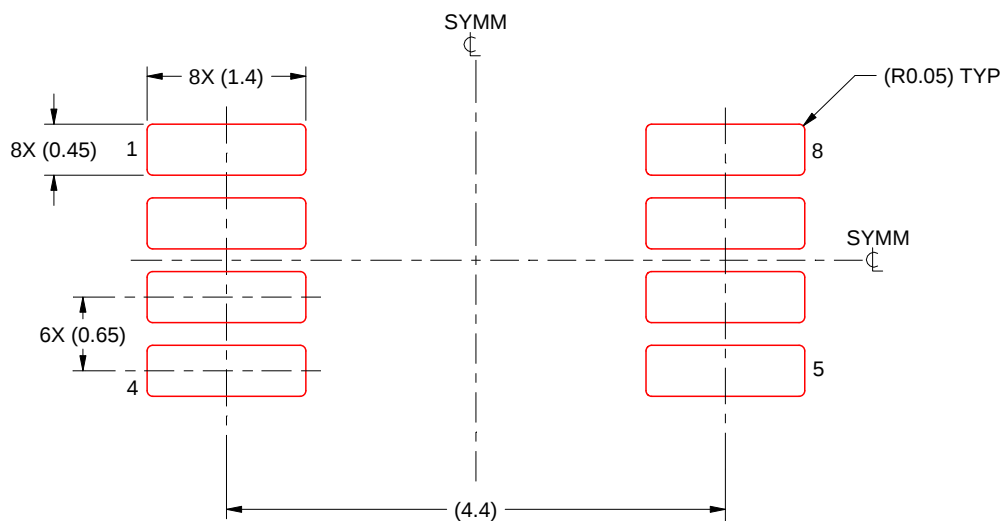
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

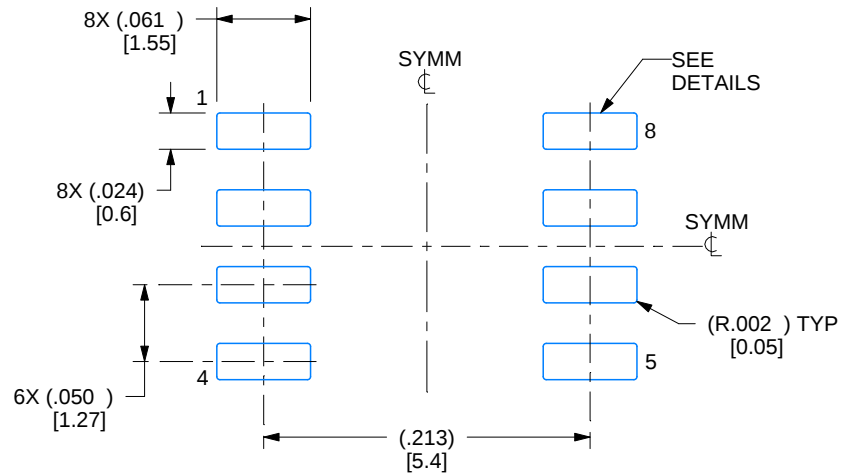


1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

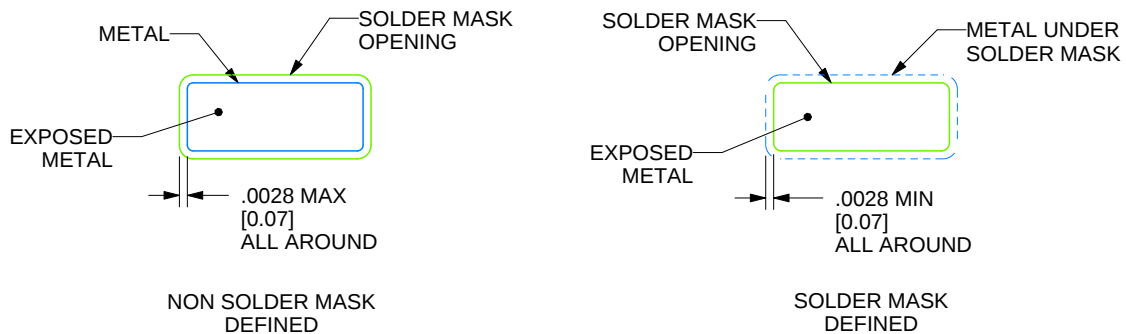
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

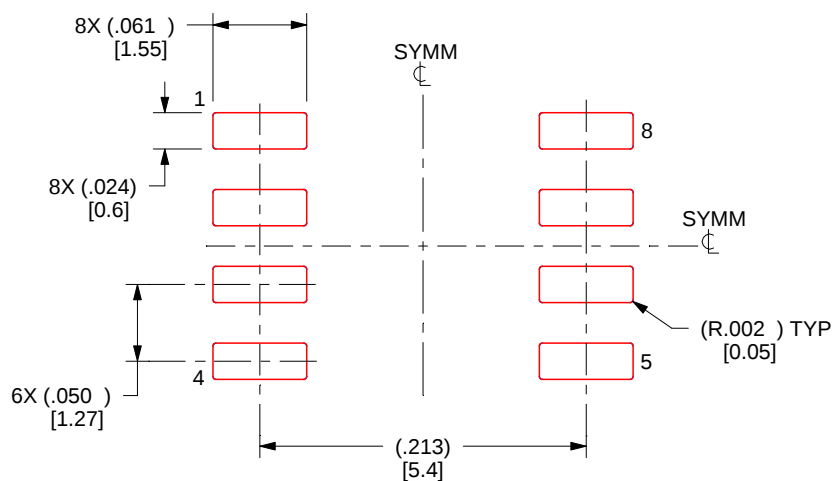
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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