SN74ACT2G101 Dual Configurable Data Flip-Flops with Clear and TTL-Compatible Inputs

1 Features

- Operating voltage range of 4.5V to 5.5V
- TTL-compatible Schmitt-trigger inputs support slow and noisy input signals
- Continuous ±24mA output drive at 5V
- Supports up to ±75mA output drive at 5V in short bursts
- Drives 50Ω transmission lines
- Fast operation with delay of 10.5ns max

2 Applications

- Hold a signal during controller reset
- Input slow edge-rate signals
- Operate in noisy environments

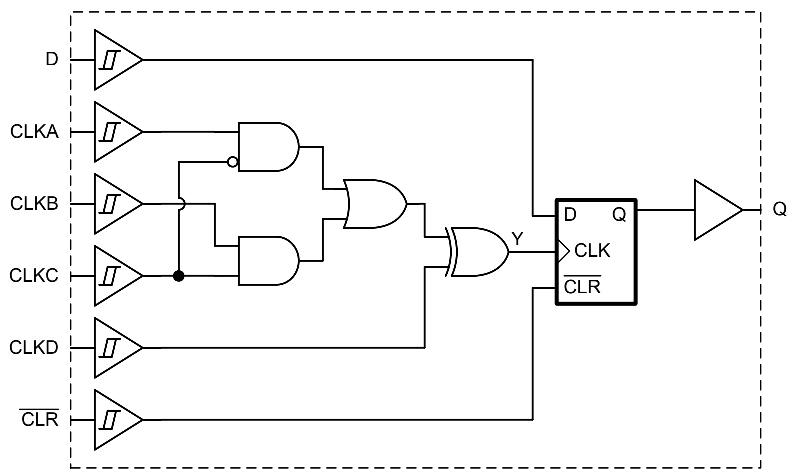
3 Description

The SN74ACT2G101 contains two independent D-type flip-flops with rising edge triggered configurable logic clock, active low clear, and data inputs. The clock inputs can be configured for many 1- and 2-input logic functions, including buffer, inverter, AND, OR, NAND, NOR, XOR, XNOR. All inputs have Schmitt-trigger architecture to support slow or noisy input signals..

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SN74ACT2G101	BQB (WQFN, 16)	3.6mm × 2.6mm	3.6mm × 2.6mm
	PW (TSSOP, 16)	6.4mm × 5mm	5mm × 4.4mm

(1) For more information, see *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable
(3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)

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4 Pin Configuration and Functions

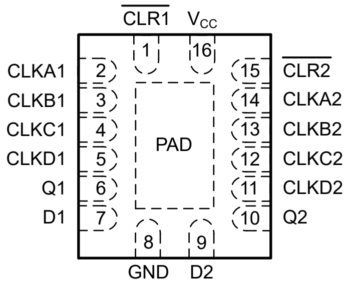


Figure 4-1. BQB Package, 16-Pin WQFN (Top View)

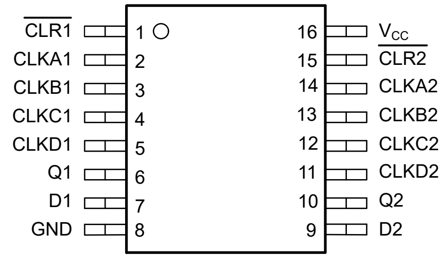


Figure 4-2. PW Package, 16-Pin TSSOP (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
$\overline{CLR1}$	1	I	Channel 1, clear, active low
CLKA1	2	I	Channel 1, clock input A
CLKB1	3	I	Channel 1, clock input B
CLKC1	4	I	Channel 1, clock input C
CLKD1	5	I	Channel 1, clock input D
Q1	6	O	Channel 1, non-inverted output
D1	7	I	Channel 1, data input
GND	8	G	Ground
D2	9	I	Channel 2, data input
Q2	10	O	Channel 2, non-inverted output
CLKD2	11	I	Channel 2, clock input D
CLKC2	12	I	Channel 2, clock input C
CLKB2	13	I	Channel 2, clock input B
CLKA2	14	I	Channel 2, clock input A
$\overline{CLR2}$	15	I	Channel 2, clear, active low
V_{CC}	16	P	Positive supply
Thermal Pad(2)		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.
(2) BQB package only

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	7	V
V_I	Input voltage range[(2)]		-0.5	V_{CC} + 0.5	V
V_O	Output voltage range[(2)]		-0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < -0.5V or V_I > V_{CC} + 0.5V		±20	mA
I_{OK}	Output clamp current	V_O < -0.5V or V_O > V_{CC} + 0.5V		±50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±50	mA
	Continuous output current through V_{CC} or GND			±200	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[(2)]	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_I	Input Voltage		0	V_{CC}	V
V_O	Output Voltage		0	V_{CC}	V
I_{OH}	High-level output current			–24	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature		–40	125	°C

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC[(1)]						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
PW (TSSOP)	16	140	80	90	30	90	N/A	°C/W
BQB (WQFN)	16	91.2	95.1	61.4	18.0	61.2	38.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{T+}	Positive-going input threshold voltage	4.5V	1.28	1.54	1.83	V
		5.5V	1.46	1.72	2.02	V
V_{T-}	Negative-going input threshold voltage	4.5V	0.65	0.91	1.2	V
		5.5V	0.71	0.99	1.29	V
ΔV_T	Hysteresis (V_{T+} - V_{T-})	4.5V	0.51		0.75	V
		5.5V	0.59		0.88	V
V_{OH}	I_{OH} = -50µA	4.5V	4.4	4.49		V
		5.5V	5.4	5.49		
	I_{OH} = -24mA	4.5V	3.7			
	I_{OH} = -24mA	5.5V	4.7			
	I_{OH} = -75mA(1)	5.5V	3.85			
V_{OL}	I_{OL} = 50µA	4.5V		0.01	0.1	V
		5.5V		0.01	0.1	
	I_{OL} = 24mA	4.5V			0.5	
	I_{OL} = 24mA	5.5V			0.5	
	I_{OL} = 75mA(1)	5.5V			1.65	
I_I	V_I = 5.5V or GND	0V to 5.5V			±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5V		0.1	2	µA
ΔI_{CC}	V_I = V_{CC} – 2.1V; Any Input	4.5V to 5.5V			1.5	mA
C_I	V_I = V_{CC} or GND	5V		2		pF

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 2ms

5.6 Timing Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V_{CC}	-40°C to 125°C		UNIT
				MIN	MAX	
f_{clock}	Clock frequency		5V ± 0.5V		120	MHz
t_W	Pulse duration	$\overline{CLR}$ low	5V ± 0.5V	4		ns
		CLKx	5V ± 0.5V	4		
t_{SU}	Set up time	D before any CLKx	5V ± 0.5V	5		ns
		$\overline{CLR}$ high before any CLKx	5V ± 0.5V	0		ns
t_{CLKX_SU}	Set up time between CLKx inputs	CLKA input pin relative to CLKB, CLKC and CLKD pins	5V ± 0.5V	8		ns
		CLKB input pin relative to CLKA, CLKC and CLKD pins	5V ± 0.5V	4		ns
		CLKC input pin relative to CLKA, CLKB and CLKD pins	5V ± 0.5V	4		ns
		CLKD input pin relative to CLKA, CLKB and CLKC pins	5V ± 0.5V	4		ns
t_H	Hold time	D before any CLKx	5V ± 0.5V	4		ns

5.7 Switching Characteristics

over operating free-air temperature range; C_L = 50pF typical values measured at T_A = 25°C (unless otherwise noted). See #i#Parameter Measurement Information

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	-40°C to 125°C			UNIT
				MIN	TYP	MAX	
t_{pd}	CLKA	Q	5V ± 0.5V			10.5	ns
	CLKB	Q	5V ± 0.5V			10.5	ns
	CLKC	Q	5V ± 0.5V			9.6	ns
	CLKD	Q	5V ± 0.5V			9.8	ns
	$\overline{CLR}$	Q	5V ± 0.5V			10.5	ns
$t_{sk(o)}$		Q	5V ± 0.5V			1	ns
C_{PD} (1)	CLK or CLK INH	Q_H	5V		15		pF

(1) Power dissipation capacitance measured with C_L = 50pF, F = 1MHz

5.8 Typical Characteristics

T_A = 25°C (unless otherwise noted)

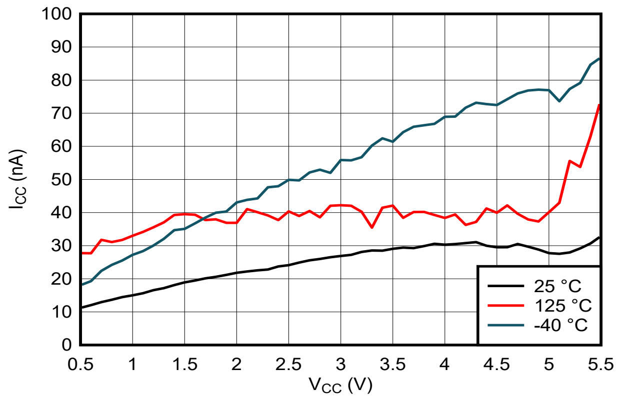


Figure 5-1. Supply Current Across Supply Voltage

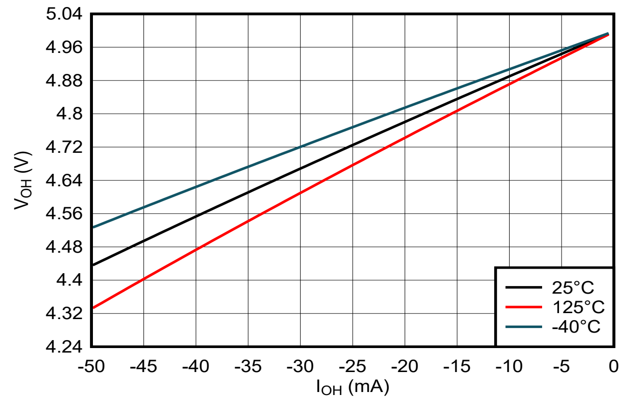


Figure 5-2. Output Voltage vs Current in HIGH State; 5V Supply

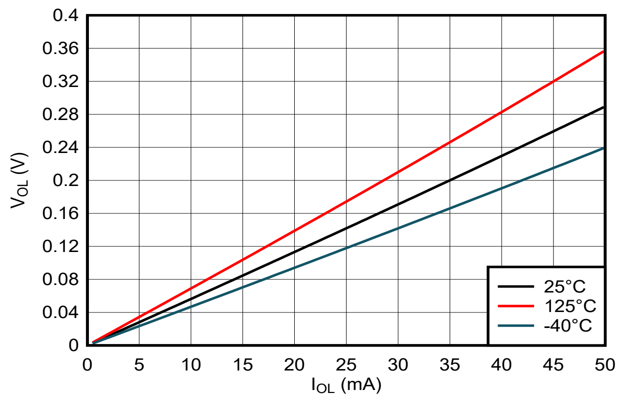


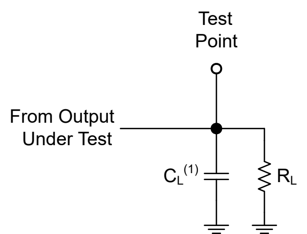
Figure 5-3. Output Voltage vs Current in LOW State; 5V Supply

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t < 2.5ns, V_t = 1.5V. For push-pull outputs, R_L = 500Ω.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured individually with one input transition per measurement.



(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs

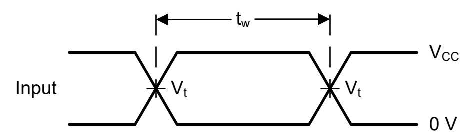


Figure 6-2. Voltage Waveforms, Pulse Duration

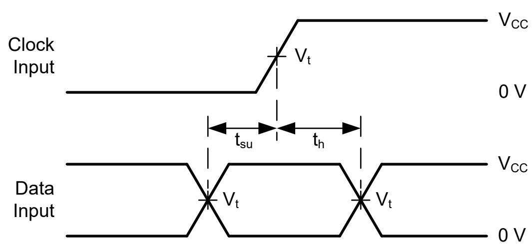
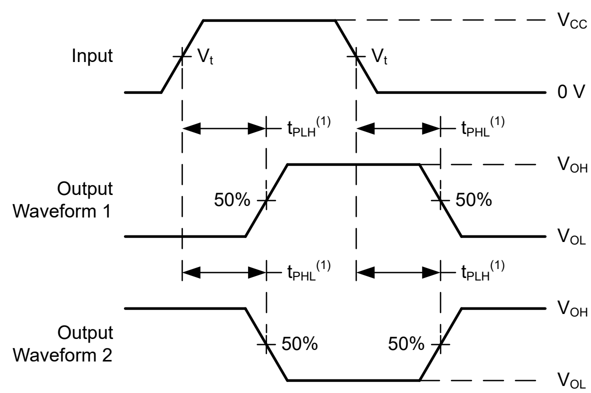
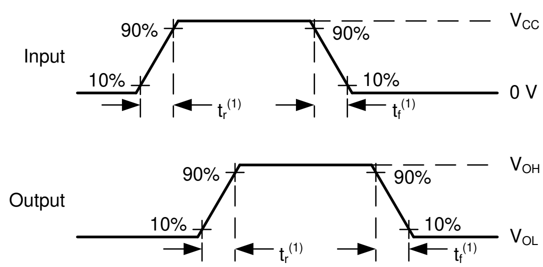


Figure 6-3. Voltage Waveforms, Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-4. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-5. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

The SN74ACT2G101 contains two independent D-type flip-flops. Each channel has separate data (D) and asynchronous active-low clear ($\overline{CLR}$) inputs, output (Q), as well as configurable clock inputs (CLKA, CLKB, CLKC, CLKD). The clock inputs utilize combinational logic to provide a variety of possible logic combinations, including common 2-input gates as well as inverted and non-inverted configurations.

7.2 Functional Block Diagram

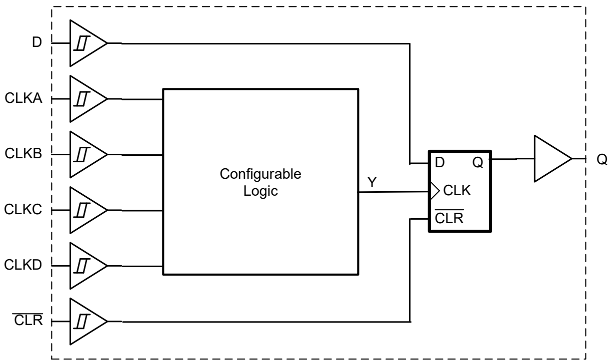


Figure 7-1. Each channel

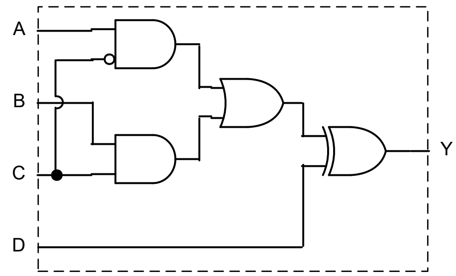


Figure 7-2. Configurable logic

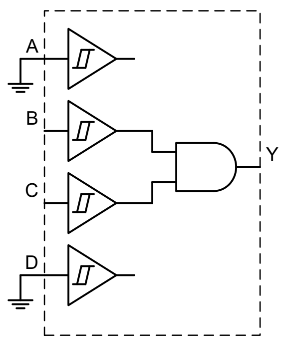


Figure 7-3. 2-input AND configuration

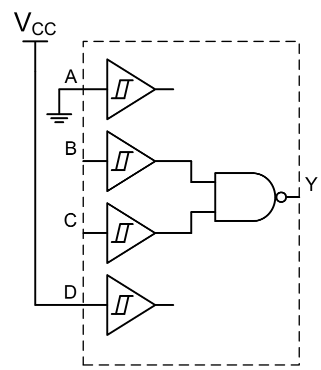


Figure 7-4. 2-input NAND configuration

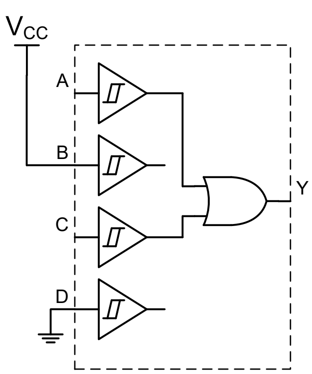


Figure 7-5. 2-input OR configuration

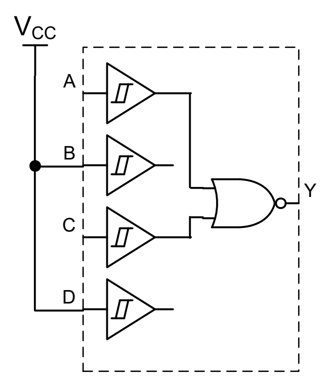


Figure 7-6. 2-input NOR configuration

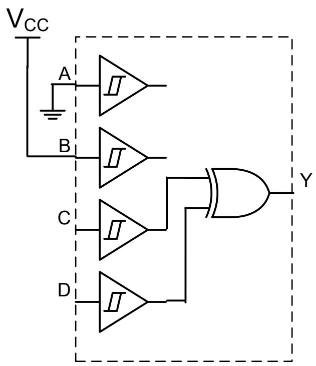


Figure 7-7. 2-input XOR configuration

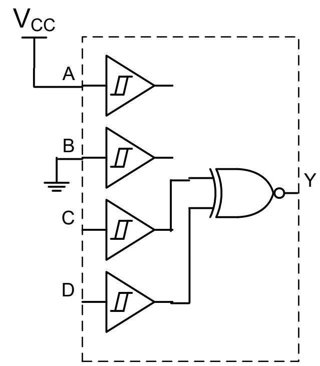


Figure 7-8. 2-input XNOR configuration

7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

7.3.2 TTL-Compatible Schmitt-Trigger CMOS Inputs

This device includes TTL-compatible CMOS inputs with Schmitt-trigger architecture. These inputs are specifically designed to interface with TTL logic devices by having reduced input voltage thresholds.

TTL-compatible Schmitt-trigger CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see Understanding Schmitt Triggers.

Do not leave TTL-compatible CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors, however a 10kΩ resistor is recommended and will typically meet all requirements.

7.3.3 Clamp Diode Structure

As shown in Figure 7-9, the inputs and outputs to this device have both positive and negative clamping diodes.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

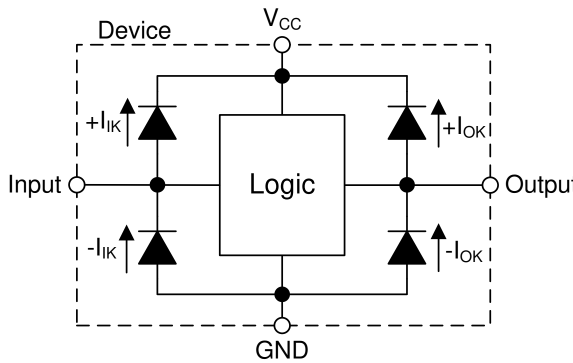


Figure 7-9. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1. Flip-Flop Function Table

INPUTS[(1)]			OUTPUT[(2)]
$\overline{CLR}$	CLK[(3)]	D	Q
L	X	X	L
H	L, H, ↓	X	Q0
H	↑	L	L
H	↑	H	H

(1) L = Input low, H = Input high, ↑ = Input transitioning from low to high, ↓ = Input transitioning from high to low, X = Don't care
(2) L = Output low, H = Output high, Q_0 = Previous state
(3) Internal flip-flop input, denoted as Y on functional block diagram

Table 7-2. Combinational Logic Function Table

INPUTS				OUTPUT
A	B	C	D	Y
L	L	L	L	L
L	L	L	H	H
L	L	H	L	L
L	L	H	H	H
L	H	L	L	L
L	H	L	H	H
L	H	H	L	H
L	H	H	H	L
H	L	L	L	H
H	L	L	H	L
H	L	H	L	L
H	L	H	H	H
H	H	L	L	H
H	H	L	H	L
H	H	H	L	H
H	H	H	H	L

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, the SN74ACT2G101 is used to read in two different active-high fault signals (FAULT1, FAULT2) and latch an output signal (LATCHED FAULT) high when the boolean logic FAULT1 OR FAULT2 has a rising edge.

At power-up, the initial state of the flip-flop is unknown. To give it a defined state of zero, the device can be cleared by applying a low signal to the clear ($\overline{CLR}$) input.

8.2 Typical Application

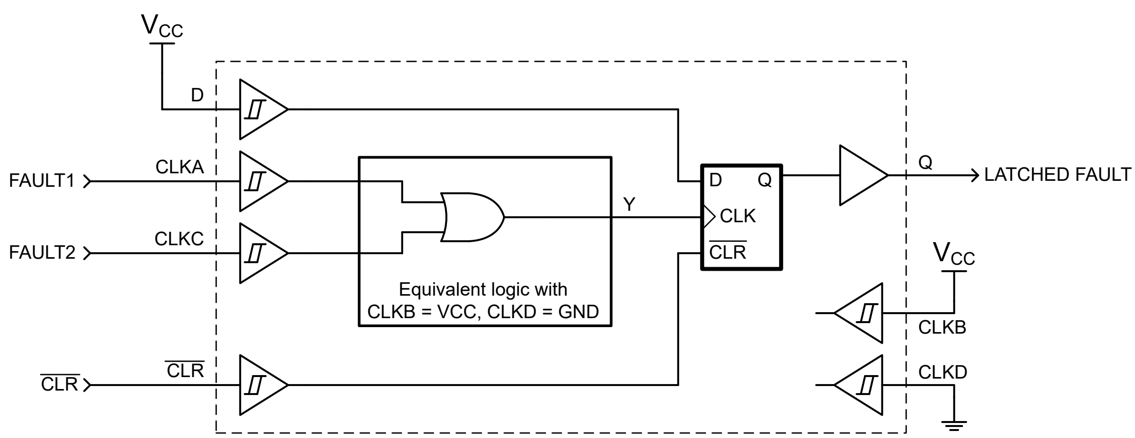


Figure 8-1. Typical Application Block Diagram

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Electrical Characteristics*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74ACT2G101 plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74ACT2G101 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74ACT2G101 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74ACT2G101 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption and Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross to be considered a logic LOW, and to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74ACT2G101 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74ACT2G101 to one or more of the receiving devices.
3. Verify that the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$)Ω. Doing this prevents the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the *CMOS Power Consumption and Cpd Calculation* application note.

8.2.3 Reference

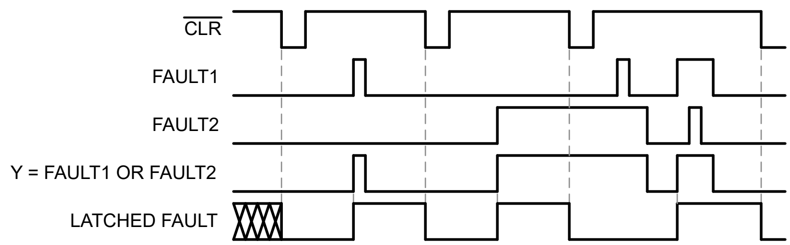


Figure 8-2. Application Timing Diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance.

A 0.1μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1μF and 1μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - Parallel traces must be separated by at least 3x dielectric thickness
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer each signal that must branch separately

8.4.2 Layout Example

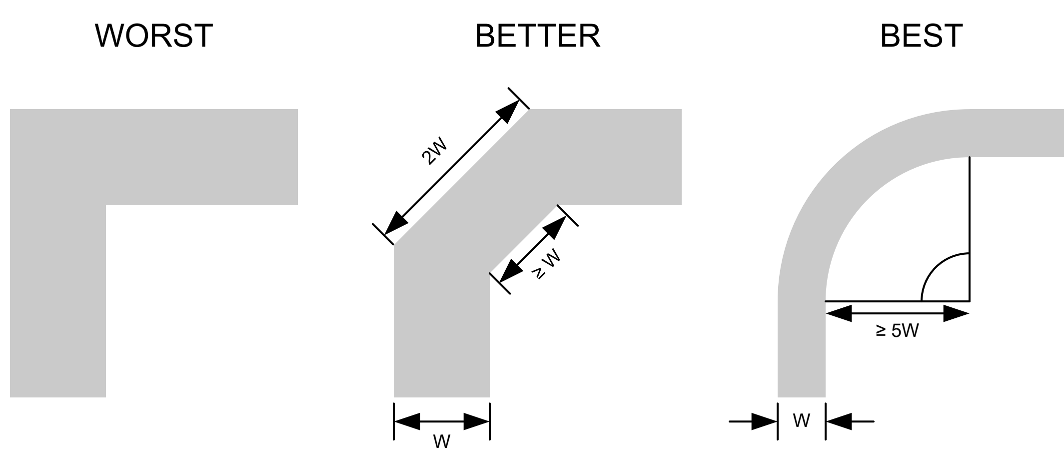


Figure 8-3. Example Trace Corners for Improved Signal Integrity

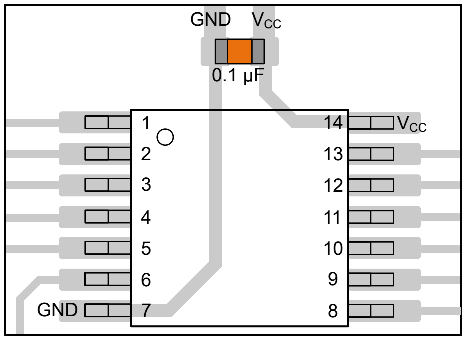


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

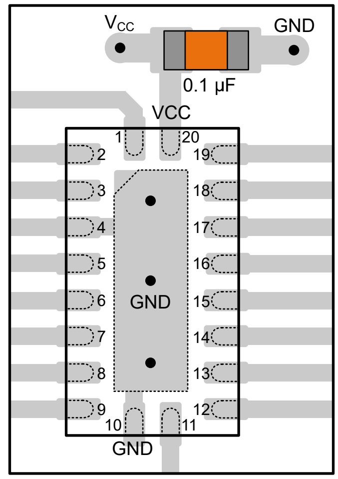


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

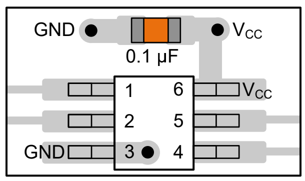


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

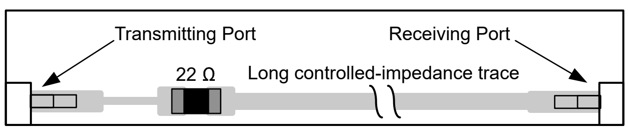


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ACT2G101BQBR	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	ACT101
SN74ACT2G101PWR	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	ACT101

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74ACT2G101 :

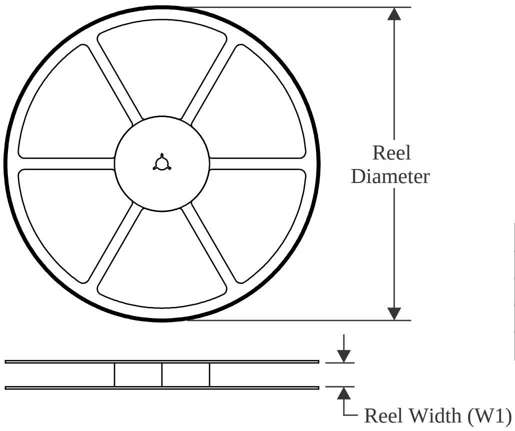
- Automotive : SN74ACT2G101-Q1

NOTE: Qualified Version Definitions:

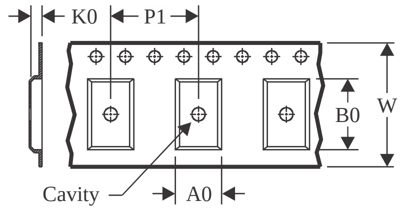
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

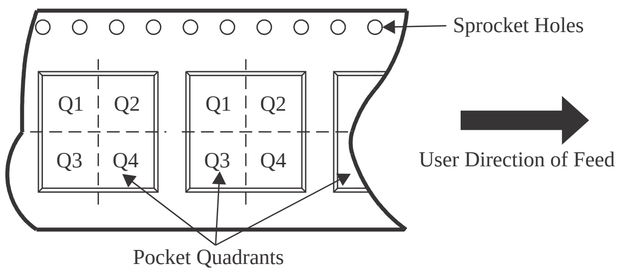


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

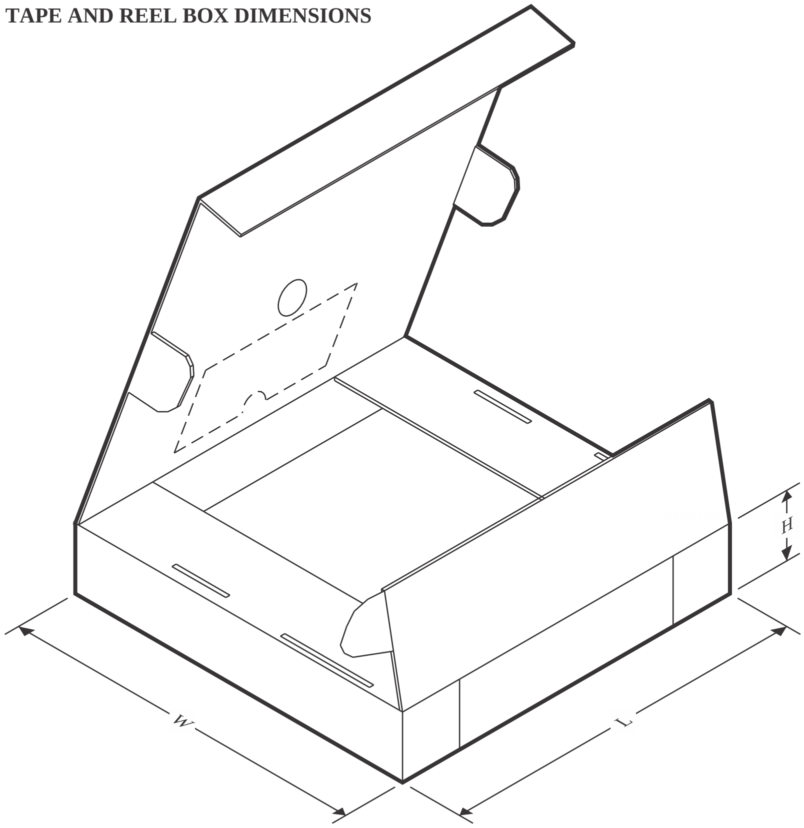
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT2G101BQBR	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
SN74ACT2G101PWR	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT2G101BQBR	WQFN	BQB	16	3000	210.0	185.0	35.0
SN74ACT2G101PWR	TSSOP	PW	16	3000	353.0	353.0	32.0

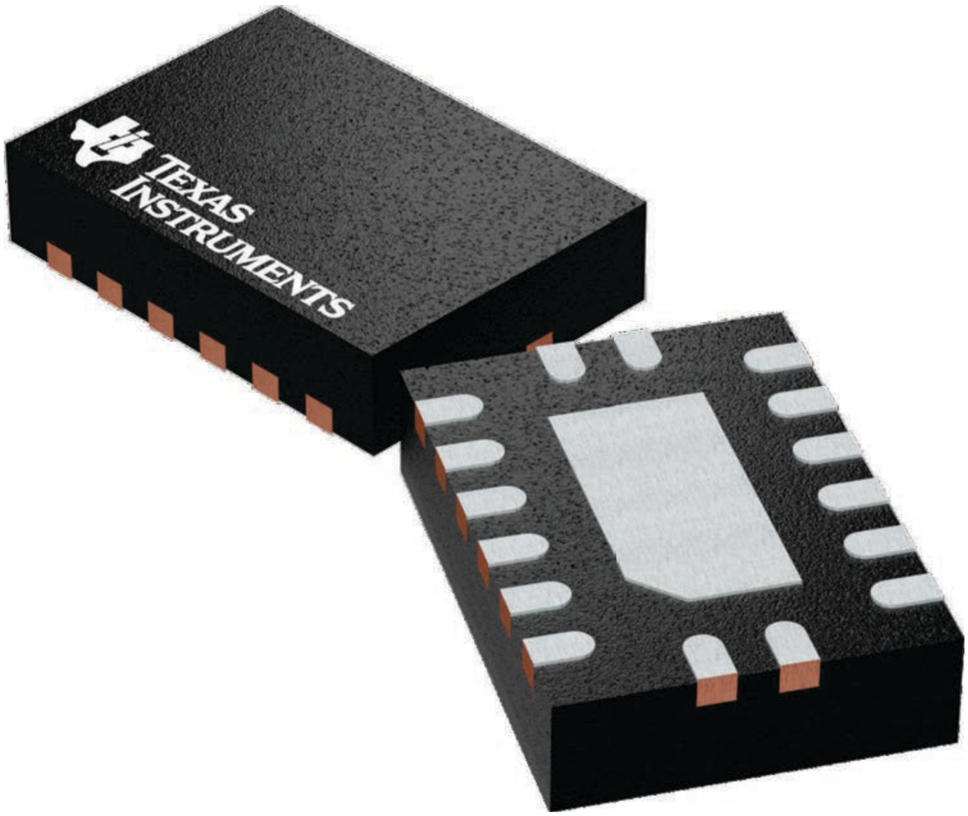
BQB 16

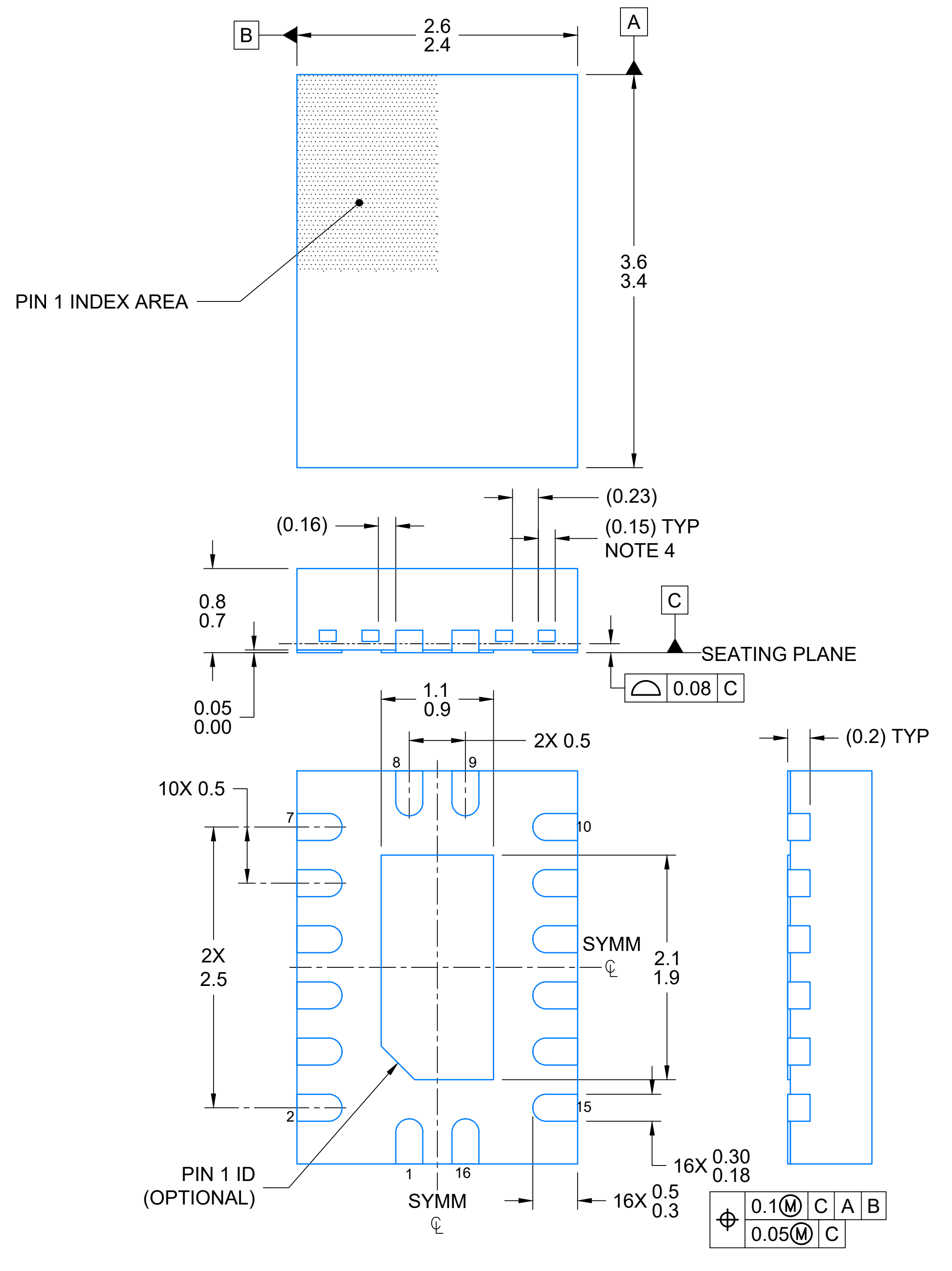
WQFN - 0.8 mm max height

2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

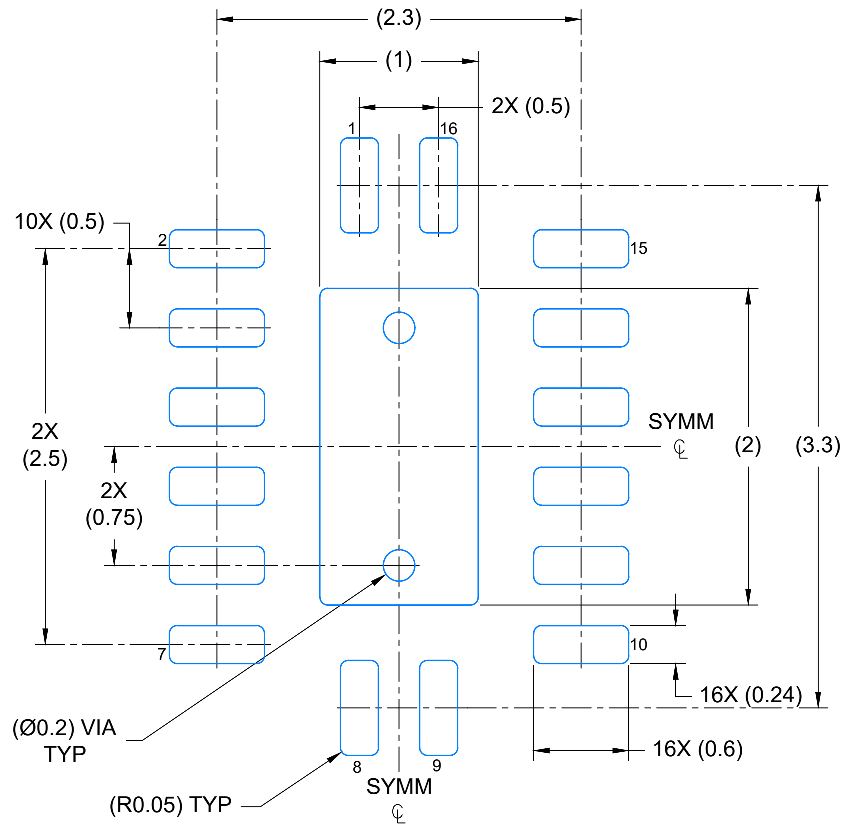




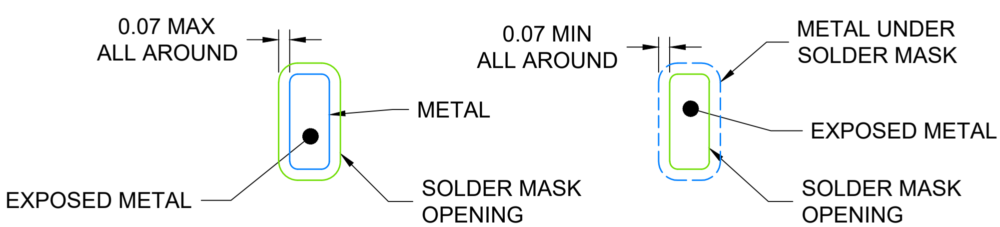
4224640/B 01/2026

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may differ or may not be present



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON-SOLDER MASK
DEFINED
(PREFERRED)

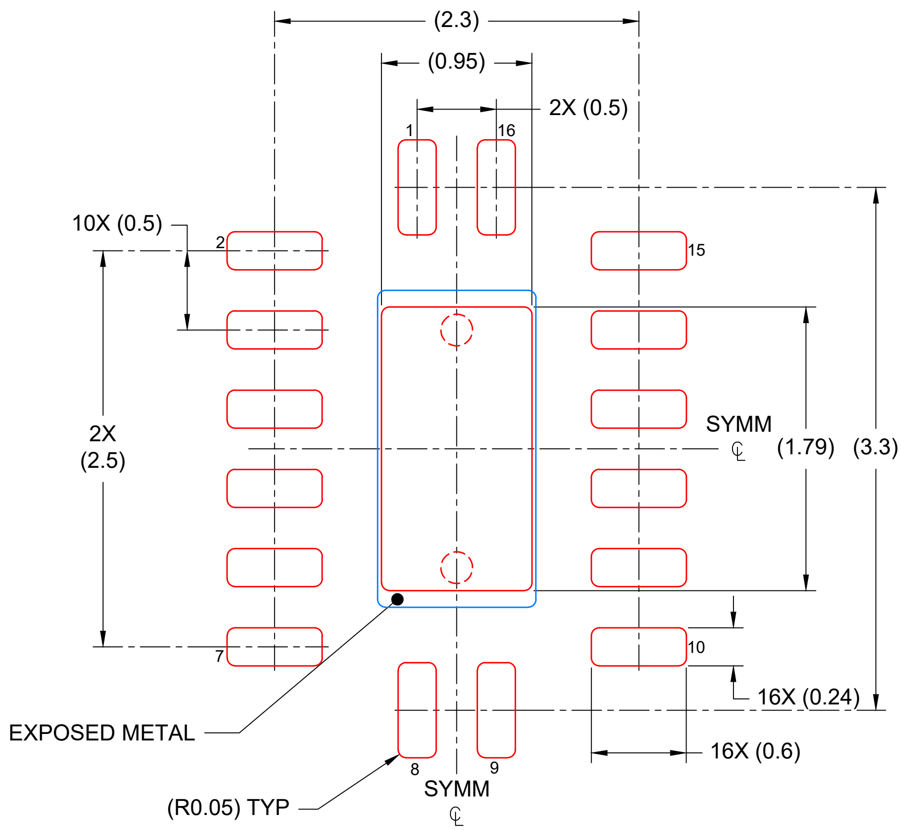
SOLDER MASK
DEFINED

4224640/B 01/2026

1. NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



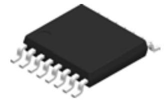
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

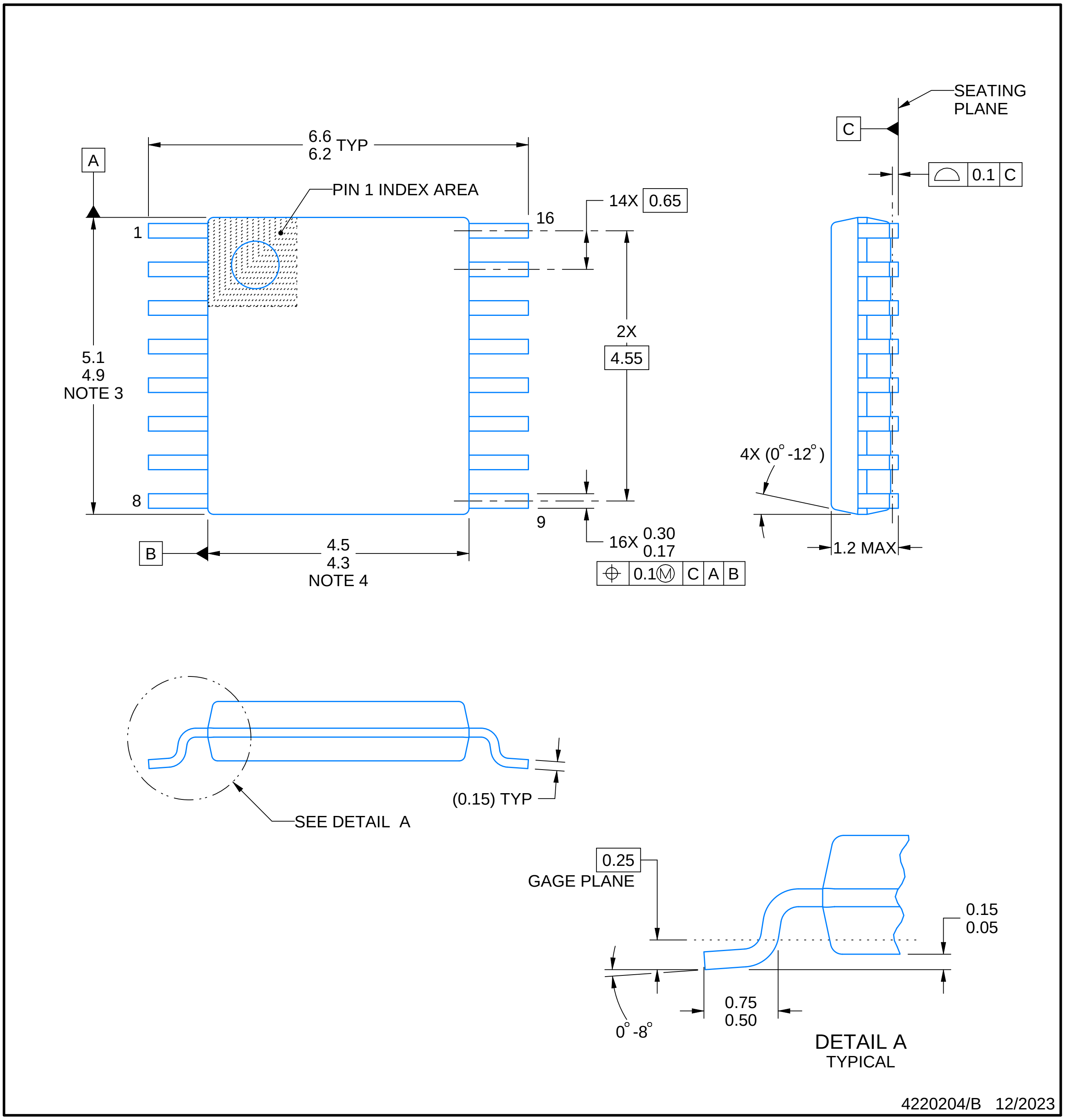
EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4224640/B 01/2026

NOTES: (continued)

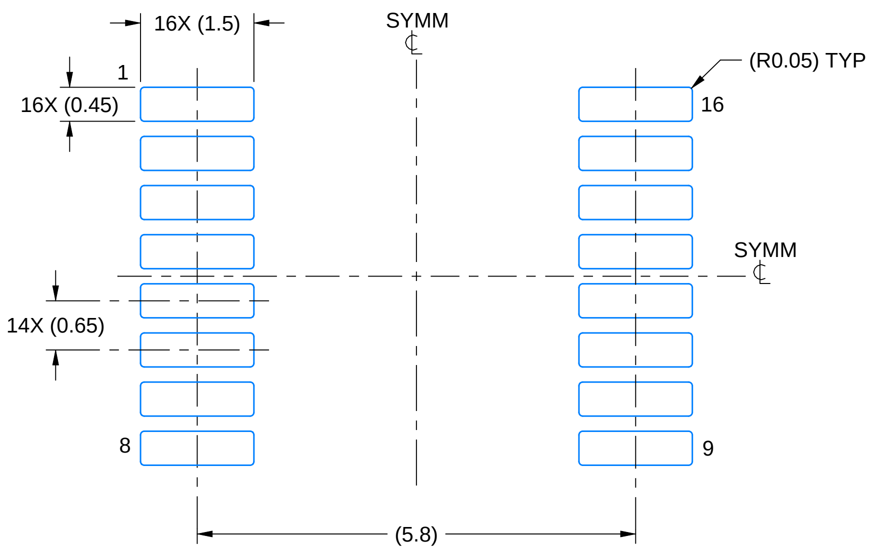
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



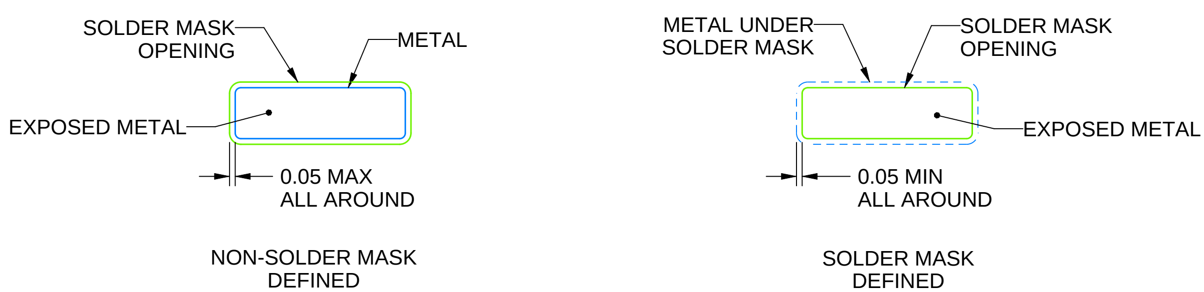


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

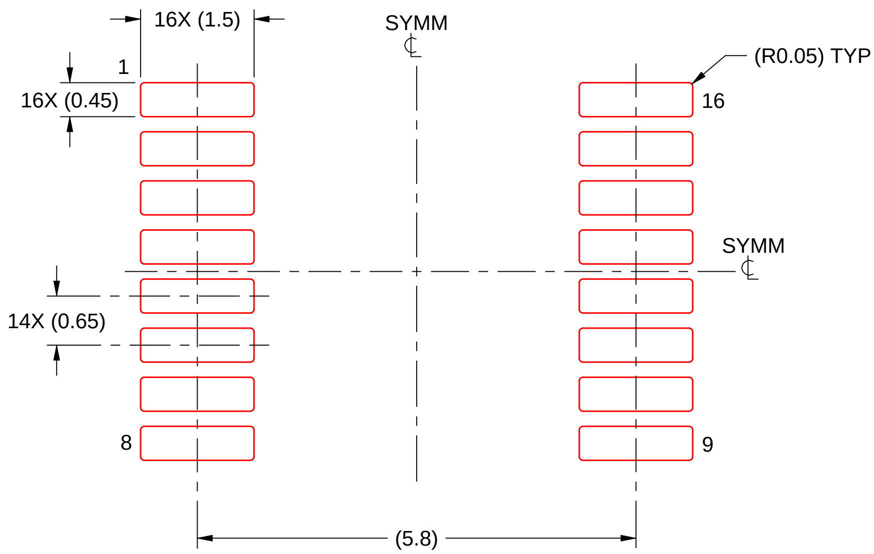


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.