

SN74AHC1G04 Single Inverter Gate

1 Features

- Operating range 2 V to 5.5 V
- Max t_{pd} of 6.5 ns at 5 V
- Low power consumption, 10- μ A max I_{CC}
- ± 8 -mA output drive at 5 V
- Schmitt-trigger action at all inputs makes the circuit tolerant for slower input rise and fall time
- Latch-up performance exceeds 250 mA per JESD 17

2 Applications

- Cameras
- E-Meters
- Ethernet Switches
- Infotainment

3 Description

The SN74AHC1G04 contains one inverter gate. The device performs the Boolean function $Y = \bar{A}$.

Package Information

| PART NUMBER | PACKAGE ⁽¹⁾ | PACKAGE SIZE ⁽²⁾ | BODY SIZE ⁽³⁾ |
|-------------|------------------------|-----------------------------|--------------------------|
| SN74AHC1G04 | DBV (SOT-23, 5) | 2.8 mm × 2.8 mm | 2.9 mm × 1.6 mm |
| | DCK (SC-70, 5) | 2.00 mm × 1.25 mm | 2 mm × 1.25 mm |
| | DRL (SOT-553, 5) | 1.6 mm × 1.6 mm | 1.6 mm × 1.2 mm |

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



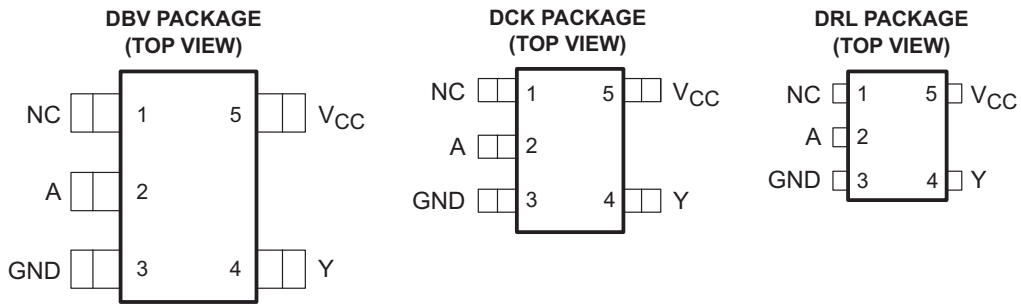
Simplified Schematic



Table of Contents

| | | | |
|---|---|--|----|
| 1 Features | 1 | 7.3 Feature Description..... | 8 |
| 2 Applications | 1 | 7.4 Device Functional Modes..... | 8 |
| 3 Description | 1 | 8 Application and Implementation | 9 |
| 4 Pin Configuration and Functions | 3 | 8.1 Application Information..... | 9 |
| 5 Specifications | 4 | 8.2 Typical Application..... | 9 |
| 5.1 Absolute Maximum Ratings..... | 4 | 8.3 Power Supply Recommendations..... | 10 |
| 5.2 ESD Ratings..... | 4 | 8.4 Layout..... | 10 |
| 5.3 Recommended Operating Conditions..... | 4 | 9 Device and Documentation Support | 11 |
| 5.4 Thermal Information..... | 5 | 9.1 Documentation Support (Analog)..... | 11 |
| 5.5 Electrical Characteristics..... | 5 | 9.2 Receiving Notification of Documentation Updates.... | 11 |
| 5.6 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 6 | 9.3 Support Resources..... | 11 |
| 5.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ | 6 | 9.4 Trademarks..... | 11 |
| 5.8 Operating Characteristics..... | 6 | 9.5 Electrostatic Discharge Caution..... | 11 |
| 5.9 Typical Characteristics..... | 6 | 9.6 Glossary..... | 11 |
| 6 Parameter Measurement Information | 7 | 10 Revision History | 11 |
| 7 Detailed Description | 8 | 11 Mechanical, Packaging, and Orderable Information | 12 |
| 7.1 Overview..... | 8 | | |
| 7.2 Functional Block Diagram..... | 8 | | |

4 Pin Configuration and Functions



NC – No internal connection

See mechanical drawings for dimensions.

Table 4-1. Pin Functions

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|-----|-----------------|---------------------|---------------|
| NO. | NAME | | |
| 1 | NC | — | No Connection |
| 2 | A | I | Input A |
| 3 | GND | — | Ground Pin |
| 4 | Y | O | Output Y |
| 5 | V _{CC} | — | Power Pin |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------|--|--|-----------------------|--------|
| V _{CC} | Supply voltage range | -0.5 | 7 | V |
| V _I | Input voltage range ⁽²⁾ | -0.5 | 7 | V |
| V _O | Output voltage range ⁽²⁾ | -0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Input clamp current | V _I < 0 | | -20 mA |
| I _{OK} | Output clamp current | V _O < 0 or V _O > V _{CC} | | ±20 mA |
| I _O | Continuous output current | V _O = 0 to V _{CC} | | ±25 mA |
| | Continuous current through each V _{CC} or GND | | | ±50 mA |
| T _{stg} | Storage temperature range | -65 | 150 | °C |
| T _J | Junction temperature | | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Section 5.3](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|--|-------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | ±3500 |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | ±1000 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|-----------------|------------------------------------|---------------------------------|-----------------|------|
| V _{CC} | Supply voltage | 2 | 5.5 | V |
| V _{IH} | High-level input voltage | V _{CC} = 2 V | 1.5 | V |
| | | V _{CC} = 3 V | 2.1 | |
| | | V _{CC} = 5.5 V | 3.85 | |
| V _{IL} | Low-level input voltage | V _{CC} = 2 V | 0.5 | V |
| | | V _{CC} = 3 V | 0.9 | |
| | | V _{CC} = 5.5 V | 1.65 | |
| V _{IH} | Input voltage | 0 | 5.5 | V |
| V _O | Output voltage | 0 | V _{CC} | V |
| I _{OH} | High-level output current | V _{CC} = 2 V | -50 | μA |
| | | V _{CC} = 3.3 V ± 0.3 V | -4 | mA |
| | | V _{CC} = 5 V ± 0.5 V | -8 | |
| I _{OL} | Low-level output current | V _{CC} = 2 V | 50 | μA |
| | | V _{CC} = 3.3 V ± 0.3 V | 4 | mA |
| | | V _{CC} = 5 V ± 0.5 V | 8 | |
| Δt/Δv | Input transition rise or fall rate | V _{CC} = 3.3 V ± 0.3 V | 100 | ns/V |
| | | V _{CC} = 5 V ± 0.5 V | 20 | |
| T _A | Operating free-air temperature | -40 | 125 | °C |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

5.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | SN74AHC1G04 | | | UNIT |
|-------------------------------|--|-------------|-------|-------|------|
| | | DBV | DCK | DRL | |
| | | 5 PINS | | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 278 | 289.2 | 328.7 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 180.5 | 205.8 | 105.1 | |
| R _{θJB} | Junction-to-board thermal resistance | 184.4 | 176.2 | 150.3 | |
| ψ _{JT} | Junction-to-top characterization parameter | 115.4 | 117.6 | 6.9 | |
| ψ _{JB} | Junction-to-board characterization parameter | 183.4 | 175.1 | 148.4 | |
| R _{θJC(bot)} | Junction-to-case (bot) thermal resistance | N/A | N/A | N/A | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | –40°C to 85°C | | –40°C to 125°C | | UNIT | |
|-----------------|---------------------------|---|-----------------------|-----|-----|---------------|-----|----------------|-----|-------|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | | |
| V _{OH} | High level output voltage | I _{OH} = –50 μA | 2 V | 1.9 | 2 | 1.9 | | 1.9 | | V | |
| | | | 3 V | 2.9 | 3 | 2.9 | | 2.9 | | | |
| | | | 4.5 V | 4.4 | 4.5 | 4.4 | | 4.4 | | | |
| | I _{OH} = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | | |
| | | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | | |
| V _{OL} | Low level output voltage | I _{OH} = 50 μA | 2 V | 0.1 | | | 0.1 | | 0.1 | | V |
| | | | 3 V | 0.1 | | | 0.1 | | 0.1 | | |
| | | | 4.5 V | 0.1 | | | 0.1 | | 0.1 | | |
| | I _{OL} = 4 mA | 3 V | 0.36 | | | 0.44 | | 0.44 | | | |
| | | 4.5 V | 0.36 | | | 0.44 | | 0.44 | | | |
| I _I | Input leakage current | V _I = 5.5 V or GND | 0 V to 5.5 V | | | ±0.1 | | ±1 | | μA | |
| I _{CC} | Supply current | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | 1 | | 10 | | 10 μA | |
| C _i | Input Capacitance V | V _I = V _{CC} or GND | 5 V | | | 2 | | 10 | | 10 pF | |

5.6 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit And Voltage Waveforms](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | OUTPUT CAPACITANCE | $T_A = 25^\circ\text{C}$ | | | $-40^\circ\text{C to } 85^\circ\text{C}$ | | $-40^\circ\text{C to } 125^\circ\text{C}$ | | UNIT |
|-----------|--------------|-------------|----------------------|--------------------------|------|-----|--|-----|---|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{PLH} | A | Y | $C_L = 15\text{ pF}$ | 5 | 7.1 | | 1 | 8.5 | 1 | 9.5 | ns |
| t_{PHL} | | | | 5 | 7.1 | 1 | 8.5 | 1 | 9.5 | | |
| t_{PLH} | A | Y | $C_L = 50\text{ pF}$ | 7.5 | 10.6 | | 1 | 12 | 1 | 13 | ns |
| t_{PHL} | | | | 7.5 | 10.6 | 1 | 12 | 1 | 13 | | |

5.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit And Voltage Waveforms](#))

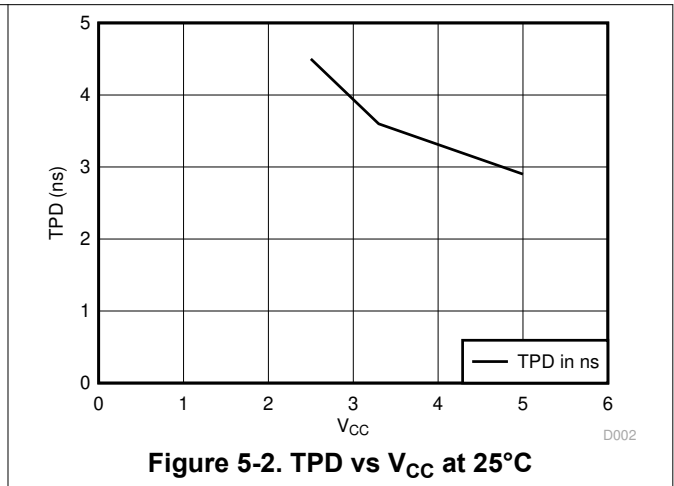
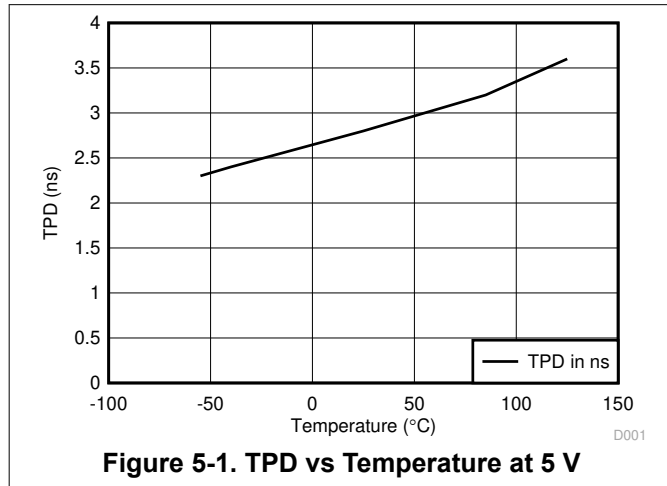
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | OUTPUT CAPACITANCE | $T_A = 25^\circ\text{C}$ | | | $-40^\circ\text{C to } 85^\circ\text{C}$ | | $-40^\circ\text{C to } 125^\circ\text{C}$ | | UNIT |
|-----------|--------------|-------------|----------------------|--------------------------|-----|-----|--|-----|---|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{PLH} | A | Y | $C_L = 15\text{ pF}$ | 3.8 | 5.5 | | 1 | 6.5 | 1 | 7 | ns |
| t_{PHL} | | | | 3.8 | 5.5 | 1 | 6.5 | 1 | 7 | | |
| t_{PLH} | A | Y | $C_L = 50\text{ pF}$ | 5.3 | 7.5 | | 1 | 6.5 | 1 | 7 | ns |
| t_{PHL} | | | | 5.3 | 7.5 | 1 | 6.5 | 1 | 7 | | |

5.8 Operating Characteristics

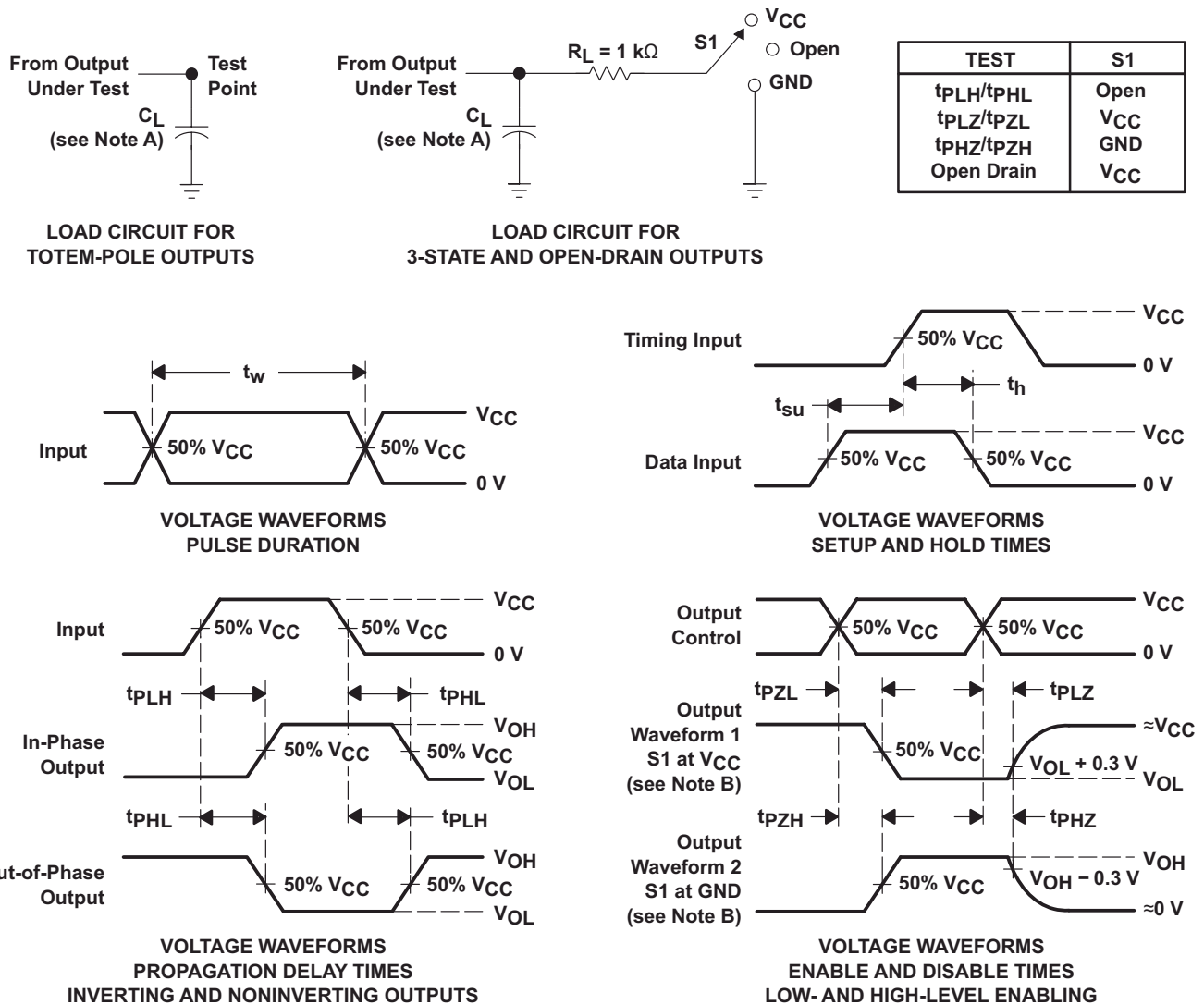
$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|--|-----------------------------|-----|------|
| C_{pd} Power dissipation capacitance | No load, $f = 1\text{ MHz}$ | 12 | pF |

5.9 Typical Characteristics



6 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit And Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74AHC1G04 device contains one inverter gate. The device performs the Boolean function $Y = \bar{A}$.

This single gate inverter has Schmitt-Trigger action on its input, allowing for slower rise and fall times and some noise rejection. This is not a true Schmitt-Trigger, so there is a limit on rise and fall times.

7.2 Functional Block Diagram



Figure 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

- Wide operating voltage range
 - Operates from 2 V to 5.5 V
- Allows down-voltage translation
 - Inputs accept voltages to 5.5 V
- Lower drive
 - This will produce slower edges and help prevent ringing on outputs

7.4 Device Functional Modes

Table 7-1. Function Table

| INPUT ⁽¹⁾ A | OUTPUT ⁽²⁾ Y |
|---------------------------|----------------------------|
| H | L |
| L | H |

- (1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care
- (2) H = Driving High, L = Driving Low, Z = High Impedance State

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

SN74AHC1G04 is a low-drive CMOS device that can be used for a multitude of inverting buffer type functions. It can produce 8 mA of drive current at 5 V, making it ideal for driving multiple outputs and good for low-noise applications. The inputs are 5.5-V tolerant, allowing it to translate down to V_{CC} .

8.2 Typical Application

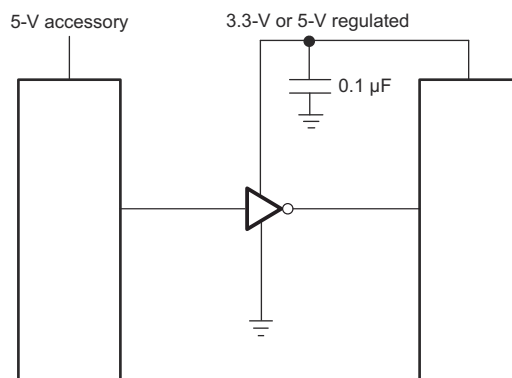


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

- Recommended Input Conditions
 - For rise time and fall time specifications, see $\Delta t/\Delta V$ in the [Section 5.3](#) table.
 - For specified High and low levels, see V_{IH} and V_{IL} in the [Section 5.3](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
- Recommend Output Conditions
 - Load currents should not exceed 25 mA per output and 50 mA total for the part.
 - Outputs should not be pulled above V_{CC} .

8.2.3 Application Curves

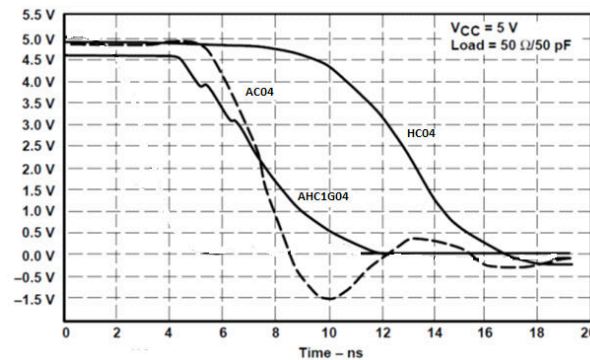


Figure 8-2. Typical Application Curve

8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Section 5.3](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple V_{CC} pins, 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 8-3](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

8.4.2 Layout Example

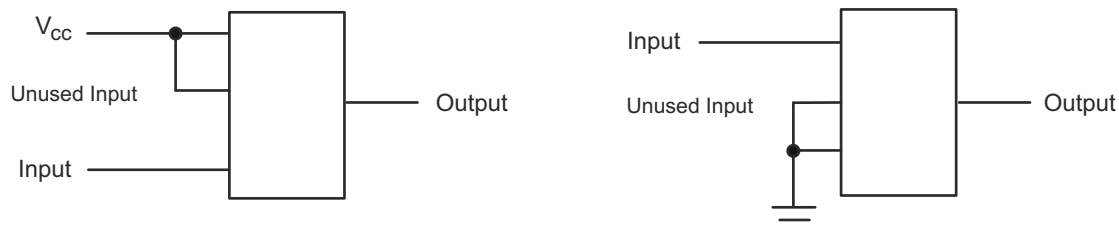


Figure 8-3. Layout Diagram

9 Device and Documentation Support

9.1 Documentation Support (Analog)

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and Cpd Calculation application note](#)
- Texas Instruments, [Designing With Logic application note](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#)
- Texas Instruments, [Implications of Slow or Floating CMOS Inputs application note](#)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

| Changes from Revision U (October 2023) to Revision V (February 2024) | Page |
|--|------|
| • Updated thermal values for DBV package from RθJA = 231.3 to 278, RθJC(top) = 119.9 to 180.5, RθJB = 60.6 to 184.4, ΨJT = 17.8 to 115.4, ΨJB = 60.1 to 183.4, RθJC(bot) = N/A, all values in °C/W | 5 |

| Changes from Revision T (January 2016) to Revision U (October 2023) | Page |
|--|------|
| • Updated the numbering format for tables, figures, and cross-references throughout the document..... | 1 |
| • Updated thermal values for DCK package from RθJA = 287.6 to 289.2, RθJC(top) = 97.7 to 205.8, RθJB = 65 to 176.2, ΨJT = 2 to 117.6, ΨJB = 64.2 to 175.1, RθJC(bot) = N/A, all values in °C/W | 5 |

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|--|
| SN74AHC1G04DBVR | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (38CH, 3BUF, A043, A04G, A04J, A04L, A04S) |
| SN74AHC1G04DBVR.A | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (38CH, 3BUF, A043, A04G, A04J, A04L, A04S) |
| SN74AHC1G04DBVRE4 | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | A04G |
| SN74AHC1G04DBVRG4 | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | A04G |
| SN74AHC1G04DBVRG4.A | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | A04G |
| SN74AHC1G04DBVT | Obsolete | Production | SOT-23 (DBV) 5 | - | - | Call TI | Call TI | -40 to 125 | (A043, A04G, A04J, A04S) |
| SN74AHC1G04DBVTG4 | Active | Production | SOT-23 (DBV) 5 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | A04G |
| SN74AHC1G04DBVTG4.A | Active | Production | SOT-23 (DBV) 5 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | A04G |
| SN74AHC1G04DCK3 | Obsolete | Production | SC70 (DCK) 5 | - | - | Call TI | Call TI | -40 to 85 | ACY |
| SN74AHC1G04DCKR | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (1R6, AC3, ACG, ACJ, ACL, ACS) |
| SN74AHC1G04DCKR.A | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (1R6, AC3, ACG, ACJ, ACL, ACS) |
| SN74AHC1G04DCKRE4 | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AC3 |
| SN74AHC1G04DCKRG4 | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AC3 |
| SN74AHC1G04DCKRG4.A | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AC3 |
| SN74AHC1G04DCKT | Obsolete | Production | SC70 (DCK) 5 | - | - | Call TI | Call TI | -40 to 125 | (AC3, ACG, ACJ, ACS) |
| SN74AHC1G04DCKTG4 | Active | Production | SC70 (DCK) 5 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AC3 |
| SN74AHC1G04DCKTG4.A | Active | Production | SC70 (DCK) 5 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AC3 |
| SN74AHC1G04DRLR | Active | Production | SOT-5X3 (DRL) 5 | 4000 LARGE T&R | Yes | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | (ACB, ACS) |
| SN74AHC1G04DRLR.A | Active | Production | SOT-5X3 (DRL) 5 | 4000 LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | (ACB, ACS) |
| SN74AHC1G04DRLRG4 | Active | Production | SOT-5X3 (DRL) 5 | 4000 LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | (ACB, ACS) |

⁽¹⁾ Status: For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AHC1G04 :

- Automotive : [SN74AHC1G04-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AHC1G04DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74AHC1G04DBVRG4 | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AHC1G04DBVTG4 | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AHC1G04DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.3 | 2.55 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74AHC1G04DCKRG4 | SC70 | DCK | 5 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74AHC1G04DCKTG4 | SC70 | DCK | 5 | 250 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74AHC1G04DRLR | SOT-5X3 | DRL | 5 | 4000 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AHC1G04DBVR | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| SN74AHC1G04DBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AHC1G04DBVTG4 | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74AHC1G04DCKR | SC70 | DCK | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74AHC1G04DCKRG4 | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AHC1G04DCKTG4 | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74AHC1G04DRLR | SOT-5X3 | DRL | 5 | 4000 | 202.0 | 201.0 | 28.0 |

EXAMPLE BOARD LAYOUT

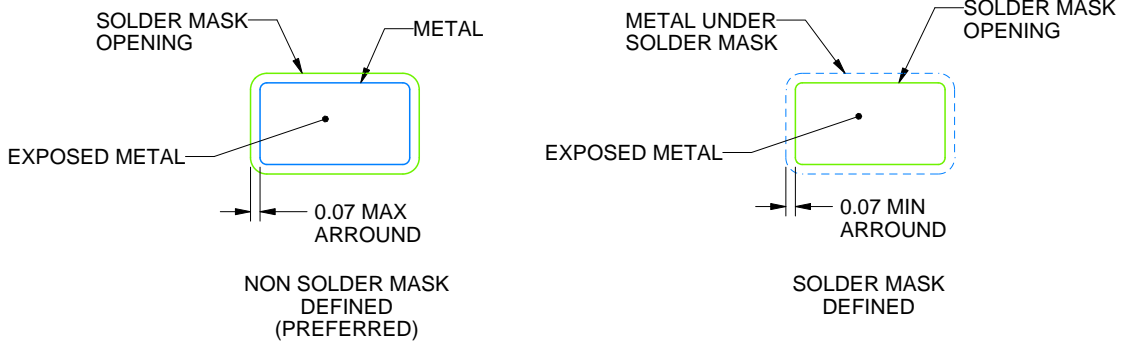
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

EXAMPLE BOARD LAYOUT

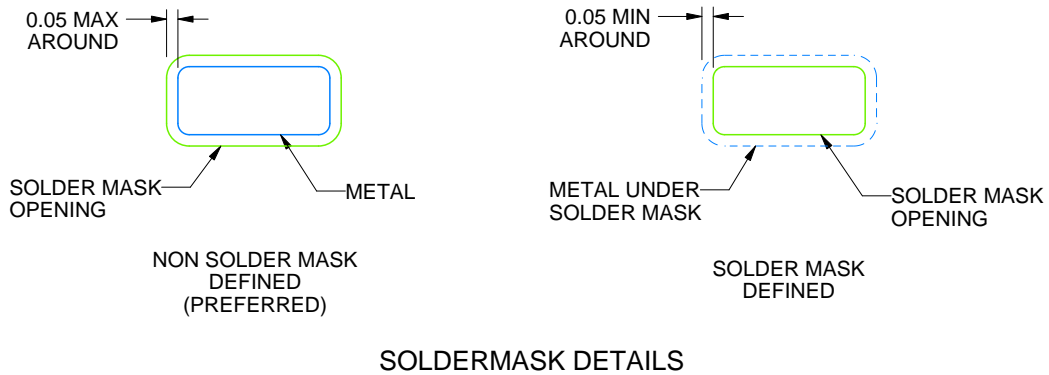
DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

EXAMPLE BOARD LAYOUT

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025