

# SNx4AHC574 Octal Edge-Triggered D-Type Flip-Flops With 3-State Outputs

## 1 Features

- Operating range 2V to 5.5V  $V_{CC}$
- 3-state outputs drive bus lines directly
- Latch-up performance exceeds 250mA per JESD 17
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.
- ESD Protection Exceeds JESD 22
  - 2000V human-body model
  - 1000V charged-device model

## 2 Applications

- Smart Grids
- TVs
- Set Top Boxes
- Audio
- Servers
- Surveillance Cameras
- Network Switches
- Infotainment

## 3 Description

The SNx4AHC574 devices are octal edge-triggered D-type flip-flops that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

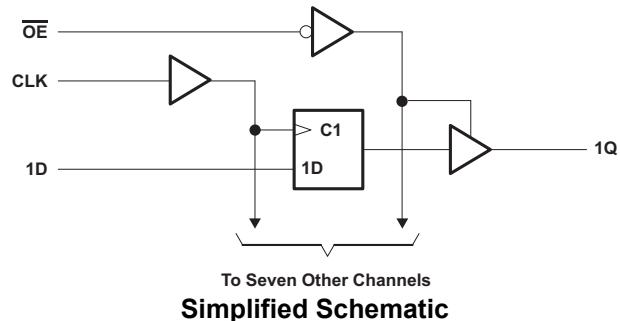
### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>	BODY SIZE <sup>(3)</sup>
SNx4AHC574	DB (SSOP, 20)	7.2mm x 7.8mm	7.50mm x 5.30mm
	DGV (TSSOP, 20)	5.00mm x 6.4mm	5.00mm x 4.40mm
	DW (SOIC, 20)	12.80mm x 10.3mm	12.8mm x 7.5mm
	N (PDIP, 20)	24.33mm x 9.4mm	25.40mm x 6.35mm
	PW (TSSOP, 20)	6.50mm x 6.4mm	6.50mm x 4.40mm

(1) For more information, see [Section 11](#).

(2) The package size (length x width) is a nominal value and includes pins, where applicable.

(3) The body size (length x width) is a nominal value and does not include pins.



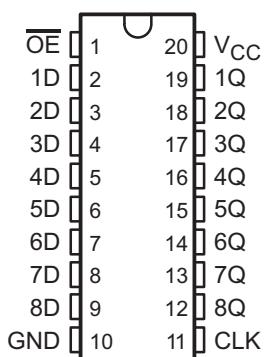
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## Table of Contents

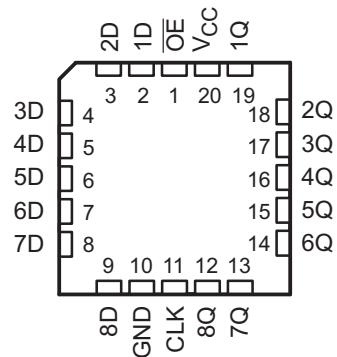
<b>1 Features</b> .....	<b>1</b>	7.1 Overview.....	<b>9</b>
<b>2 Applications</b> .....	<b>1</b>	7.2 Functional Block Diagram.....	<b>9</b>
<b>3 Description</b> .....	<b>1</b>	7.3 Feature Description.....	<b>9</b>
<b>4 Pin Configuration and Functions</b> .....	<b>3</b>	7.4 Device Functional Modes.....	<b>9</b>
<b>5 Specifications</b> .....	<b>4</b>	<b>8 Application and Implementation</b> .....	<b>10</b>
5.1 Absolute Maximum Ratings.....	4	8.1 Application Information.....	10
5.2 ESD Ratings.....	4	8.2 Typical Application.....	10
5.3 Recommended Operating Conditions.....	4	8.3 Power Supply Recommendations.....	11
5.4 Thermal Information.....	5	8.4 Layout.....	11
5.5 Electrical Characteristics.....	5	<b>9 Device and Documentation Support</b> .....	<b>12</b>
5.6 Timing Requirements, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ .....	5	9.1 Documentation Support.....	12
5.7 Timing Requirements, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .....	6	9.2 Receiving Notification of Documentation Updates.....	12
5.8 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ .....	6	9.3 Support Resources.....	12
5.9 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .....	6	9.4 Trademarks.....	12
5.10 Noise Characteristics.....	7	9.5 Electrostatic Discharge Caution.....	12
5.11 Operating Characteristics.....	7	9.6 Glossary.....	12
5.12 Typical Characteristics.....	7	<b>10 Revision History</b> .....	<b>12</b>
<b>6 Parameter Measurement Information</b> .....	<b>8</b>	<b>11 Mechanical, Packaging, and Orderable</b> <b>Information</b> .....	<b>13</b>
<b>7 Detailed Description</b> .....	<b>9</b>		

## 4 Pin Configuration and Functions

**SN54AHC574 . . . J OR W PACKAGE  
SN74AHC574 . . . DB, DGV, DW, N, NS, OR PW PACKAGE  
(TOP VIEW)**



**SN54AHC574 . . . FK PACKAGE  
(TOP VIEW)**



PIN		TYPE	DESCRIPTION
NO.	NAME		
1	OE	I	Output Enable Pin
2	1D	I	1D Input
3	2D	I	2D Input
4	3D	I	3D Input
5	4D	I	4D Input
6	5D	I	5D Input
7	6D	I	6D Input
8	7D	I	7D Input
9	8D	I	8D Input
10	GND	—	Ground Pin
11	CLK	I	Clock Pin
12	8Q	O	8Q Output
13	7Q	O	7Q Output
14	6Q	O	6Q Output
15	5Q	O	5Q Output
16	4Q	O	4Q Output
17	3Q	O	3Q Output
18	2Q	O	2Q Output
19	1Q	O	1Q Output
20	V <sub>CC</sub>	—	Power Pin

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		-0.5	7	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>		-0.5	7	V
V <sub>O</sub>	Output voltage range <sup>(2)</sup>		-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-20	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>		±20	mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>		±25	mA
	Continuous current through V <sub>CC</sub> or GND			±75	mA
T <sub>stg</sub>	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [Section 5.3](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		SN54AHC574		SN74AHC574		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	2	5.5	2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5	1.5		V
		V <sub>CC</sub> = 3 V	2.1	2.1		
		V <sub>CC</sub> = 5.5 V	3.85	3.85		
V <sub>IL</sub>	Low-level Input voltage	V <sub>CC</sub> = 2 V	0.5	0.5		V
		V <sub>CC</sub> = 3 V	0.9	0.9		
		V <sub>CC</sub> = 5.5 V	1.65	1.65		
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V	-50	-50	μA	mA
		V <sub>CC</sub> = 3.3 V ± 0.3 V	-4	-4		
		V <sub>CC</sub> = 5 V ± 0.5 V	-8	-8		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V	50	50	μA	mA
		V <sub>CC</sub> = 3.3 V ± 0.3 V	4	4		
		V <sub>CC</sub> = 5 V ± 0.5 V	8	8		
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 3.3 V ± 0.3 V	100	100		ns/V
		V <sub>CC</sub> = 5 V ± 0.5 V	20	20		

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		SN54AHC574		SN74AHC574		UNIT
		MIN	MAX	MIN	MAX	
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	125	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN74AHC574						UNIT	
	DB	DGV	DW	N	NS	PW		
	20 PINS							
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	97.9	117.2	81.1	53.3	79.2	116.8	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	59.6	32.7	48.9	40.0	45.7	58.5	
R <sub>θJB</sub>	Junction-to-board thermal resistance	53.1	58.7	53.8	34.2	46.8	78.7	
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	21.3	1.15	19.5	26.4	19.3	12.6	
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	52.7	58.0	53.1	34.1	46.4	77.9	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54AHC574		SN74AHC574		UNIT	
						-40°C to 85°C		-40°C to 85°C			
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	2 V	1.9	2		1.9		1.9		V	
		3 V	2.9	3		2.9		2.9			
		4.5 V	4.4	4.5		4.4		4.4			
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		2.48			
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V	0.1			0.1		0.1		V	
		3 V	0.1			0.1		0.1			
		4.5 V	0.1			0.1		0.1			
	I <sub>OH</sub> = 4 mA	3 V	0.36			0.5		0.44			
	I <sub>OH</sub> = 8 mA	4.5 V	0.36			0.5		0.44			
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V	±0.1			±1 <sup>(1)</sup>		±1		μA	
I <sub>OZ</sub> <sup>(2)</sup>	V <sub>O</sub> = V <sub>CC</sub> or GND V <sub>I</sub> (OE) = V <sub>IL</sub> or V <sub>IH</sub>	5.5 V	±0.25			±2.5		±2.5		μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V	4			40		40		μA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V	3		10			10		pF	
C <sub>O</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V	3							pF	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

(2) For input and output pins, I<sub>OZ</sub> includes the input leakage current.

## 5.6 Timing Requirements, V<sub>CC</sub> = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	T <sub>A</sub> = 25°C	SN54AHC574		SN74AHC574		UNIT	
		-40°C to 85°C		-40°C to 85°C			
		MIN	MAX	MIN	MAX		
t <sub>w</sub>	Pulse duration, CLK high or low	5		5		5.5	ns

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	$T_A = 25^\circ\text{C}$		SN54AHC574		SN74AHC574		UNIT
			-40°C to 85°C		-40°C to 85°C		
	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{su}$	Setup time, data before CLK↑	3.5	3.5	3.5	4	ns	
$t_h$	Hold time, data after CLK↑	1.5	1.5	1.5	2	ns	

## 5.7 Timing Requirements, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	$T_A = 25^\circ\text{C}$		SN54AHC574		SN74AHC574		UNIT
			-40°C to 85°C		-40°C to 85°C		
	MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration, CLK high or low	5	5	5	5.5	ns	
$t_{su}$	Setup time, data before CLK↑	3	3	3	3.5	ns	
$t_h$	Hold time, data after CLK↑	1.5	1.5	1.5	2	ns	

## 5.8 Switching Characteristics, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC574		SN74AHC574				UNIT	
							-40°C to 85°C		-40°C to 85°C		-40°C to 125°C			
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$f_{MAX}$			$C_L = 15 \text{ pF}$	80 <sup>(1)</sup>	125 <sup>(1)</sup>		65 <sup>(1)</sup>		65	65			MHz	
			$C_L = 50 \text{ pF}$	50	75		45		45	45				
$t_{PLH}$	CLK	Q	$C_L = 15 \text{ pF}$	8.5 <sup>(1)</sup>	13.2 <sup>(1)</sup>		1 <sup>(1)</sup>	15.5 <sup>(1)</sup>	1	15.5	1	17	ns	
$t_{PHL}$				8.5 <sup>(1)</sup>	13.2 <sup>(1)</sup>		1 <sup>(1)</sup>	15.5 <sup>(1)</sup>	1	15.5	1	17		
$t_{PZH}$	$\overline{OE}$	Q	$C_L = 15 \text{ pF}$	8.2 <sup>(1)</sup>	12.8 <sup>(1)</sup>		1 <sup>(1)</sup>	15 <sup>(1)</sup>	1	15	1	16	ns	
$t_{PZL}$				8.2 <sup>(1)</sup>	12.8 <sup>(1)</sup>		1 <sup>(1)</sup>	15 <sup>(1)</sup>	1	15	1	16		
$t_{PHZ}$	$\overline{OE}$	Q	$C_L = 15 \text{ pF}$	8.5 <sup>(1)</sup>	13 <sup>(1)</sup>		1 <sup>(1)</sup>	15 <sup>(1)</sup>	1	15	1	16	ns	
$t_{PLZ}$				8.5 <sup>(1)</sup>	13 <sup>(1)</sup>		1 <sup>(1)</sup>	15 <sup>(1)</sup>	1	15	1	16		
$t_{PLH}$	CLK	Q	$C_L = 50 \text{ pF}$	11	16.7		1	19	1	19	1	20.5	ns	
$t_{PHL}$				11	16.7		1	19	1	19	1	20.5		
$t_{PZH}$	$\overline{OE}$	Q	$C_L = 50 \text{ pF}$	10.7	16.3		1	18.5	1	18.5	1	19.5	ns	
$t_{PZL}$				10.7	16.3		1	18.5	1	18.5	1	19.5		
$t_{PHZ}$	$\overline{OE}$	Q	$C_L = 50 \text{ pF}$	11	15		1	17	1	17	1	18	ns	
$t_{PLZ}$				11	15		1	17	1	17	1	18		
$t_{sk(o)}$			$C_L = 50 \text{ pF}$	1.5 <sup>(2)</sup>							1.5	ns		

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

## 5.9 Switching Characteristics, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC574		SN74AHC574				UNIT	
							-40°C to 85°C		-40°C to 85°C		-40°C to 125°C			
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$f_{MAX}$			$C_L = 15 \text{ pF}$	130 <sup>(1)</sup>	180 <sup>(1)</sup>		110 <sup>(1)</sup>		110	110			MHz	
			$C_L = 50 \text{ pF}$	85	115		75		75	75				
$t_{PLH}$	CLK	Q	$C_L = 15 \text{ pF}$	5.6 <sup>(1)</sup>	8.6 <sup>(1)</sup>		1 <sup>(1)</sup>	10 <sup>(1)</sup>	1	10	1	11	ns	
$t_{PHL}$				5.6 <sup>(1)</sup>	8.6 <sup>(1)</sup>		1 <sup>(1)</sup>	10 <sup>(1)</sup>	1	10	1	11		
$t_{PZH}$	$\overline{OE}$	Q	$C_L = 15 \text{ pF}$	5.9 <sup>(1)</sup>	9 <sup>(1)</sup>		1 <sup>(1)</sup>	10.5 <sup>(1)</sup>	1	10.5	1	11.5	ns	
$t_{PZL}$				5.9 <sup>(1)</sup>	9 <sup>(1)</sup>		1 <sup>(1)</sup>	10.5 <sup>(1)</sup>	1	10.5	1	11.5		

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	TA = 25°C			SN54AHC574				SN74AHC574				UNIT	
							-40°C to 85°C		-40°C to 85°C		-40°C to 125°C					
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t <sub>PHZ</sub>	OE	Q	C <sub>L</sub> = 15 pF	5.5 <sup>(1)</sup>	9 <sup>(1)</sup>	10.5 <sup>(1)</sup>	1	10.5	1	11.5	ns	ns	ns	ns		
t <sub>PLZ</sub>				5.5 <sup>(1)</sup>	9 <sup>(1)</sup>	10.5 <sup>(1)</sup>	1	10.5	1	11.5						
t <sub>PLH</sub>	CLK	Q	C <sub>L</sub> = 50 pF	7.1	10.6	12	1	12	1	12	1	13	ns	ns		
t <sub>PHL</sub>				7.1	10.6	12	1	12	1	12	1	13				
t <sub>PZH</sub>	OE	Q	C <sub>L</sub> = 50 pF	7.4	11	12.5	1	12.5	1	13.5	ns	ns	ns	ns		
t <sub>PZL</sub>				7.4	11	12.5	1	12.5	1	13.5						
t <sub>PHZ</sub>	OE	Q	C <sub>L</sub> = 50 pF	7.1	10.1	11.5	1	11.5	1	12.5	ns	ns	ns	ns		
t <sub>PLZ</sub>				7.1	10.1	11.5	1	11.5	1	12.5						
t <sub>sk(o)</sub>			C <sub>L</sub> = 50 pF		1 <sup>(2)</sup>					1		1		ns		

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

## 5.10 Noise Characteristics

V<sub>CC</sub> = 5 V, C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C<sup>(1)</sup>

PARAMETER	SN74AHC574		UNIT
	MIN	MAX	
V <sub>OL(P)</sub> Quiet output, maximum dynamic V <sub>OL</sub>	0.8		V
V <sub>OL(V)</sub> Quiet output, minimum dynamic V <sub>OL</sub>	-0.8		V
V <sub>OH(V)</sub> Quiet output, minimum dynamic V <sub>OH</sub>	4.2		V
V <sub>IH(D)</sub> High-level dynamic input voltage	3.5		V
V <sub>IL(D)</sub> Low-level dynamic input voltage	1.5		V

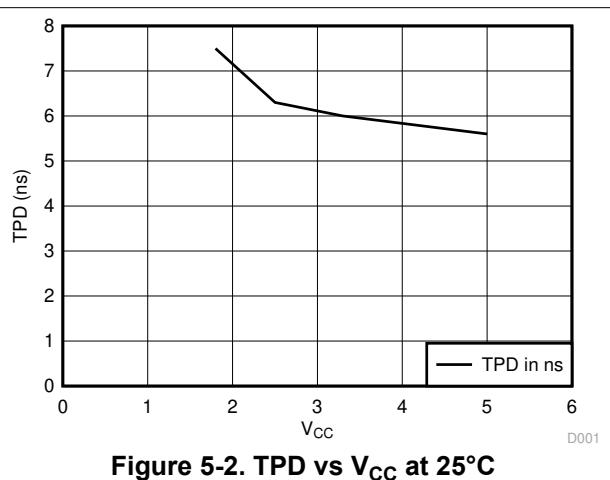
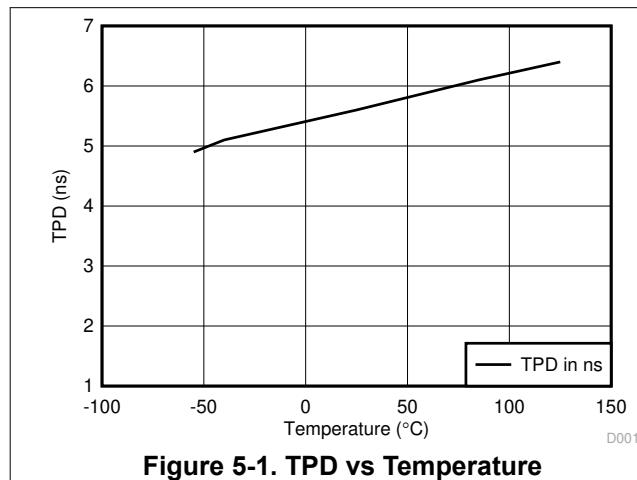
(1) Characteristics are for surface-mount packages only.

## 5.11 Operating Characteristics

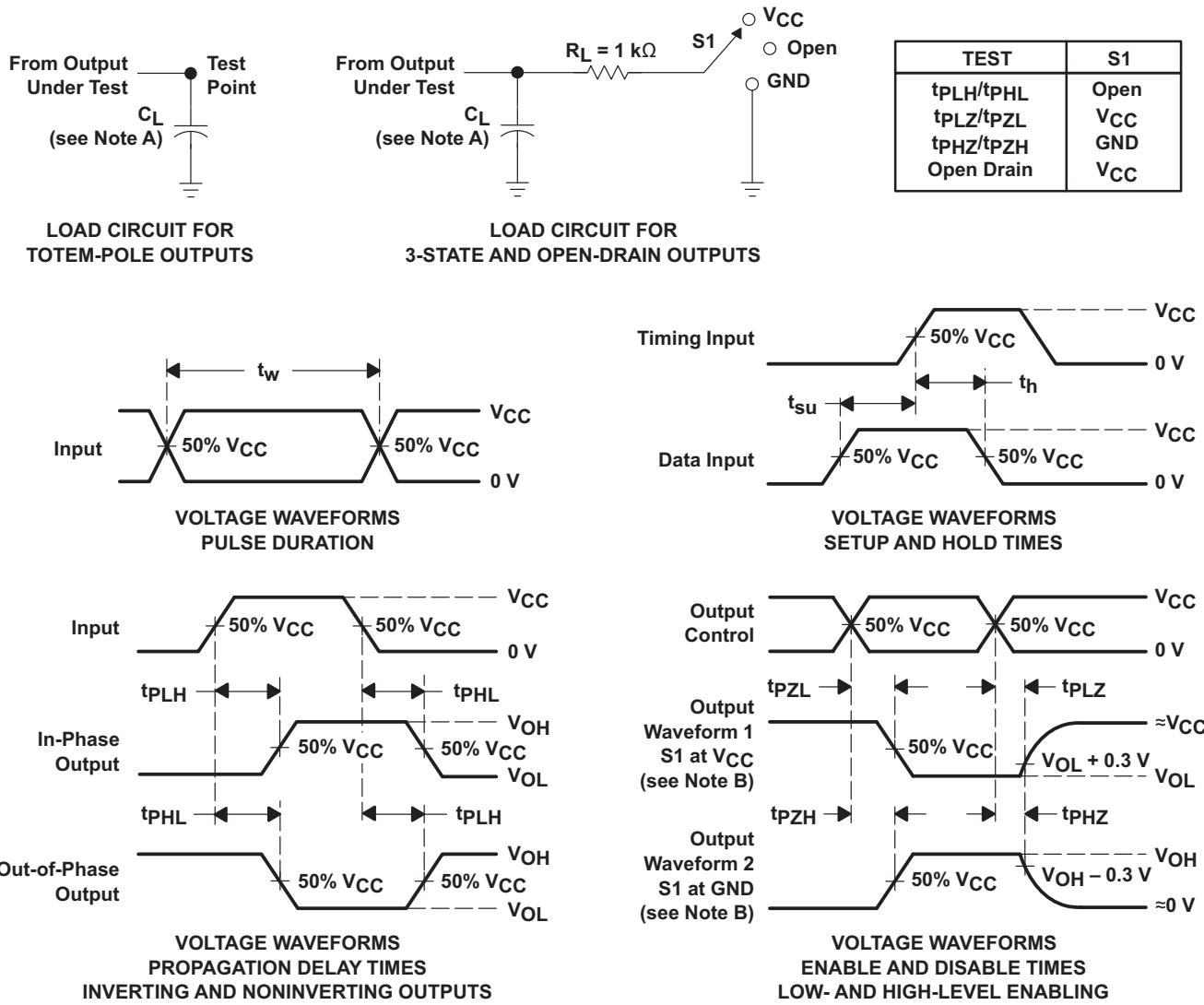
V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	No load, f = 1 MHz	28	pF

## 5.12 Typical Characteristics



## 6 Parameter Measurement Information



NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.
- The outputs are measured one at a time with one input transition per measurement.
- All parameters and waveforms are not applicable to all devices.

**Figure 6-1. Load Circuit and Voltage Waveforms**

## 7 Detailed Description

### 7.1 Overview

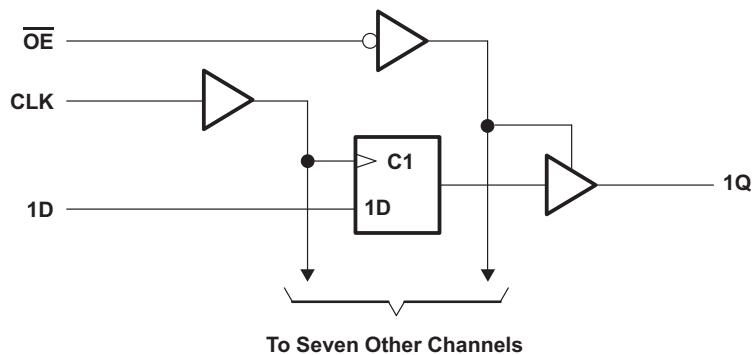
The SNx4AHC574 devices are octal edge-triggered D-type flip-flops that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs.

The states of the Q outputs are not predictable until the first valid clock.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pull-up components.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

- 5.5-V tolerant input allows for 5 V to 3.3 V voltage translation
- Slow edges reduce output ringing

### 7.4 Device Functional Modes

**Table 7-1. Function Table  
(Each Flip-Flop)**

INPUTS			OUTPUT
OE	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	$Q_0$
H	X	X	Z

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

SN74AHC574 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs can accept voltages to 5.5 V at any valid  $V_{CC}$  making it ideal for down translation

### 8.2 Typical Application

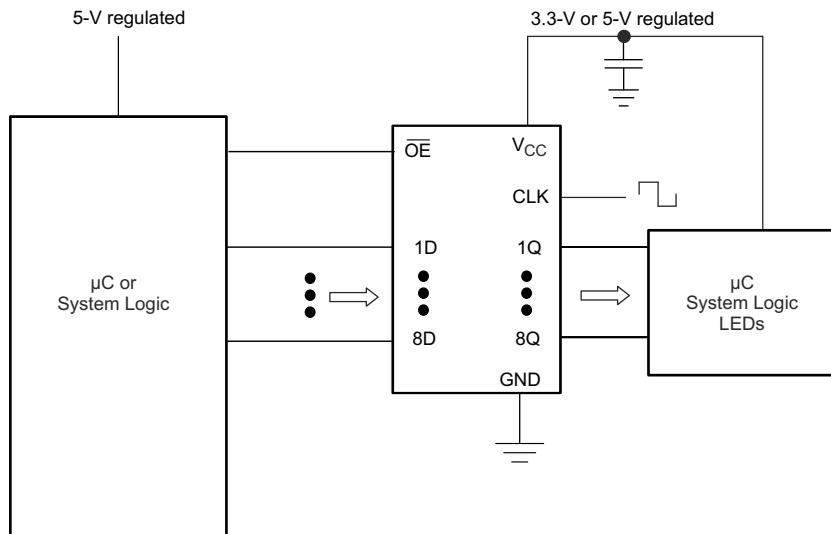


Figure 8-1. Typical Application Schematic

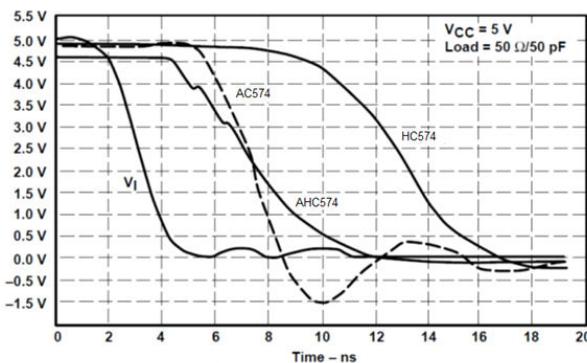
#### 8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

#### 8.2.2 Detailed Design Procedure

1. Recommended Input Conditions
  - For rise time and fall time specifications, see  $\Delta t/\Delta V$  in the [Section 5.3](#) table.
  - For specified High and low levels, see  $V_{IH}$  and  $V_{IL}$  in the [Section 5.3](#) table.
2. Recommend Output Conditions
  - Load currents should not exceed 25 mA per output and 75 mA total for the part.
  - Outputs should not be pulled above  $V_{CC}$ .

### 8.2.3 Application Curves



**Figure 8-2. Switching Characteristics Comparison**

## 8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Section 5.3](#) table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu$ F is recommended. If there are multiple  $V_{CC}$  pins, 0.01  $\mu$ F or 0.022  $\mu$ F is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu$ F and 1  $\mu$ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

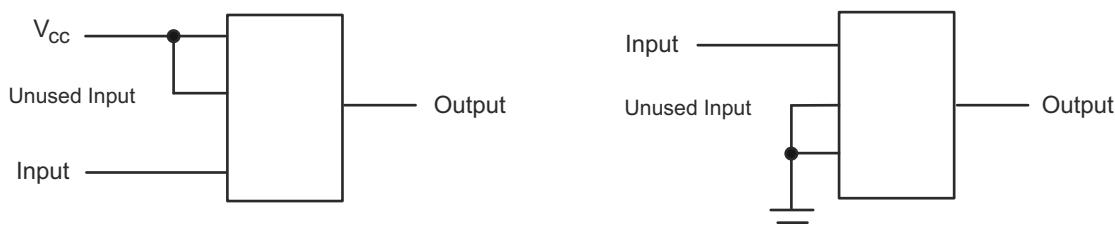
## 8.4 Layout

### 8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 8-3](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

### 8.4.2 Layout Example



**Figure 8-3. Layout Diagram**

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AHC574	<a href="#">Click here</a>				
SN74AHC574	<a href="#">Click here</a>				

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

**TI E2E™ support forums** are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

Changes from Revision J (December 2014) to Revision K (July 2024)	Page
• Deleted machine model from <i>Features</i> section and <i>ESD Ratings</i> table.....	1
• Updated R0JA values: PW = 103.3 to 116.8, DW = 79.4 to 81.1; Updated PW and DW packages for R0JC(top), R0JB, ΨJT, ΨJB, and R0JC(bot), all values in °C/W .....	5

Changes from Revision I (July 2003) to Revision J (December 2014)	Page
• Added <i>Applications</i> , <i>Device Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i> , <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.....	1
• Deleted <i>Ordering Information</i> table.....	1
• Added Military Disclaimer to <i>Features</i> list.....	1

- Changed MAX operating temperature to 125°C in *Recommended Operating Conditions* table. .... 4

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## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9685401Q2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9685401Q2A SNJ54AHC574FK
5962-9685401QRA	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9685401QR A SNJ54AHC574J
5962-9685401QSA	Active	Production	CFP (W)   20	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9685401QS A SNJ54AHC574W
SN74AHC574DBR	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA574
SN74AHC574DBR.A	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA574
SN74AHC574DGSR	Active	Production	VSSOP (DGS)   20	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC574
SN74AHC574DGVR	Active	Production	TVSOP (DGV)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA574
SN74AHC574DGVR.A	Active	Production	TVSOP (DGV)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA574
SN74AHC574DWR	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC574
SN74AHC574DWR.A	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC574
SN74AHC574DWRE4	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC574
SN74AHC574N	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC574N
SN74AHC574N.A	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC574N
SN74AHC574NSR	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC574
SN74AHC574NSR.A	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC574
SN74AHC574PW	Obsolete	Production	TSSOP (PW)   20	-	-	Call TI	Call TI	-40 to 125	HA574
SN74AHC574PWR	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA574
SN74AHC574PWR.A	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA574
SN74AHC574RKS	Active	Production	VQFN (RKS)   20	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC574
SNJ54AHC574FK	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9685401Q2A SNJ54AHC574FK

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54AHC574FK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9685401Q2A SNJ54AHC574FK
SNJ54AHC574J	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9685401QR A SNJ54AHC574J
SNJ54AHC574J.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9685401QR A SNJ54AHC574J
SNJ54AHC574W	Active	Production	CFP (W)   20	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9685401QS A SNJ54AHC574W
SNJ54AHC574W.A	Active	Production	CFP (W)   20	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9685401QS A SNJ54AHC574W

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

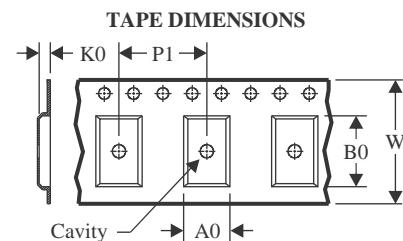
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54AHC574, SN74AHC574 :**

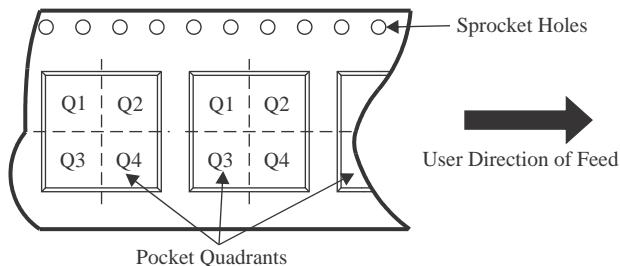
- Catalog : [SN74AHC574](#)
- Military : [SN54AHC574](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

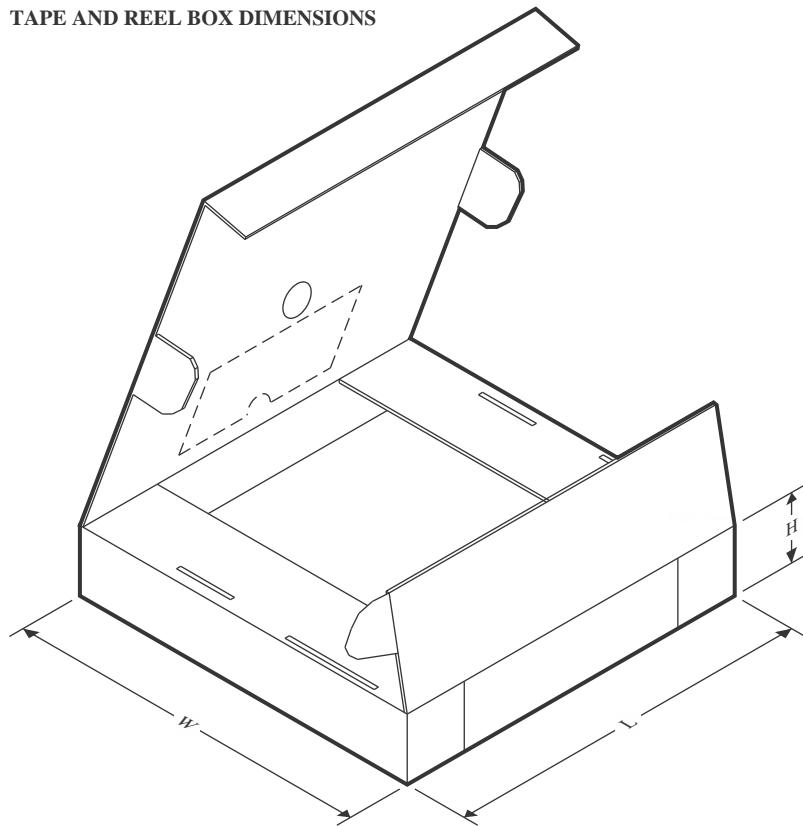
**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC574DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHC574DGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74AHC574DGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC574DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHC574DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74AHC574NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AHC574PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHC574RKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC574DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74AHC574DGSR	VSSOP	DGS	20	5000	353.0	353.0	32.0
SN74AHC574DGVR	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74AHC574DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AHC574DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AHC574NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74AHC574PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74AHC574RKS	VQFN	RKS	20	3000	210.0	185.0	35.0

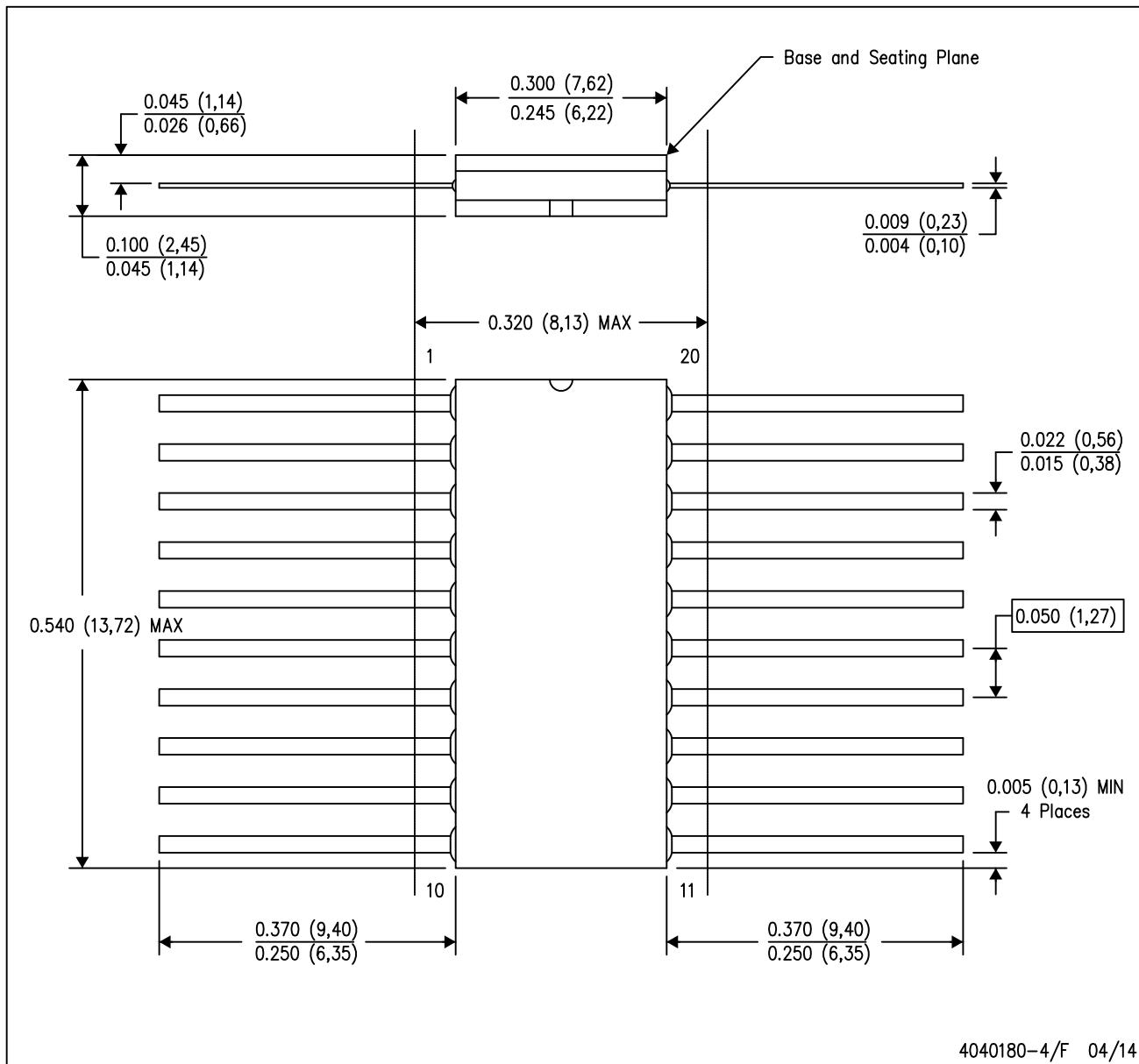
**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T ( $\mu$ m)	B (mm)
5962-9685401Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9685401QSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74AHC574N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AHC574N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54AHC574FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC574FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC574W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54AHC574W.A	W	CFP	20	25	506.98	26.16	6220	NA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20

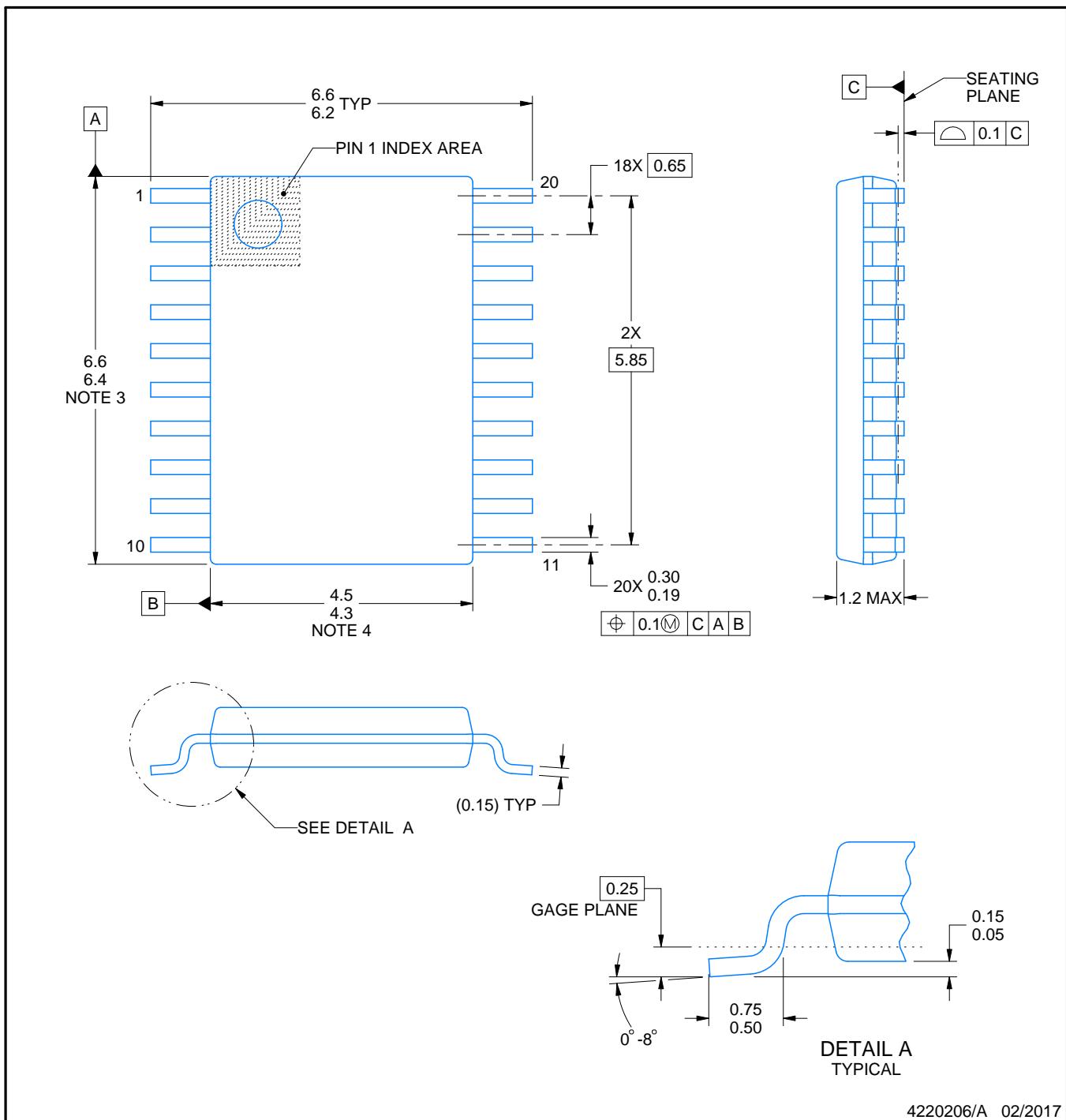
## PACKAGE OUTLINE

**PW0020A**



## **TSSOP - 1.2 mm max height**

## SMALL OUTLINE PACKAGE



## NOTES:

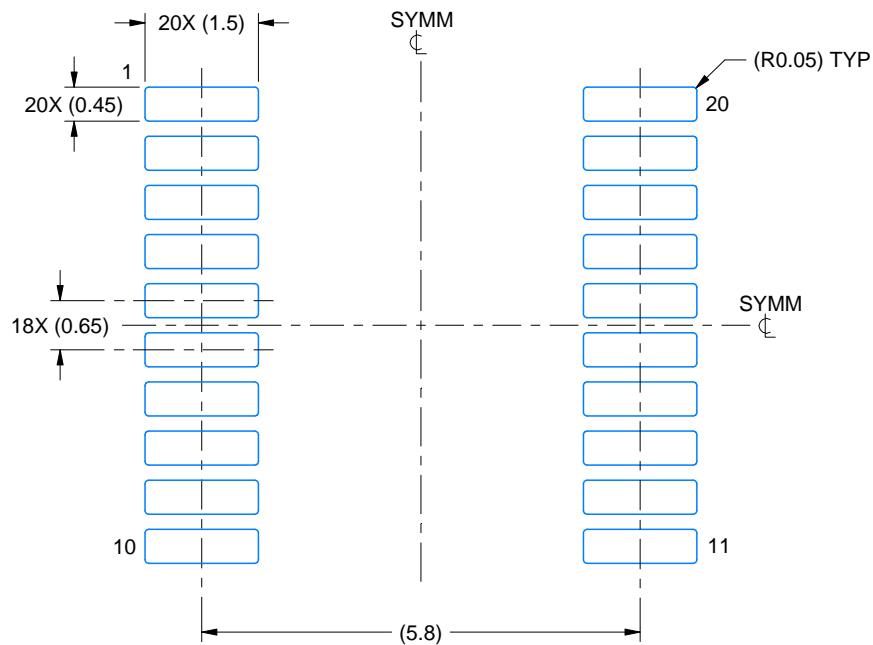
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

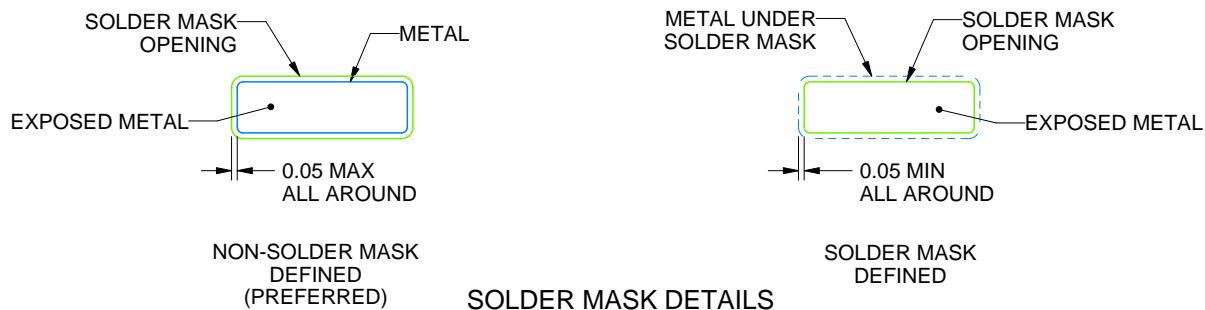
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

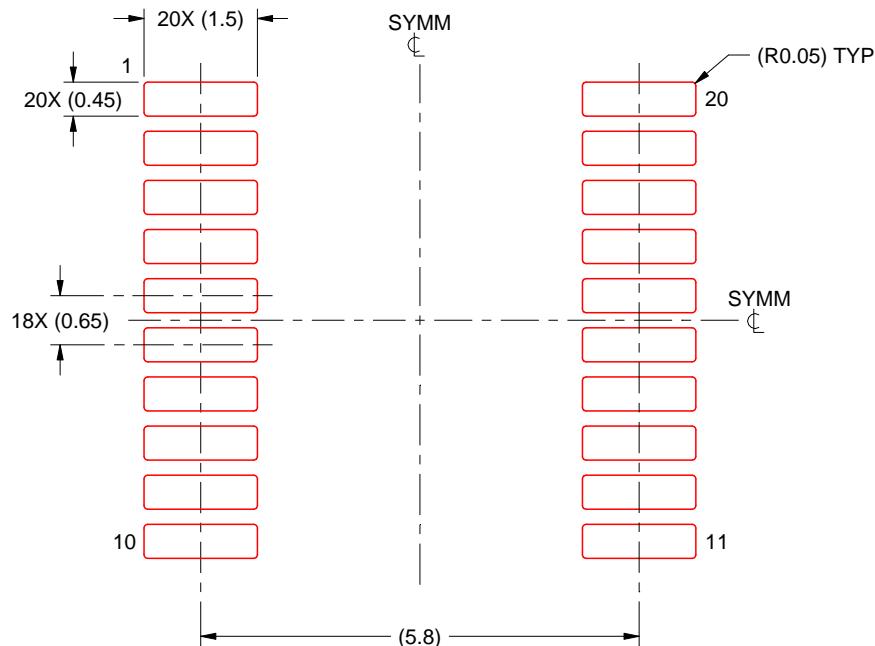
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

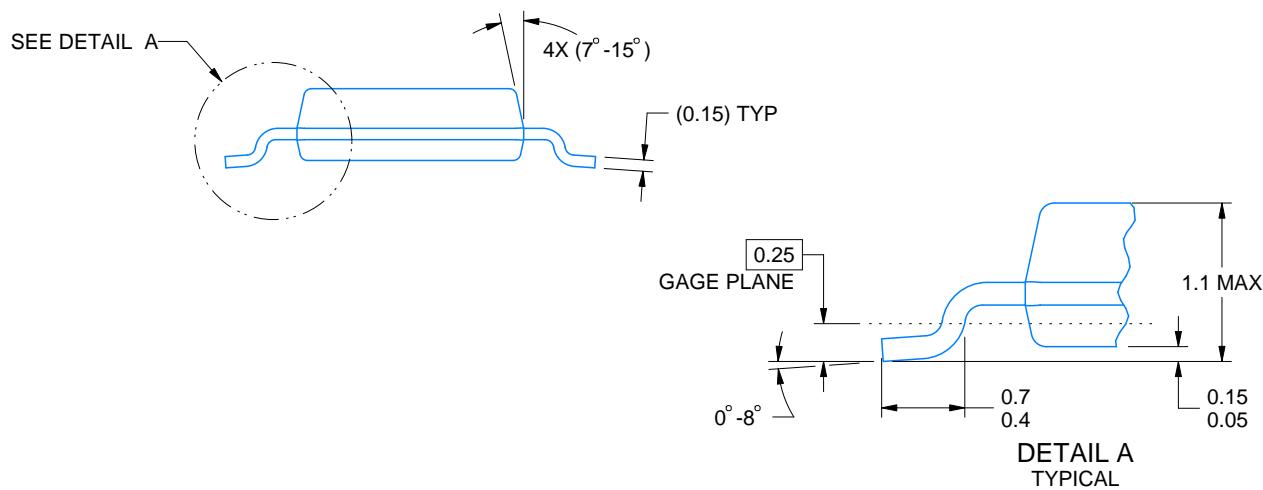
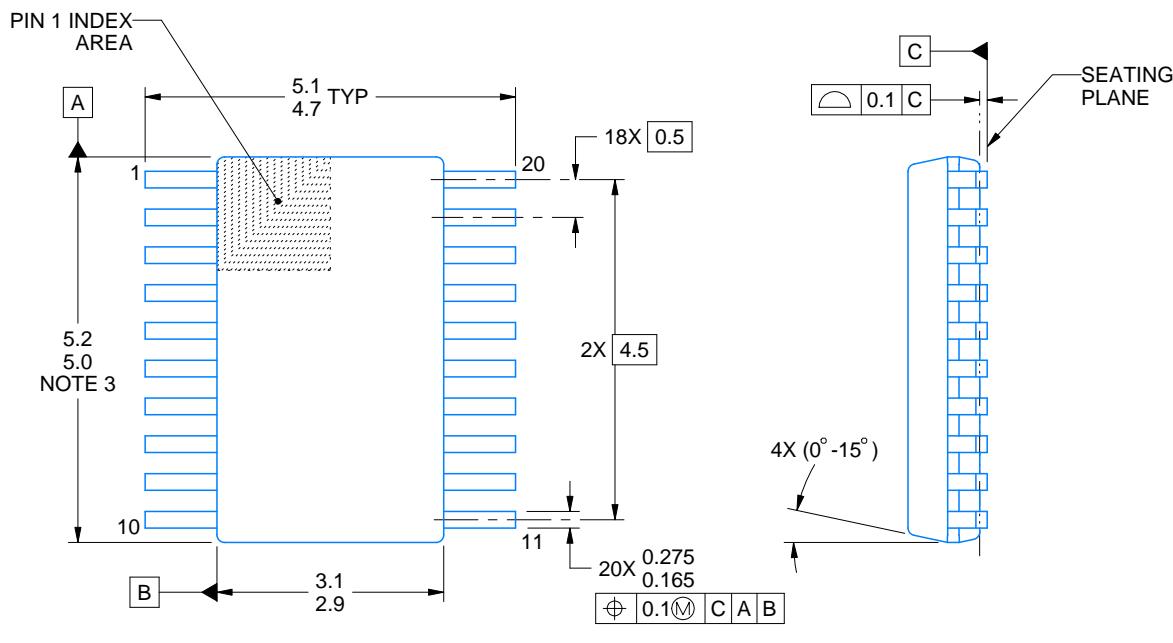
## PACKAGE OUTLINE

**DGS0020A**



## **VSSOP - 1.1 mm max height**

## SMALL OUTLINE PACKAGE



4226367/A 10/2020

## NOTES:

PowerPAD is a trademark of Texas Instruments.

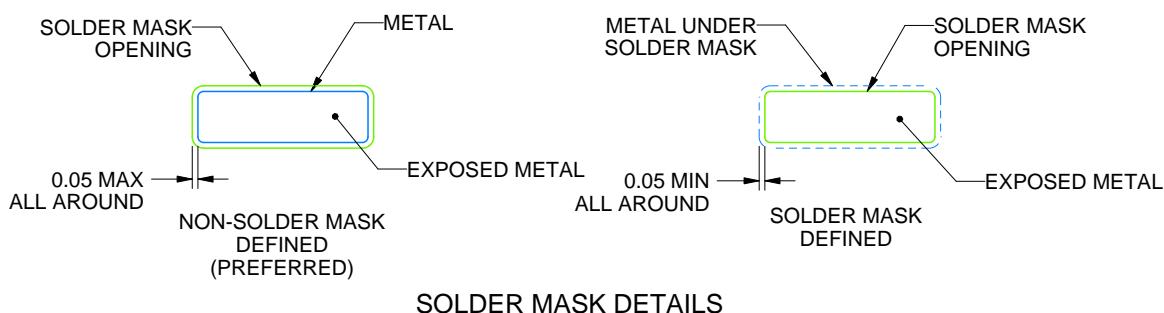
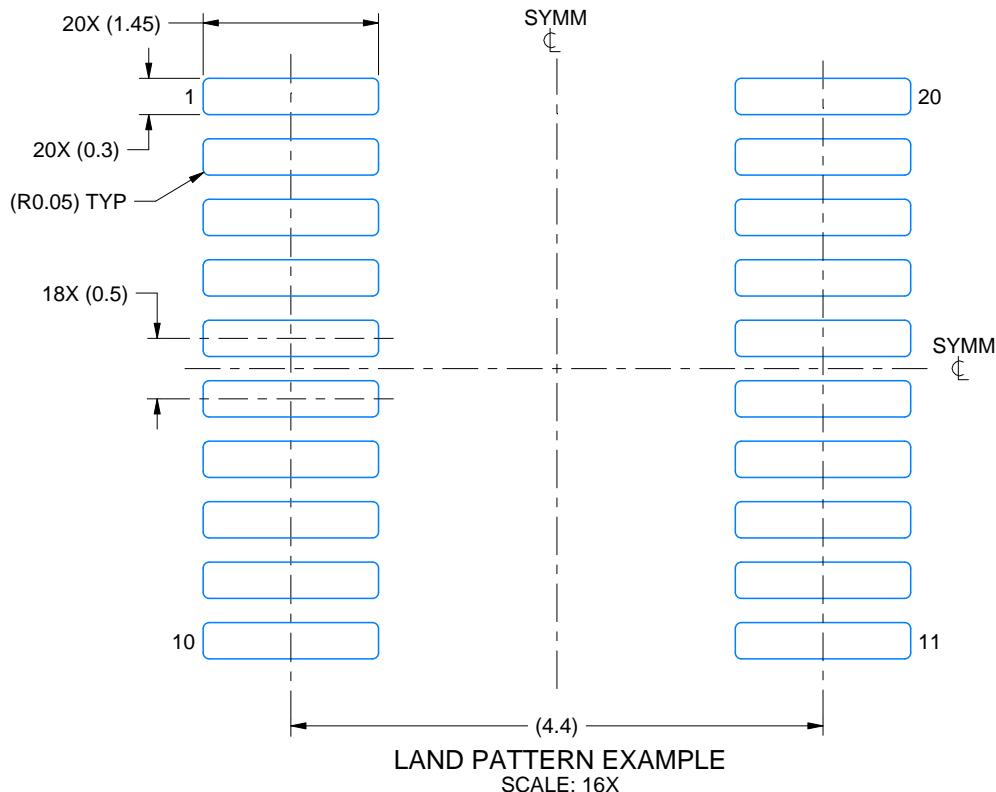
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

# EXAMPLE BOARD LAYOUT

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4226367/A 10/2020

NOTES: (continued)

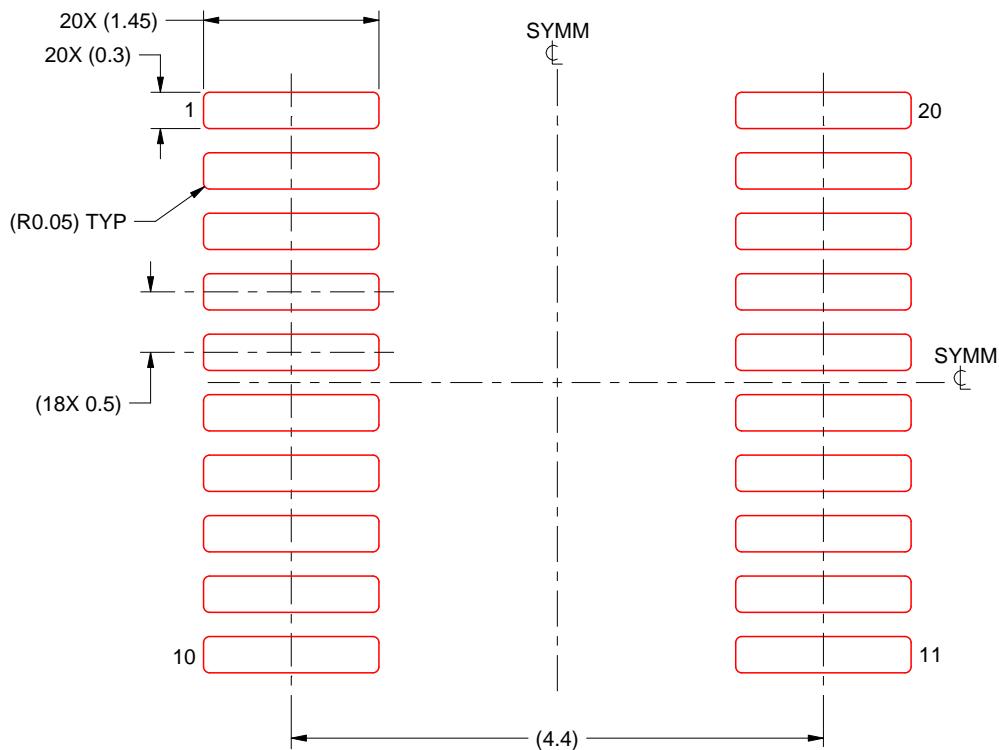
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

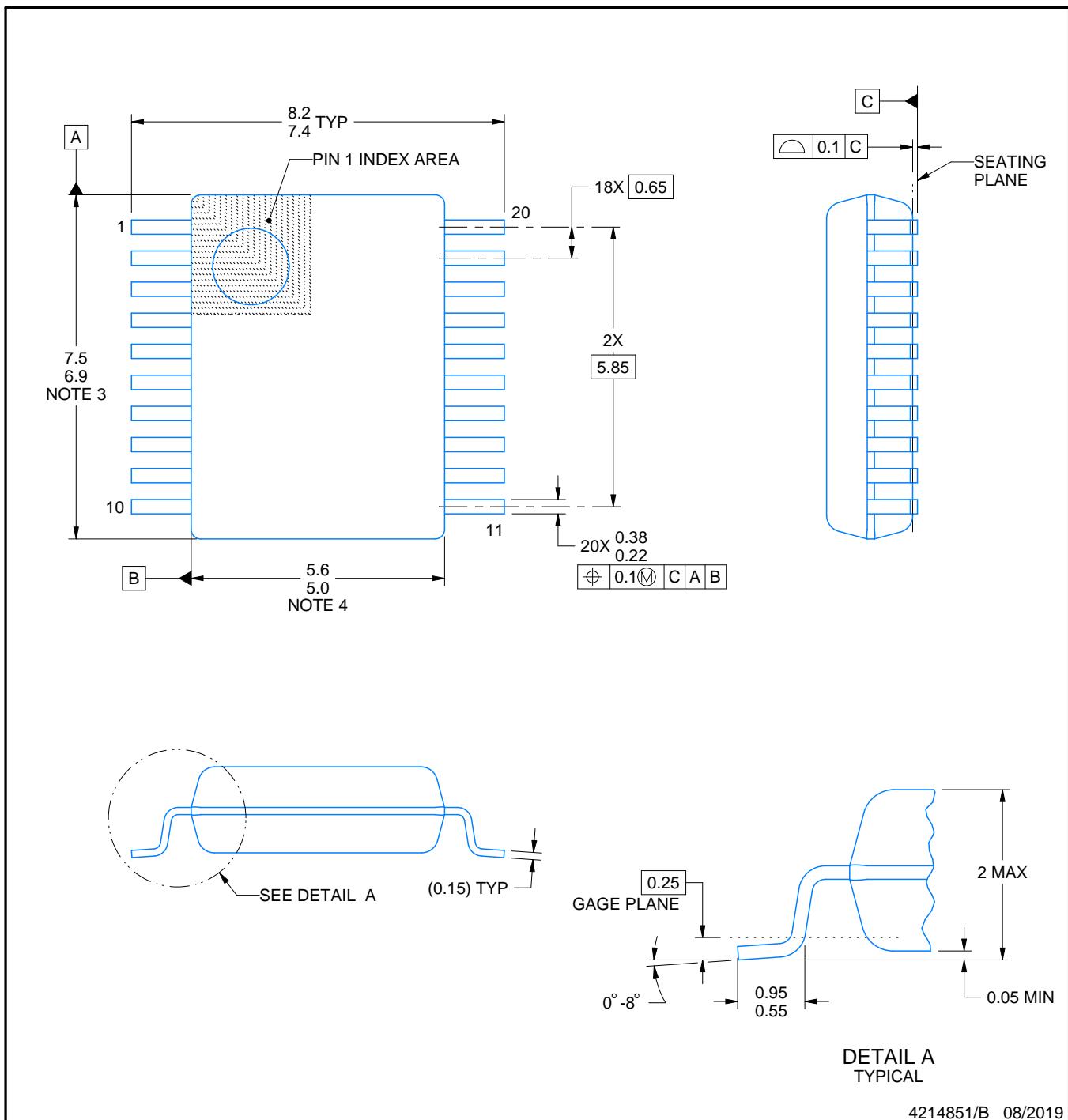
# PACKAGE OUTLINE

DB0020A



SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



## NOTES:

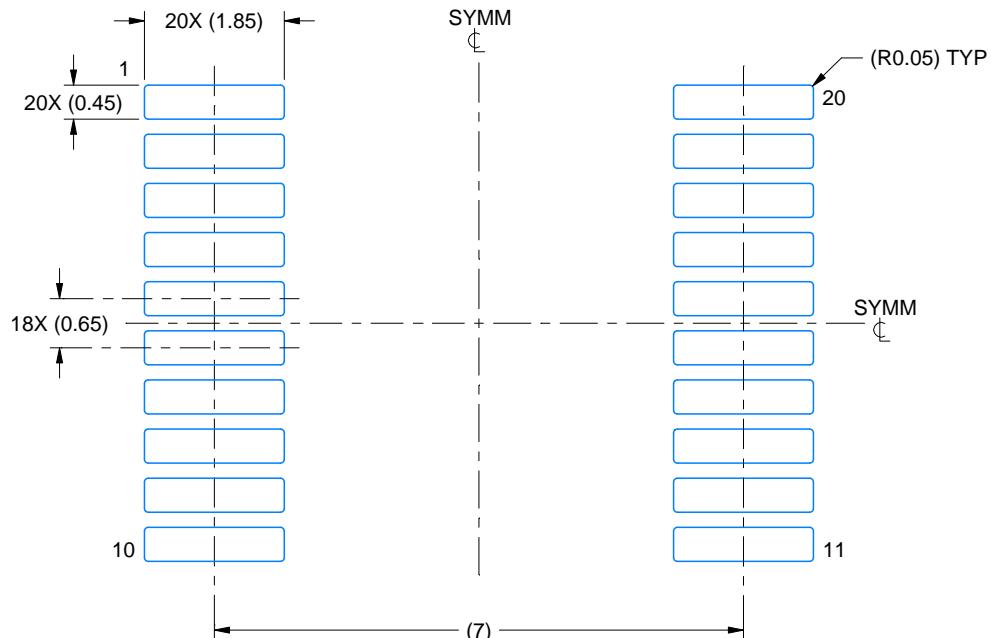
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

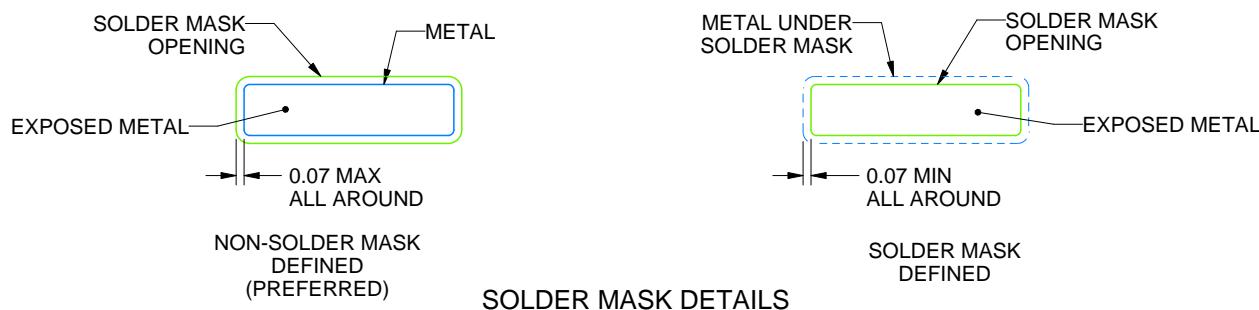
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

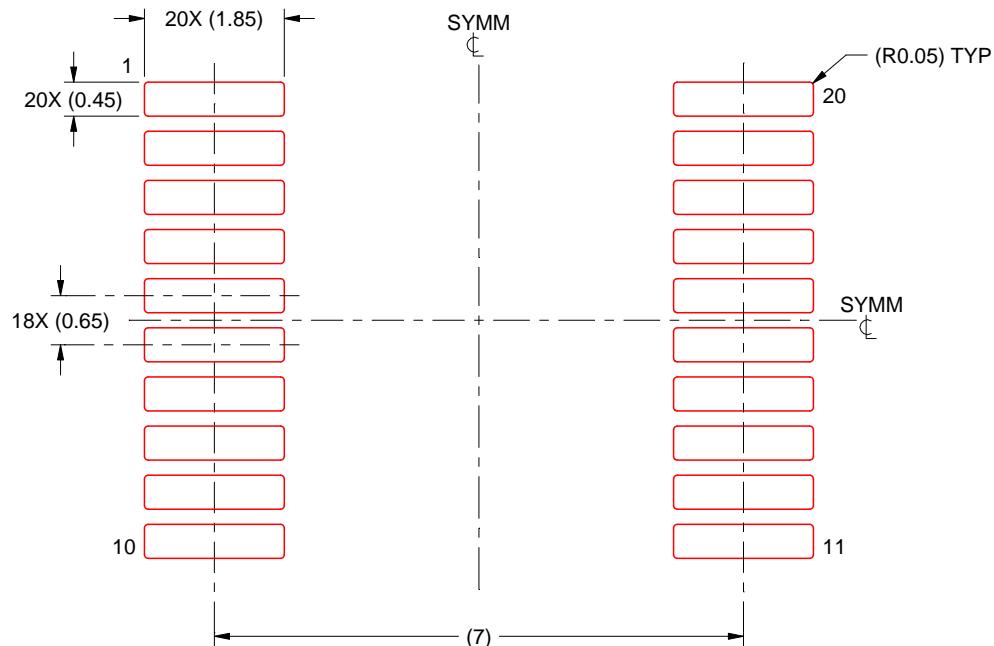
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

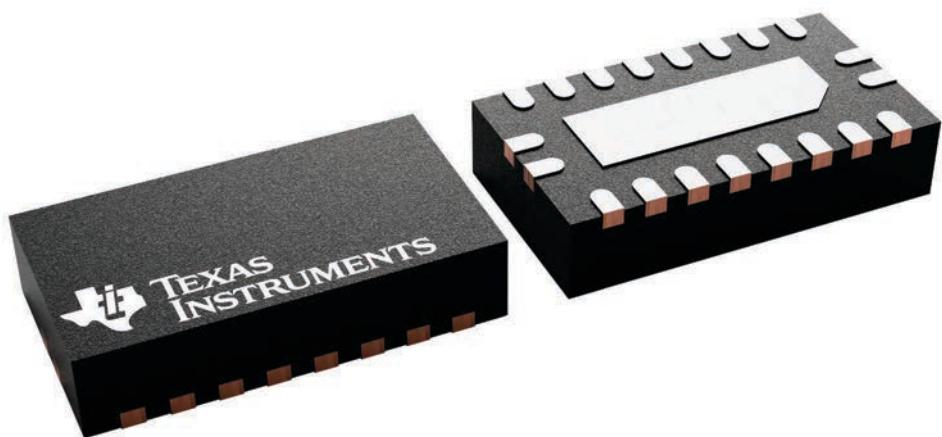
**RKS 20**

**VQFN - 1 mm max height**

**2.5 x 4.5, 0.5 mm pitch**

**PLASTIC QUAD FLATPACK - NO LEAD**

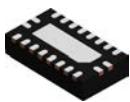
This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4226872/A

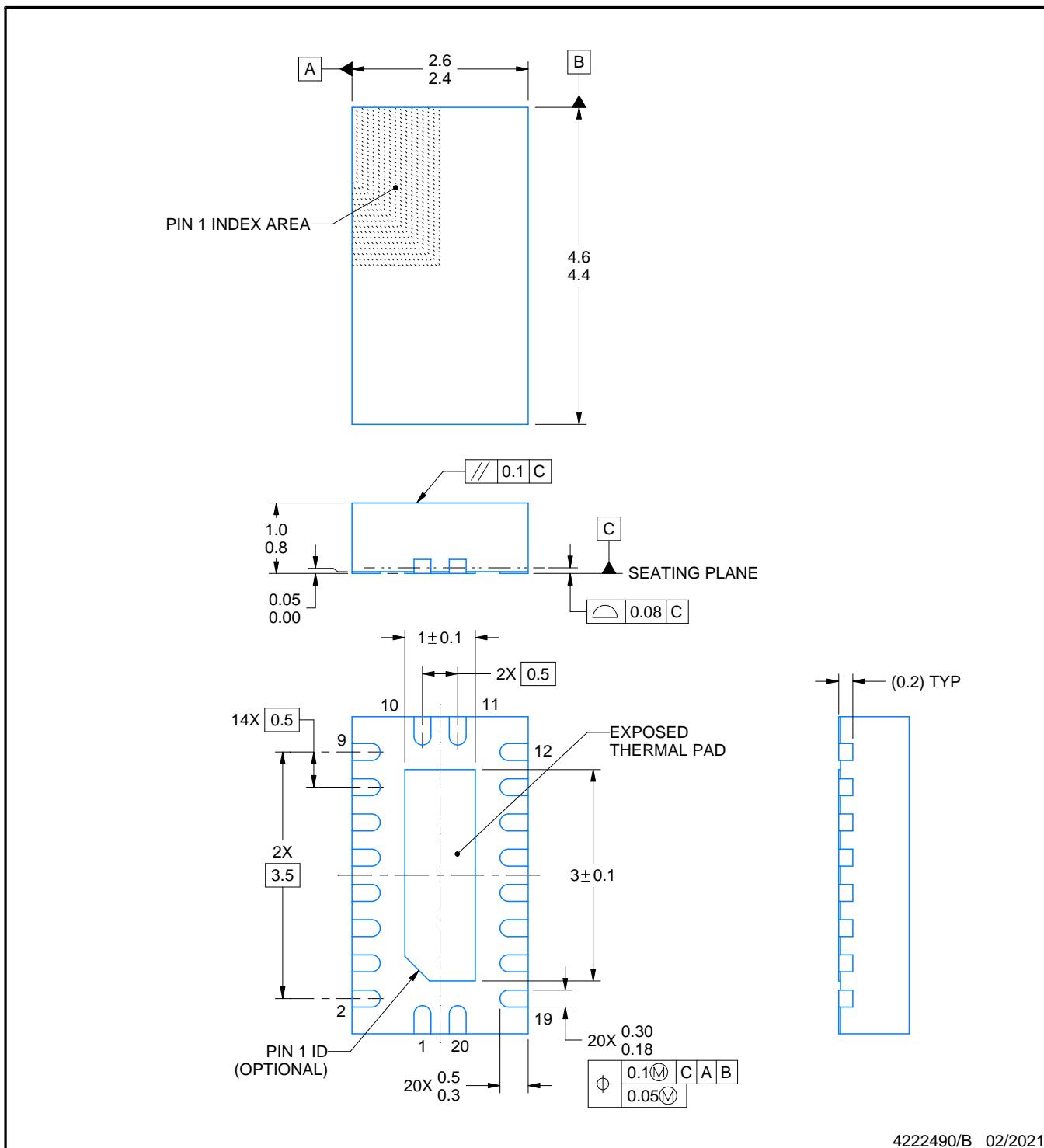
# PACKAGE OUTLINE

RKS0020A



VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4222490/B 02/2021

## NOTES:

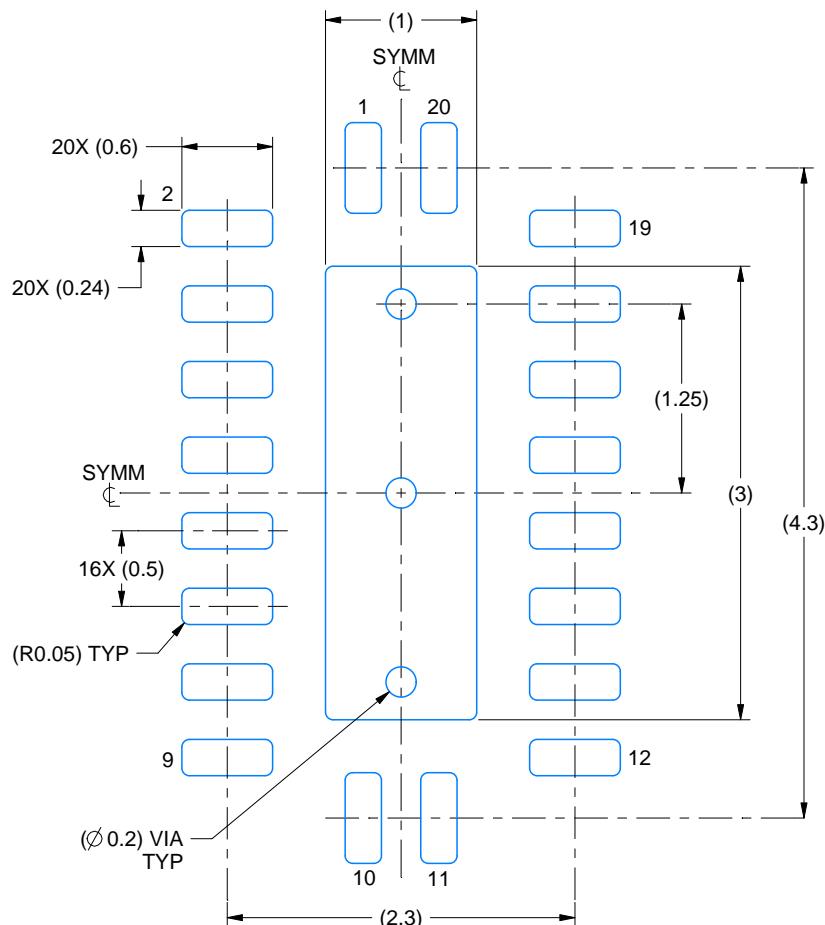
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

## EXAMPLE BOARD LAYOUT

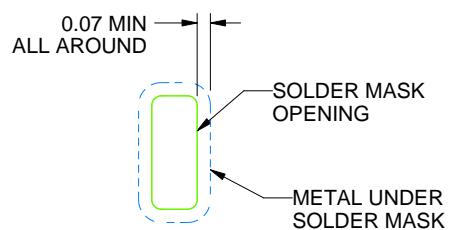
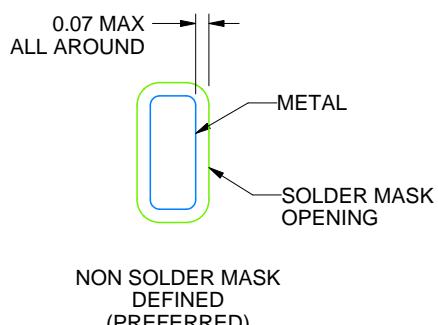
**RKS0020A**

## VQFN - 1 mm max height

## PLASTIC QUAD FLATPACK - NO LEAD



## LAND PATTERN EXAMPLE



## SOLDER MASK DETAILS

4222490/B 02/2021

#### NOTES: (continued)

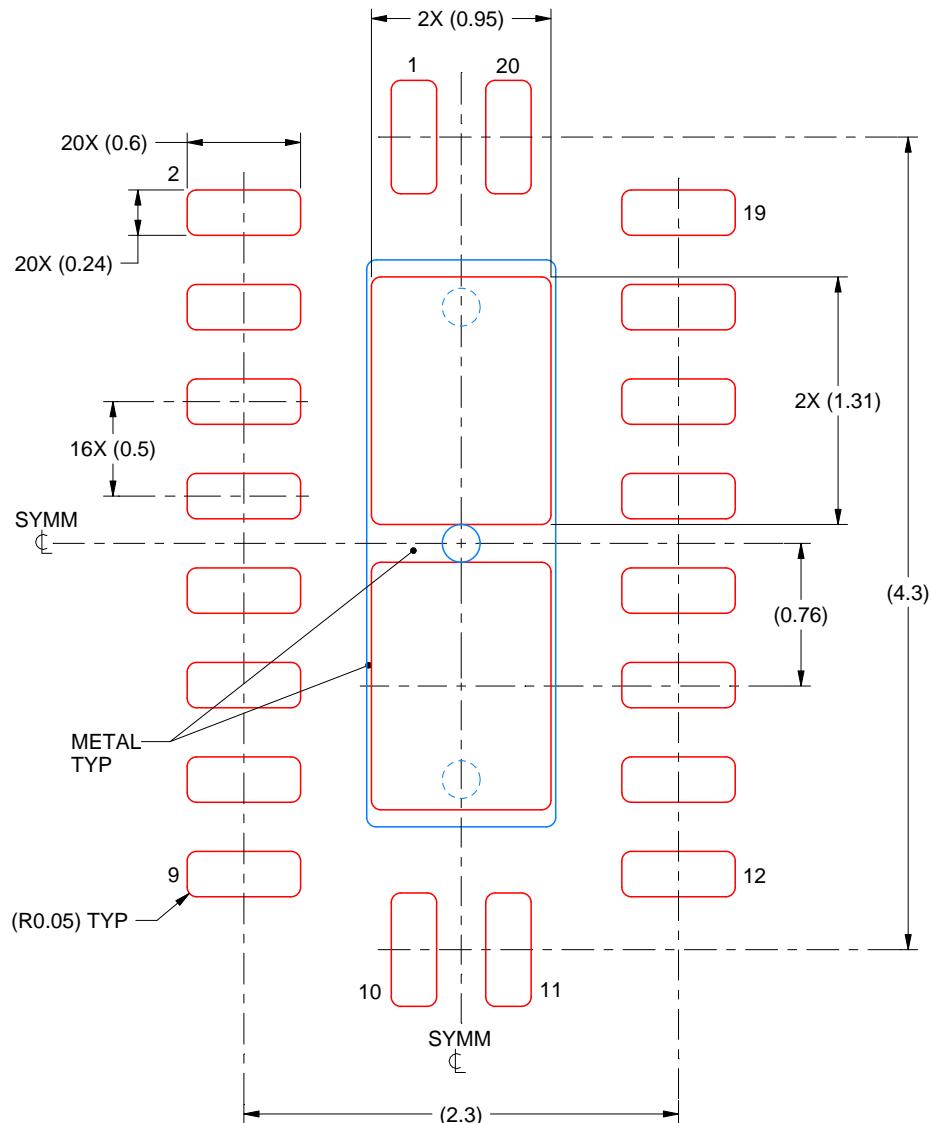
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

# EXAMPLE STENCIL DESIGN

RKS0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
83% PRINTED SOLDER COVERAGE BY AREA  
SCALE:25X

4222490/B 02/2021

NOTES: (continued)

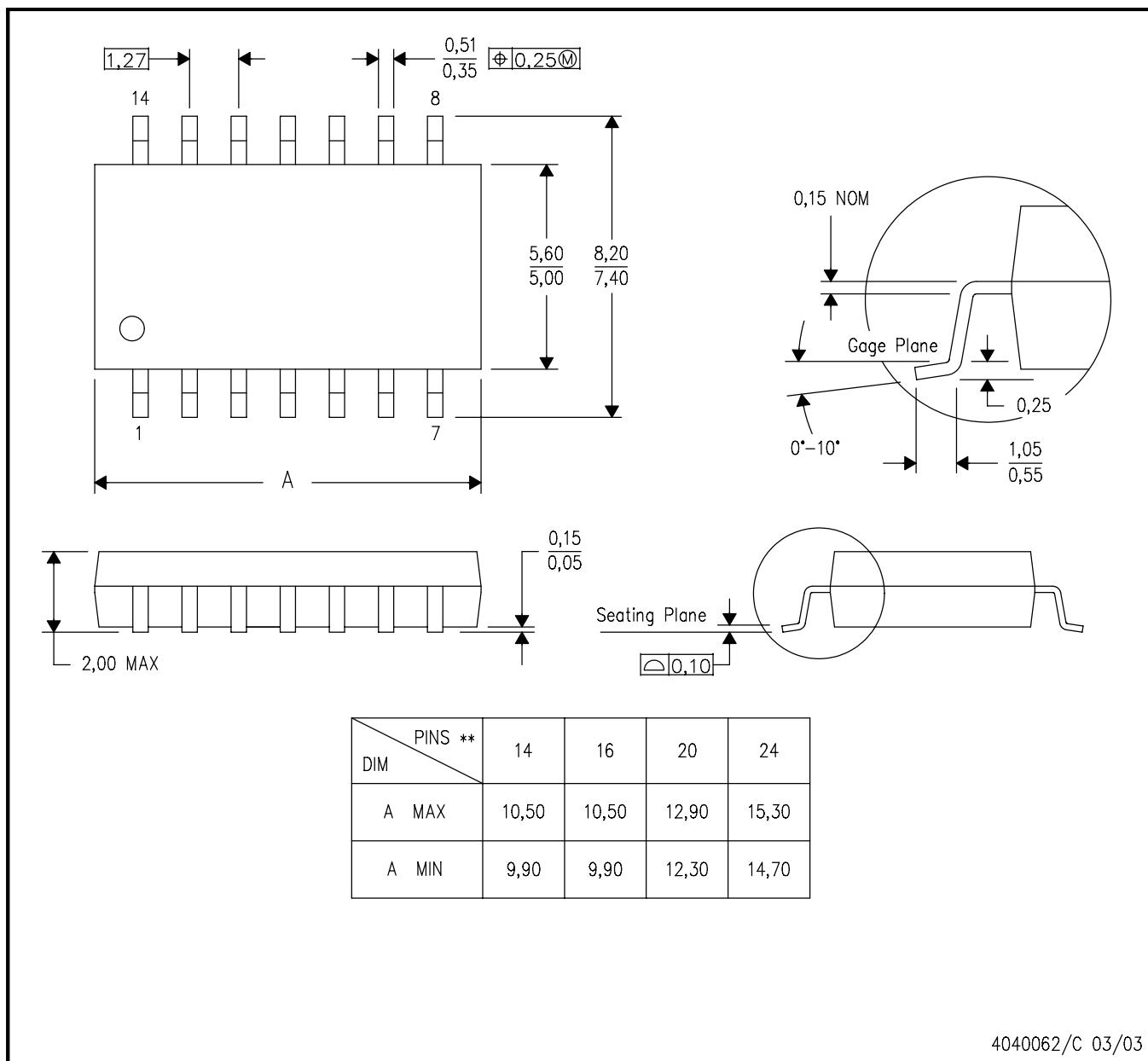
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



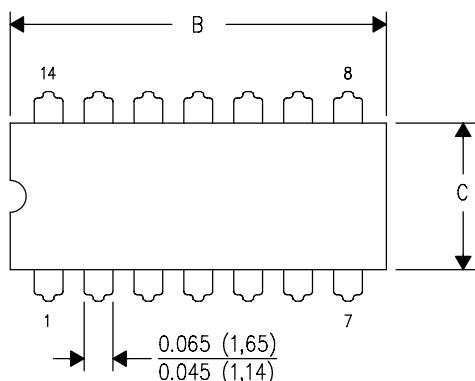
4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

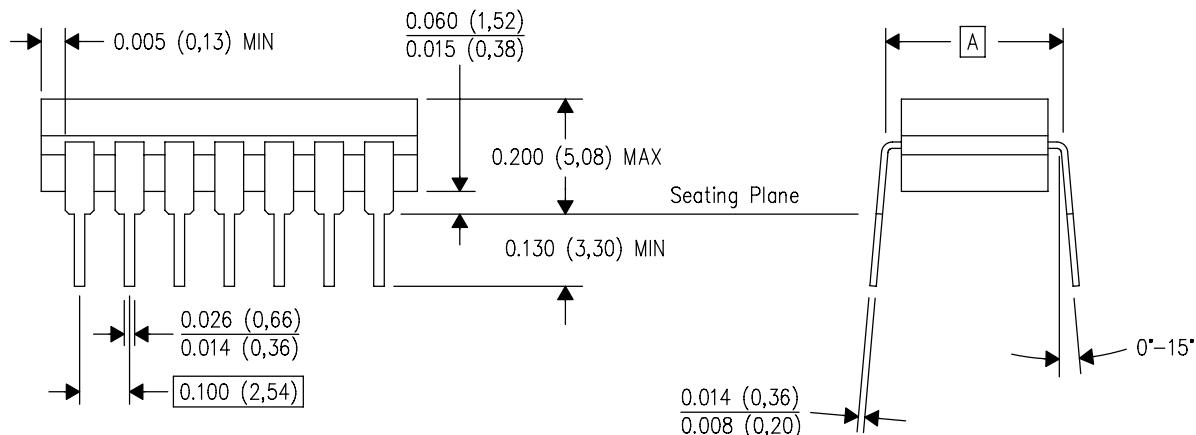
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



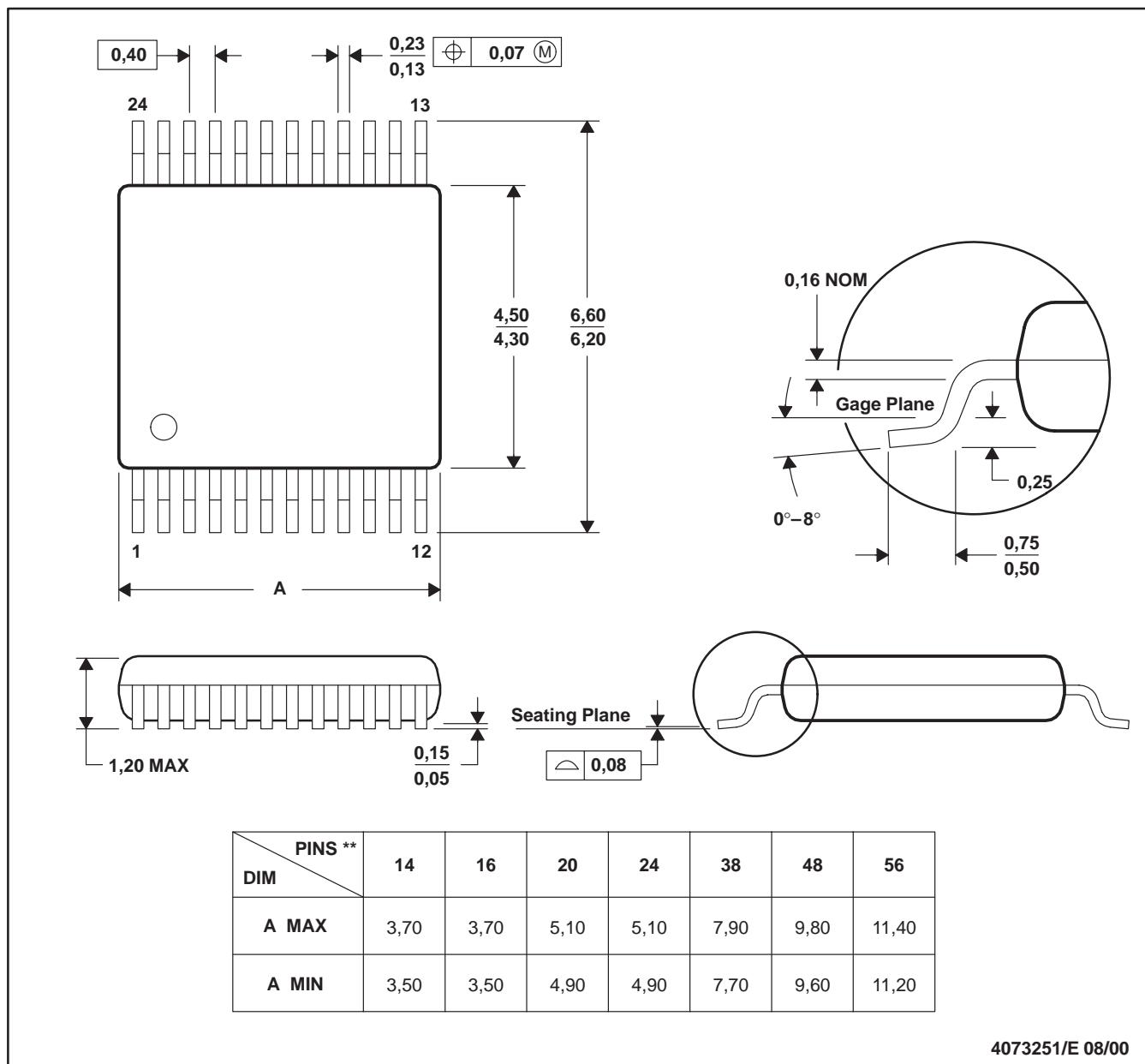
4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

# GENERIC PACKAGE VIEW

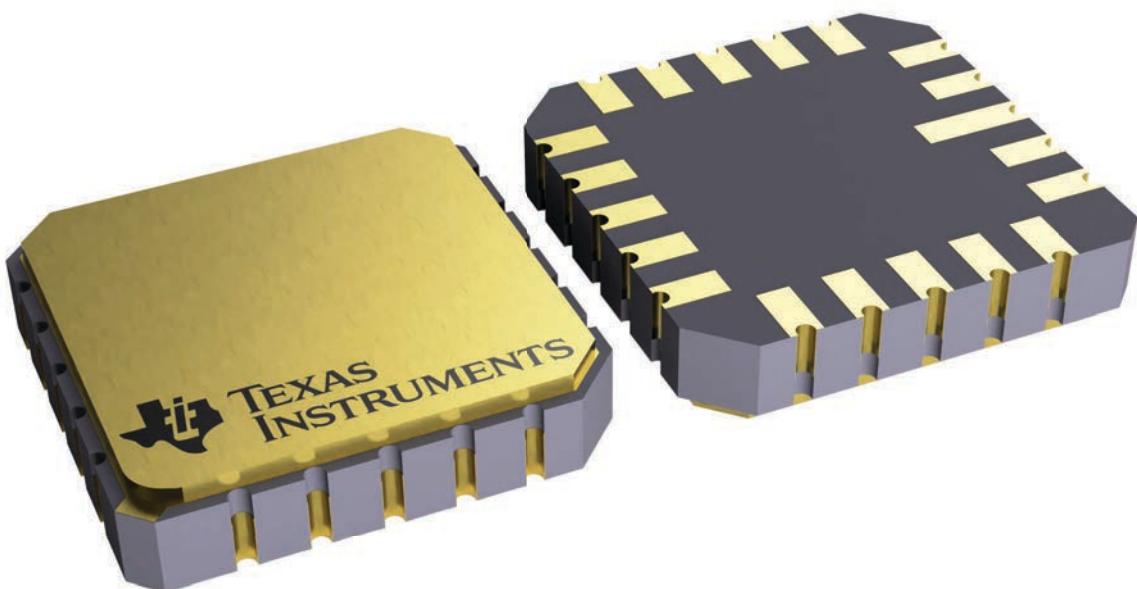
**FK 20**

**LCCC - 2.03 mm max height**

**8.89 x 8.89, 1.27 mm pitch**

**LEADLESS CERAMIC CHIP CARRIER**

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

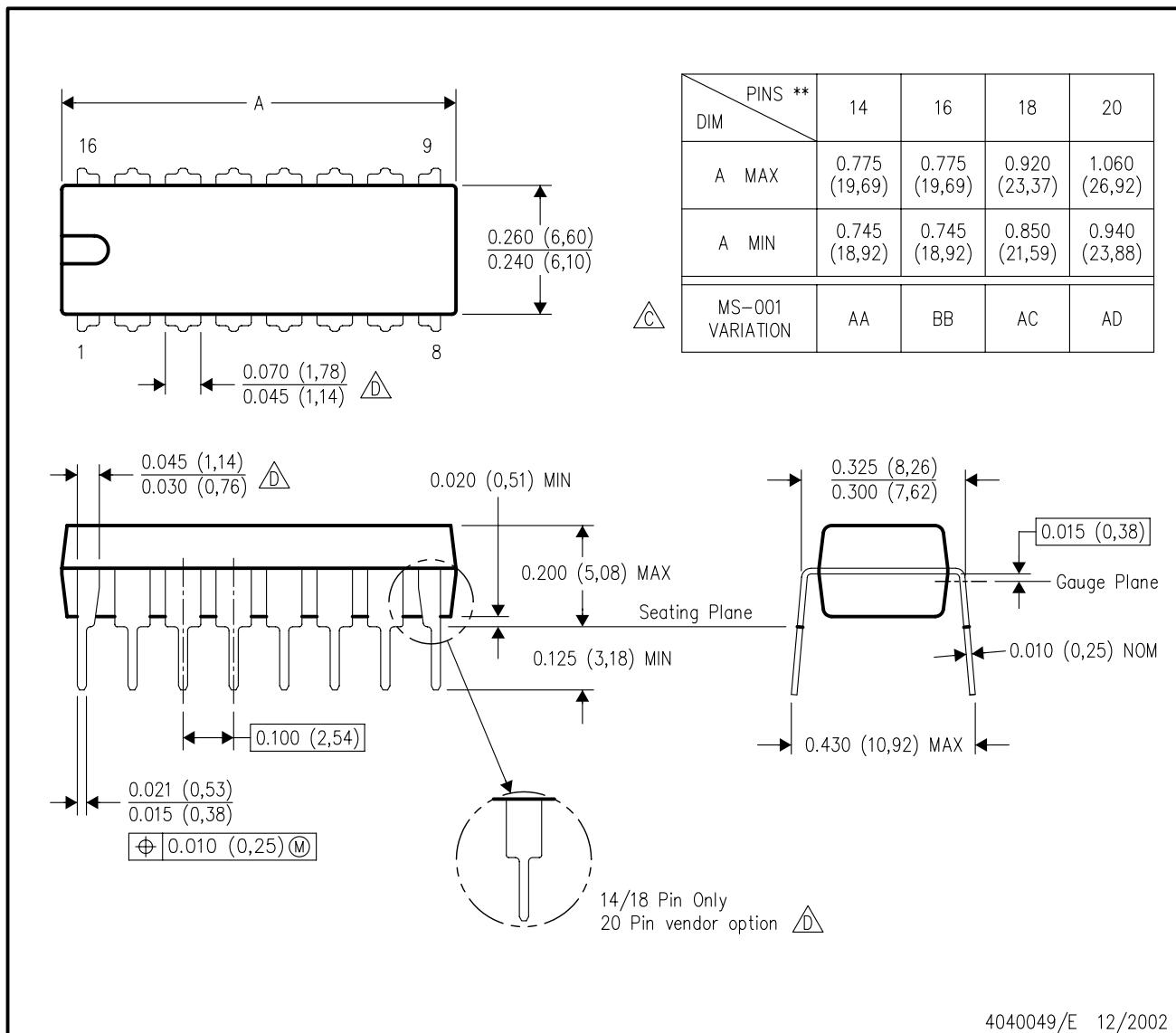


4229370VA\

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

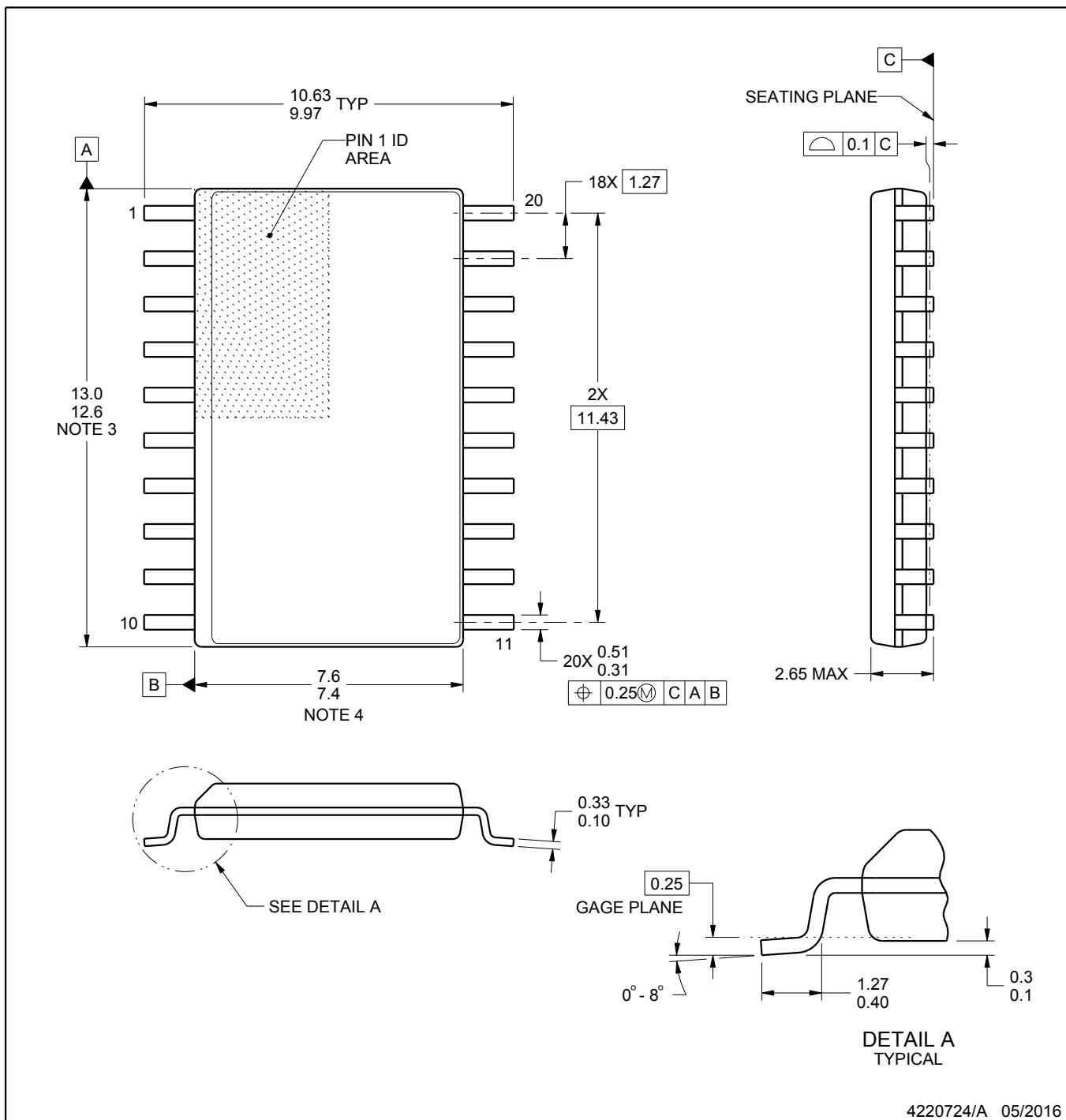
# PACKAGE OUTLINE

DW0020A



SOIC - 2.65 mm max height

SOIC



## NOTES:

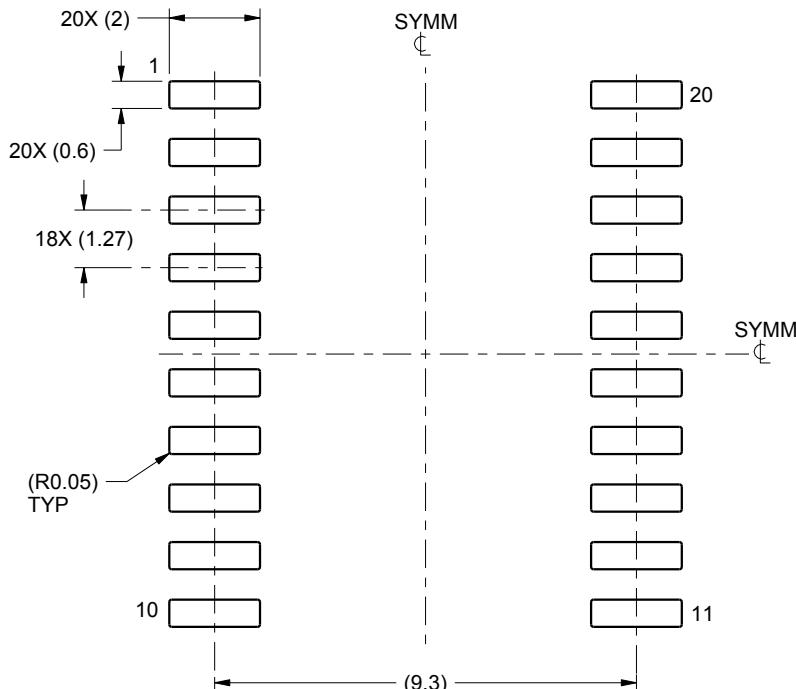
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

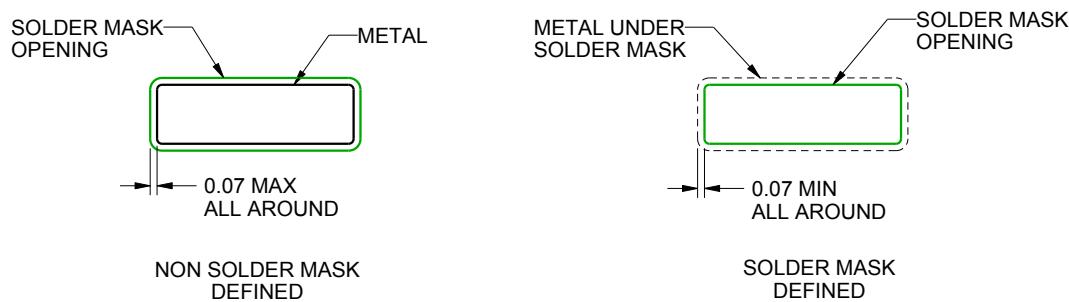
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

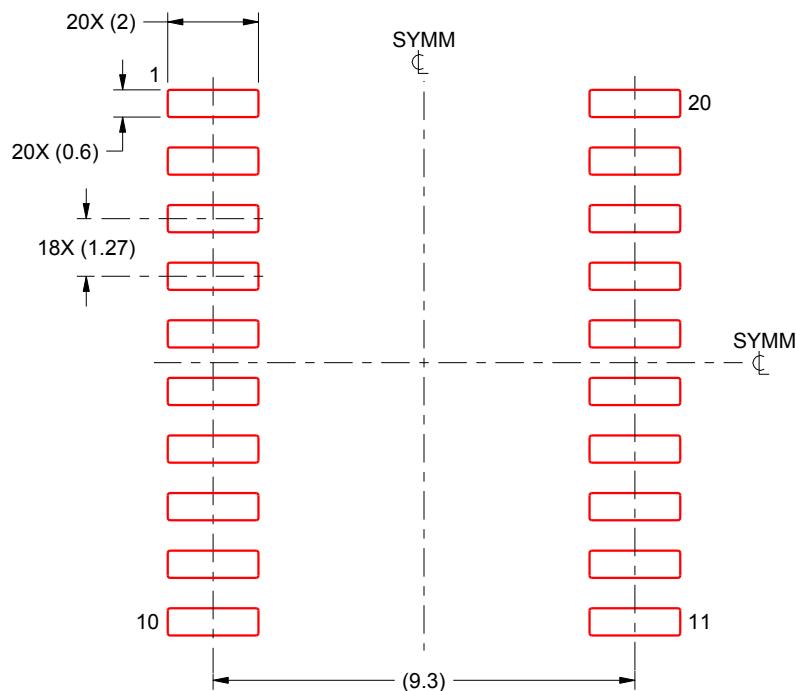
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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